Design of Gain Booster for Sample and Hold Stage of High Speed-Low Power Pipelined Analog-To-Digital Converter

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Abstract **-** This paper presents the full custom design of an operational transconductance amplifier (OTA) for the sample and hold (SHA) stage of a 10-bit 50-MS/s pipelined analog-to-digital converter (ADC) implemented in a TSMC 0.35µm CMOS process. The OTA chosen for this design is folded cascode with gain boost topology. It is demonstrated through the design analysis and HSPICE simulation that such a structure realizes the best trade-off between power, speed and gain. The simulation results show the OTA achieves DC gain of 88.05dB, unity gain bandwidth of 430.03MHz and 84.06 degree of phase margin. The OTA achieves 62.13 dB SNR at the sampling rate of 50MHz with the input frequency of 24MHz. Power consumption is 9.68 mW from a single 3V supply. The settling time to 2^{-11} accuracy is 8.2ns.

Index Terms - Gain boost, folded cascode, sample and hold amplifier, pipelined ADC.

I. INTRODUCTION

Speed and accuracy are two of the most important properties of analog circuits such as switch-capacitor filters, sigma-delta converters, sample and hold amplifier and pipeline ADC; however, designing high performance analog circuits is becoming increasing challenging with persistent trend towards reduced voltage supply. The main bottleneck in the analog circuit design is the operational amplifier. Speed and accuracy are determined by the settling behavior of operational amplifiers. Fast settling requires a high unity-gain frequency and a single-pole settling behavior of the op amp, whereas accurate settling requires a high dc gain. In a low voltage circuit, the realisation of the CMOS operational amplifier that combines high DC gain with high unity gain bandwidth has proven to be a difficult problem.

Cascading is a most useful technique to achieve DC requirement of the amplifier without degrading its high frequency performance. But cascading is not possible in low voltage circuits owing to output voltage swing consideration. Gain-boosting technique was introduced to remedy this problem. It allows increasing the DC gain without sacrificing the output voltage swing. Furthermore this technique decouples the DC gain and the frequency response of the amplifier [2]. It is therefore possible to achieve high speed and high gain at the same time.

This paper is organized as follows. Section II describes the design methodology. Section III provides an overview of the gain boost techniques of a folded cascode amplifier. Section IV illustrates detailed circuit implementation of the OTA. Section V presents the specification of pipelined ADC. Section VI explains the design analysis of the OTA, biasing and common mode feedback circuit employ in the OTA. Section VII and VIII discuss about the SHA and Fast Fourier Transform (FFT). The simulation result and discussion from different process corner is comment on section IX. Section X shows the post layout simulation result. Conclusion is finally drawn in the last section.

II. METHODOLOGY

The design of the OTA employs full custom design approach as shown in Figure 1. The design flow is started by determining the design specifications following by schematic entry in which netlist is created. Then the circuit is simulated in HSPICE until the satisfying performance is achieved. After that the layout is constructed in Mentor-Graphic. The layout is then verified using IC Station verification tools i.e. Calibre DRC and Calibre LVS. Design Rule Check (DRC) is implemented to make sure the layout comply with fab process design rules. The layout is verified using Calibre Layout-vs-Schematic (LVS) to validates the connectivity of the layout against the schematic i.e. equality between schematic and layout. Finally, the layout is then extracted for post layout simulation to analyze the performance of the full custom design.

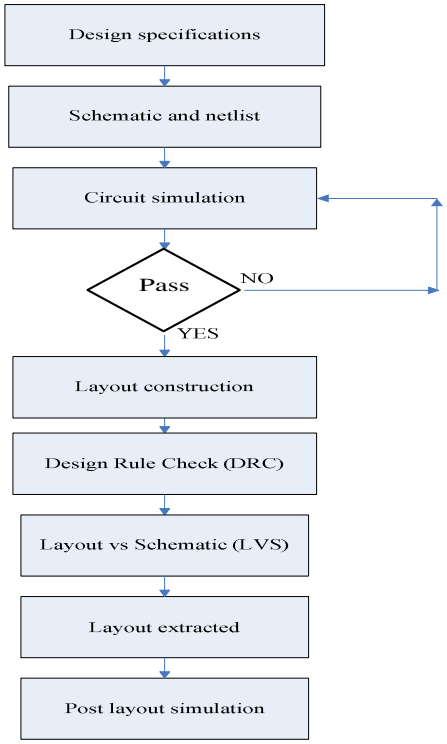

Figure 1: Design flow

III. FOLDED CASCODE WITH GAIN BOOST TOPOLOGY

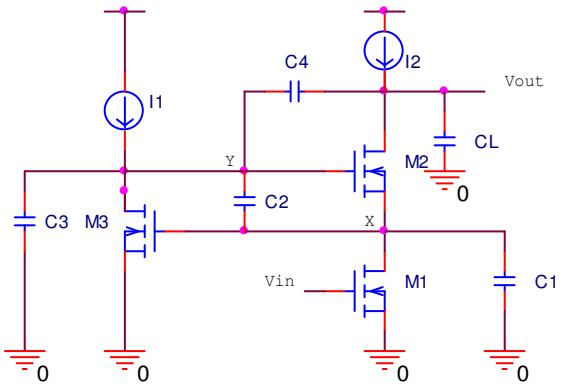

Figure 2: Gain boosted folded cascode topology

The difficulties in using two-stage op-amps at high speeds have motivated extensive work on new topologies. Gain Boosted amplifiers are proposed instead of the normal folded cascode amplifiers to get both high gain and high bandwidth from a single stage amplifier. The idea of gain boosting is to maximize the output impedance without adding more cascode devices. It is usually widely used for high-impedance current source [1].

Figure 2 show the gain-boosted folded cascode topology where transistors M1 and M2 form the main folded amplifier (M1=Input device, M2=Cascode device). C_1, C_2, C_3, and C_4, are the parasitic capacitances between drain to source and gate-to-source of different transistors. C_L, is the load capacitance seen at the output node. The gain obtainable from just these two transistors is limited (around 60 dB for a fully-telescopic amplifier) as the gain increase further, the parasitic poles becomes more dominant and hence the bandwidth starts dropping [3]. M3 (gain boost device) is put which creates a negative feedback loop that makes the source of M2 less sensitive to the output voltage to overcome this problem [2] .M3 drives the gate of M2 and force V_X to be equal to V_Y .Thus, voltage variation at the drain of M2 now affect Vx to a lesser extent because the gain boost devices regulated the voltage [1].

The gain boost device with gain A_{dd} increase the output resistance approximately A_{dd} times larger than that of normal folded cascode amplifier [4]. Therefore gain boosting technique increased the output impedance and DC gain by the additional gain stage A_{dd} without adding more cascode devices. From figure 1,with transconductance gm1,gm2 and output resistance rds1,rds2 of M1 and M2 respectively, the output resistance Rout and DC gain Adc of the gain boost cascode OTA is given by equation below [2] :-

$$R_{out} = g_{m2}r_{ds2}r_{ds1}A_{add} \quad (1)$$

$$A_{dc} = g_{m1}g_{m1}r_{ds1}r_{ds2}A_{add} \quad (2)$$

IV. CIRCUIT IMPLEMENTATION

Figure 3 shows the fully differential folded cascode gain boost topology. The differential amplifier is choose over single-ended signaling because of higher immunity to environmental noise [1]. Now consider the circuit is symmetric, noise on VDD affects Vop and Vom but not the difference between these nodes. Thus the circuit is much more robust to the supply noise [1]. Another reason is to increase the maximum achievable output swing. The differential circuit produce double maximum output swing than that in the single ended circuit. Other reasons using differential circuits is simpler biasing and high linearity [1].

The topology consists of folded cascode device and gain boost device. The cascode device is made up of folded-cascode stage that consists of input transistors Mip, Mim, current sources Mep, Mem, current sinks Msp, Msm, PMOS cascode transistors Mdp, Mdm, NMOS cascode transistors Mcp, Mcm and tail current source Mt. The gain boost device consist of N-gain boost device and P-gain boost device. The N-gain boost device for Mcp and Mcm are transistors Macp, Macm, Mlcp, Mlcm while the P-gain boost device for Mdp and Mdm are transistors Madp, Madm, Mldp and Mldm. The gain boost devices use only single transistors to keeps the design simple and

adds minimal power. Since the main function of the gain boost device is to increase the gain of the OTA, longer channel length are used to get larger output resistance.

Transistors in the signal path are biased in deep inversion instead of at edge of saturation to ensure that they remain in saturation at all process corners. For cascode transistors (Mcp, Mcm, Mdp, Mdm) minimum channel lengths were chosen for both NMOS and PMOS in order to place the non-dominant pole of the OTA at high frequency.

The use of small device sizes reduces the parasitic capacitance seen at the output node, thus improving the OTA's speed. This also minimizes capacitive load seen by the gain boost devices, which

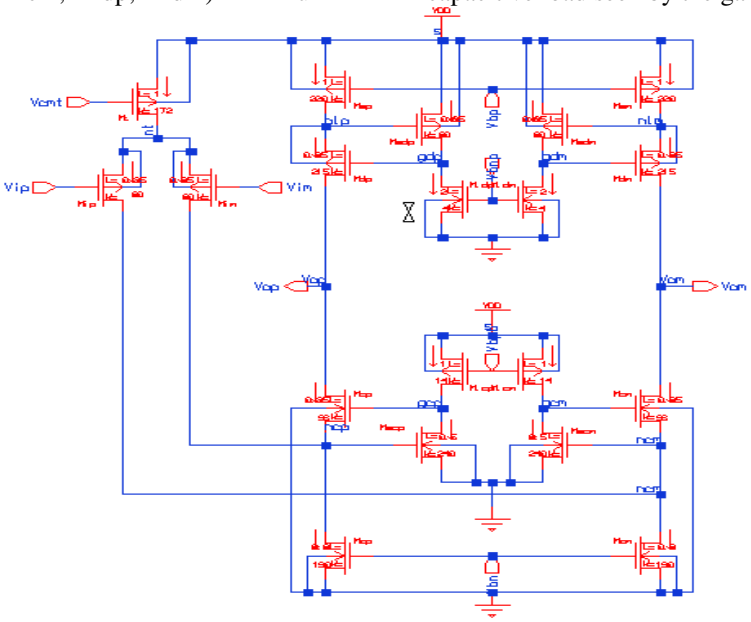

Figure 3 : Fully differential folded cascode topology

results in lowering the power dissipation of the gain boost devices. For the PMOS current source and the NMOS current sink in the cascode device, longer channel lengths are used to obtain higher open loop gain and for better matching .

V. SPECIFICATION OF PIPELINED ADC

The method of designing a pipelined analog-to-digital converter for minimum power consumption has been described at the system level [5]. The front end of the converters has a sample and hold stage followed by eight 1.5-bit residue amplifiers and at the back end of the ADC is only 2-bit flash converter as shown in figure 4:-

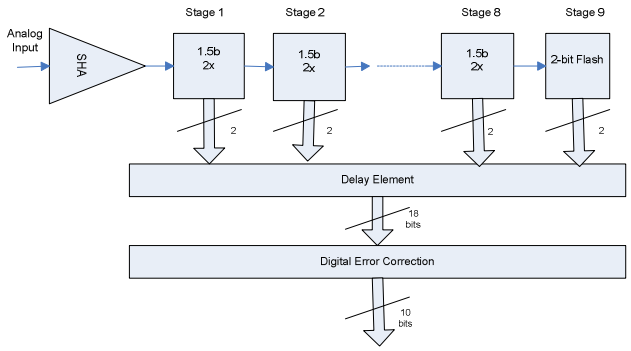

Figure 4: 10-bits 50MS/s pipelined ADC architecture

The design goal is to meet the specification for the SHA stage of the pipelined ADC over all process corners while minimizing power. The specification is tabulated below:-

Table 1 ; Design specification

Parameters	Specification
Stage Capacitor (C_f)	1.22pF
Load Capacitor (C_L)	1.2pF
Settling Accuracy (e_{ss})	2^{-11}
Settling Error	0.1%
Feedback Factor (β)	0.9
Input Voltage Swing	1Vp-p
DC Gain (A_{Vdc})	>72dB
GainBandWidth (GBW)	>350MHz
Phase Margin (PM)	>65°
Settling Time (t_s)	<9ns
Power Consumption	<20mW

VI. DESIGN ANALYSIS

A. OTA

This section describes the salient point in optimizing the design to meet the specification. The hand calculations of sizing of each transistor are shown. From [5], the first approach is to obtain the input transistor current for the OTA using the parameters values specified.

$$I_i = 2\frac{V_{FS}C_L}{t_S}\left(1+\frac{\ln(e_{ss}^{-1}).V_{effi}}{2\beta.V_{FS}}\right) \quad (3)$$

Where V_{FS} is the single ended voltage swing, half of the differential full-scale voltage that is 1V. V_{effi} is chosen as the smallest effective voltage that keeps the input transistors in the strong inversion region and satisfies the other op-amp specifications such as gain that is 0.25V. Then the input transconductance of the OTA can be obtained using the value of the input transistor current calculated.

$$gm_i = \frac{2I_i}{Veff_i} \quad (4)$$

Then the sizing of the input transistor is obtained using this equation:-

$$(W/L)_i = \frac{gm_i^{\,2}}{2I_i\mu_p C_{ox}} \quad (5)$$

To obtain sizing of other transistors, use this equation:-

$$(W/L) = \frac{2I_D}{\mu_o C_{ox} Veff^{\,2}} \quad (6)$$

After doing hand calculation and some optimization during simulation, the design parameters is summarize as table 2.

Table 2: Summary of design parameter

Devices		W (µm)	L (µm)	I_D (mA)	V*eff* (v)
Input	Mip, Mim	80	0.35	0.6	0.25
Current sources	Mep, Mem	220	1	0.6	0.25
Current sinks	Msp, Msm	190	0.8	1.2	0.25
PMOS cascode	Mdp, Mdm	215	0.35	0.6	0.15
NMOS cascode	Mcp, Mcm	96	0.35	0.6	0.15
N-gain booster	Macp, Macm	240	0.5	0.1	0.05
N-gain booster	Mlcp, Mlcm	14	1	0.1	0.4
P-gain booster	Madp, Madm	80	0.35	0.025	0.05
P-gain booster	Mldp, Mldm	4	2	0.025	0.4
Tail current source	Mt	172	1	1.2	0.4

B. Biasing

Figure 5 shows the biasing network for the OTA. One master current source is used and a variety of bias currents are generated using current mirrors. The key property of this topology is that it allows precise copying current with no dependence on process and temperature. The ratio of master current is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy [1]. In order to maximize performance, a robust biasing circuit must be employed. A high-swing cascode current mirror is used to maximize robustness over process and supply voltage variation while also providing excellent current mirroring.

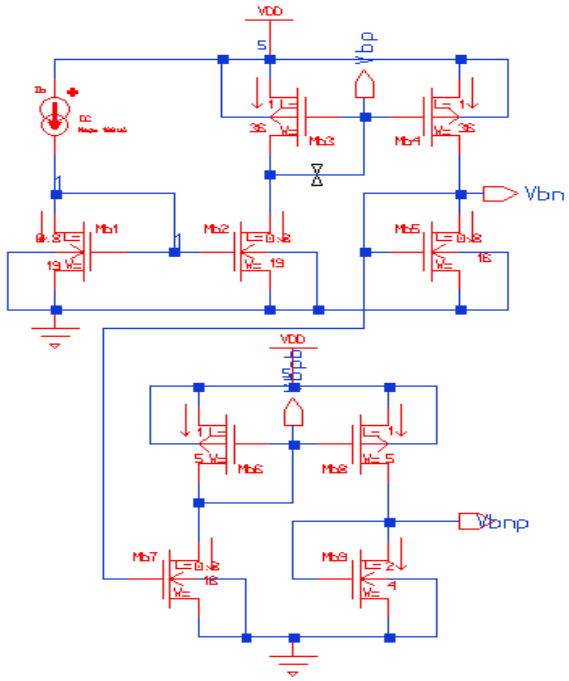

Figure 5 : Biasing Circuit

Table 3 shows the transistors sizing after optimizing during simulation to obtain a proper biasing current.

Table 3: Biasing device's parameters.

Devices	W(µm)	L(µm)
Mb1	19	0.8
Mb2	19	0.8
Mb3	36	1
Mb4	36	1
Mb5	16	0.8
Mb6	5	1
Mb7	16	0.8
Mb8	5	1
Mb9	4	2

C. Common-Mode Feedback

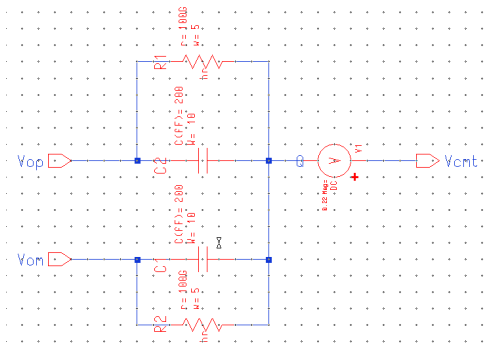

Figure 6: Common Mode Feedback circuit

Figure 6 is common mode feedback for the OTA. For the full differential signal circuitry, because of the increased symmetry, all common mode signals and even-order distortions cancel out, except for the influence of component mismatches. However, as the signal is no longer referred to ground, the operating point of the circuitry cannot be stabilized with the differential feedback loop. A common-mode feedback loop (CMFB) is required to determine the output common-mode voltage and to control it to be equal to some specified voltage. This voltage is feedback to control the current levels. Thus, both side carried larger currents and bring the common mode voltage of output nodes back to value Vcmt [8]. So, the common-mode feedback is needed to fix the voltages at the high impedance output nodes to the desired value.

VII. SAMPLE AND HOLE AMPLIFIER (SHA)

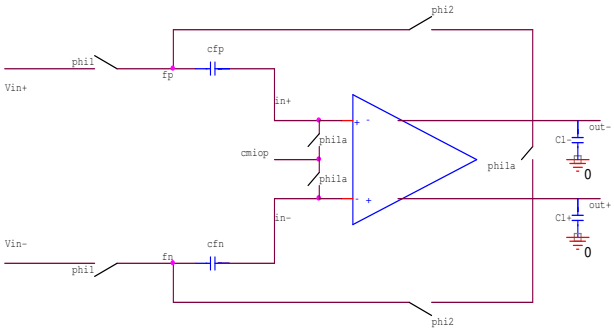

Figure 7: Sample & hold stage of a pipelined ADC

Sample-and-hold amplifier circuits are key building blocks for many discrete time signal processing applications including pipeline A/D converters. Its basic function is to transform input continuous signals into discrete time signals and amplify them. Using the techniques of precharging and output capacitor coupling can mitigate the requirements for the opamp, resulting in low power dissipation The conventional flip-around SHA shown in Fig. 7 has been extensively employed for high-speed and high-resolution CMOS SHA. When *phi1* = 1, the SHA is in the sample mode, and the input is sampled on the *Cfp* and *Cfn* capacitors. When *phi*2 = 1, the SHA is in the hold mode, the sampling capacitors are connected to the outputs of the op-amp. The op-amp and the two sampling capacitors form a feedback loop to drive the *Cl*- and *Cl*+ capacitive loads [6].

VIII. FAST FOURIER TRANSFORM (FFT)

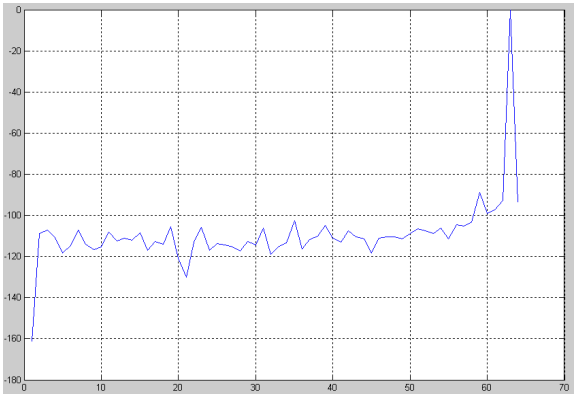

Figure 8 : FFT spectrum

The simulation results from HSPICE are post processed by the software of MATLAB to obtain the Fast Fourier Transform (FFT) spectrum. FFT is used as a tool for measuring and analyzing signals from captured data records. It captured time-domain signals, measure their frequency content, convert the results to convenient units, and display them. FFT produced the average of a signal's frequency content over the time interval that the signal was acquired. FFT focus on the positive half of the frequency spectrum only, noting that the spectrum of a real signal is symmetrical. In a two-sided spectrum, half the energy resides in the positive frequencies and half in the negative frequencies. Therefore, to convert from a two-sided spectrum to a single-sided spectrum, the second half of the matrix is discarded and multiplies every point by two.

The number of frequency points in the FFT spectrum is N/2, where N is the number of sampling points captured in the time domain. From HSPICE, a total of 128 data are collected. Since N=128, the FFT only display the first 64 points. Figure 8 show a FFT spectrum of power represent in decibels (dB) versus sampling point frequency. SNR is calculated by dividing overall signal power to the sum of noise power. The signal power is the highest power spectrum which occurs at the 64^{th} sampling point which also known as the fundamental frequency. According to the FFT spectrum, The OTA has 62.13dB SNR at the sampling rate of 50MHz with the input frequency of 24MHz which is higher than the expected SNR that is 60dB. Only in worst case scenario the SNR drops below specification.

IX. SIMULATION RESULT AND DISCUSSION

The following process corner conditions are used in verification of the OTA design. Usually for commercially product, temperatures varies from 0°C to 90°C, these are combined with process variations to derive worst case scenario. For example, highest temperature gives rise to the highest thermal noise figure. Combined with the slow process parameters. It places the toughest test on the dynamic range performance. On the contrary, the fast process corner combined with low temperature will probably introduce instability problem.

Table 4 : Corner conditions used for design verification.

Process variation	Typical	Slow	Fast
Temperature variation	25°C	90°C	0°c

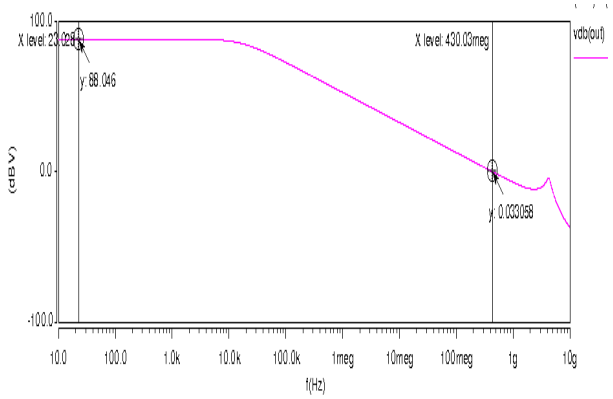

Figure 9: DC gain graph

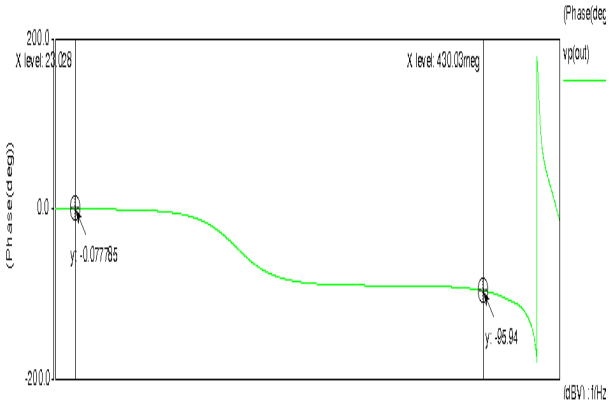

Figure 10: Phase margin graph

The OTA has a DC gain of 88.05dB as seen in figure 9 while the unity gain bandwidth reaches 430.03MHz with an approximate 84.06 phase margin in figure 10.It shows the effect of gain boosting technique; the OTA exhibit a high DC gain measurements without affecting the gain or phase for higher frequencies.

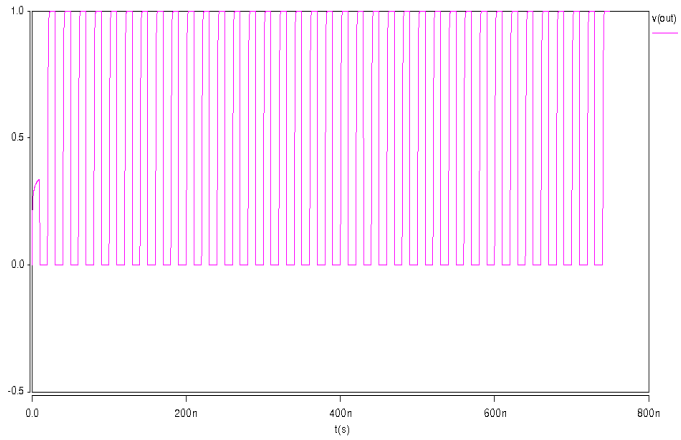

Figure 11: Transient response graph

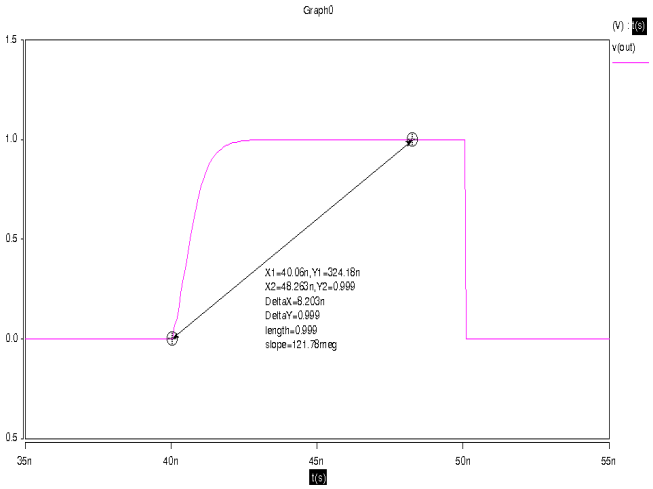

Figure 12: Settling time

Figure 11 show the transient response of the OTA to see the settling behaviour. Settling time is the time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified error, usually symmetrical about the final value. To see the result, the OTA must be placed in a closed loop configuration. The setup to be used in the SHA stage of a 10-bit 50-Ms/s pipelined ADC is shown in Figure 7. From the figure, *phi1* and *phi2* are non overlapping clocks, *Cfp, Cfn* are both the sampling and feedback capacitors depending on which clock phase the circuit operates. From figure 12, the settling time of the OTA is 8.2ns which is faster than the expected result that is 9ns. It is predictable result since gain boosting technique decouples the DC gain and frequency response. Therefore a high speed and gain is possible to achieve at the same time.

Power consumption is calculated by summing the total current running through each supply path through the entire current by the supply voltage. Total consumption is found to be 9.68mW under normal operating conditions which is much better than the expected value.

Table 5 summarizes the achieved performance of the design. The specifications are met throughout the corner conditions.

Table 5 : Performance summary

Process Corner	Worst ,90°C	Typical ,25°C	Best ,0°C
DC Gain (dB)	87.16	88.05	88.12
Gain BandWidth (MHz)	367.47	430.03	477.55
Phase Margin (degree)	83.68	84.06	84.46
Settling Time (ns)	8.43	8.2	8.16
Power Consumption (mW)	9.65	9.68	9.82
SNR (dB)	57.78	62.13	69.08
Voltage (V)	3	3	3

X. POST LAYOUT SIMULATION

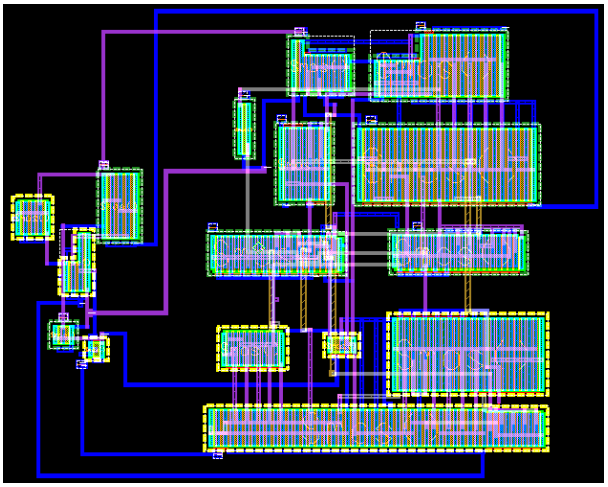

Figure 13 : Op-amp layout

Figure 13 is the layout of the op-amp. The layout is generated by performing Schematic Driven Layout (SDL) in IC station Mentor-Graphic using TSMC 0.35µm CMOS process in the Mentor-Graphic environment. The performance of a full-custom design can be best analyzed by performing a post-layout simulation on the extracted circuit netlist. The parasitic capacitances extracted according to how the layout is designed. At this point the circuit should have passed the DRC and LVS steps with no violations.

The post layout simulation is performed by obtaining the netlist of the layout design from Mentor-Graphic and run it in HSPICE. There are subtle differences in the post-layout simulation results as compared to the pre-layout simulation as shown in Table 6 but it is acceptable since it is still within the specifications.

Table 6 : Pre and post-layout performance

Performance	Pre-layout	Post-layout
DC Gain (dB)	87.25	87.25
GainBandWidth (MHz)	418.9	408.08
Phase Margin (degree)	79.9	79.74
Settling Time (ns)	8.27	8.162
Power Consumption (mW)	9.59	9.59
SNR(dB)	54.61	51.02

XI. CONCLUSION

This paper presents the full custom design of an operational transconductance amplifier (OTA) implemented in a 0.35µm CMOS process using HSPICE. The choosen OTA is a single stage folded cascode with gain booster to fulfill the high DC gain and unity gain bandwidth requirement. All the design specs have been verified throughout the process corners and temperature variations and has satisfied all the specifications given in advance. The HSPICE simulation results show the OTA achieves DC gain of 88.05dB, unity gain bandwidth of 430.03MHz and 84.06 degree of phase margin. From the MATLAB simulation, the OTA achieves 62.13 dB at the sampling rate of 50MHz with the input frequency of 24MHz. Power consumption is 9.68 mW from a single 3V supply. The settling time to 2^{-11} accuracy is 8.2ns. The low power, low voltage, high speed result has been successfully achieved for both the performance and robustness. It is concluded that this architecture is suitable for low power-high speed pipeline ADC.

FUTURE DEVELOPMENT

The design of the OTA can be further analyze by considering other performance specifications and also implemented it in a low-power low-voltage technology such as TSMC 0.18µm but needs major modification in order to work in lower supply voltage.

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