Microelectronics Reliability 50 (2010) 1283–1289

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

NBTI degradation effect on advanced-process 45 nm high-*k* PMOSFETs with geometric and process variations

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ARTICLE INFO

Article history:
Received 1 July 2010
Accepted 8 July 2010
Available online 4 August 2010

ABSTRACT

Negative bias temperature instability (NBTI) has become an important reliability concern for nano-scaled complementary metal oxide (CMOS) devices. This paper presents the effect of NBTI for a 45 nm advanced-process high-*k* dielectric with metal gate PMOS transistor. The device had incorporated advanced-process flow steps such as stress engineering and laser annealing in order to achieve high on-state drain current drive performance. To explore NBTI effects on an advanced-process sub-micron device, the 45 nm high-*k* PMOS transistor was simulated extensively with a wide range of geometric and process variations. The device was simulated at varying thicknesses in the dielectric layer, oxide interfacial layer, metal gate and polysilicon layer. In order to observe the NBTI effect on process variation, the NBTI degradation of the 45 nm advanced-process PMOS is compared with a 45 nm PMOS device which does not employ process-induced stress and incorporates the conventional rapid thermal annealing (RTA) as compared to the laser annealing process which is integrated in the advanced-process device flow. The simulation results show increasing degradation trend in terms of the drain current and threshold voltage shift when the thicknesses of the dielectric layer, oxide layer as well as the metal gate are increased.

1. Introduction

Deep-sub-micron device scaling is a phenomenon which is rapidly evolving for ultra-scaled MOSFETs and the design of this technology requires stringent control of short-channel effects (SCE) and sub-threshold behavior. With this in mind, the gate dielectrics should be thinned to less than 1.0–1.5 nm equivalent oxide thickness (EOT) [1]. It has been reported that due to quantum mechanical tunnelling, the typical leakage current of SiO_2 at gate voltage, V_g of 1 V can change from 10^{-12} A/cm^2 with EOT of 3.5 nm to 10 A/cm^2 with EOT of 1.5 nm [2]. To achieve the EOT target stated above and to counter the issue of leakage currents, dielectric materials with higher permittivity, k values as compared to SiO_2 ($k > 3.9$) are introduced. Compounds of hafnium (Hf), zirconium (Zr), and aluminium (Al) have been proposed as potential high-*k* dielectric materials and hafnium oxide (HfO_2) has emerged as a promising gate dielectric to replace the conventional SiO_2 due its high dielectric constant ($k = 25$), wide bandgap ($E_0 = 5.7$ eV) [3], acceptable band offset with respect to silicon ($\Delta E_c = 1.5$ eV) [3], and process conditions which are compatible with silicon process flow integration. An ultimate reliability issue in sub-micron CMOS devices is the negative bias temperature instability (NBTI) phenomenon. Transistors tend to exhibit changes in transistor characteristics over time such as shifts in threshold voltage ($\Delta|V_{th}|$), as well as significant changes in drain current (I_D) and transconductance (G_m). This phenomenon is due to the creation of interface states (N_{it}) and oxide trapped charged (N_{ot}) whereby the mechanism is accelerated by negative bias and elevated temperature. This paper presents the NBTI degradation effect on advanced-process 45 nm PMOS device in which transistor parameters such as the drain current and threshold voltage shifts will be observed consequent to the application of stress temperature. This work will look into the variation of each stack layer of the device and the influences of each stack layer to the NBTI effect.

2. Methodology of advanced-process 45 nm PMOS device

An advanced- process sub-micron technology device incorporates advanced process steps in order to overcome process-related challenges such as ultra-shallow junction (USJ) formation, reduction in current leakage, suppressing transient-enhanced diffusion and achieving device's performance targets, such as the on- and off- current targets, while controlling short-channel effects. A distinct procedure which promotes advanced-process technology is the millisecond laser annealing for ultra-shallow junction formation. This procedure replaces the conventional procedures of ion implantation and subsequent rapid thermal annealing, in forming the doped region of a sub-micron transistor. The process flow of

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doi:10.1016/j.microrel.2010.07.022

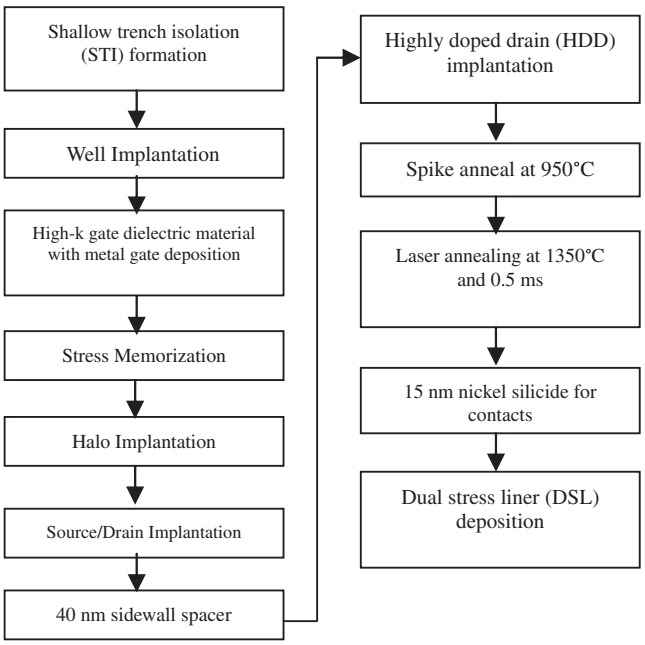

Fig. 1. Process flow of the simulated advanced-process 45 nm high-*k* PMOS transistor.

a PMOS device consisting of an advanced-process flow is given in Fig. 1 [4].

2.1. Devices and simulation conditions

The device used in this simulation is a 45 nm hafnium-based dielectric combined with TiN metal gate PMOS transistor and its process steps reflects the standard manufacturing trends for a sub-micron device. The process flow of the simulated device is as presented in Fig. 1 whereby it adopts the deposition of high-*k* dielectrics with metal gate, application of stress engineering as well as the adoption of laser annealing as compared to the conventional rapid thermal annealing. To further explore the NBTI effects on different structures of advanced high-*k* devices, the high-*k* PMOS device was simulated extensively with a wide range of geometric and process variations. NBTI was studied by varying geometric properties which are the thicknesses of the high-*k* dielectric layer, oxide interfacial layer, TiN metal gate layer and polysilicon layer respectively. The varied geometric properties of the device are as presented in Fig. 2. In regards to process variations, the NBTI degradation of the device was studied by simulating and comparing devices with and without process-induced stress effects as well as comparing devices which are processed with the conventional RTA to the devices which are processed with both RTA and laser annealing (LA). The technology CAD (TCAD) Sentaurus Synopsys simulator tool was used to study the NBTI effects of these geometric and process variations.

3. Simulation results

The following subsections present the simulation results, which are the drain current degradation, the threshold voltage shifts and the interface trap concentration subsequent to bias temperature stress. The geometric properties of the advanced-process 45 nm device were extensively varied and the after-effects are presented in subsection 3.1 whereas subsection 3.2 presents the comparison of simulated results of the device which incorporates advanced process-induced stress and LA steps, compared to the device which follows the conventional process flow.

3.1. Geometric variation of device

The high-*k* PMOS device is varied in terms of the thicknesses of the high-*k* dielectric layer, oxide interfacial layer, metal gate layer and polysilicon layer. NBTI effect is observed by analysing the drain current degradation, threshold voltage shifts and interface trap concentration when the device is stressed at stress temperatures ranging from 300 K to 400 K, as had been carried out in most experimental works [5]. For the simulation of each varied device parameters, the unvaried parameter thicknesses were set to the standard sub-micron device specification highlighted in [6].

3.1.1. Influence of high-k dielectric thickness on NBTI

When biased at room temperature of 300 K, the drain current degradation is found to be significant as the dielectric thickness is decreased. However, it is observed that at a higher stress temperature of 400 K, the drain current degradation becomes more significant as the thickness of the HfO_2 dielectric layer is increased. This is in agreement to the single-pulse measurement carried out by [7] which had also obtained a current degradation of around 300 μA/μm for the similar range of gate biases and HfO_2 thicknesses which were used in this current work. From Eqs. (1) and (2) below, it is shown that the oxide thickness is inversely proportional to the drain current and thus it is in agreement with the graph in Fig. 3 for the HfO_2 dielectric thickness variation [8]. As the dielectric thickness increases, the drain current would be further reduced leading to higher drain current degradation.

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (1)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad (2)$$

$$V_T = V_{FE} - |2\phi_F| - \frac{\sqrt{2\varepsilon_s q N_d(|2\phi_F| - V_{SB}}}{C_{ox}} \quad (3)$$

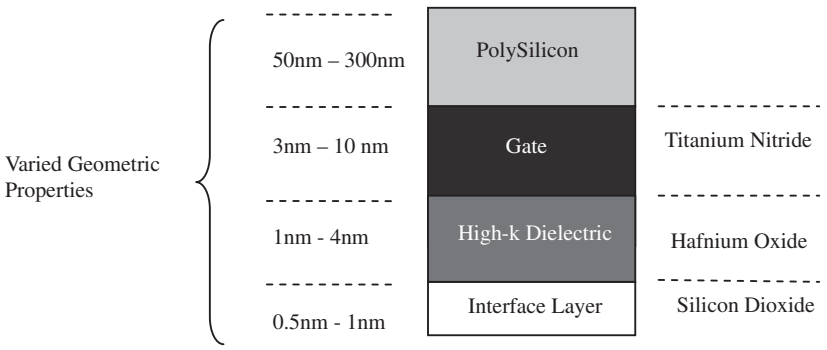

Fig. 2. Schematic view of the simulated high-*k*/metal gate with its varied geometric properties.

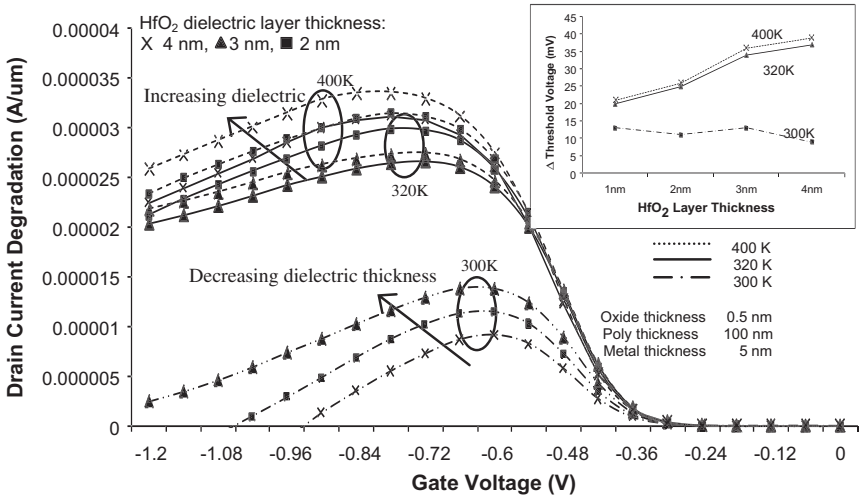

Fig. 3. Drain current degradation of a 45 nm high-*k* PMOS stressed at temperatures 300–400 K. The high-*k* dielectric layer thickness had been varied from 2 nm to 4 nm. Inset caption is the threshold voltage shift of when the HfO_2 layer thickness is varied from 1 nm to 4 nm.

The uppermost right hand side of Fig. 3 presents the threshold voltage shift versus HfO_2 dielectric thickness. It is observed that the threshold voltage increases in proportion with the HfO_2 dielectric thickness and this can be described from Eqs. (2) and (3) [8] where the threshold voltage is proportional with oxide thickness. The device with thinner HfO_2 layer exhibits less threshold voltage shift. This is due to less charge trapping/de-trapping at pre-existing defects in the bulk high-*k* layer [9]. Fig. 4 presents the interface trap concentration (N_{it}) as a function of stress time (t) with a variation of HfO_2 dielectric thicknesses and temperature. From this figure, it is shown that N_{it} increases as the temperature is increased for all three different HfO_2 dielectric thicknesses. For every applied stress temperature, it shows that the N_{it} increases as the HfO_2 dielectric thickness is decreased. This behavior is in agreement with a review paper done by Ribes et al. [10] in which he stated that the NBTI degradation is due to holes trap (metastable states) which recovers and interface state which are stable and does not recover. It is also observed that the devices stressed at higher stress temperature tend to reach steady-state occupation at an earlier time.

3.1.2. Influence of oxide interfacial layer thickness on NBTI

The introduction of the HfO_2 gate stack would consists of two layers which are the HfO_2 film and a thin 0.5- to 1.5-nm SiO_2 interfacial layer (IL) [11]. This interfacial layer is grown either intentionally or spontaneously in the Si surface as a consequence of when the Hf-based dielectric is deposited onto the silicon. In this section the oxide interface layer thickness had been varied (1 nm, 0.7 nm, 0.5 nm) and the drain current versus gate voltage ($I_D - V_G$) characteristic along with the threshold voltage and interface trap concentration shifts were analysed. The oxide interface layer variation observed in Fig. 5 shows an $I_D - V_G$ trend which is similar to that described in the previous section. The threshold voltage shift also exhibits a similar behavior as in the previous section whereby the threshold increases with the oxide thickness increment. The interface trap concentration increases as the oxide interfacial layer thickness decreases as shown in Fig. 6 and the trend is similar as in the previous section. Devices with thinner gate oxide would experience a higher gate oxide electric field and this vertical electric field tends to accelerate the NBTI effect by increasing the speed of the diffusing hydrogen species, thus generating interface traps.

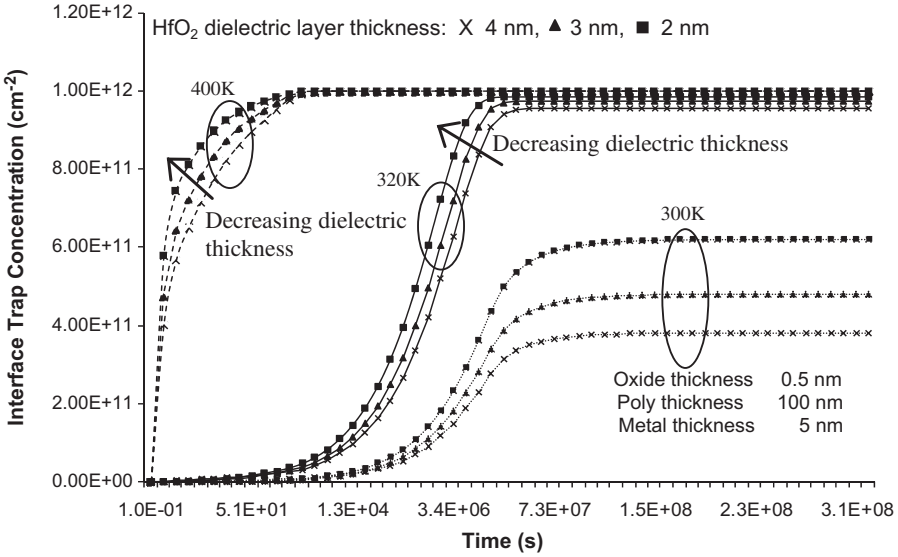

Fig. 4. Interface trap concentration for various thicknesses of the HfO_2 dielectric layer subsequent to bias temperature stress.

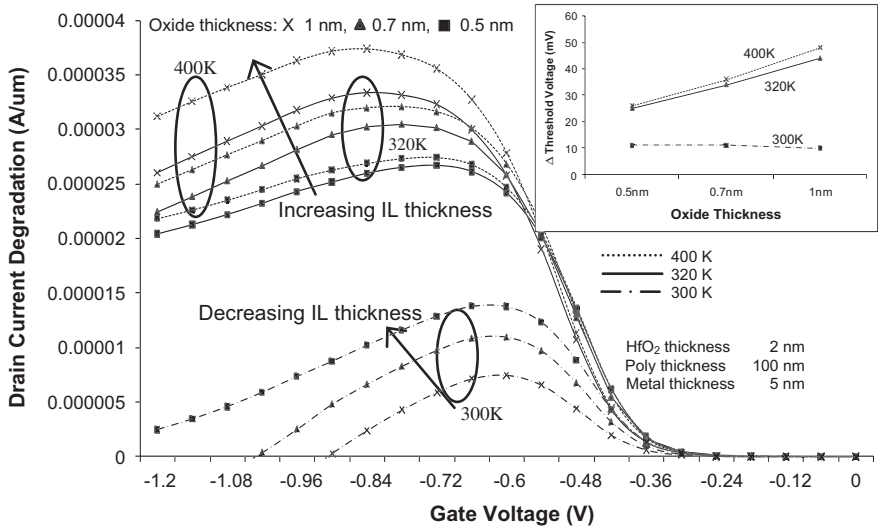

Fig. 5. Drain current degradation of a 45 nm high-*k* PMOS stressed at temperatures 300–400 K. The interface layer (IL) thickness had been varied at 0.5–1 nm. Inset caption is the threshold voltage shift of when the oxide thickness is varied at 0.5–1 nm.

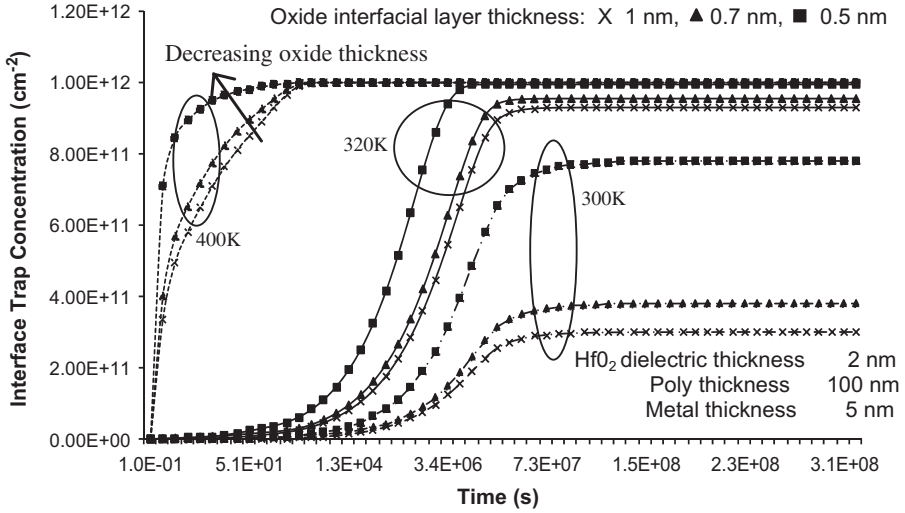

Fig. 6. Interface trap concentration for various thickness of the SiO_2 interfacial layer subsequent to bias temperature stress.

It is observed that the slope of the trap density is steeper for the device with thinner oxide layer which indicates higher contribution of the interface charges. This phenomenon is verified through experimental studies carried out by [12–14].

3.1.3. Influence of metal gate thickness on NBTI

In this work, the metal gate TiN is used as a capping layer before the polysilicon deposition and the influence it imposed to the effect of NBTI is studied by varying its thickness from 3 nm (thin TiN) to 10 nm (thick TiN). It can be observed in Figs. 7 and 8 that at high stress temperature of 400 K, the NBTI degradation becomes more significant as the thickness of the TiN metal gate layer increases. Similar to the cases of when the thickness of the high-*k* dielectric and the SiO_2 interfacial layer were varied, it is observed that the drain current degradation increases as the thickness of the layer is increased. However in terms of the interface trap concentration ΔN_{it}, the trap density is observed to increase as the metal gate thickness layer is increase. This is in agreement with the experimental work carried out by [15] where it had been deduced that by reducing the metal gate thickness, the mobility degradation and NBTI effect are significantly reduced. The observation on the interface trap density characteristic is in reverse when compared to the effects imposed when varying the thicknesses of the HfO_2 dielectric and SiO_2 interfacial layers. It is also observed that the ΔN_{it} arrives at the same level of steady-state occupation, when the device is stressed at 320 K and 400 K.

A charge pumping technique and pulsed $I_d - V_g$ measurement had been carried out by [16] to analyse the reliability of a device with a variation of the metal gate thickness. In agreement to the current work, thicker TiN results in higher interface trap concentration. It had been found that for thick TiN metal gates, high interface density at high stress temperatures was evident due to stress from the metal nitride layer. This stress is as a result of the agglomeration effect which evolves from the growing of the crystallites of TiN films which in turn causing elastic deformation and thus causing stress in the TiN metal layer. The increasing of the TiN gate thickness results in the increase of the nitrogen species diffusion towards the Si interface which enhances degradation. The mechanism of this effect is as follows; when the nitrogen species diffuses towards the $Si0_2$/Si interface, the carrier mobility is degraded by

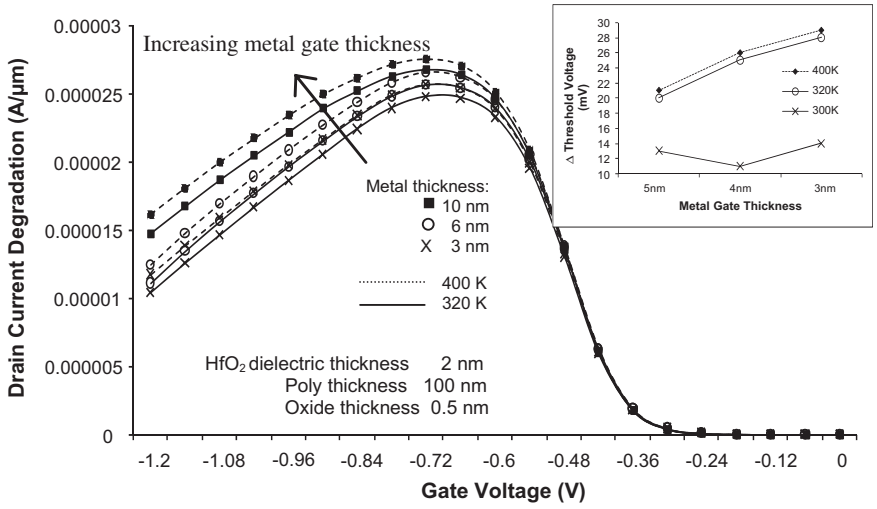

Fig. 7. Drain current degradation of the 45 nm high-k PMOS stressed at temperatures 320 K and 400 K. The metal gate thickness had been varied at 3 nm, 6 nm and 10 nm.

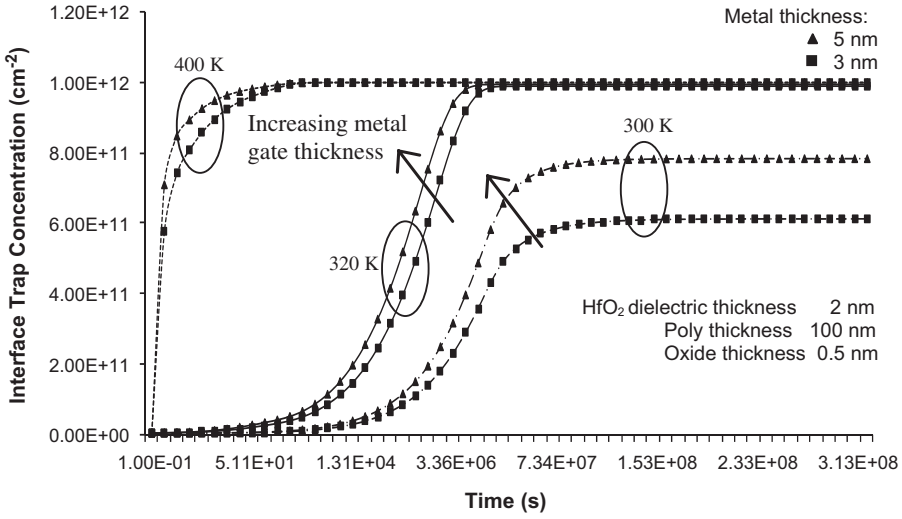

Fig. 8. Interface trap concentration of the 45 nm high-*k* PMOS stressed at temperatures 300 K, 320 K and 400 K. The metal gate thickness had been varied at 3 nm and 5 nm.

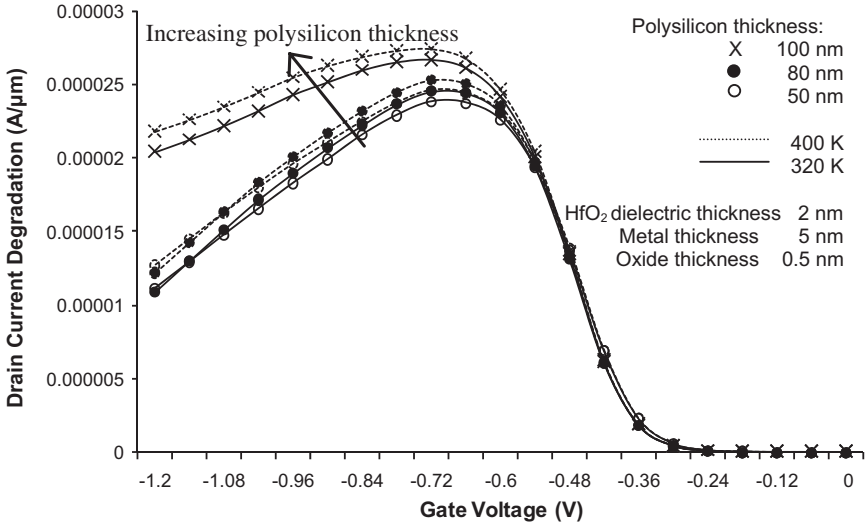

Fig. 9. Drain current degradation of a 45 nm high-*k* PMOS stressed at temperatures 320 K and 400 K for a variation of polysilicon thickness.

means of the coulomb-scattering mechanism. The degradation of the carrier mobility results in the hole trapping which governs the effect of NBTI. The inset figure in Fig. 7 shows the threshold voltage shifts for a variation of the TiN metal gate layer thickness. It can be observed that as the metal gate becomes thinner, the threshold voltage shift becomes more significant. Thinner TiN layer would result in lesser diffusion of nitrogen as described above and elaborated by [17]. This will lead to lower electronegativity [18] of the nitrogen atoms which in turn lowers the workfunction. Hence, as TiN becomes thinner, the threshold voltage of the device moves to a higher negative value and thus suggesting that the thinner TiN has a lower workfunction.

3.1.4. Influence of polysilicon thickness on NBTI

The polysilicon thickness in this work had been varied at 100 nm, 80 nm and 50 nm. Figs. 9 and 10 show that the NBTI effect is increased as the polysilicon thickness is increased. The device with the polysilicon thickness of 100 nm exhibits a significant current degradation when it is biased at high negative voltage, irrespective of the stress temperature. For thinner devices with polysilicon thicknesses of 80 nm and 50 nm, the device degradation is significant when biased at higher temperature, which is 400 K in this work. It is observed that as the polysilicon layer thickness is increased, the interface trap density increases. This may be due to the diffusion of Si from the polysilicon layer towards the high-*k* dielectric layer [19]. There are reports claiming that the device should be built with a single metal electrode layer without the deposition of polysilicon on top [20] but this may result in stress-induced damage [21]. In order to improve the thermal stability of the electrode, the polysilicon/TiN stack is to be incorporated and the polysilicon layer thickness needs to be optimized in order to obtain better device reliability.

3.2. Process variation of device

From the Fig. 11, it is observed that the advanced-process flow, which incorporates millisecond laser annealing and process-induced stress, results in less drain current degradation as compared to the conventional process flow. The former process flow exhibits less amount of shift in the threshold voltage as the stress temper-

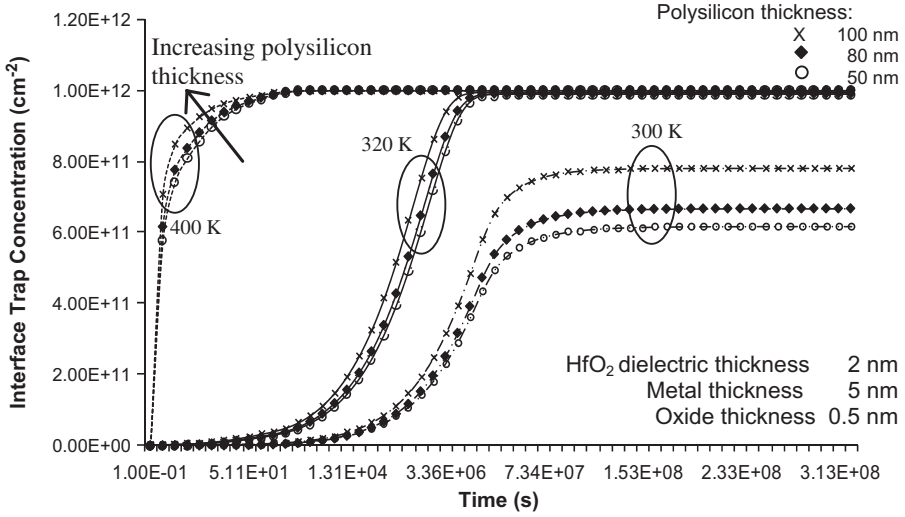

Fig. 10. Interface trap concentration of a 45 nm high-*k* PMOS stressed at temperatures 320 K and 400 K for a variation of polysilicon thickness.

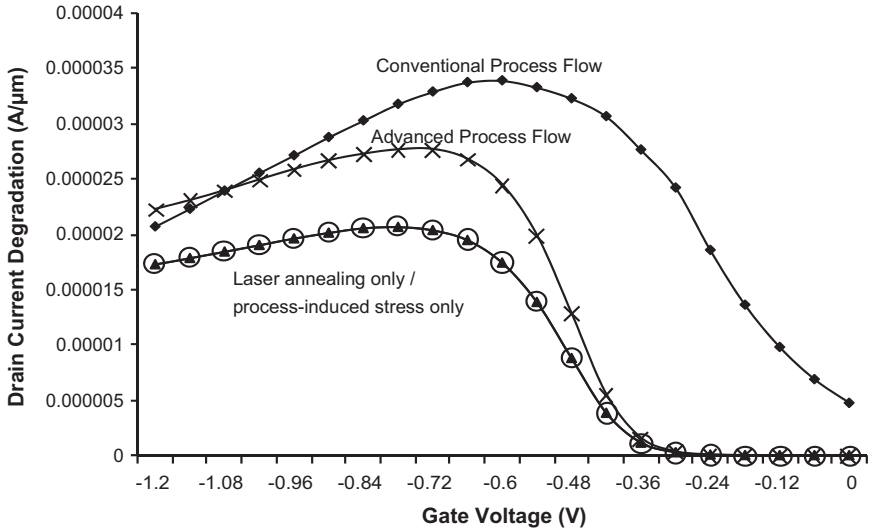

Fig. 11. Comparison of drain current degradation of a conventional-process 45 nm high-*k* PMOS with advanced-process 45 nm high-*k* PMOS when stressed at 400 K.

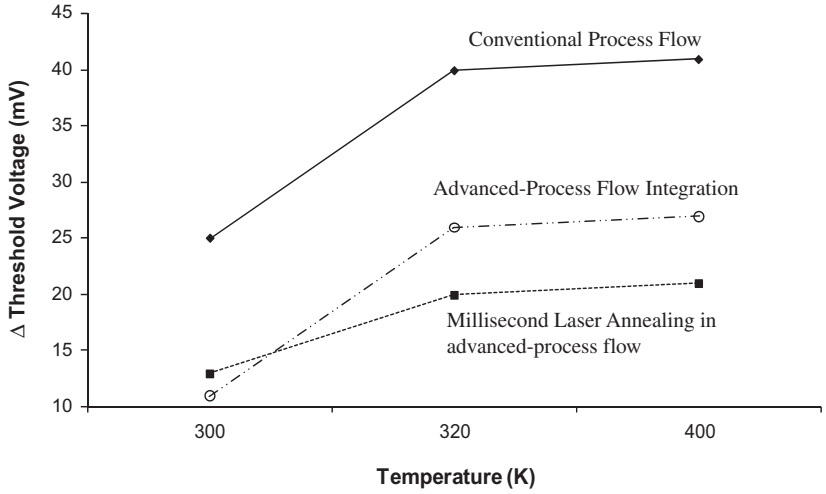

Fig. 12. Threshold voltage shift for different process flows of the high-*k* PMOS device.

ature is increased, as shown in Fig. 12. The incorporation of the millisecond laser annealing promotes device reliability due low interfacial state density [22]. It can be deduced that the incorporation of millisecond laser annealing and process-induced stress favours the reduction in the NBTI effect of the 45 nm high-*k* device.

4. Conclusions

This paper presents the NBTI degradation analysis on geometric and process variation on an advanced-process 45 nm PMOS device. The drain current degradation and threshold voltage shift were observed to increase considerably when the device is stressed at 400 K and the increase in degradation is more significant as the thickness of the dielectric layer, oxide layer and metal layer increases. It is also shown that the NBTI degradation is less for an advanced-process device, by which laser annealing and process-induced stress are incorporated, as compared to a device which employs a conventional process flow.

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