Electric Power Components and Systems, 38:1546–1557, 2010

ISSN: 1532-5008 print/1532-5016 online
DOI: 10.1080/15325008.2010.482092

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A Simple Approach of Space-vector Pulse Width Modulation Realization Based on Field Programmable Gate Array

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Abstract *Employing a field programmable gate array to realize space-vector pulse width modulation is a solution to boost system performance. Although there is much literature in the application of three-phase space-vector pulse width modulation based on field programmable gate arrays, most is on conventional space-vector pulse width modulation with designs that are complicated. This article will present a simple approach to realize five-segment discontinuous space-vector pulse width modulation based on a field programmable gate array, in which the judging of sectors and the calculation of the firing time are simpler with fewer switching losses. The proposed space-vector pulse width modulation has been successfully designed and implemented to drive on a three-phase inverter system that is loaded by an induction machine of 1.5 kW using the APEX20KE Altera field programmable gate array (Altera Corporation, San Jose, California, USA).*

Keywords electric drives, field programmable gate array applications, motor controls, power converters, space-vector pulse width modulation

1. Introduction

The space-vector pulse width modulation (SVM) method is an advanced pulse width modulation (PWM) method and is the best among all the PWM techniques in the application of variable frequency drives. SVM provides a better fundamental output voltage, better harmonic performance, and is easy to implement [1–13]. In recent years, the SVM method has gradually obtained widespread application in power electronics and electrical drives due to its superior performance characteristics. Compared with sinusoidal pulse width modulation (SPWM), SVM is more suitable for digital implementation because the obtainable DC voltage utilization ratio can highly be increased. As the

Received 26 August 2009; accepted 23 March 2010.
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result, a better voltage total harmonic distortion (THD) factor can be obtained [1, 2, 10–12, 14]. A comparison of switching losses P_L, junction temperature of the insulated-gate bipolar transistor (IGBT) T_J, and weighted THD of the different modulation schemes are shown in Table 1 [15]. From the comparison, the discontinuous SVM shows the lowest switching losses and the lowest junction temperature of the IGBT compared with SPWM and conventional SVM, although it has a slightly higher weighted THD compared with the conventional SVM method.

In most engineering practices, the SVM algorithm is mainly implemented through software based on microcontroller or digital signal processors (DSPs) [16–18]. From here, designers must sequentially perform the control procedure by exploiting their mathematically oriented resources. The instructions of different procedures need to be executed one after the other. Thus, the purely software-based technique is not an ideal solution. The field programmable gate array (FPGA) is an appropriate alternative over analog and software solutions (DSP and microcontroller) [19–24], and its architecture offers a significant integration density [25] within a flexible programmable environment. Designers can get a new degree of freedom by the applying the FPGA in SVM, because the dedicated hardware architectures of the FPGA matches all of the requirements in terms of control performance as well as the implementation constraints [19]. Employing the FPGA in SVM strategies provides many advantages, such as shorter design cycle, fair cost, rapid prototyping, simpler hardware and software design, and higher switching frequency. Differing with the software implementation, the FPGA performs the entire procedure with a concurrent operation (allowing parallel processing by means of a hardware mode and not occupying) by using its reconfigurable hardware. With its powerful computation ability and flexibility, an FPGA is quite mature in the application of electrical drives, and it is considerable as a solution to boost the system performance when including the SVM algorithm [6, 19, 26–29].

The digital hardware FPGA-based solution has been widely implemented in many control applications, including SVM realization [6, 19, 26–29]. However, conventional SVM suffers from drawbacks such as computational burden, inferior performance at high modulation indices, and high switching losses of the inverters. Hence, to reduce the switching losses and to improve the performance in the high-modulation region, several discontinuous SVM methods have been proposed [5, 15, 30–32].

Literature on the implementation of three-phase conventional SVM and discontinuous SVM based on the FPGA is not lacking. However, most of the designs are based on conventional SVM without consideration of the hardware-resource saving and are more complex. In this article, new approaches of FPGA-based SVM will be discussed, where the judging of sectors and the calculation of the firing time to generate the

Table 1
Comparison of switching losses, temperature, and weighted THD of the different modulation schemes [15]

Parameters	SPWM	Conventional SVM	Discontinuous SVM
Switching losses P_L (per unit of SPWM)	1.00	1.33	0.83
T_J (increase, °C)	35	45	32
Weighted THD (%)	4.0	1.8	2.9

SVM waveform is simple with low switching losses and hardware-resource saving. A novel five-segment discontinuous SVM design based on the basic idea from [33] and [18] is proposed, and the scheme with lower switching losses and a simpler algorithm is implemented through the APEX20KE Altera FPGA (Altera Corporation, San Jose, California, USA).

2. Novel Method of SVM Algorithm

The conventional principle of the SVM algorithm relies too much on the judging of sectors, and firing time (duration of active vectors) calculation and the method of switching sequence generation is too complex. As a solution to overcome the problems from the conventional SVM algorithm, this article proposes the principle of a symmetrical five-segment discontinuous switching sequence that has not yet been revealed as a novel method of SVM algorithm.

2.1. *Proposed SVM Switching Pattern (Five-segment Discontinuous Switching Sequence)*

Many discontinuous SVM patterns have been reported [5, 6, 30, 31, 34]. However, these patterns performed with high switching losses and used a complicated algorithm that is not easily implemented based on an FPGA. In this article, a novel symmetric five-segment discontinuous SVM is proposed, the design of which mainly originated from the ideas of [33] and [18]. The pattern has been successfully implemented by Yu based on DSP [18]. This pattern resulted in lower switching losses, a simpler algorithm, and easy implementation. Therefore, this article will focus on implementation of a discontinuous SVM pattern based on an FPGA in order to boost system performance. In this proposed pattern, there is always a leg that stays constant for the entire PWM period. The state sequence in this pattern is X-Y-Z-Y-X, where Z = 1 in Sectors I, III, and V; Z = 0 in the remaining sectors. Thus, the number of switching times for this pattern is less than the conventional pattern, and the obvious result is reduced switching losses.

2.2. *Proposed Identification of the Sector*

There are many different methods to judge the sector where the reference space voltage vector lies. Zhi-pu [35] compared the reference space vector's angle with 0°, 60°, 120°, 180°, 240°, and 300° to obtain the number of the sector where V_{ref} is Yu *et al.* [36], Jiang *et al.* [37], and Xing and Zhao [7] obtained the sector number by analyzing the relationship between V_α and V_β. To determine the sector, the inverse Clark transformation is used for the calculation of projections V_a, V_b, and V_c of V_α and V_β in the (a, b, c)-plane, as follows:

$$\begin{cases} V_a = V_\beta \\ V_b = \dfrac{\sqrt{3}V_\alpha - V_\beta}{2} \\ V_c = \dfrac{-\sqrt{3}V_\alpha - V_\beta}{2} \end{cases} . \tag{1}$$

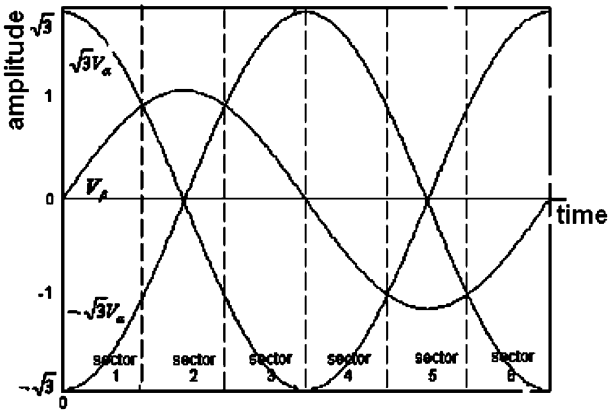


Figure 1. The plotting of $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ wave.

Then, based on Eq. (1), $N = \text{sign}(V_a) + 2 * \text{sign}(V_b) + 4 * \text{sign}(V_c)$, mapping N to the actual sector of the output voltage reference by referring to the following relationship:

N	1	2	3	4	5	6
Sector	II	VI	I	IV	III	V

In [38], Zeliang *et al.* adopted two new intermediate vectors X_α and X_β, whereby $X_\alpha = \frac{3}{2}V_\alpha$ and $X_\beta = \sqrt{3}V_\beta$. Decomposing the conventional SVM will properly counteract the redundant calculations to identify sector location, but it results in complicated matrix calculations. In this article, by analyzing on the principle of SVM in [7, 36–38] and to reduce the burden of computation, a new method to determine the sectors of voltage vectors based on a comparison between V_β, $\sqrt{3}V_\alpha$, $-\sqrt{3}V_\alpha$, and 0, as shown in Figure 1, is proposed. Through the comparison, sectors of voltage vectors, as shown in Table 2, can be determined.

2.3. *Determination of the Duration of Active Vectors*

The space-vector technique synthesizes a desired vector V_{ref} from two adjacent actives, V_α and V_β (among V_1 and V_2, as shown in Figure 1) during time interval T_a and T_b. The

Table 2
Proposed identification of the sectors

Sector	Vector angle	$V_\beta > 0$	$V_\beta > \sqrt{3}V_\alpha$	$V_\beta > -\sqrt{3}V_\alpha$
I	(0°, 60°)	1	0	1
II	(60°, 120°)	1	1	1
III	(120°, 180°)	1	1	0
IV	(180°, 240°)	0	1	0
V	(240°, 300°)	0	0	0
VI	(300°, 360°)	0	0	1

Note: 1: satisfied; 0: not satisfied.

Table 3
Switching time of the active vector for each sector

Sector	T_a	T_b	$T_a + T_b$
I	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
II	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
III	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
IV	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
V	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
VI	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$

null vectors (V and V_7) are also applied to reduce the inverter switching frequency. In the proposed design, only one null vector is inserted in a PWM period, whereby V_7 is used for odd sectors and V for even sectors:

$$V_{ref} = V_\alpha + jV_\beta = \frac{2T_a}{T}V_\alpha + \frac{2T_b}{T}, \tag{2}$$

$$\frac{T}{2} = T_a + T_b + T_0. \tag{3}$$

Hence, the half PWM period T is composed of the switching times T_a, T_b, and T. The total time of the null vectors can be expressed as

$$T_0 = \frac{T}{2} - T_a - T_b. \tag{4}$$

In this design, the switching times of the active vectors for each sector can be calculated as shown in Table 3.

2.4. Proposed SVM Switching Sequence Generating Method Based on Calculation of the Duration of Active Vectors

In this article, a new method of SVM switching sequence is proposed, whereby the PWM signal for odd sectors are realized through comparison between the triangle waveform with T_a and $T_a + T_b$. A high signal will be generated when the triangle waveform is higher than signal A or B, and another leg is always set to 1. For even sectors, the generation of the PWM signal is a complement to the odd sectors, whereby the signal will be set high when the triangle waveform is lower than signal A or B and another leg is set to 0.

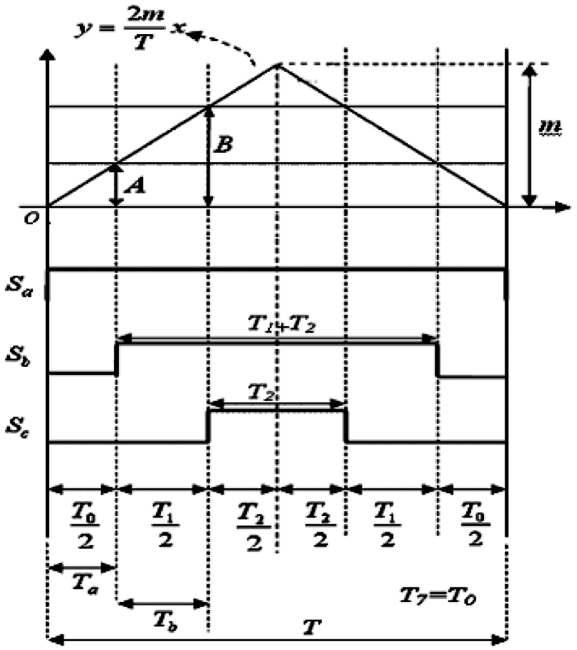


Figure 2. Proposed SVM switching sequence generating method.

To simplify the design process, the term $\frac{2m}{T}$ will set to 1 so that y will be always equal to x ($x = \frac{T_0}{2} = T_a$, then $y = x = T_a$; and if $x = \frac{T_1}{2}$, then y = $\frac{T_1}{2} = T_b$). Obviously if $x = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$, then $y = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$. Therefore, the generation of PWM for S_b and S_c legs in Sector I can be obtained by comparing the triangle waveform with T_a, and $T_a + T_b$, respectively, and the S_a leg is set to 1 due to the odd sector position, as shown in Figure 2.

3. FPGA Implementation of Proposed Novel SVM

After the discussion on the principle of SVM generation, this section focuses on the implementation of an FPGA in SVM. The overall proposed SVM design is shown in Figure 3. It can be seen from this figure that the design consists of five blocks or modules, namely *ajust_freq*, *Vbeta_Valfa*, *find_sector*, *SVM_generator*, and *deadtime_sytem module*. Each of these modules is explained in the following subsections.

3.1. First Module: ajust_freq

From Figure 3, the function of *ajust_freq* is to generate a suitable clocking frequency. In the proposed SVM design, this module functions as a frequency divider by generating a carrier frequency of 20 kHz and a fundamental frequency of 50 Hz from the FPGA board, which have a clocking signal of 33.33 Mhz. Since the triangle signal generator in this design is sampled to be 32 times per period, in order to get a carrier frequency of 20 kHz, the main clock generator from the FPGA board was divided by 13 (33.33 MHz: $(13 \times 32) = 20$ kHz).

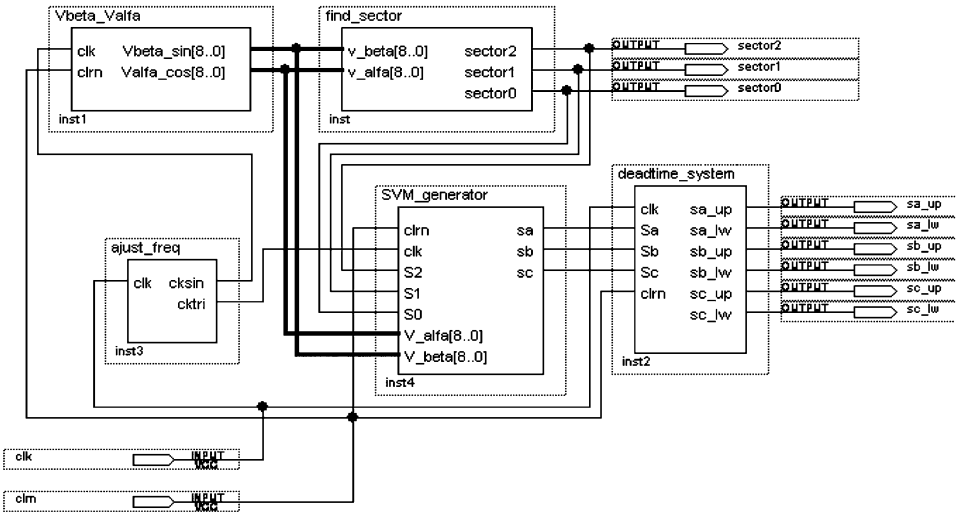


Figure 3. Overall of the proposed SVM design.

3.2. *Second Module:* Vbeta_Valfa

In the proposed method, V_{alfa} and V_{beta} are generated based on sine and cosine functions through the look-up table (LUT) with a memory mapping of 360 addresses. There are three lines, categorized as lower, base, and upper, that are represented with 96, 224, and 352, respectively, into 9 unsigned bits. With the memory mapping of 360 addresses, the counter mod-360 will used to count the LUT of V_{alfa} and V_{beta}.

3.3. *Third Module:* find_sector

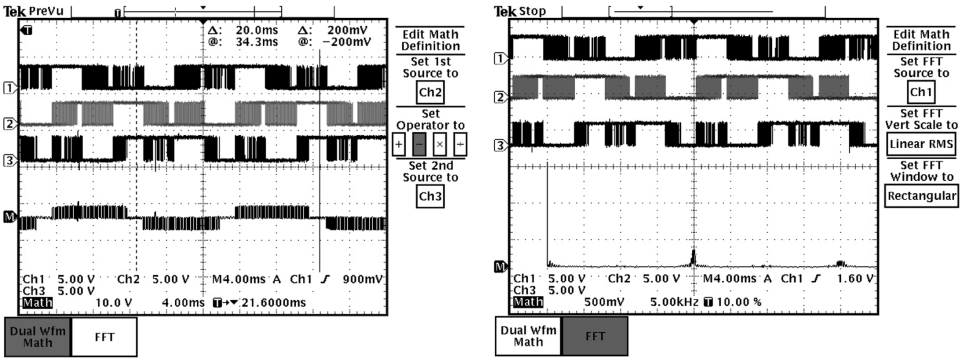
Due to the different switching time equations, a reference voltage sector is necessary. The sector finder (SF) module in this design is used to judge the reference vector sector by referring to Table 2. This module determines the number of sectors and simplifies the truth table by comparing the above-mentioned results.

3.4. *Fourth Module:* SVM_generator

This module was divided into four sub-modules, namely *Triangle*, *Duration_Ta*, *Duration_TaTb*, and *SVM pattern* modules. The *Triangle* module functions as a triangle signal generator. In the proposed SVM design, one period of triangle signal generation is sampled 32 times and is represented in the digital number of 9 unsigned bits with lower (in this case, it is the same with the base number) and upper numbers of 224 and 352, respectively. The *Duration_Ta* and *Duration_TaTb* modules are digital solutions for each second and fourth column, respectively. Finally, the *SVM pattern* module is used to generate the SVM sequence as described in Section 2.4.

3.5. *Fifth Module:* deadtime_system

A dead-time of at least 2 μs is required to avoid short circuit within a leg. A combination



(a) (b)

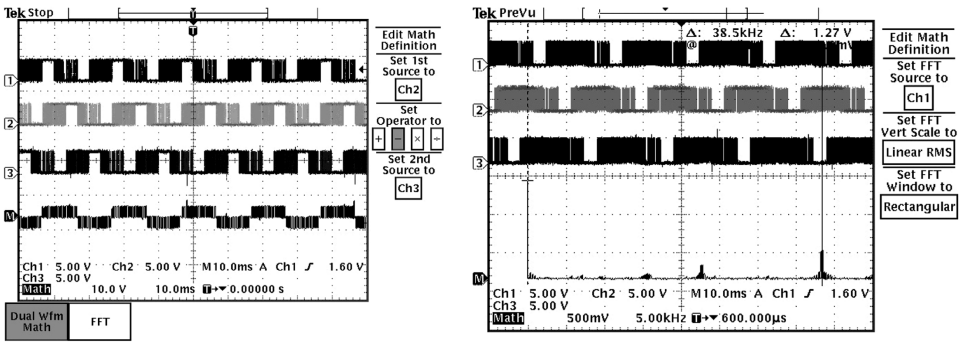
Figure 4. Hardware implementation of proposed SVM generator at carrier frequency 20 kHz: (a) the switching state and its line to line and (b) the signal gating and its frequency spectrum.

of a 16-bit counter and a 16-bit comparator is used to construct the dead-time generator for each leg.

4. Results and Discussions

In this research, the proposed SVM generator with different carrier frequencies was successfully carried out using of the APEX20KE Altera FPGA. Figure 4 shows the results from hardware implementation with this proposed SVM generating method at carrier frequency of 20 kHz. Probes 1, 2, and 3 in Figures 4(a) and 4(b) are represented as switching states of S_a, S_b, and S_c, respectively, whereby probe M is a $(S_a + S_b)$ line-to-line switching state with its frequency spectrum. The harmonics due to the 20 kHz switching frequency are clearly visible in Figure 4(b).

A similar condition is shown in Figure 5. In this case, the carrier frequency is set to 40 kHz, although the result in Figure 5(b) shows 38.5 kHz (an error of 3.75%). A



(a) (b)

Figure 5. Hardware implementation of proposed SVM generator at carrier frequency 40 kHz: (a) the switching signals and line-to-line switching and (b) the signal gating and its frequency spectrum.

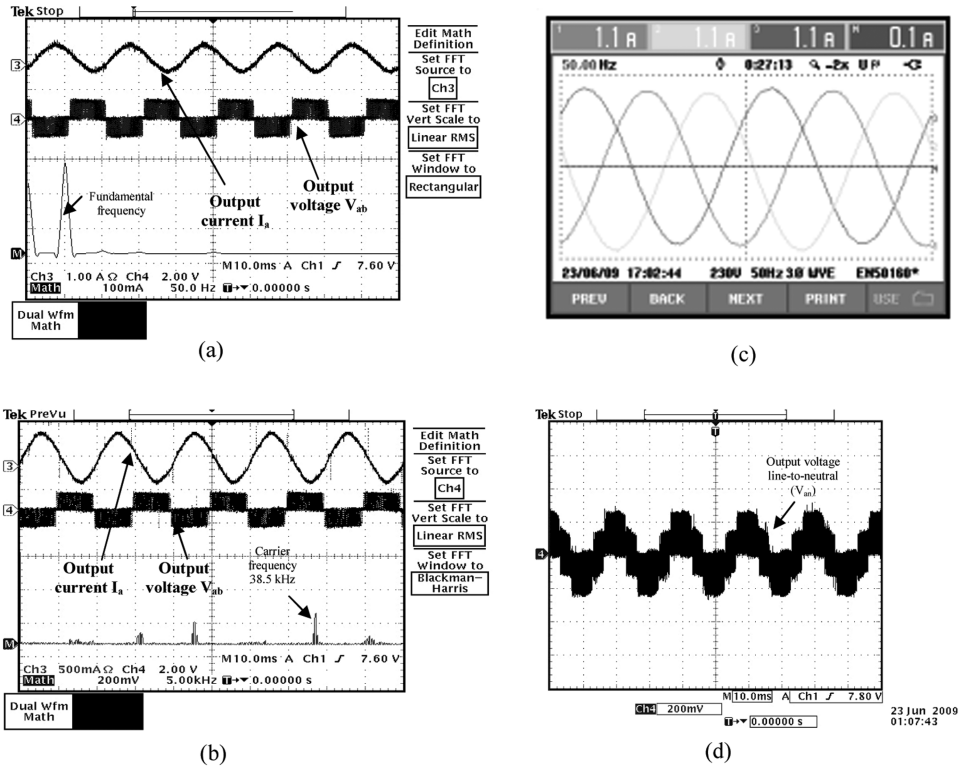


Figure 6. The performance of FPGA-based proposed SVM generator design: (a) output current and voltage, (b) frequency spectrum, (c) output threephase current, and (d) output voltage line to neutral.

three-phase inverter system together with an induction machine of 1.5 kW is used to test the performance for the proposed SVM-generator-based FPGA design.

Figure 6 shows the practical result for output stator current (I_a), output phase-to-phase voltage (V_{ab}), frequency spectrum, output three-phase current, and output voltage line-to-neutral (V_{an}). The results show that this proposed SVM-generator-based FPGA design is successful when implemented through a hardware platform.

Furthermore, a comparison of current and voltage THD between the proposed SVM and other SVMs is shown in Table 4. From the table, the proposed SVM shows a lower percentage in current and voltage THD compared with other SVMs. However, the current THD from the proposed SVM (6.4%) is slightly higher than the hybrid type IV proposed by Zhao *et al.* [40], which is 6.34%. In addition, the voltage THD is 11.10% and is slightly higher than the pattern III proposed by Bharatiraja *et al.* [34] with 9.90%

5. Conclusion

This article mainly presents the design and realization of a simple five-segment discontinuous SVM based on the application of an FPGA. The judging of sectors and the calculation of the firing time to generate the SVM waveform become simpler, and switching losses can also be reduced by using this new approach of SVM-based

Table 4
Comparison of current and voltage THD between the proposed SVM and other SVMs

Strategy	Current THD (%)	Voltage THD (%)
Proposed SVM based on FPGA	**6.4**	**11.10**
Bharatiraja *et al.* [34]		
Pattern I	15.07	17.60
Pattern II	19.31	**9.90**
Pattern III	23.96	24.27
Saad *et al.* [39]		
Rising-edge aligned sequence scheme (SVM1)	Not reported	54.49
Falling-edge aligned sequence scheme (SVM2)	Not reported	54.47
Symmetric aligned sequence scheme (SVM3)	Not reported	54.45
Alternative sequence scheme (SVM4)	Not reported	39.86
Zhang and Yu [31]		
Three-segment SVM	Not reported	69.38
Five-segment SVM	Not reported	68.52
Seven-segment SVM	Not reported	66.59
Narayanan *et al.* [32]		
Conventional SVM	20.29	Not reported
Discontinuous SVM	15.37	Not reported
Three-zone hybrid PWM	13.00	Not reported
Five-zone hybrid PWM	12.72	Not reported
Seven-zone hybrid PWM	12.58	Not reported
Zhao *et al.* [40]		
Conventional SVM	10.07	Not reported
Minimum switching loss PWM (MSLPWM)	10.11	Not reported
Discontinuous SVM	7.64	Not reported
Hybrid type I	6.43	Not reported
Hybrid type IV	**6.34**	Not reported

FPGA. The proposed SVM scheme has been successfully designed and implemented through the APEX20KE Altera FPGA without computing the number and angles of each sector as well as the commutation pattern. A three-phase inverter system loaded by an induction machine of 1.5 kW was successfully driven by the proposed design with a carrier frequency up to 40 kHz.

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