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Abstract

Ultra-fast solid electric double layer capacitors (EDLCs) have been developed in both sandwich and planar interdigitated configurations using vertically-oriented graphene nanosheet (VOGN) electrodes with a hydroxide ion-conducting tetraethylammonium hydroxide (TEAOH)-polyvinyl alcohol (PVA) polymer electrolyte. These solid-state EDLCs could be scanned at a rate of 1000 Vs^{-1} in cyclic voltammetry and demonstrated response times of less than 1 ms. They retained high performance over 18 months of shelf storage and after 100,000 charge/discharge cycles with limited packaging, demonstrating the high stability of TEAOH-PVA electrolyte. The solid-state capacitors are capable of

performing at elevated temperatures and have demonstrated a response time of 0.35 ms at 90 °C. Given their ultra-fast rate capability, excellent shelf-life and cycle life, and excellent temperature stability, these solid-state EDLCs are promising smaller and lighter alternatives to the bulky electrolytic capacitors now used for ac line-filtering.

1. Introduction

In modern electronics, removing voltage fluctuations (rectification ripple) is necessary when converting alternating current (AC) to direct current (DC). Generally a capacitor is used for this purpose. The present solution for 120 Hz power filtering (double the value of the 60 Hz standard ac line frequency in the United States) is electrolytic capacitors. However, these devices are bulky and generally have low reliability.

Electric double layer capacitors (EDLCs), often referred to as supercapacitors or ultracapacitors, have much higher volumetric charge storage and high reliability compared with electrolytic capacitors and potentially allow for a size reduction. For an EDLC to be capable of efficient ac line-filtering, its impedance phase angle at 120 Hz must be near -90°. Typical EDLCs based on porous activated carbon electrodes perform poorly at this frequency and exhibit an impedance phase angle near 0°.This is primarily due to use of high-surface-area electrode material, which leads to distributed charge storage (porous electrode behavior) with a resulting response time of approximately 1s.

Efficient ac line-filtering by an EDLC was first demonstrated in 2010 using vertically-oriented graphene electrodes [1]. Both series resistance and distributed charge storage were minimized to reach this level of performance. Since then, various materials, including carbon black, exfoliated graphene, reduced graphene oxide, activated reduced

graphene oxide, graphene/carbon nanotube carpets, and others, have been used to achieve ac line-filtering performance [2-9]. Most of these studies used liquid electrolytes, which presents practical problems related to creating packaged, multi-cell EDLCs. Replacing liquid electrolytes with solid-state polymer electrolytes overcomes these practical problems needed to create next-generation EDLCs.

Earlier, we demonstrated a tetraethylammonium hydroxide (TEAOH)-based polymer electrolyte that outperformed widely-used KOH-based systems[10]. In this study, we leveraged this polymer electrolyte and vertically-oriented graphene nanosheet (VOGN) electrodes to demonstrate solid-state EDLC cells in both "sandwich" and planar interdigitated configurations. The TEAOH-polyvinyl alcohol (PVA) polymer electrolyte has relatively high ionic conductivity (5-10 $mScm^{-1}$), good film forming capability, and high environmental stability [10] while the VOGN electrodes exhibit minimum distributed charge storage behaviour as well as low electronic resistance[1, 11]. We combined the advantages of these two elements to achieve high-rate, solid-state EDLCs. The developed solid-state capacitors were tested at room temperature for shelf-life and cycle stability as well as high-temperature stability.

2. Material and Methods

2.1 Preparation of TEAOH-PVA polymer electrolyte

A polymer electrolyte precursor solution was prepared by mixing 5% PVA (MW=145,000) aqueous solution and a TEAOH solution at room temperature. Based on our previous study, an optimized TEAOH-PVA electrolyte composition of ca. 81 wt% TEAOH and ca. 19 wt% PVA was used[10].

2.2 Preparation of VOGN electrodes and construction of solid cells

The electrodes were VOGN grown on Ni by microwave plasma enhanced chemical vapor deposition on either round discs or rectangular plates [11-13]. Both solid-state sandwich and solid-state planar interdigitated EDLCs were fabricated as shown in Fig. 1. In the latter case, laser ablation was used to cut a 20-μm-wide gap through the VOGN and the 1-μm thick nickel current collector below it. The planar cell capacitance was 30-35 $\mu Fcm^{-2}$for an electrolyte of 1 M tetraethylammonium tetrafluoroborate salt in acetonitrile or propylene carbonate solvent[13].

The solid-state sandwich cell was constructed using the following steps: (i) The electrolyte precursor solution was coated onto the VOGN round discs electrodes via solution casting. (ii) Two electrolyte-coated electrodes were fused together for 20 minutes at ambient temperature under 20 to 30 kPa pressure. (iii) An insulating tape was applied to cover the cell for protection. Typical VOGN spacing is ca. 200 nm and the height ca. 1 μm. The geometric area of the electrodes is 1.27 cm^2.

The solid-state $1cm^2$ planar interdigitated EDLC was constructed by drop casting a measured volume of polymer electrolyte precursor solution onto the electrode surface. The water from the precursor solution was allowed to evaporate at room temperature, forming a polymer electrolyte layer covering the interdigitated pattern (Fig. 1).

2.3 Electrochemical characterizations

All cells were characterized using cyclic voltammetry (CV), galvanostatic charge/discharge (GCD), and electrochemical impedance spectroscopy (EIS). CV and GCD was performed either using a CHI 760D bipotentiostat or an EG&G PAR 263A potentiostat/galvanostat. EIS was performed using a Solartron 1255 frequency response

analyzer interfaced with the EG&G 263A. The EIS spectra were recorded from 100 kHz to 1 Hz with 5 mV amplitude under zero-volt bias. Unless otherwise specified, electrochemical experiments were carried out at room temperature.

For the shelf-life study, the solid-state cells were stored in a controlled condition of 25 °C and 45% (±3%) relative humidity. A temperature/humidity chamber (Espec SH-241) was used to conduct thermal stability tests from 25 to 100 °C (10 °C interval, 50% relative humidity) with a 30 min equilibrium time at each temperature.

3. Results and discussion

Detailed structure and morphologies of the VOGN were reported previously [1, 11-13]. Characterizations of the solid-state sandwich EDLC focused on its rate capability, cycle life, and shelf life. Studies on a solid-state planar EDLC focused on performance at higher temperatures.

3.1 Solid-state sandwich EDLC

The CVs (normalized by capacitance) of the solid-state sandwich EDLC at different scan rates are depicted in Fig. 2a. All CVs showed a near rectangular profile. The device was able to charge and discharge at anultra-high rate of 1000 Vs^{-1}. At this rate, the EDLC exhibited a capacitance of ca. 80 μFcm^{-2}, 65% of the capacitance at 1 Vs^{-1}. Although the profiles of the solid-state device appeared slightly tilted with increasing scan rate, the combination of easily accessible VOGN electrodes (especially on the edge plane of the graphene sheets) and the highly conductive TEAOH-PVA polymer electrolyte enabled extremely fast ion transport.

Charge/discharge curves of the solid-state sandwich EDLC under different current densities are shown in Fig. 2b. The linearity and symmetry of the curves confirmed the

capacitive nature of the device, in good agreement with the CV results (Fig. 2a). Also shown in Fig. 2bis the discharge capacitance calculated from the slope of the discharge curves. For example, the capacitance was 119 μFcm^{-2} under a current density of 0.39 $mAcm^{-2}$. A ten-fold increase in current density led to only a 10% reduction in capacitance. More importantly, the extremely small charge/discharge times in the range of milliseconds demonstrated the rapid charge/discharge characteristics of this solid-state EDLC.

The cycling stability of the solid-state EDLC was investigated using GCD and EIS. Nyquist plots of the capacitor before and after 100,000 charge/discharge cycles are shown in Fig. 3a, with an expanded view in the inset. Both sets of data exhibited a nearly vertical line, suggesting an almost ideal capacitor having an equivalent circuit model of a series-RC circuit. No features associated with porous electrode behavior were observed. The equivalent series resistance (ESR), i.e. data intersection with the real axis, decreased from 0.95 to 0.85Ωcm^2after the cycling, which may be due to improved contact at the electrode-electrolyte interface. The Bode plots of the EIS results are shown in Fig. 3b. Curves from before and after cycling overlap, confirming the excellent cycleability of this solid-state EDLC. The impedance phase angle of this solid-state EDLC reached -45° at ca. 1,585 Hz, which can be translated into a 0.63 ms response time. At 120 Hz, the impedance phase angle was -81°. These results demonstrate the fast response of this solid-state capacitor and the retention of high performance during 100,000 charge/discharge cycles.

To study the shelf-life stability of the solid-state EDLC, further analyses were performed. Assuming a series-RC circuit model and using the impedance data, cell

capacitance was calculated as $C=-1/(2\pi fZ'')$, where f is frequency in Hz and Z'' is the imaginary part of the impedance. Capacitance versus frequency at various times during shelf-storage is plotted in Fig. 4. For the initial measurements, capacitance increased from 40 μFcm^{-2} at 10^4 Hz to 110 μFcm^{-2}at 1 Hz and the capacitance at 120 Hz was approximately 86 μFcm^{-2}.Measured resistance at 120 Hz was 1.9 Ω, which yields an RC time constant of 0.16 ms. This capacitor was tested again after 9 and 18 months of storage. After 9 months, the capacitor showed about 74 μFcm^{-2} with a series resistance of 2.9 Ω, yielding an RC time constant of 0.22 ms. After 18-month storage, the capacitor appeared to perform better at high frequency than it did after 9 months. This demonstrates the excellent stability of TEAOH-PVA electrolyte[10]. Both Fig. 3 and 4 provide strong evidence that the developed solid-state EDLC exhibits excellent cycleability and a long shelf-life with minimal packaging. Further investigations are needed to understand shelf-life details.

3.2 Solid-state planar interdigitated EDLC

The conventional sandwich configuration is not optimal for capacitor cells made with VOGN electrodes because of the low volumetric efficiency[13].A planar design offers volumetric advantages since it can greatly reduce the non-active volume. Laser ablation can be used to cut interdigitated patterns on the VOGN surface, creating two electrodes from a single electrode on the same substrate (Fig. 1).

Similar characterizations were performed for the sandwich EDLC. Fig. 5a shows the CVs of a solid-state planar EDLC at different scan rates. At 1 Vs^{-1}, this capacitor had a capacitance of ca. 45 μFcm^{-2}, which is in the same range reported for this type of cell using organic electrolytes[13]. A further increase in scan rate caused a reduction in

capacitance, as shown by the CV at 1000 Vs^{-1}. Fig. 5b shows the capacitance of the planar EDLC as a function of frequency. At 1 Hz, the capacitance was 40 μFcm^{-2}, consistent with the CV results (Fig. 4a). At 120 Hz, the capacitance was 32μFcm^{-2} and the resistance was 7.8 Ω, yielding a RC time constant of 0.25 ms.

The performance of the solid-state planar EDLC at elevated temperatures is presented in Fig. 6. CV studies were conducted on the solid-state capacitor at an ultra-high rate to explore the performance limitations of this device. Fig. 6a shows the CVs at a scan rate of 1000 Vs^{-1}at temperatures up to 100 °C. This cell showed rectangular CV profiles. Capacitance increased from 30 to 45 μFcm^{-2}, while the ESR decreased as observed from the less tilted CVs. Even at 100 °C, the solid-state capacitor demonstrated capacitive behaviour. EIS analyses showing the capacitance of the solid-state planar capacitor at different temperatures is depicted in Fig. 6b. The overall trend was a capacitance increase with temperature. At 120 Hz, the capacitance increased from 30 to 46 μFcm^{-2} across the tested temperature range (see Fig. 7a). However, a reduction in high-frequency capacitance was observed at 100 °C, which is believed to be due to reduced ionic conductivity of TEAOH-PVA caused by its dehydration. Ion conduction in TEAOH-PVA is strongly dependent on the presence of free water molecules.

Also shown in Fig. 7a is the ESR of the capacitor as a function of temperature. Resistance continuously declined until reaching its minimum at 90 °C, followed by an increase at 100 °C. This is in a good agreement with the trends observed in Fig. 6b, suggesting the optimum operating temperature of this solid-state capacitor should be below 100 °C. Fig. 7b shows the response time calculated at a frequency where the phase angle was -45° as a function of temperature. Similar to the trend of ESR, the fastest

response occurred at 90 °C, primarily due to the minimum ESR value occurring at this temperature. The temperature-dependent behaviour of the response time was more dominated by the reduction in resistance rather than the increase in capacitance: From 25 to 100 °C, ESR decreased more than 65%, while capacitance increased less than 50%. Nonetheless, the response time of this solid-state capacitor was still in the range of 0.35 to 0.4 ms at temperatures above 50 °C.

By combining the thin VOGN electrodes with highly conductive TEAOH-PVA polymer electrolytes, we are able to achieve key requirements for ultra-high rate solid-state EDLCs in both sandwich and planar designs. It will be interesting to explore performance limits by (a) optimizing the polymer electrolyte materials, (b) using this electrolyte in an asymmetric cell design, and (c) examining its use in series-connected (high voltage) planar EDLCs, ultimately achieving performance sufficient to replace electrolytic capacitors in ac line-filtering applications.

4. Conclusions

Solid-state EDLCs were developed using VOGN electrodes and a TEAOH-PVA polymer electrolyte in both sandwich and planar interdigitated configurations. The high ionic conductivity of TEAOH-PVA and the easily accessible VOGN surface maximize the performance of the solid-state capacitors. The capacitors could be scanned at an ultra-high rate of 1000 Vs^{-1}in CV, with response times of less than 1 ms, demonstrating the ultra-high rate capability of the devices. The capacitors also showed high stability with essentially no performance loss after 18 months of shelf storage or after 100,000 charge/discharge cycles. Faster response was observed for a solid-state capacitor tested at elevated temperatures. Both the ESR and the response time data show that the solid-state

EDLC reaches its highest performance level at around 90 °C. The developed solid-state EDLCs show electrical performance like electrolytic capacitors now used for ac line-filtering.

Acknowledgments

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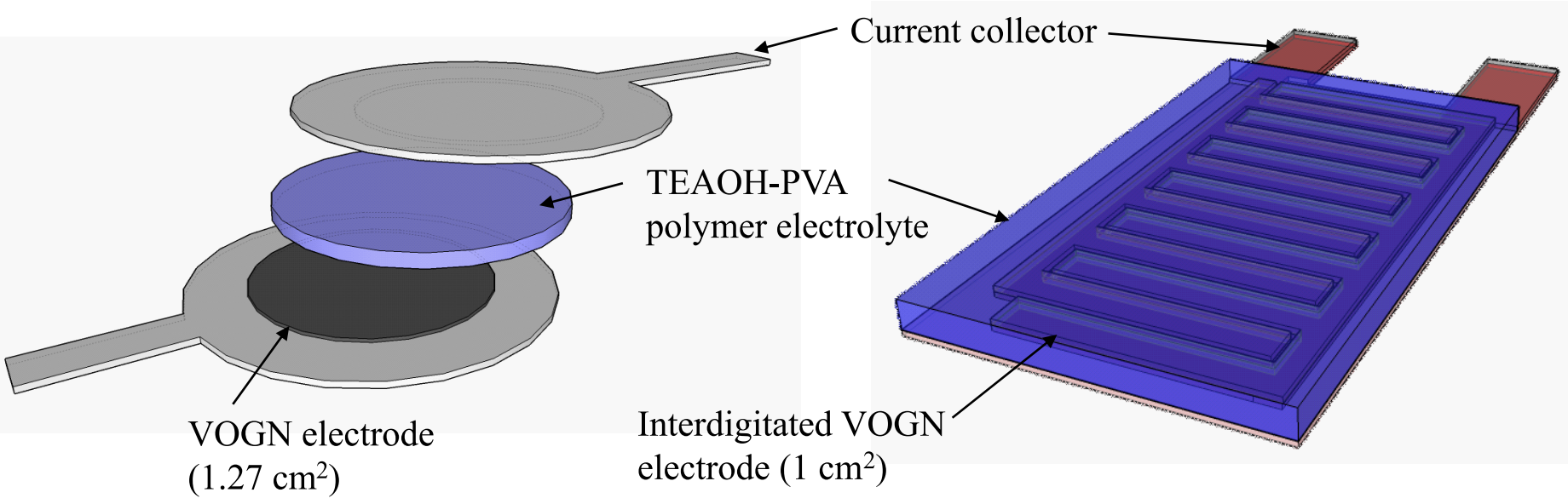
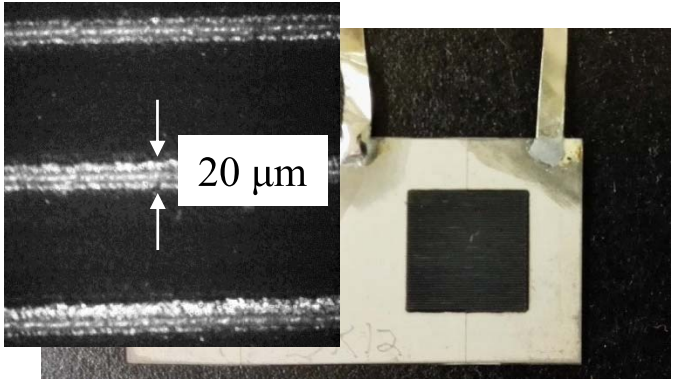
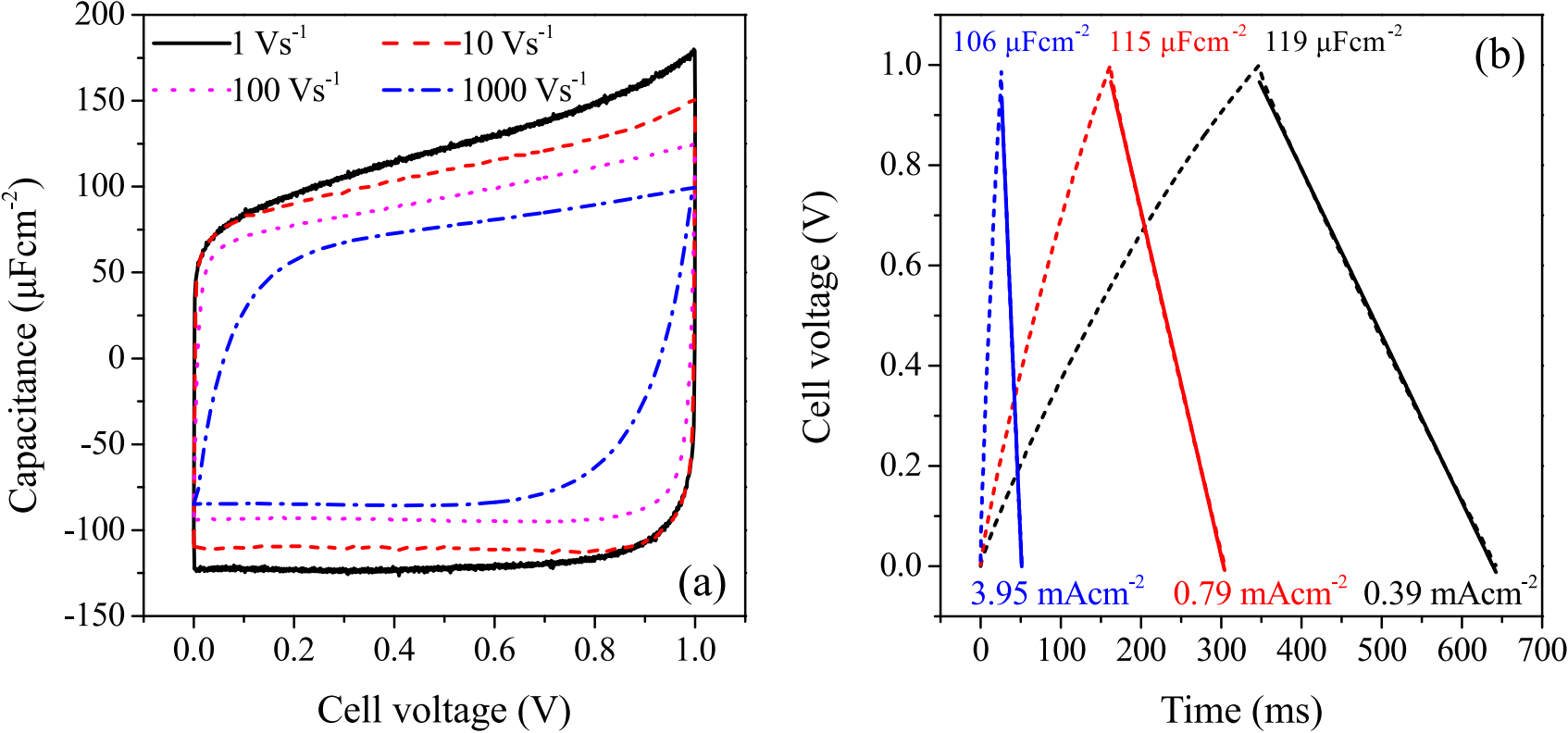
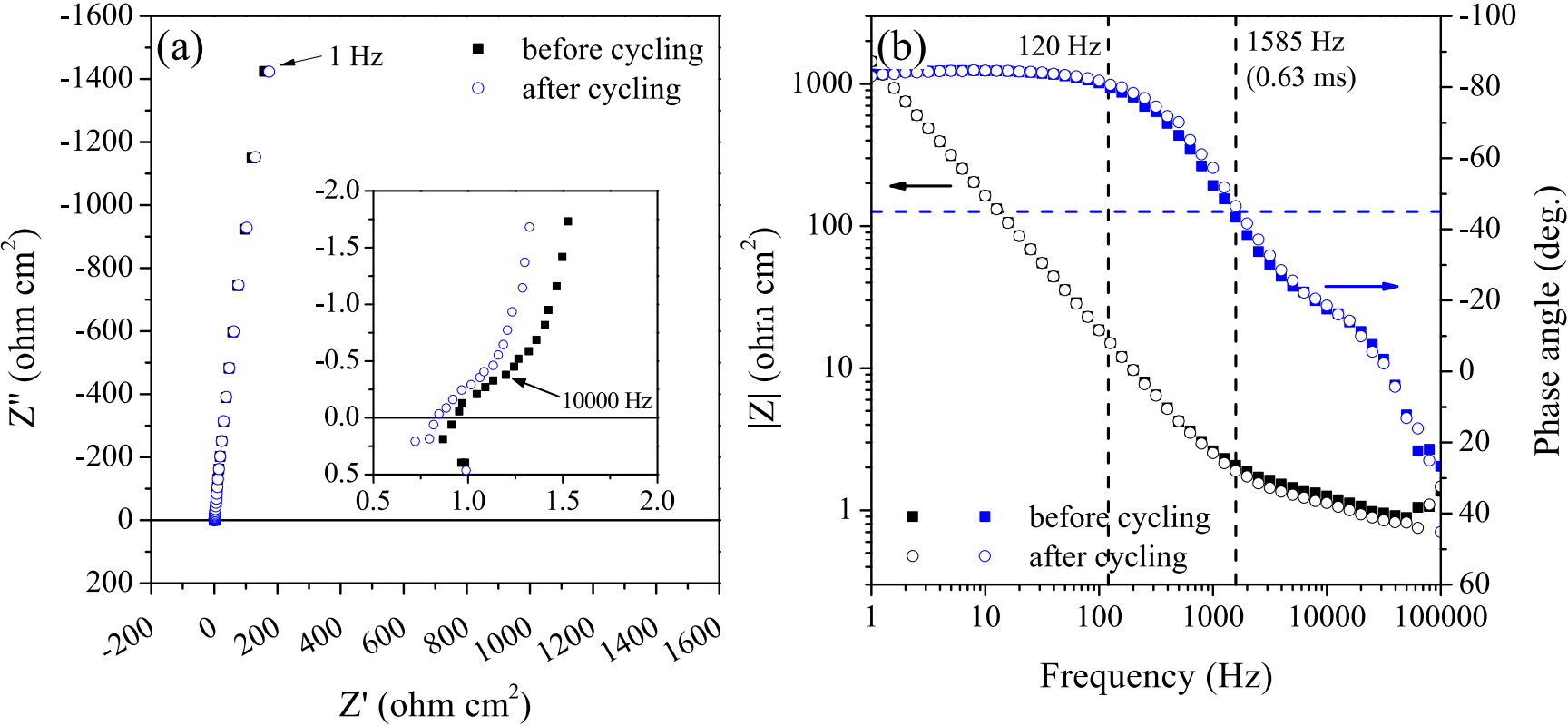
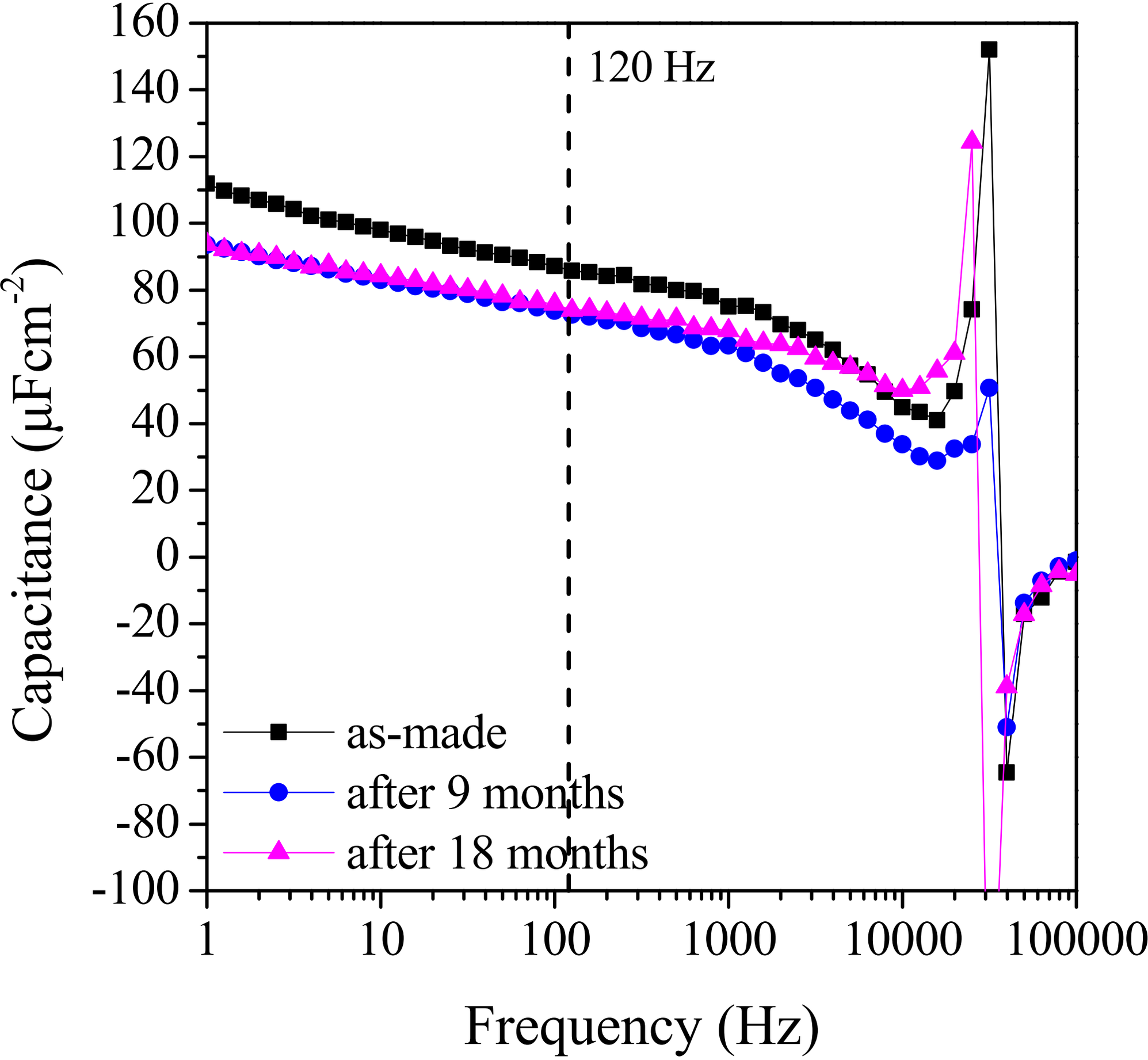
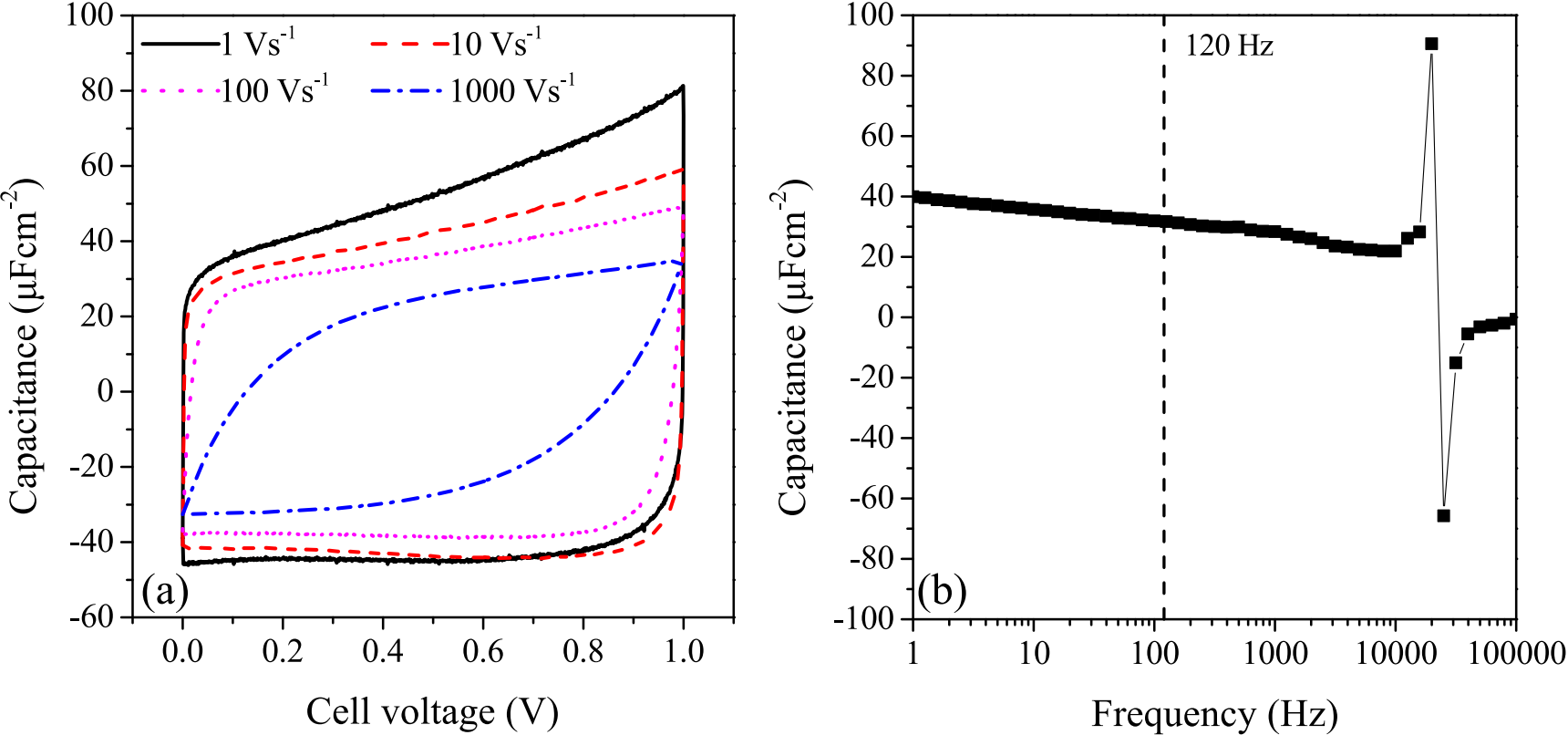

Current collector
TEAOH-PVA
polymer electrolyte
VOGN electrode
(1.27 cm2)
Interdigitated VOGN
electrode (1 cm2)

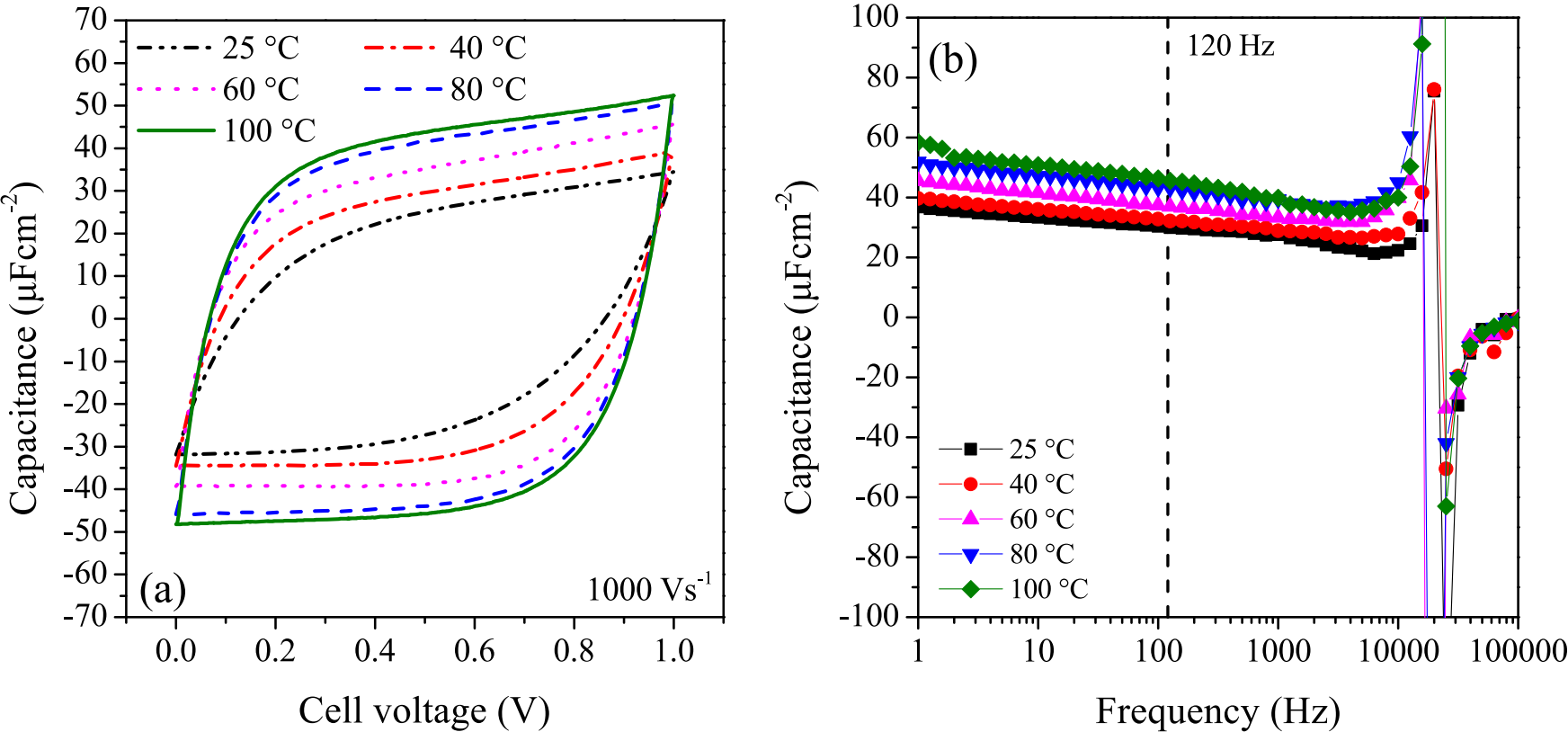

20 µm

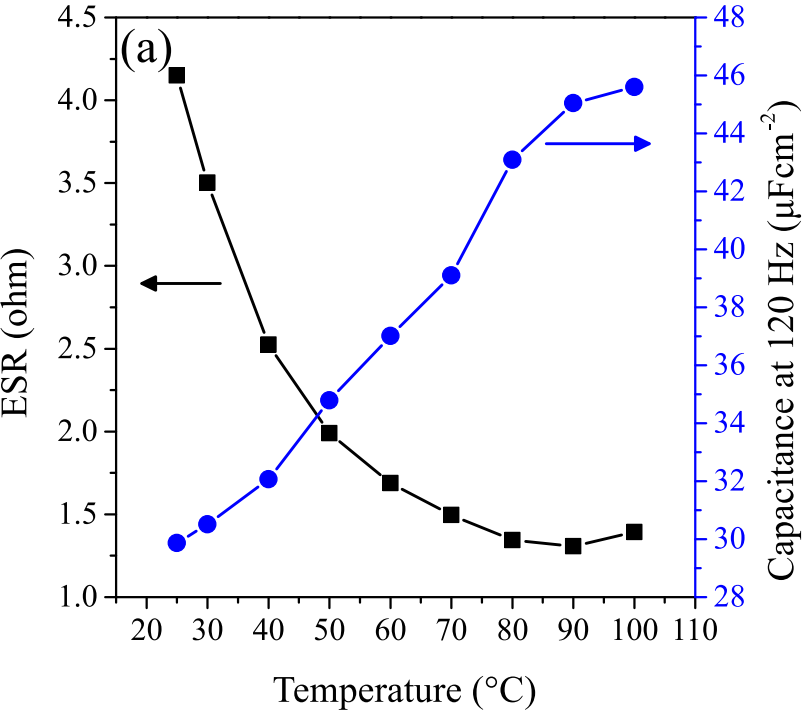

1 Vs-1
10 Vs-1
100 Vs-1
1000 Vs-1
Capacitance (μFcm-2)
Cell voltage (V)
(a)
106 μFcm-2
115 μFcm-2
119 μFcm-2
3.95 mAcm-2
0.79 mAcm-2
0.39 mAcm-2
Cell voltage (V)
Time (ms)
(b)

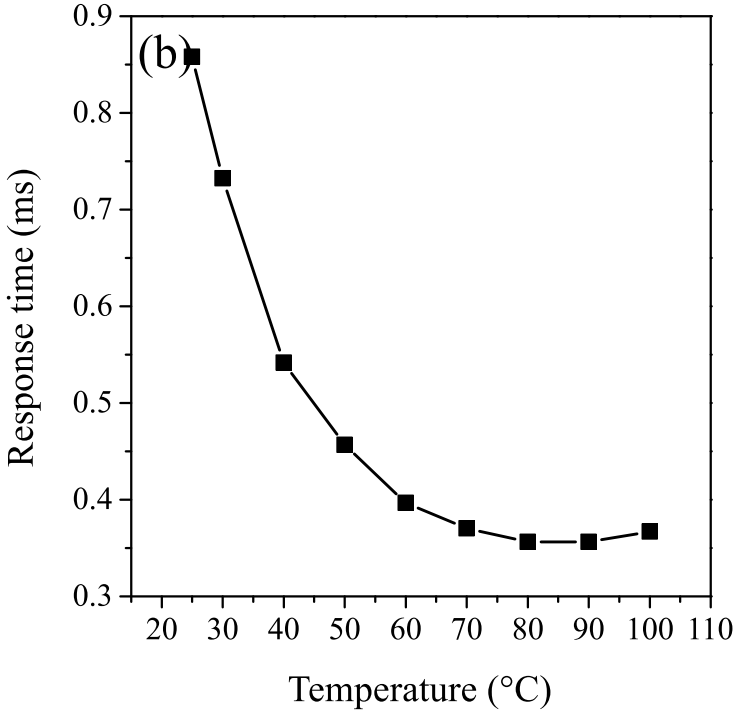

(a)
1 Hz
before cycling
after cycling
10000 Hz
Z'' (ohm cm2)
Z' (ohm cm2)
(b)
120 Hz
1585 Hz
(0.63 ms)
|Z| (ohm cm2)
Phase angle (deg.)
before cycling
after cycling
Frequency (Hz)


120 Hz
as-made
after 9 months
after 18 months
Capacitance (μFcm-2)
Frequency (Hz)
160
140
120
100
80
60
40
20
0
-20
-40
-60
-80
-100
1
10
100
1000
10000
100000


1 Vs-1
10 Vs-1
100 Vs-1
1000 Vs-1
(a)
Capacitance (μFcm-2)
Cell voltage (V)
120 Hz
(b)
Capacitance (μFcm-2)
Frequency (Hz)


25 °C
40 °C
60 °C
80 °C
100 °C
(a)
1000 Vs-1
Capacitance (μFcm-2)
Cell voltage (V)
(b)
120 Hz
Frequency (Hz)


(a)
ESR (ohm)
Capacitance at 120 Hz (μFcm-2)
Temperature (°C)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
48
46
44
42
40
38
36
34
32
30
28
20
30
40
50
60
70
80
90
100
110


(b)
Response time (ms)
Temperature (°C)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
20
30
40
50
60
70
80
90
100
110