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Design and Simulation of an 8-Bit Successive Approximation Register Charge-Redistribution Analog-To-Digital Converter

Sumit K. Verma
University of Texas at Tyler

DESIGN AND SIMULATION OF AN 8-BIT SUCCESSIVE APPROXIMATION REGISTER CHARGE-REDISTRIBUTION ANALOG-TO-DIGITAL CONVERTER

by

SUMIT KUMAR VERMA

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SUMIT KUMAR VERMA

has been approved for the thesis requirement on
2nd November 2017
for the Master of Science in Electrical Engineering degree

Approvals:

David M. Beams
Thesis Chair: David Beams, Ph.D.

Ron Pieper
Member: Ron Pieper, Ph.D.

Member: Mukul Shirvaikar, Ph.D.

Graduate Coordinator: Mukul Shirvaikar, Ph.D.

Chair, Department of Electrical Engineering

FOR JAK
Dean, College of Engineering

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Abstract

DESIGN AND SIMULATION OF AN 8-BIT SUCCESSIVE APPROXIMATION REGISTER CHARGE-REDISTRIBUTION ANALOG-TO-DIGITAL CONVERTER

Sumit Kumar Verma

Thesis Chair: David Beams, Ph.D.

The University of Texas at Tyler
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Successive approximation register (SAR) analog-to-digital converter (ADC) is a topology of choice in today's market for medium to high resolution conversions. It typically provides a resolution of 8 to 18-bits with under 5Msps sample rate, which makes it ideal for applications like data acquisition, battery powered instruments, industrial controls etc.

The SAR ADC implements a binary search algorithm i.e. the converter tries all possible values starting from the most significant bit (MSB) to least significant bit (LSB) and keeps comparing with the analog input signal. This process is continued until a binary output equal to the original decimal number is not obtained. This 'trial and fit' method requires an inbuilt digital-to-analog converter (DAC) for its operation. Although any type of DAC can be utilized for this purpose, charge-redistribution capacitor array DAC has been used in this work.

This thesis initially investigates the history of the monolithic ADCs. The next chapter explores the different types of ADCs available in the market today. Next, the operation of a 4-bit SAR ADC has been studied. Based on this analysis, an 8-bit charge-redistribution SAR ADC has been designed and simulated with Multisim (National Instruments, Austin, TX). The design is divided into different blocks which are individually implemented and tested. Level-1 SPICE MOSFET models representative of 5µm devices were used wherever individual MOSFETs were used in the design. Finally, the power dissipation during the conversion period was also estimated, which was found to be 20.46mW. The supply voltage for the ADC is 5V and the clock frequency is 500KHz.

Chapter 1

History of the monolithic analog to digital converter

The earliest data converter in the recorded history can be traced back to 18th century in Turkey, under the Ottoman Empire. It was a hydraulic system acting as a binary digital to analog converter (DAC), used to meter the public water supply. This system used reservoirs maintained at a constant depth and the output was controlled by gated binary-weighted nozzles submerged below the water level. Functionally, this is just a manual input DAC [1]. During the 1940s and 1950s, the development of digital electronic systems created a need for devices capable of bridging the analog (continuously-valued) and digital (discrete-valued) domains. This made the data converters a necessity in the industry, especially in the field of communication. This chapter summarizes the history of monolithic analog to digital converters (ADCs) along with examples of the devices which were breakthroughs in their time.

1.1 Early History

Research on various data converter architectures was already being done during the late 1930s. Data converters were built for specialized applications like pulse-code modulation (PCM) and message encryption during World War II. The real revolution in this field began in the mid-1950s when electronic circuit designs began to migrate from vacuum tubes to transistors, thereby opening many new possibilities in data conversion products. Key data-converter architectures and building blocks were being perfected in the 1960s and the first monolithic converters began to appear in the early 1970s.

Most of the ADCs of the early 1970s were hybrids i.e. some components of the circuit like voltage references, amplifiers, comparators etc. were not integrated on the same chip, instead were required to be connected externally. Considerable effort was devoted to building a fully monolithic ADC. One of the earliest examples is the AD7570 10-bit, 20-μs complementary metal oxide semiconductor (CMOS) successive approximation register (SAR) ADC introduced in 1975. However due to difficulty of designing an on-chip comparator, it used an external LM311 comparator and a voltage reference.

In 1976, Analog Devices introduced the 13-bit AD7550 with a unique architecture called ‘quad slope’, patented by Ivar Wold.

The first complete monolithic ADC was the 10-bit, 25-μs AD571 SAR ADC introduced in 1978 and designed by Paul Brokaw. Its design was based on a bipolar process with laser wafer trimmed (LWT) thin film resistors. Logic functions of the SAR ADC were implemented with integrated-injection logic (I^2L). This process allowed reasonably dense low-voltage logic to be included on the same chip as precision linear circuitry.

The 10-bit AD571 and 8-bit AD570 included an internal clock, buried Zener voltage reference, laser-trimmed DAC and three stage output buffers. Fig 1.1 shows the simplified diagram of AD571 [1].

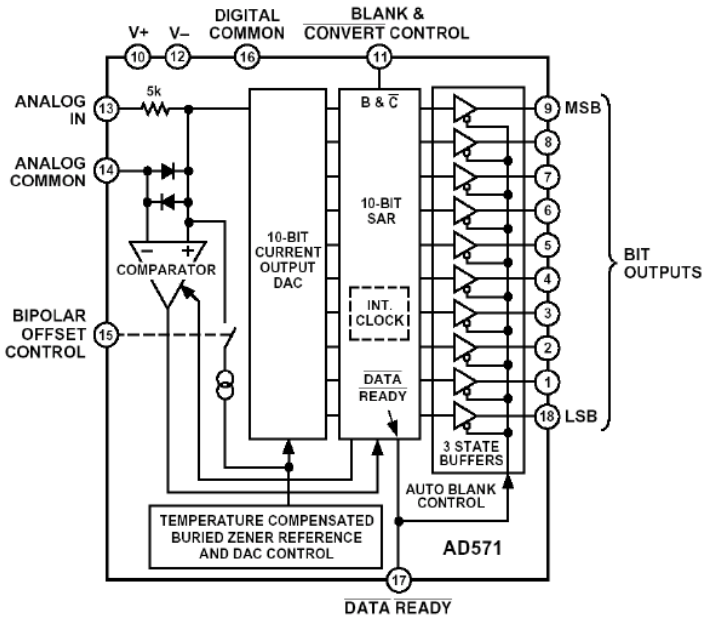

Fig 1.1 AD 571 10-bit 25µs ADC

1978 saw the introduction of the AD574, a 12-bit, 35µs SAR ADC by Analog Devices. It had a buried Zener reference, timing circuits, and three-state output buffers for direct interfacing to an 8-, 12-, or 16-bit microprocessor bus. In its early form, AD574 was manufactured based on two chips – one an AD565 12-bit current-output DAC and the other containing a SAR, microprocessor interface logic functions and a precision latching comparator.

In 1985, the AD574 became available in single-chip monolithic form. Fig 1.2 [1] shows a simplified block diagram of the AD574.

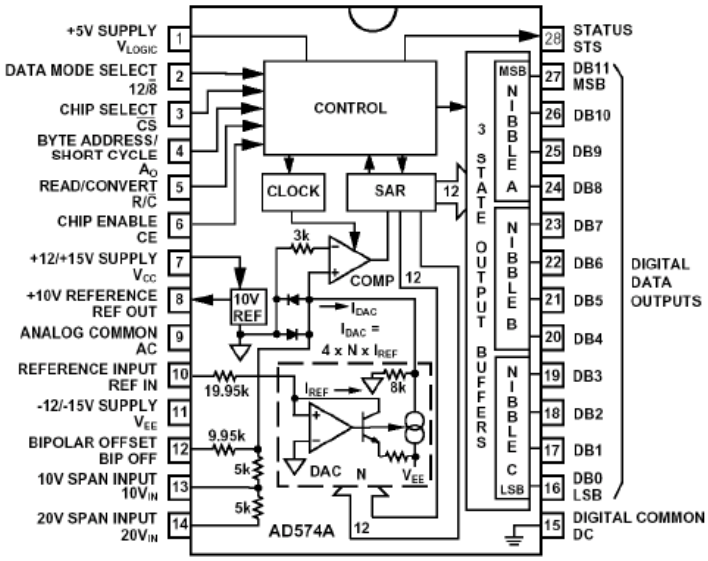

Fig 1.2 AD574 12-bit, 35µs ADC

The end of 1970s saw a few other ADCs emerge in the –market, such as the first high-speed video flash ADCs. (The flash ADC architecture is described in Ch. 2.1). The 8-bit TDC-1007J achieved 30 MSPS (megasamples per second); a lower-power 6-bit version (TDC-1014J) was also available. Both were developed by the LSI division of TRW in 1979; The 4-bit 100-MSPS AM6688 flash ADC was also introduced by Advanced Micro Devices in 1979.

The 1980s saw large growth in the data-converter domain for applications such as data acquisition, instrumentation, computer graphics and many more. Data sheets began to include specifications like signal-to-noise ratio (SNR), signal-to-noise and distortion (SINAD), effective number of bits (ENOB), noise power ratio (NPR) etc. Wide dynamic range and ac performance also started to emerge as important criteria.

Two CMOS SAR devices ADC0804 and ADC0808 were made available in the 1980s by Texas Instruments and remain in production today. The ADC0804 is a single-input device, while the ADC0808 has an eight-input multiplexer (MUX) allowing the user to select one of eight analog inputs for conversion.

The first commercial monolithic sigma-delta ADC, the CSZ5316 was introduced in 1988 by Crystal Semiconductor. It had 16-bit resolution and a 20 KSPS throughput rate. (The sigma-delta architecture is described in Ch. 2.6).

The 1980s saw a rise in the production of flash ADCs which continued until the early 1990s. Some examples of devices introduced during this time are as follows:

- SDA6020, 6-bit, 50MSPS by Siemens (1980)
- TLM1070, 7-bit, 20MSPS, by Telmos (1982)
- MP7684, 8-bit, 20MSPS by Micro Power (1983)
- TDC1048, 8-bit, 30MSPS by the LSI division of TRW (1983)
- AD9000, 6-bit, 75MSPS by Analog Devices (1984)
- AD9002, 8-bit, 50MSPS by Analog Devices (1987)
- AD9006/AD9016, 6-bit, 500MSPS by Analog Devices (1989)

The market for data converters grew more diverse in the 1990s; one of the important factors for this was developments in the communication domain. Due to the emergence of wireless communication, low power and high-performance data converters were in high demand for use in modems and cell phones.

These market demands brought much innovation to data converters. Traditional DIP (dual in-line) packaging and through-hole circuit board construction methods were replaced by small surface-mount packaging. Many applications required both ADC and DAC functions which led to integration of both on a single chip known as a CODEC (Coder-Decoder). Flash ADCs were virtually replaced by devices using a pipelined architecture. For general purpose data converters, CMOS became the major process and BiCMOS was reserved for high-end devices. Due to CMOS process, the sigma-delta ADC became the topology of choice for audio and video applications.

One of the major achievements in 1990s was that parasitic capacitance was no longer a limiting factor for high speed devices. The reduced device dimensions greatly reduced parasitic capacitances allowing very high performance, high speed and low power loss devices to emerge which eventually shaped many technological developments in the years to follow.

Analog Devices launched the 12-bit, 100 KSPS AD1674 ADC in 1990 which was pin-compatible to the AD574, which had itself become an industry standard by that time. A block diagram of AD1674 is shown in Fig 1.3 [1].

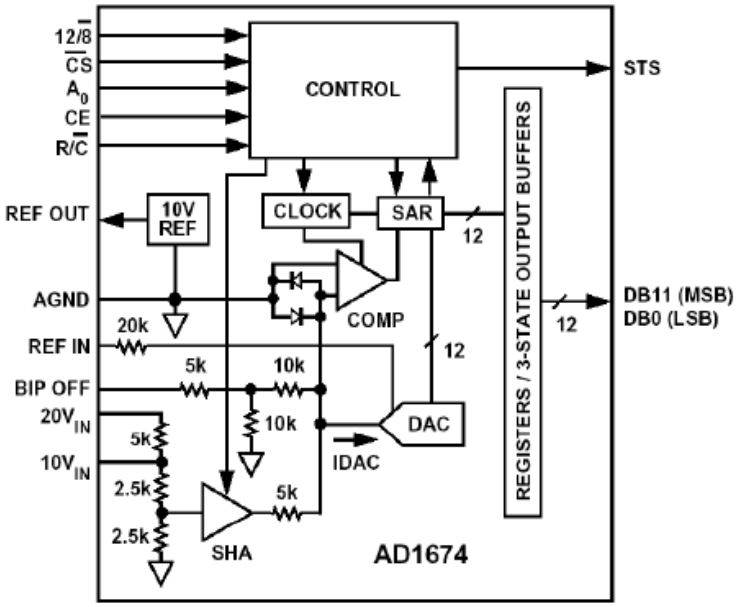

Fig 1.3 AD1674 12-bit, 100μs ADC

Analog Devices also introduced a sampling ADC (the AD7880) in 1990. Although it required an external voltage reference circuit, it was a breakthrough because of its low power of 25mW and only one +5V supply was required for its operation. The block diagram of the 12-bit, 66 KSPS ADC is shown in Fig. 1.4 [1].

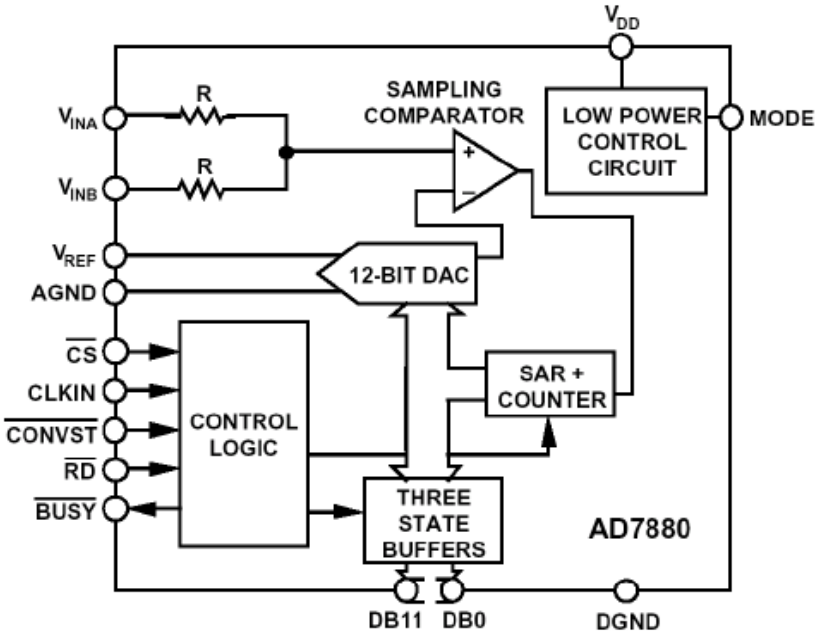

Fig 1.4 AD7880 12-bit, 66KSPS sampling SAR ADC

In 1992, a significant breakthrough in speed and performance was also achieved with the release of the AD872. It was a 12-bit, 10-MSPS BiCMOS sampling ADC which also used the pipelined architecture with error correction. Fig 1.5 [1] shows the block diagram of the device.

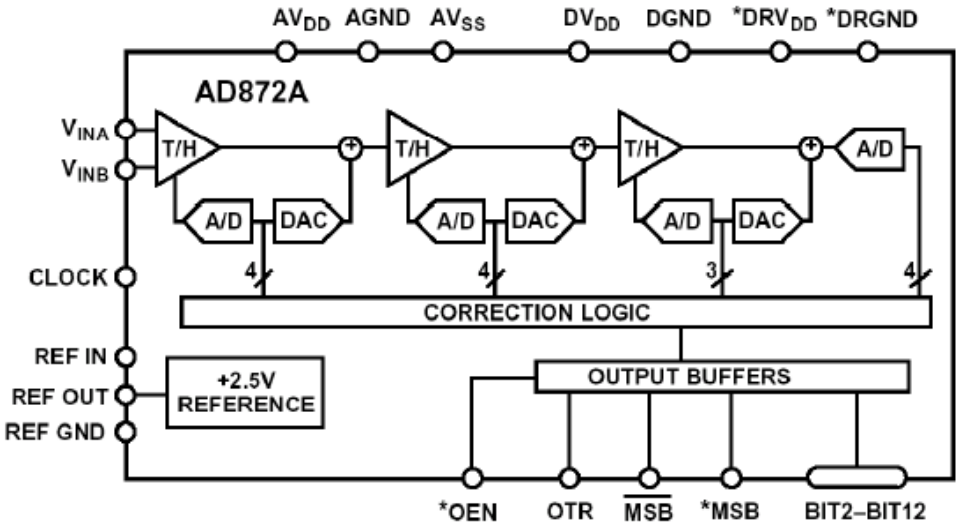

Fig 1.5 AD872 12-bit, 10 MSPS sampling ADC

In 1995, Analog Devices launched the 12-bit, 41 MSPS AD9042. It was the first converter to achieve greater than 80dB spurious-free dynamic range (SFDR), which was a breakthrough in the field of wide dynamic intermediate frequency (IF)- sampling ADCs. Fig 1.6 [1] illustrates a functional diagram of the device.

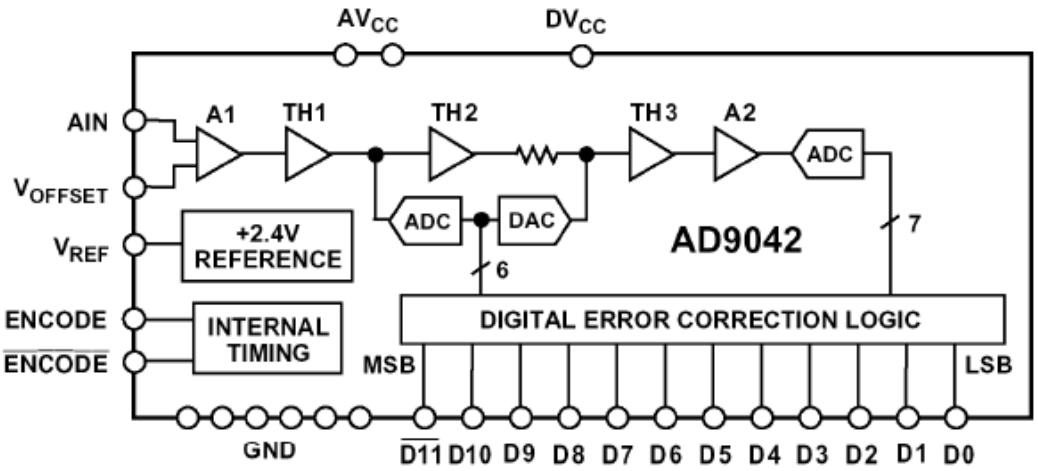

Fig 1.6 AD9042 12-bit 41 MSPS sampling ADC

The AD7001, launched in 1990, was the first baseband converter for global system for mobile communications (GSM). It was based on a CMOS sigma-delta architecture which became widely used in ADCs for audio, measurement and voiceband applications at that time. This device eventually gave rise to many measurement and voiceband converters like Analog Devices' AD771x-family in 1992.

The 2000s saw major advances in the chip technology. CMOS feature size shrank from 0.6μm to 0.18μm permitting a high level of integration in a very small area. Supply voltage dropped from 5V to 1.8V which also reduced the power dissipation.

Sixteen-bit and 18-bit SAR ADCs with built-in sample and hold circuits started coming to market in 2002 when Analog Devices launched the AD9430. IF sampling ADC which was a breakthrough in sampling rate and dynamic range. Significant multichip modules were also introduced in 2000s, along with system on chip microcontroller based ADCs. Two examples of the multichip module are AD10678 and AD12400 ADC introduced in 2003.

Chapter 2

Common ADC architectures

This chapter provides the information about various ADCs that are used in the industry today. A summary is presented about these devices containing the architecture, operation, and its application.

2.1 Flash ADC

Flash ADCs (also known as parallel ADCs) are the fastest type of ADC available. Fig 2.1 [18] shows a 3-bit flash ADC consisting of 2N resistors and 2^N–1 comparators. Each comparator has a reference voltage from the resistor string which is 1 LSB higher than that of the one below it in the chain. All comparators whose reference voltages are less than the input voltage will have logic 1 outputs; all other comparators will have logic 0 outputs. The 2^N–1 comparator outputs are processed by a decoder to generate an *N*-bit binary output. The strobe acts as the enable input for the comparators and the priority encoder.

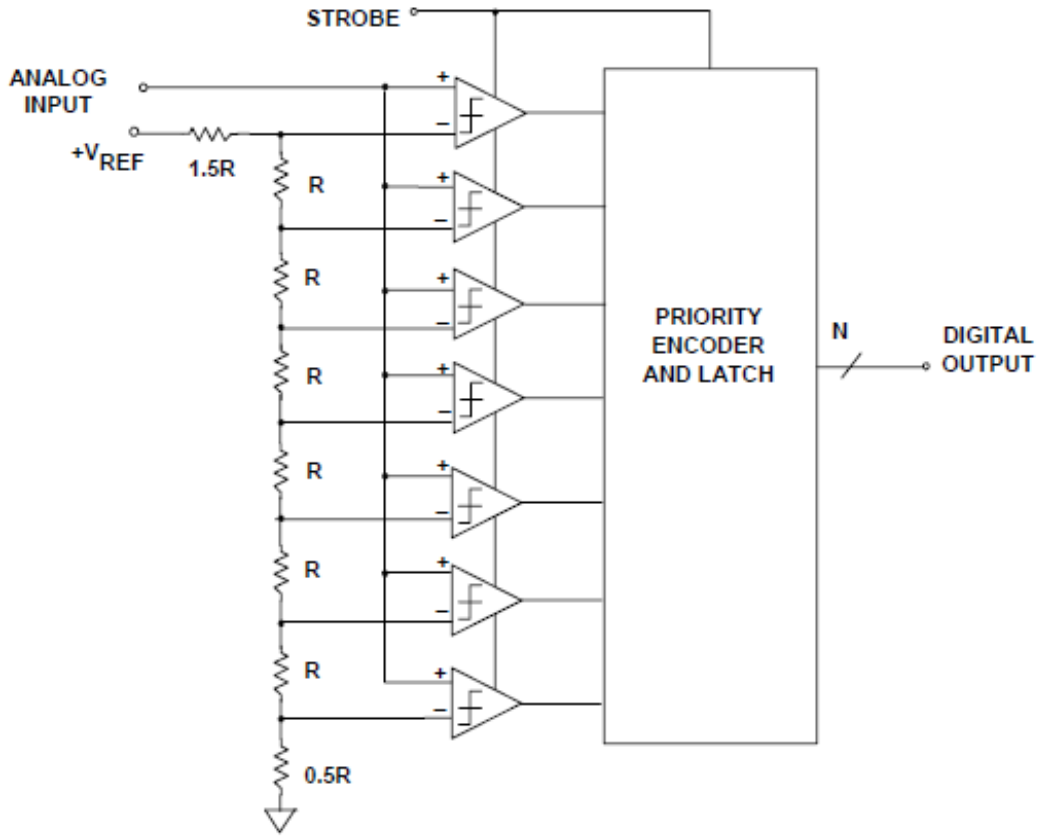

Fig 2.1 3-bit flash converter

The input signal is applied to all the comparators at once, therefore the total delay between application of the analog input signal and the appearance of the digital output is the delay of one comparator plus the delay of the encoder. A major drawback of this architecture is that due to the presence of large numbers of resistors and comparators (for example, an 8-bit ADC will require 2^7-1 i.e. 255 comparators), the device draws a significant power level and a requires very complex priority encoder. Hence, the problems of flash ADCs include limited resolution, high power dissipation and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to avoid errors due to input-bias currents of the comparators, so the voltage reference has to source relatively large currents.

Flash ADCs are suitable for applications requiring large bandwidth such as data acquisition, satellite communication, sampling oscilloscopes, and radar processing.

2.2 Single-Slope ADC

The simplest form of an integrating ADC uses the single-slope architecture shown in Fig 2.2 [3]. This converter has been the topology of choice for the Wilkinson ADC which is used in pulse-height analysis in gamma-ray and X-ray spectroscopy. The reason being its faster conversion rate than dual-slope ADCs, which is necessary for pulse-height analysis.

The process involves sampling an unknown input voltage first, and then comparing this value to the integral of a known reference value. A counter determines the number of clock pulses that are required before the integrated value of a reference voltage is equal to the sampled input signal.

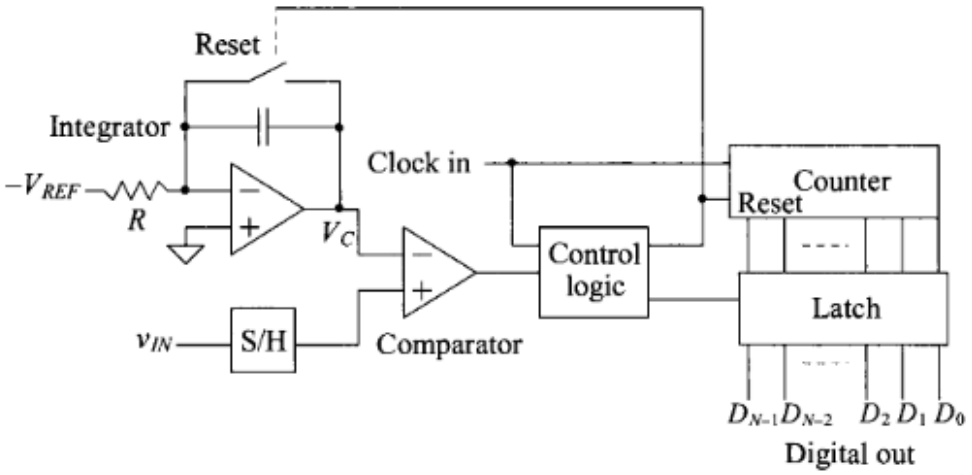

Fig 2.2 Single slope ADC

The output voltage of the integrator (V_C in Fig. 2.2) is initially reset to zero, and once conversion begins, it increases linearly at a rate that depends upon the reference voltage ($-V_{ref}$) and the gain of

the integrator. The negative reference voltage causes the output voltage of the inverting integrator to have a positive slope. Therefore, the topology of Fig. 2.2 is useful only for positive input voltages. The output voltage of the comparator switches from high to low when the output voltage of the integrator exceeds the input voltage, thus triggering the control logic to latch the value of the counter. It also resets the system for the next sample. Fig 2.3 [3] illustrates the output waveforms and the clock signal.

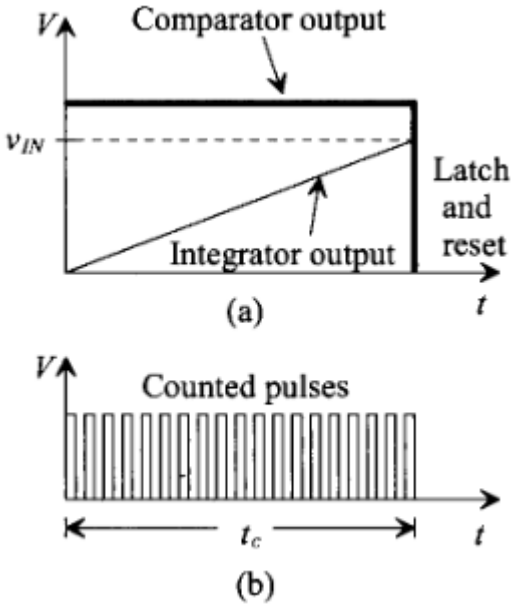

Fig 2.3 a) Comparator input and output waveforms b) Counted pulses

If the input signal is at full-scale value, the counter must increment to its maximum in 2^N clock cycles where N is the number of bits of resolution of the counter Thus, the clock frequency must be considerably greater than the bandwidth of the input signal. The conversion time t_c can be defined as

$$t_c = \frac{V_{in}}{V_{ref}} \times 2^N \times T_{clk}$$

where T_{clk} is the period of the clock.

One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and C values. Thus, in a production environment, each unit may have to be individually calibrated to maintain the measurement repeatability. To overcome this sensitivity to the component values, the dual-slope integrating architecture is used.

2.3 Dual Slope ADC

The dual-slope ADC architecture was truly a breakthrough for high resolution applications with good noise rejection. It does not suffer from issues of component tolerances that are a drawback of the single-slope ADC. A simplified block diagram of a unipolar dual-slope ADC is shown in Fig 2.4, and the integrator output waveforms are shown in Fig 2.5. These devices are used in applications application where low throughput is acceptable and high noise rejection is important, like digital multimeters and panel meters.

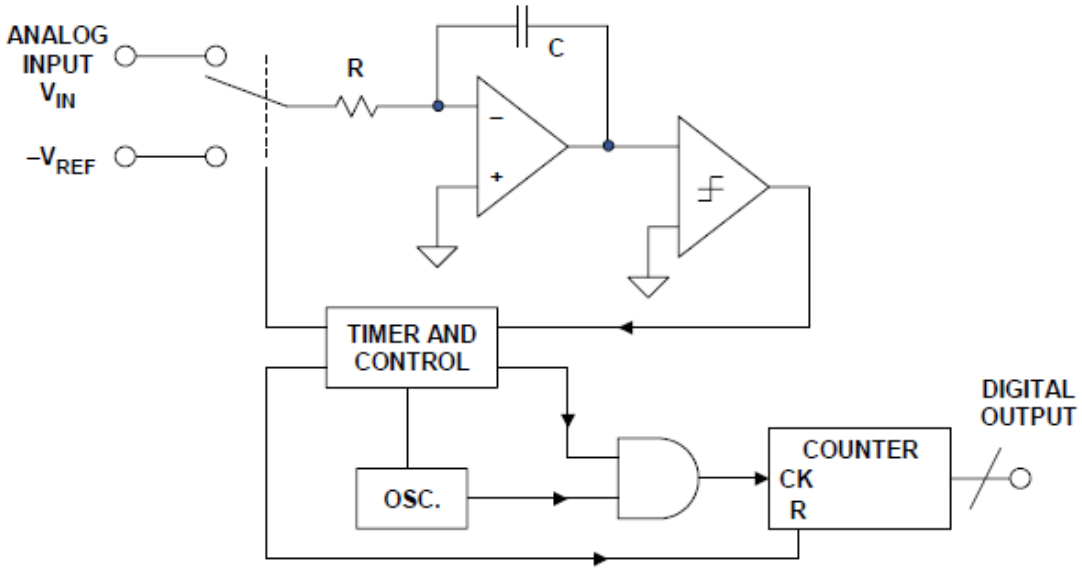

Fig 2.4 Unipolar dual slope ADC

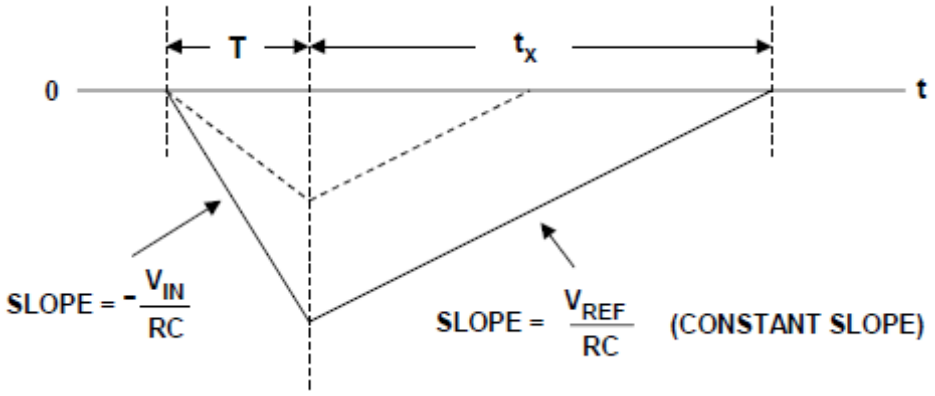

Fig 2.5 Dual slope ADC integrator output waveform

Unlike single-slope, here two integrations take place, one on input signal and the other at V_{REF}. The input signal is applied to an integrator and at the same time a counter is started, counting clock pulses.

After a pre-determined amount of time (T), a reference voltage having opposite polarity is applied to the integrator. At this instant, the charge accumulated on the capacitor is proportional to the average value of the input over the time interval T.

The voltage V_{REF} is now integrated and at the same time, the counter is again started from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $V_{IN} \cdot T$, and the equal amount of charge lost is proportional to $V_{REF} \cdot t_x$, then the number of counts relative to the full-scale count is proportional to t_x/T, or V_{IN}/V_{REF}.

Dual-slope integration has many advantages. Conversion accuracy is independent of both the capacitance and the clock frequency, because they affect both the up-slope and the down-slope by the same ratio. The fixed input signal integration period results in rejection of noise frequencies on the analog input that have periods that are equal to or a sub-multiple of the integration time T. Proper choice of T can therefore result in excellent rejection of voltage fluctuations.

Errors caused by bias currents and the offset voltages of the integrating amplifier and the comparator as well as gain errors can be cancelled by using additional charge/discharge cycles to measure "zero" and "full-scale" and using the results to digitally correct the initial measurement.

2.4 Pipelined ADC

The pipelined ADC has become the most popular ADC architecture for sampling rates from a few megasamples per second to more than 100 Msps. Its resolution ranges from eight bits at the faster sample rates up to 16 bits at the lower rates. The term "pipelined" topology refers to the ability of one stage to process data from the previous stage during any given clock cycle. At the end of each phase of a clock cycle, the output of a given stage is passed on to the next stage and new data are shifted into the stage. Fig 2.6[17] shows a block diagram of N-bit pipelined ADC with four stages of 3-bit each.

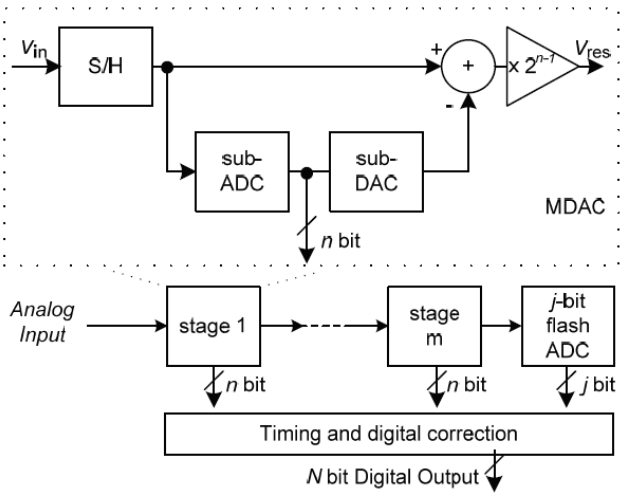

Fig 2.6 Block diagram of N-bit pipelined ADC

The analog input signal is first sampled and then held in the sample and hold (S/H) circuit while a flash ADC is quantizing it into three bits in stage 1. The output then goes into 3-bit DAC which converts this output into an analog signal. This signal is then subtracted from the input. The difference, known as the residue, is then amplified by a gain of +4 and fed into the next stage. Amplified residues then continue through the pipeline, providing 3-bit inputs to the rest of the stages until reaching the 4-bit ADC which resolves the last 4 bits. Since, the bits from different stages are obtained at different times, the digital outputs of all but the last stage are stored in shift registers. This keeps the outputs of the same sample time-aligned. Finally, the outputs are fed to a digital error-correction circuit. The operation can be better understood by the following example:

Consider a 12-bit pipelined ADC with Vref = 5V and input voltage to be converted is Vin = 3V. Figure 2.7 shows a 3-bit flash ADC being used in every stage. Since it is a 3-bit flash ADC, the amplification of the residue will be 2^{N-1} i.e. 4 times. Table 2.1 presents the output, input and the residue of each iteration of the conversion process.

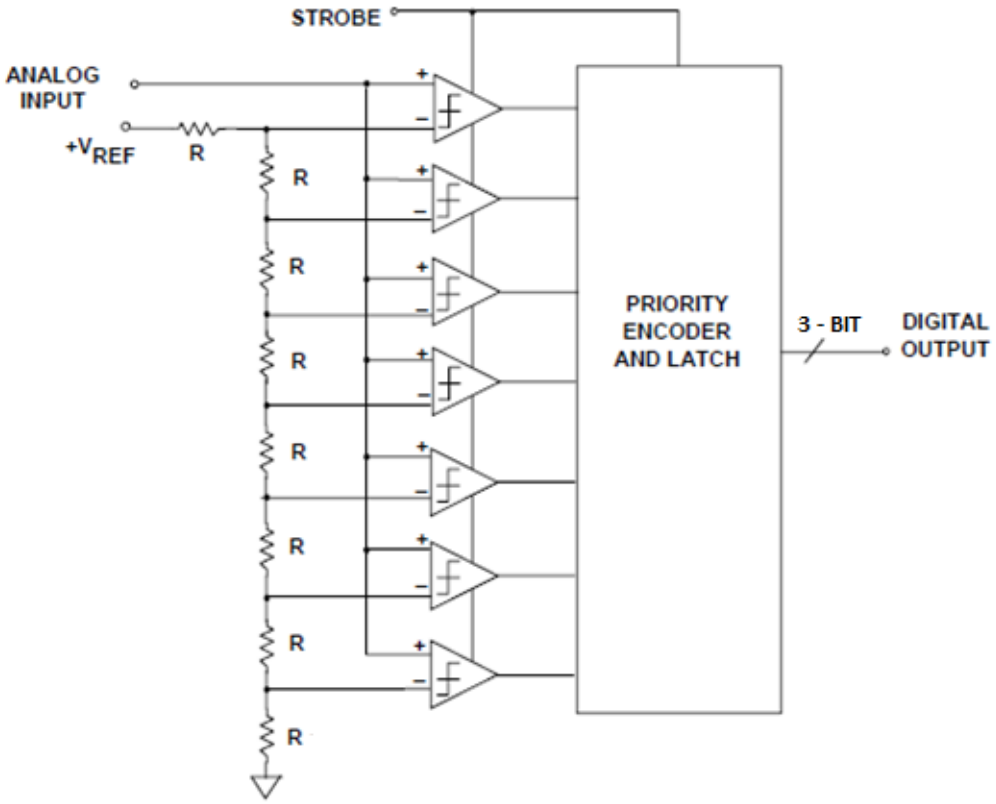

Fig 2.7 3-bit flash ADC

Table 2.1 Iterations of 12-bit pipelined ADC with Vin = 3V and Vref = 5V

Iteration	Vin	ADC code	VoDAC	Residue (Vin – VoDAC)	Amplifier (4 × Residue)
1	3 V	100	2.5 V	0.5 V	2V
2	2 V	011	1.875 V	0.1250 V	0.5V
3	0.5 V	000	0 V	0.5 V	2 V
4	2 V	011	1.875 V	0.1250 V	0.5 V
5	0.5 V	0001	-	-	-

In the above example, the four iterations take place in different stages of the ADC and generates a 3-bit output. In each iteration, the input voltage is converted into a digital output which then gets converted back to analog voltage VoDAC. The VoDAC is subtracted from the original Vin to give the residue. This residue gets amplified to produce the input for the next stage. However, the last iteration takes place in a 4-bit flash ADC, therefore generating a 4-bit output. After the outputs are obtained, the timing and digital correction circuit adds these bits as given below to produce the 12-bit final output.

```
  1 0 0
    0 1 1
      0 0 0
        0 1 1
          0 0 0 1
--------------------------------
  1 0 0 1 1 0 0 1 1 0 0 1
--------------------------------
```

The binary digital output obtained when converted to decimal gives the value 2457.
The output according to the calculations should be equal to

$$V_{\text{in}} \times (2^{12-1})/V_{\text{ref}} = 3 \times 4095/5 = 2457$$

The pipelined ADC makes use of a process called ‘1-bit overlap’. In the example, each stage generates 3 bits. Since, the inter-stage gain is 4, each stage resolves only 2 bits. The extra bit is to half the size of the residue. This allows extra range in the next 3-bit ADC for digital error correction. Hence, the effective number of bits from each stage comes out to be 2+2+2+2+4 = 12.

When a stage finishes processing a sample, it becomes available for processing the next sample from the sample and hold circuit. Each stage has its own sample and hold circuit so that preceding stages can convert different later analog inputs, allowing for multiple conversions to be in progress at the same time. This ‘pipelined’ process gives a high throughput to the circuit. These ADCs are generally used in ultrasonic medical imaging, digital receivers, HDTV, cable modems etc.

2.5 Successive Approximation Register ADC

The successive approximation register (SAR) ADC is one of the most commonly used ADC topologies in industry. In SAR ADC, the output voltage of DAC is compared to the input voltage, one bit at a time, proceeding from MSB to the LSB. It usually employs either a binary weighted capacitor network or an R-2R ladder network as the DAC. The SAR logic is basically a binary search algorithm in which every bit is successively tested. The whole conversion is a 3-step process – sample mode, hold mode and conversion mode. Fig 2.8 [13] shows the block diagram of a basic SAR ADC. A 5-bit charge redistribution capacitive DAC is shown in Fig 2.9 [19].

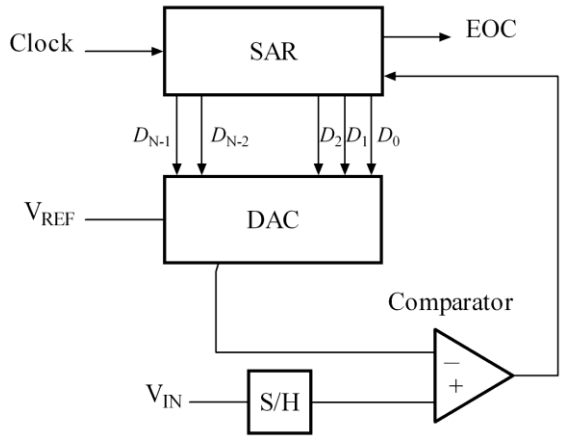

Fig 2.8 Block diagram of SAR ADC

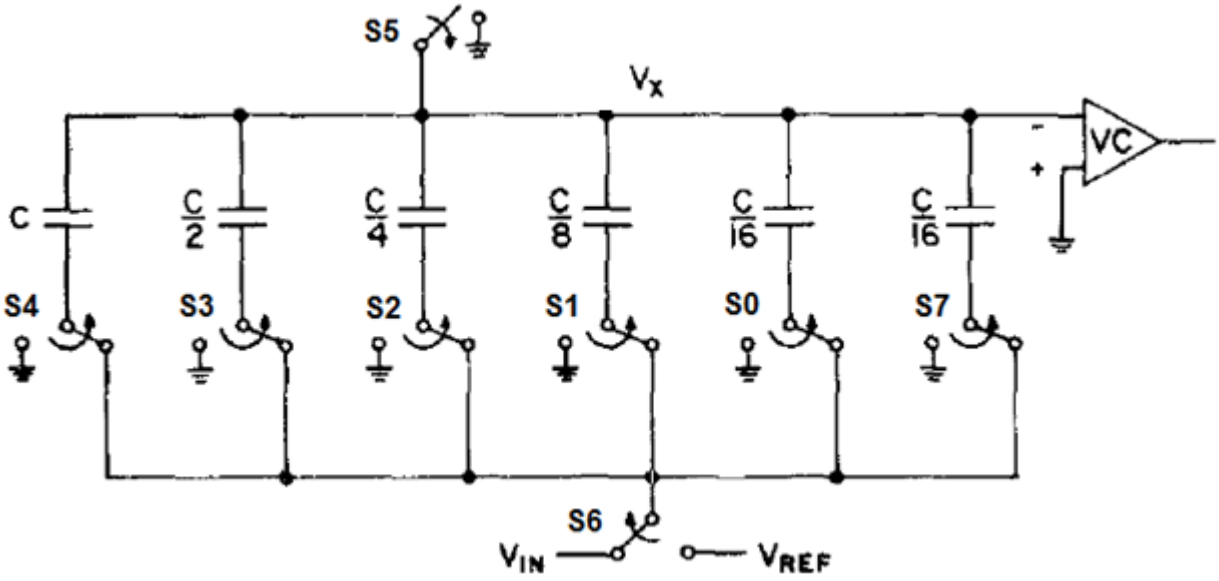

Fig 2.9 Charge redistribution DAC

In the sample phase, the capacitive array is first completely discharged. Then switch S5 is opened, switches S0 – S4 and S7 are simultaneously turned to Vin and finally switch S6 is toggled to Vin. This fully charges every capacitor in the array with a total charge of -2C × Vin.

During the hold phase, switch S5 is closed, switches S0 – S4 and S7 are turned to ground and switch S6 is turned to Vref. This phase is used to hold the voltage Vx = -Vin until the conversion starts.

The third phase is the charge redistribution phase. This is where the actual conversion takes place. It starts with the most significant bit i.e. the switch S4 of capacitor C is turned to Vref. This makes the voltage Vx = -Vin + Vref/2. This can produce two results, either Vx < 0 or Vx > 0.

If Vx > 0, the comparator gives a logic 0 at the output. In this case, the switch S4 is connected back to ground.

If Vx < 1, the comparator yields a logic 1 at the output. In this case, the switch S4 is left connected to Vref.

In this manner, the conversion takes place bit by bit in sync with each clock pulse, until the LSB is obtained. Every bit is stored in a register and finally an end of conversion signal is passed from the SAR logic block which discharges the capacitors and resets the ADC for next input signal.

A similar principle applies to the SAR ADC with an R-2R ladder as the DAC. Fig 2.10 [18] shows a 4-bit R-2R ladder with comparator. N1-N4 represents different nodes between the R-2R pattern.

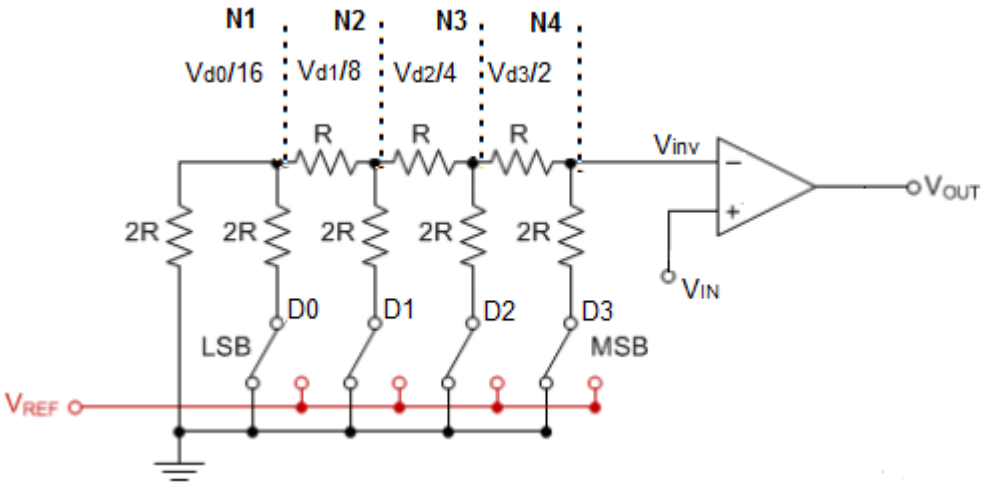

Fig 2.10 4-bit R-2R ladder with comparator

Using Thevenin's equivalent circuit on these nodes, it can be demonstrated that the open circuit voltages at each node will be double of the previous node when going from LSB to MSB. That is, the voltage at node N1 is $V_{d0}/16$ and keeps doubling until reaching $V_{d3}/2$ at node N4. Therefore, the total output voltage obtained at the inverting terminal of the comparator will be given as

$$V_{inv} = \frac{V_{d0}}{16} + \frac{V_{d1}}{8} + \frac{V_{d2}}{4} + \frac{V_{d3}}{2}$$

The switches D0-D3 are toggled sequentially to Vref starting from D3 and going towards D0. At every toggle, the output Vinv is compared with the input voltage Vin. If the output of comparator is logic 1 than the switch stays as it is, else its set back to ground. This process continues until all the switches bits are tested and the output of each bit has been latched by a flip-flop in the main circuit of the ADC.

SAR ADCs have a sampling rate under 5 MSPS, a resolution of 8 to16 bits and provide a very low power consumption. This makes it ideal for battery powered instruments, industrial controls, signal acquisition etc. More in-depth research is performed for this device and an attempt is made to design and simulate an 8-bit SAR ADC later in this thesis.

2.6 Sigma-Delta ADC

Sigma-delta ADCs are also known as oversampling type ADCs which had its origins in the early development phases of pulse code modulation (PCM) systems. Modern sigma-delta converters offer high resolution, low power consumption, and low cost. They are now ideal for converting analog signals over a wide range of frequencies, from DC to several megahertz making them a good choice for applications such as process control, precision temperature measurements etc.

The architecture of a sigma-delta ADC has two parts – the analog part which is an oversampling modulator, and the digital part which includes filtering and decimation. Fig 2.11 [10], shows the block diagram of a sigma-delta ADC presenting an overview of its working.

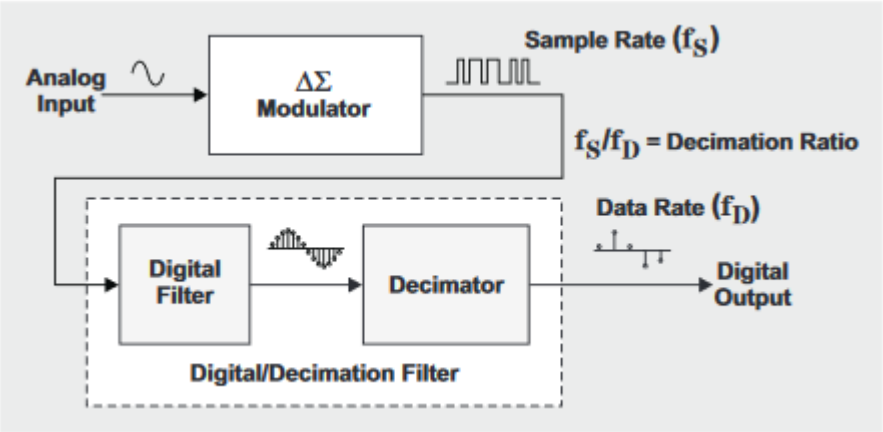

Fig 2.11 Block diagram of sigma-delta ADC

An analog signal is applied to the input of the modulator which needs to be relatively slow, so the modulator can sample it multiple times, a technique known as oversampling. The modulator samples

the input signal at a very high rate into a 1-bit stream. Each individual sample is accumulated over time and "averaged" with the other input-signal samples through the digital/decimation filter. The digital/decimation filter takes this sampled data and converts it into a high-resolution, slower digital code. Sigma-delta ADC have two sampling rates – input sampling rate f_s and output data rate f_d. The ratio of f_s and f_d is known as the decimation ratio.

The initial part of the architecture is the sigma-delta modulator, which is essentially the heart of the system. Besides sampling the incoming analog signal, it also performs another important function known as noise shaping. The modulator pushes the low-frequency noise up to higher frequencies outside the band of interest. Fig 2.12 [10] illustrates the working of a sigma-delta modulator in time domain.

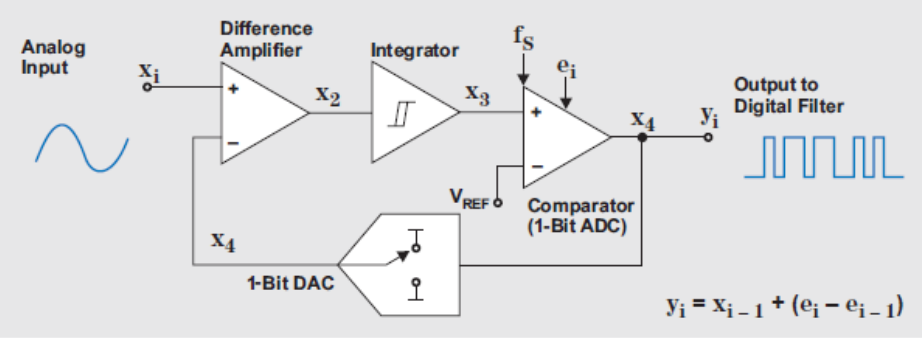

Fig 2.12 Σ-Δ modulator in time domain

The modulator acquires many samples of the analog input signals to produce a 1-bit stream of data. The system clock works in conjunction with 1-bit DAC to determine the sampling interval of the input. The loop begins with integrating the difference between the analog input and the DAC output. The output of the integrator goes into a comparator which converts it into a 1 or a 0 by comparing the input with a reference voltage. In this manner, quantization takes place at a high sample rate which is equal to the system clock. The ratio of number of ones and zeros represent the input analog voltage. Fig 2.13 shows the circuit of a sigma delta modulator designed on NI Multisim.

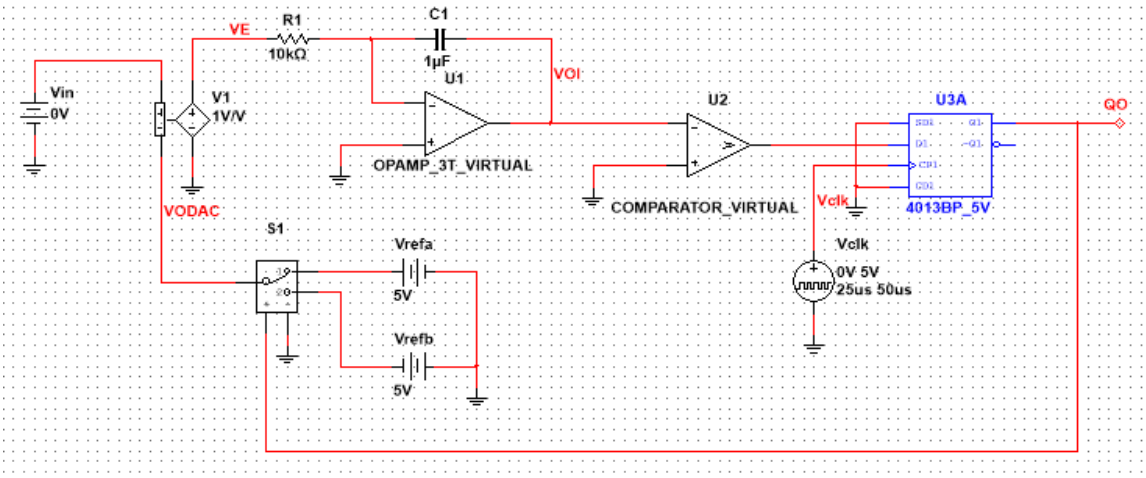

Fig 2.13 Σ-Δ ADC modulator circuit

Fig 2.14, 2.15 and 2.16 demonstrates the output waveforms of the flip-flop and integrator at input voltages 0V, 2.5V and -2.5V respectively.

It can be seen that at Vin = 0V, the duty cycle of the output is 50% and therefore the positive and negative slopes of the integrator are equal. Similarly, for Vin = 2.5V, the output is high for 3 clock cycles and low for 1 clock cycle. Therefore, the duty cycle here is 75. Finally, for Vin = -2.5V, the output of the flip-flop is high for 1 cycle and low for 3 cycles. So, the duty cycle here is 25%.

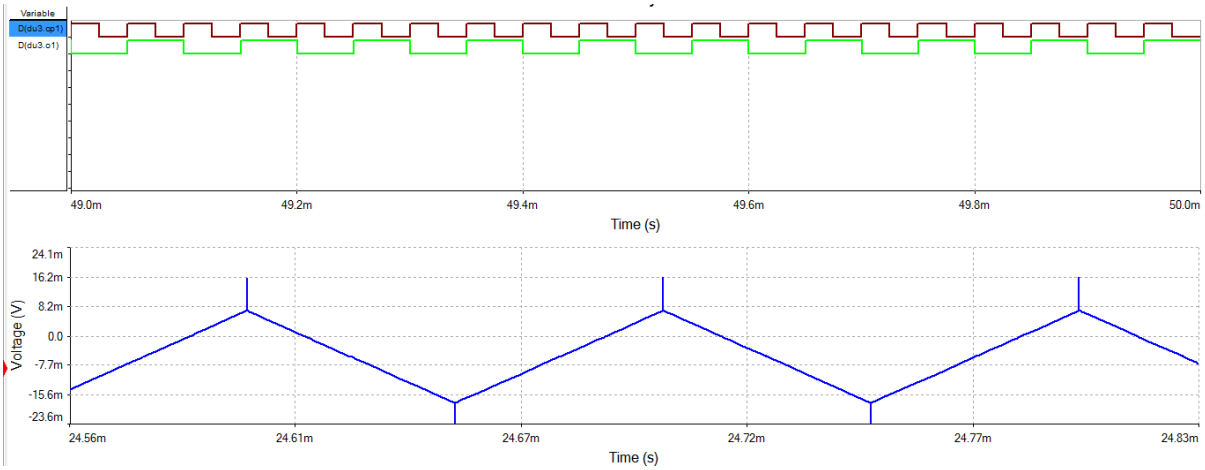

Fig 2.14 Output waveforms for Vin = 0V

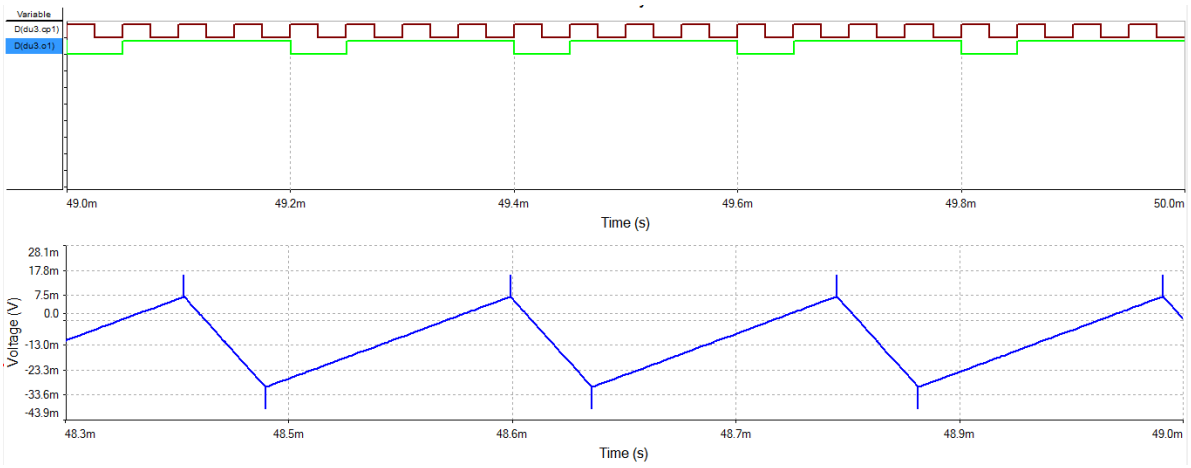

Fig 2.15 Output waveform for Vin = 2.5V

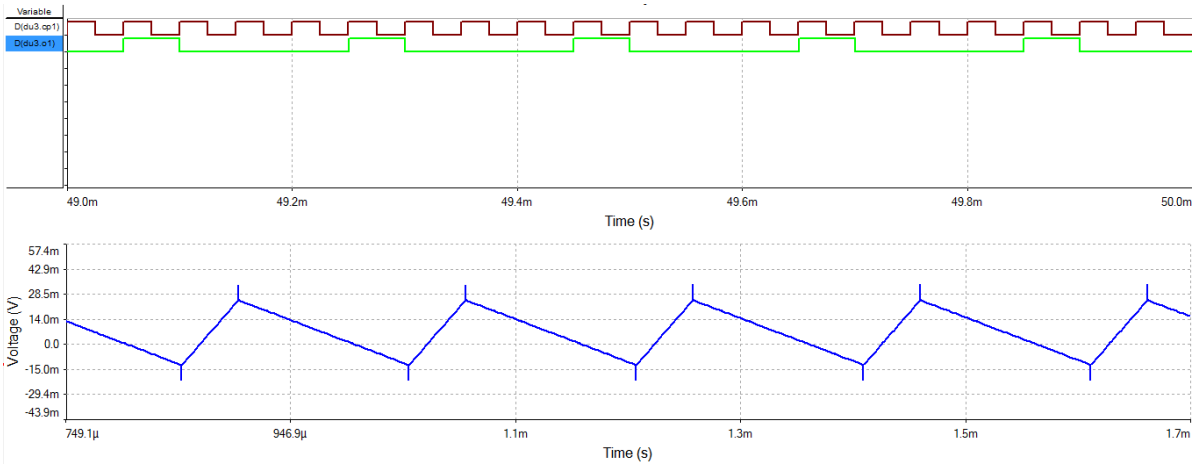

Fig 2.16 Output waveform for Vin = -2.5V

The output of the DAC in this circuit is

$V_{\text{oDAC}} = D.V_{\text{ref}} - (1-D)V_{\text{ref}}$, where D is the duty cycle of the output.

The integrator must cross a zero point once every cycle for the circuit to be stable. This was proven to be true in the output waveforms above. Therefore,

$$V_{\text{in}} - V_{\text{oDAC}} = 0$$

Or,

$$V_{\text{in}} - (2D-1)V_{\text{ref}} = 0$$

Therefore, the duty cycle is given as,

$$D = 0.5 \times (1 + V_{\text{in}}/V_{\text{ref}})$$

The integrator present in the system shapes the quantization noise to higher frequencies hence removing the low frequency noise from the conversion. Some sigma-delta modulators use two or more integrators to lower the in-band quantization noise even further.

The second part of the sigma-delta ADC is the digital/decimation filter. A low-pass averaging filter is the most common type of digital filter used in sigma-delta ADCs. The filter attenuates the modulator's quantization noise and reduces the frequency bandwidth. With the quantization noise reduced, the signal is now a high-resolution, digital version of the input signal.

The output rate of a digital filter is the same as the sampling rate which is still too fast to be useful. This is when the decimator comes into play. This circuit discards some of the samples from the digital filter output, hence reducing the output rate of the signal. The discarded samples don't contain any important information in the signal, instead they can be thought of as the filter's work-in-process samples. Therefore, after decimating the few samples, the new signal obtained has the same informational content as previous signal but now is at a slower data speed. Fig 2.17 [11] shows the waveform after the decimation process.

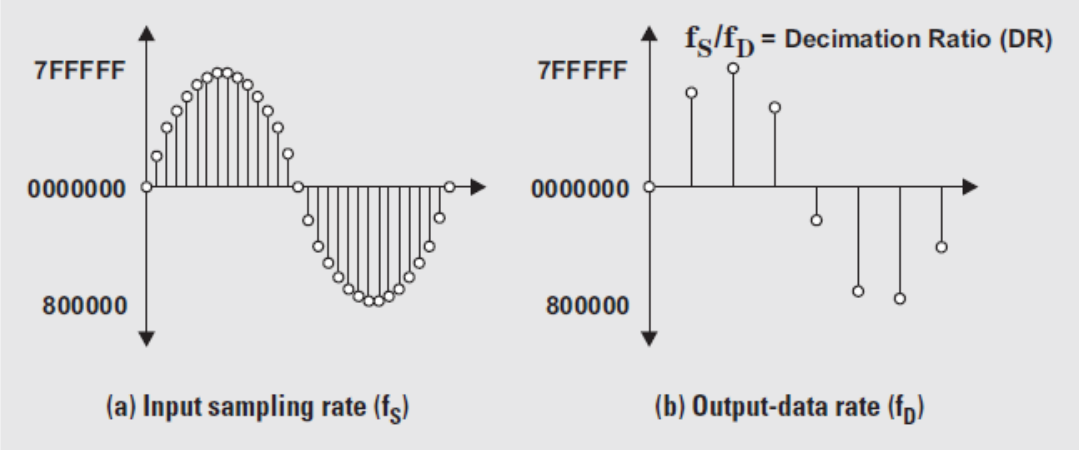

Fig 2.17 Decimation process output

Chapter 3

Operation of ADC circuit

The operation of a charge-redistribution SAR ADC takes place in three phases: (1) sample phase (2) hold phase and (3) bit-cycling phase. In this chapter, the process is explained with the help of a 4-bit ADC model.

3.1 Sample Phase

Figure 3.1 represents a 4-bit ADC model and the equivalent circuit of the capacitor array respectively. In the sample phase, the switch S_o is closed making the op-amp a voltage follower, the switch S_in is toggled to Vin and the switches S_c and S0-S3 are toggled toward the signal. During this phase, the op-amp holds a virtual ground at the inverting input and the capacitors are being charged with voltage Vin.

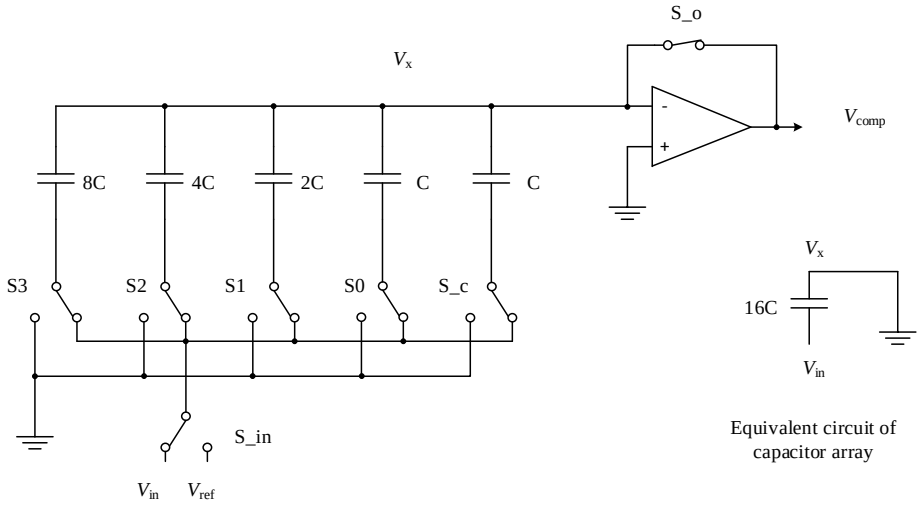

Fig 3.1 a) 4-bit ADC diagram b) equivalent circuit of capacitor array

3.2 Hold Phase

In the hold phase, the switches S_o, S_c, S0-S3, and S_in are toggled sequentially in the given order. First the switch S_o is opened which makes the op-amp function as a comparator. After this, the switches S_c and S0-S3 are toggled to ground making the capacitors hold the charge. Finally, the switch S_in is toggled to Vref and the circuit is ready for bit-cycling. The inverting input node voltage Vx in this phase is held at -Vin. The reason for sequentially toggling these switches is that in any other order, the inverting input voltage will not be Vin, hence making the conversion erroneous. Fig 3.2 shows the 4-bit ADC model and the equivalent capacitor array circuit in the hold phase.

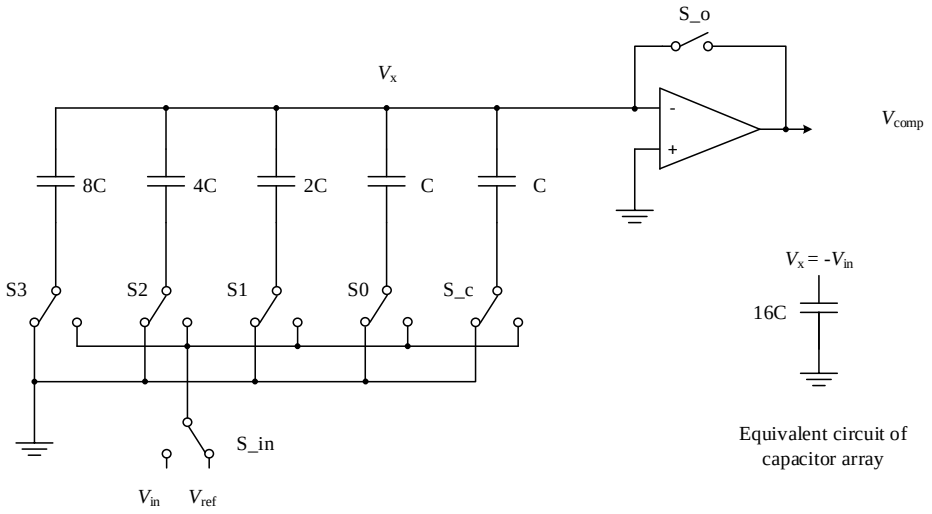

Fig 3.2 4-bit ADC model and the equivalent capacitor array circuit in the hold phase

3.3 Bit-cycling Phase

The bit-cycling phase is the final phase of the conversion process. The testing of the bits starts by toggling the MSB switch S3 towards Vref. This makes the voltage Vx equal to -Vin + Vref/2. The new Vx is now compared with 0V by the comparator. There are two outputs possible here:

1) If the Vcomp is low, Vref/2 > Vin and S3 is returned to ground.
2) If Vcomp is high, Vref/2 < Vin and S3 is left at Vref.

Fig 3.3 shows the 4-bit ADC model and the corresponding equivalent capacitive circuit for S3 in the bit-cycling phase.

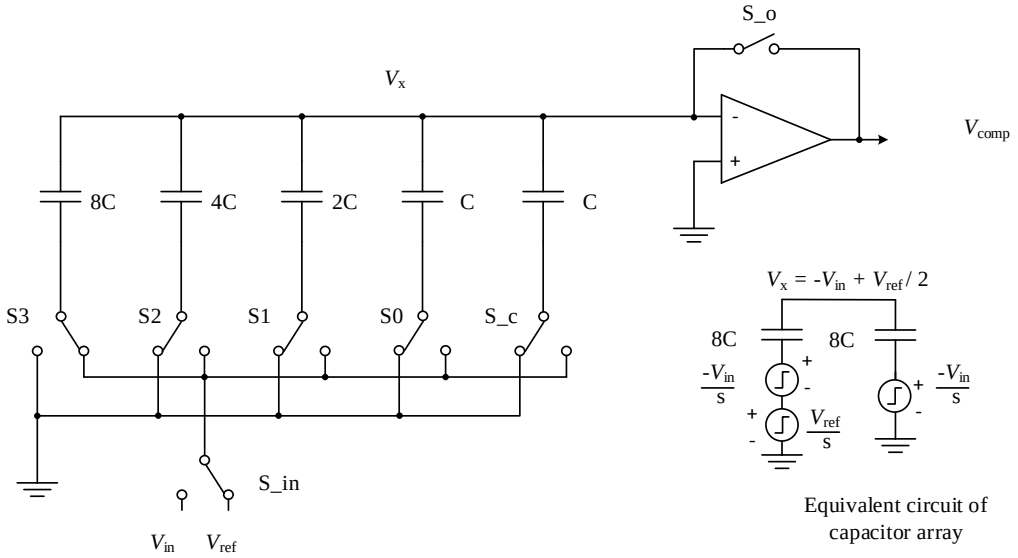

Fig 3.3 4-bit ADC model and the equivalent capacitor array circuit for bit S3

Once the output is generated by the comparator, it is stored in a latch and the next bit testing starts by toggling the switch S2 to Vref. Fig 3.4 shows an equivalent circuit of the capacitive array for the second bit-cycling step.

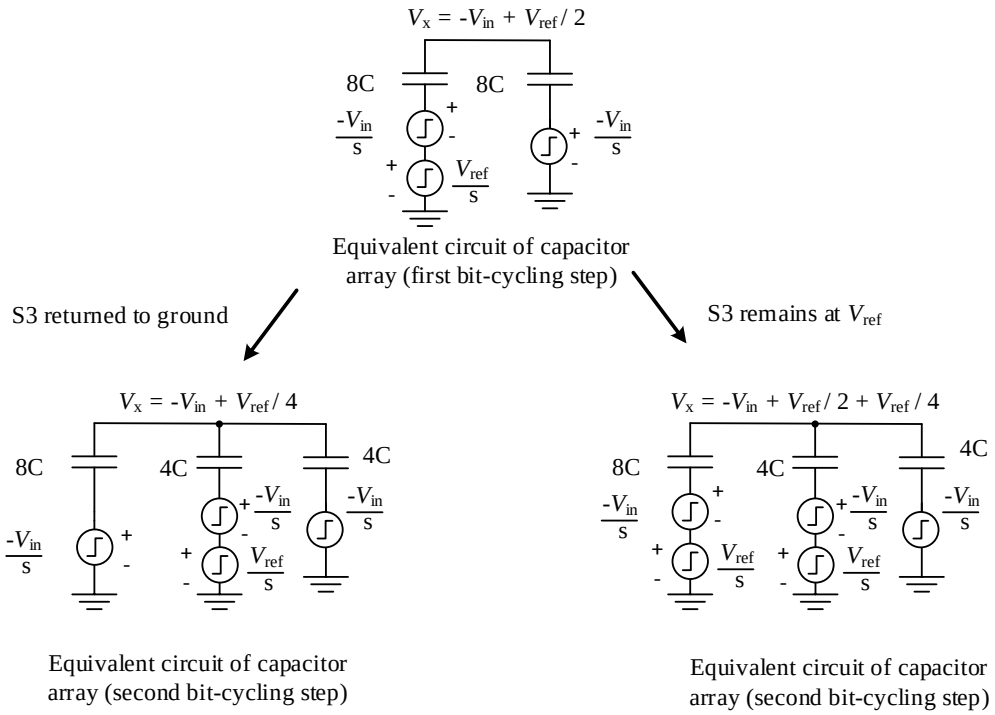

Fig 3.4 Equivalent capacitor array circuit for second bit-cycling step

For the second bit voltage Vref/4 is now added to the Vx. In the previous step, if the switch S3 was returned to ground, voltage Vx becomes -Vin + Vref/2. Whereas if S3 was left at Vref, voltage Vx becomes -Vin + Vref/2 + Vref/4. This voltage is again compared and Vcomp is also stored for second bit. This process continues sequentially until LSB is tested.

Once the conversion is complete, an end of signal (EOC) is generated by the bit-cycling circuit. The conversion is now stopped, and all the devices are reset to their initial states.

Chapter 4

Design of ADC circuit

To implement the ADC, it was first divided into different modules. These modules were designed and tested individually and later interfaced together to form the complete circuit. This chapter explains the design aspect and the working of these modules.

4.1 Clock Generation Circuit

The ADC logic employed requires a two phase non-overlapping clock as shown in the Fig 4.1. The signal Vclk provides a 500 KHz clock signal which is divided in frequency by two by U1A which is connected as a toggle flip-flop. U3A, U3B, and their associated inverters convert the outputs of U1A into non-overlapping signals PHI_A and PHI_B. Vclk, PHI_A, and PHI_B are present at all times.

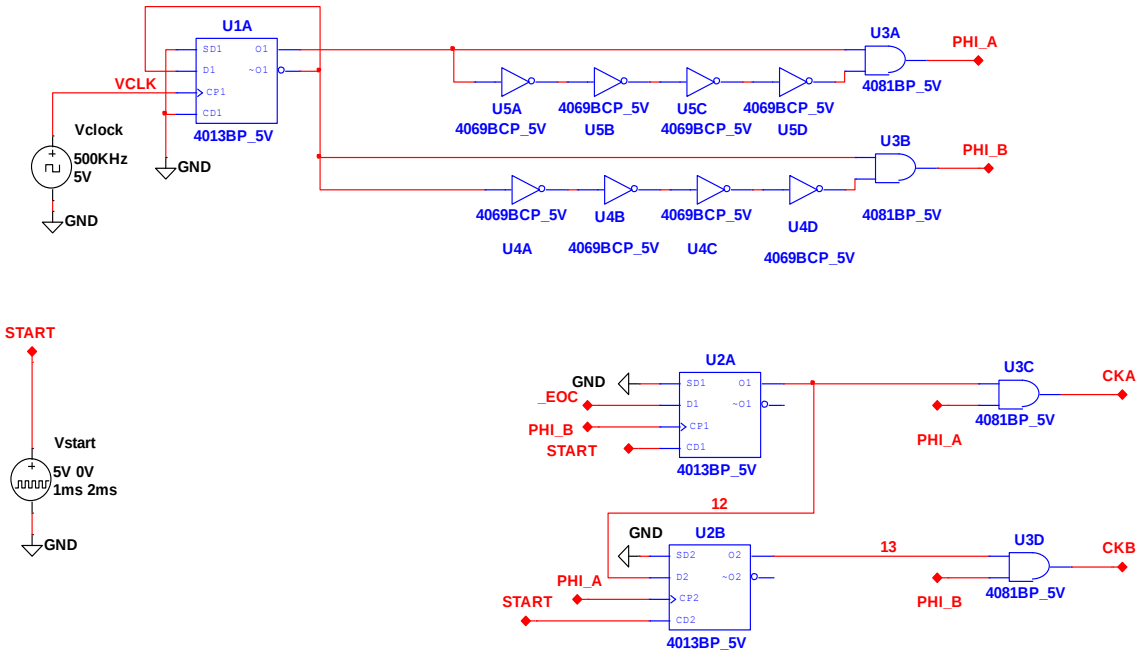

Fig 4.1 Clock generation circuit

On the rising edge of the clock Vclk, logic 1 is generated on Q1 and logic 0 on Q1_bar of U1A. The gate U3A receives logic 1 on one terminal which is directly connected to Q1, but the other terminal receives it after four propagation delays due to the 4 inverters present in the path. Therefore, to get PHI_A high the circuit has to wait for 4 propagation delay. Now, on the falling edge of Vclk, Q1 instantly goes low which in turn makes PHI_A low. Hence, to make it a logic 0 requires only one propagation delay.

The similar process takes place at the output Q1_bar but on opposite clock edges of Vclk. The purpose of this topology was to obtain to non-overlapping square waves PHI_A and PHI_B which were further used to obtain clock pulses CKA and CKB.

A conversion cycle is begun by asserting the active-high START signal. The START signal used in this work is a square wave that stays high for 5µs and then remains low throughout the conversion process. Fig 4.2 shows the clock generation and the START signal.

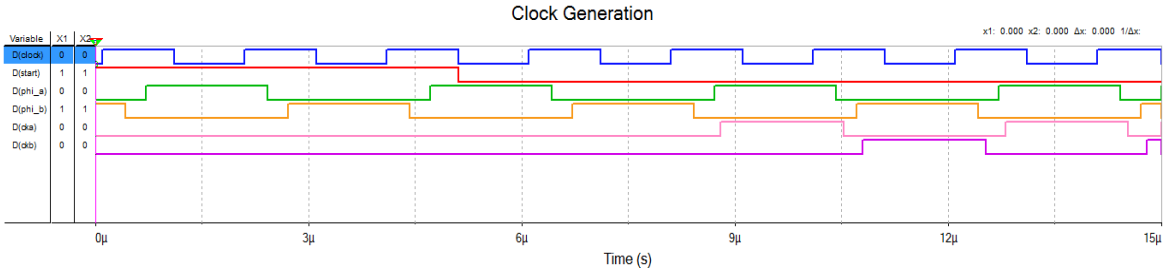

Fig 4.2 Output of the clock generation circuit with the START signal

Flip-flops U2A and U2B and associated AND-gates U3C and U3D are used to develop synchronized non-overlapping clock signals CKA and CKB. CKA is activated on the rising edge of PHI_B after the START line returns low, and activation of CKB occurs on the rising edge of PHI_A after CKA becomes active. Both CKA and CKB will continue to be active until the end of conversion.

At the end of the conversion cycle, the End of Conversion line (EOC) will go high, and /EOC will go low. CKA will be disabled on the rising edge of PHI_B after /EOC goes low, and CKB will be disabled on the rising edge of PHI_A after CKA is disabled. Fig 4.3 shows the shutdown process of clocks CKA and CKB after an EOC signal is received.

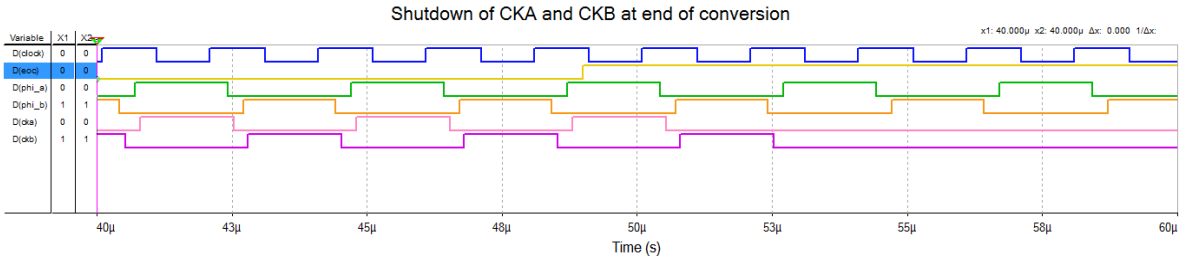

Fig 4.3 Shutdown of CKA and CKB

4.2 Switch Sequencing Logic Circuit

Fig 4.4 presents the charge redistribution circuit. In this circuit, three D flip-flops U1B, U6A and U6B are cascaded in series. The output Q2_bar of U6B goes to the two inputs of an AND gate U8, one directly and other through 3 inverters to provide suitable propagation delay.

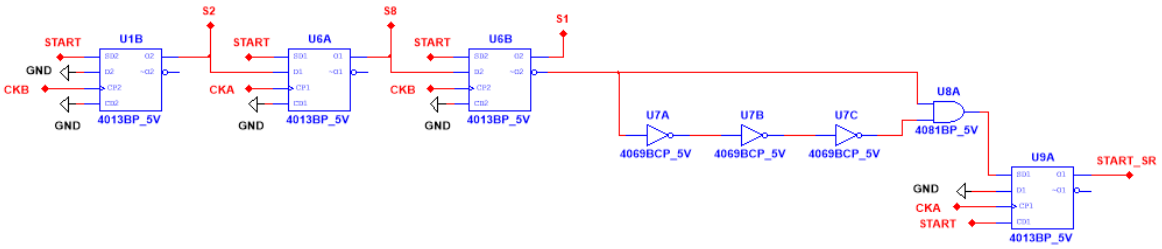

Fig 4.4 Switch sequencing logic circuit

The output S2 controls the feedback switch of the op-amp/comparator. Initially this switch is closed making the op-amp a voltage follower. The signal S8 controls the switch connected to the first capacitor C1. Finally, the signal S1 controls the switch which toggles between the input voltage Vin and the reference voltage Vref. The working of the capacitor array and these switches are explained later chapters. The key point here is that the signals S2, S8 and S1 are produced sequentially, hence making the switches a 'break before make' type. Once all these switches are toggled, the D flip-flop U9A gets set on the rising edge of CKB and presets the bit-cycling circuit. Fig 4.5 shows the signals S2, S8 and S1 being produced.

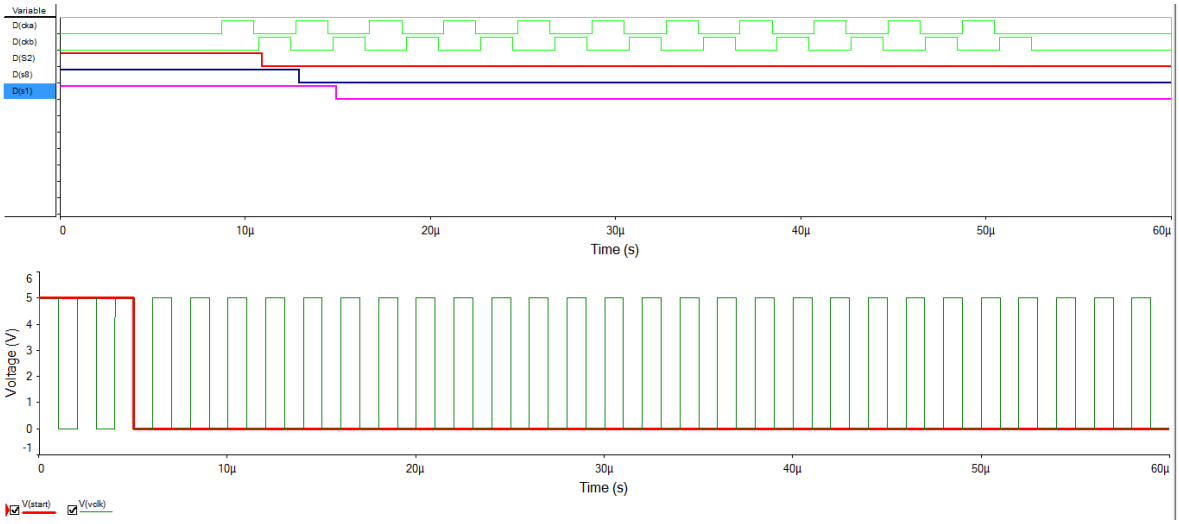

Fig 4.5 Signals S2, S8 and S1 produced sequentially

4.3 Bit Cycling Circuit

Fig 4.6 and Fig 4.7 demonstrates the bit-cycling circuits. The circuit (a) is for controls the first 3 most significant bits (MSB) of the converter. The circuit (b) controls the final 5 bits and produce the EOC signal. The flip-flops U10A, U14A, U13A, U17A, U19A, U54A, U59A, U64A and U20A form a 1-bit shift register. Whereas, the flip-flops U10B, U14B, U13B, U17B, U19B, U54B, U59B and U64B acts as latches.

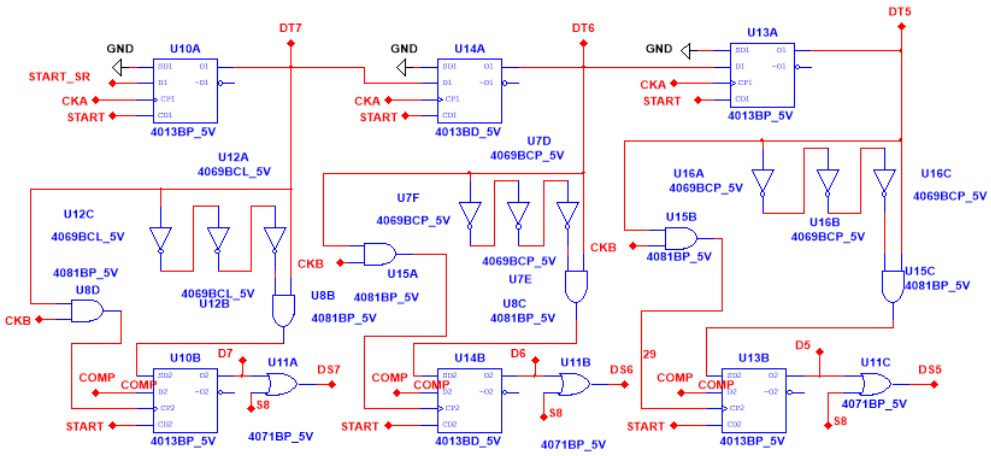

Fig 4.6 Bit-cycling circuit (a)

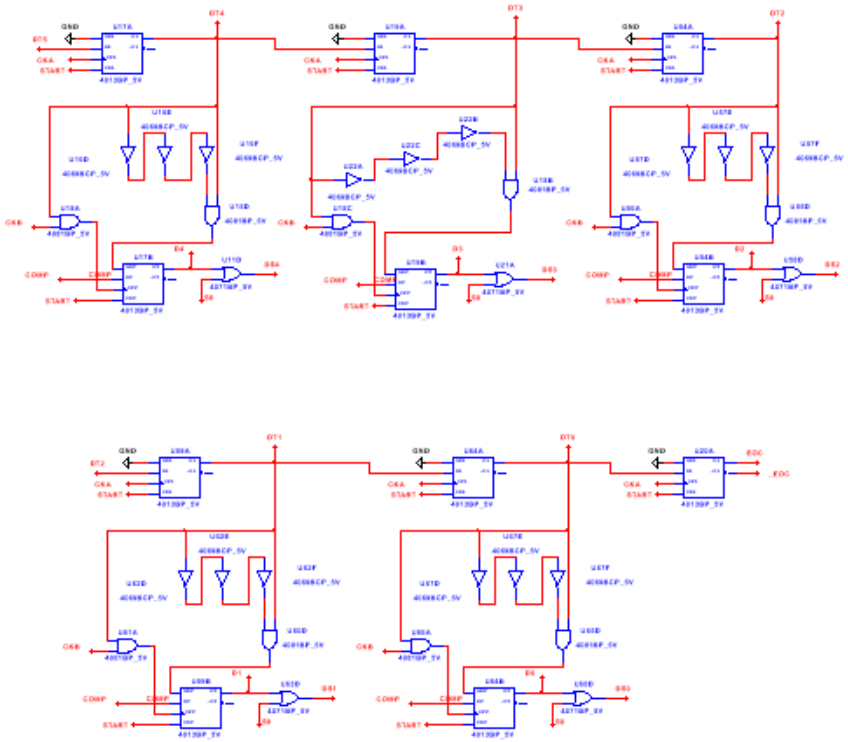

Fig 4.7 Bit-cycling circuit (b)

For demonstration, the bit-cycling circuit of the MSB is shown in the Fig 4.8. When the START_SR signal arises from the preset flip-flop U9A, it activates the flip-flop U10A. Now U10A sets the flip-flop U10B which flips the switch connected to MSB capacitor towards Vref. The comparator output COMP is received on D input of U10B and gets latched in the output. The latching process takes place on the rising edge of CKB. Hence, at every rising edge of CKA the shift register shifts logic 1 towards right, which means the next bit from MSB is ready to be checked. Then on rising edge of CKB the output gets latched. This process continues until an EOC signal is obtained which signifies the conversion is complete. To start the conversion again, the START signal must be asserted again. The outputs of the bit-cycling circuit are displayed in the Fig 4.9.

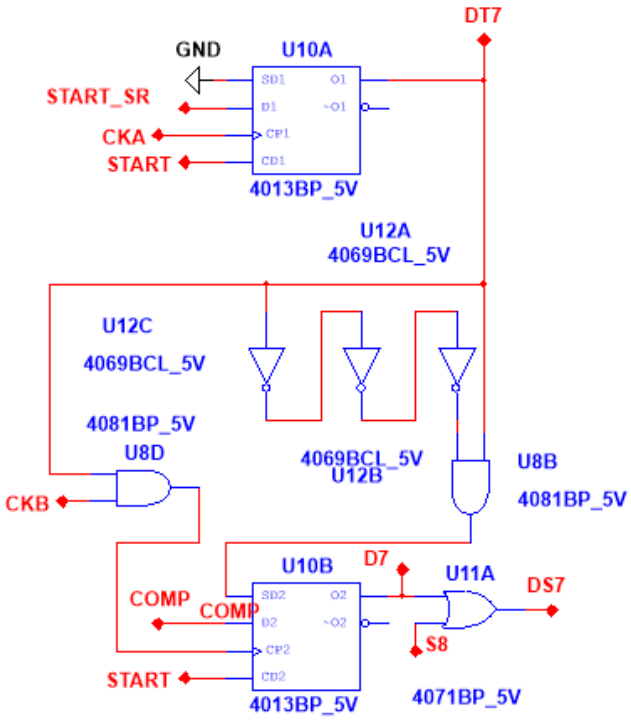

Fig 4.8 Bit-cycling circuit for the MSB

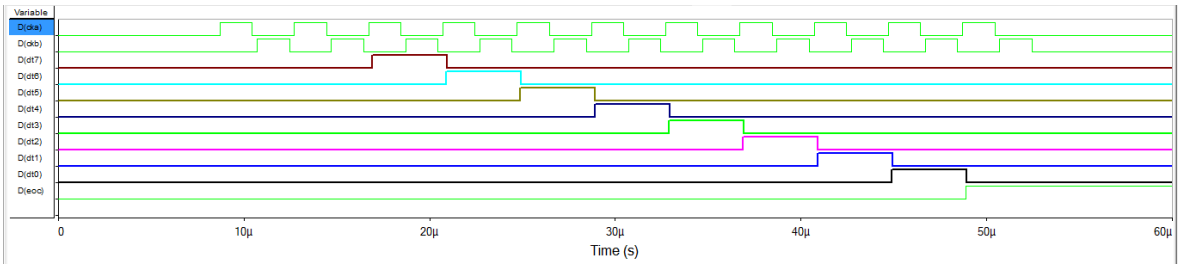

Fig 4.9 Output of the bit-cycling circuit

4.4 Binary Weighted Capacitive Array

Fig 4.10 displays the 8-bit binary-weighted capacitive array. This array functions as a charge-redistribution DAC. The capacitor values start from 1pF and continue increasing in the power of 2 until 128pF is obtained, hence, giving a total capacitance of 256pF. The highest value is signifying the MSB of the data and the lowest to LSB. The capacitor C1 doesn't represent any bit. One end of the array is shorted and fed into the inverting terminal of the comparator. The other ends are individually connected to the output of the logic switches.

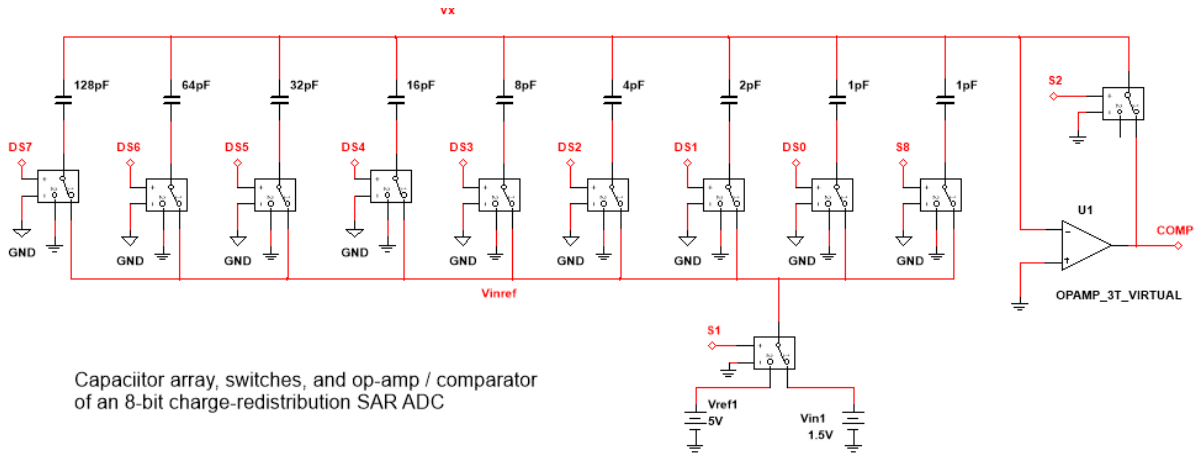

Fig 4.10 Binary weighted capacitive array

4.5 Switch Implementation

As described previously in the charge redistribution section, the ADC utilizes switches at eleven places. These switches are controlled by signal S1, S2 and bit-cycling switches controlled by digital signals DS0-DS7 ORed with S8. The accurate working of the ADC depends on the efficiency and the timing of these switches. These 11 switches are explained below:

Fig 4.11 shows the switch controlled by the signal S1. This switch is responsible for toggling between the reference voltage and the input voltage and acts a single pole double throw switch. This switch was designed using NMOS and PMOS devices employed in the transmission gate configuration. One transmission gate has the input Vin and the other Vref. These gates are controlled by the signal S1 being fed to the gates of the MOSFETs after an appropriate delay. When the signal S1 is logic 1, the output of the switch is Vin. Similarly, for logic 0, the output is Vref.

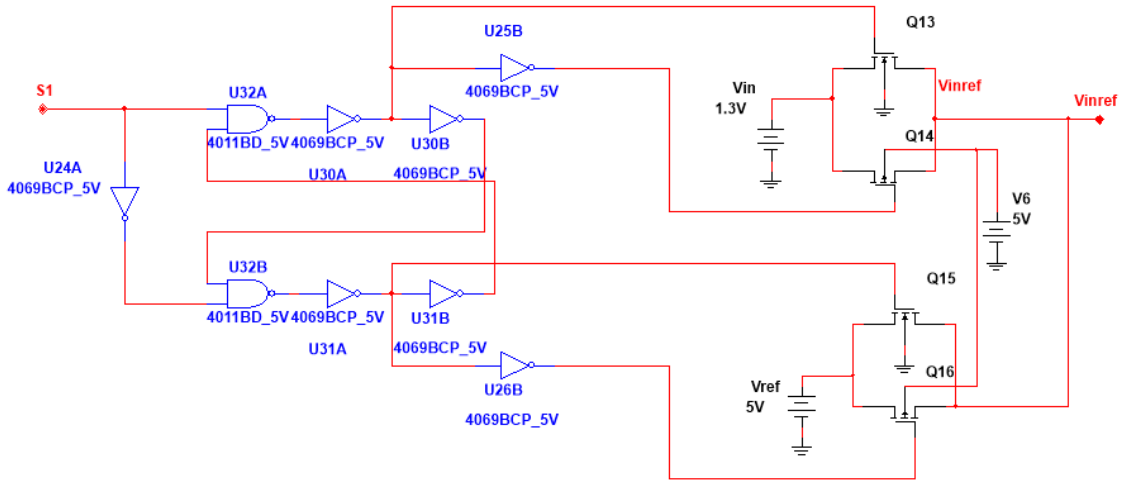

Fig 4.11 Logic switch controlled by signal S1

The second switch shown in the Fig 4.12 is the one controlling the feedback loop of the comparator. This switch functions as a single pole single throw here, therefore, it was implemented using only a NMOS Q1. It is controlled by the signal S2. Since, the drain of Q1 is connected to the inverting terminal of the comparator, it needs to handle negative voltage also. Therefore, the gate of Q1 have to be below the drain voltage to properly switch off. This was not possible with the signal S2 as it is a 0V to 5V signal. To resolve this, a voltage level shifter was designed that can convert a 0V to 5V input into -5V to +5V signal. The voltage shifter is described later in this chapter.

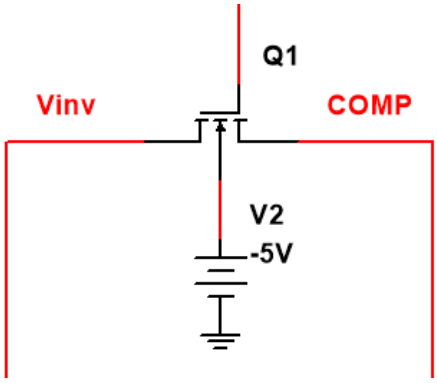

Fig 4.12 Feedback loop switch controlled by signal S2

The switch shown in the Fig 4.13 is for the MSB capacitor of the capacitor array. Controlling signal DS7 activates the switches that connect the capacitor (connected to DSO7) to either ground (through NMOS switch Q12) or to Vin/Vref (through CMOS transmission gate Q2/Q11). The logic gates ensure “break-before-make” action of the switches. The rest eight switches are similar.

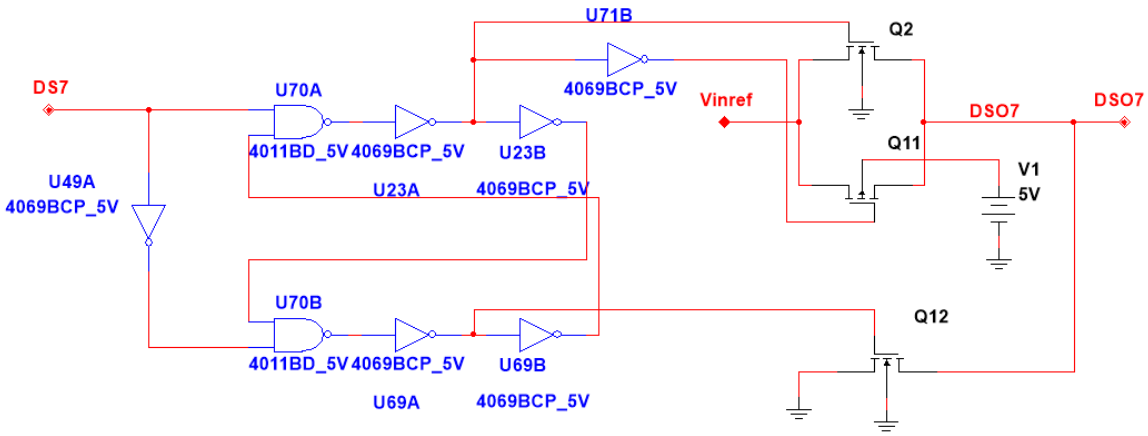

Fig 4.13 Logic switch connected to the MSB capacitor in the array

4.6 Voltage Level Shifter

As described in the previous section, a voltage level shifter was required to convert the 0-5V logic signal S2 into a -5V to +5V signal for the NMOS switch Q1. A 2-stage op-amp with common source output was designed to be used in open loop configuration. Fig 4.14, displays the schematic of the voltage level shifter.

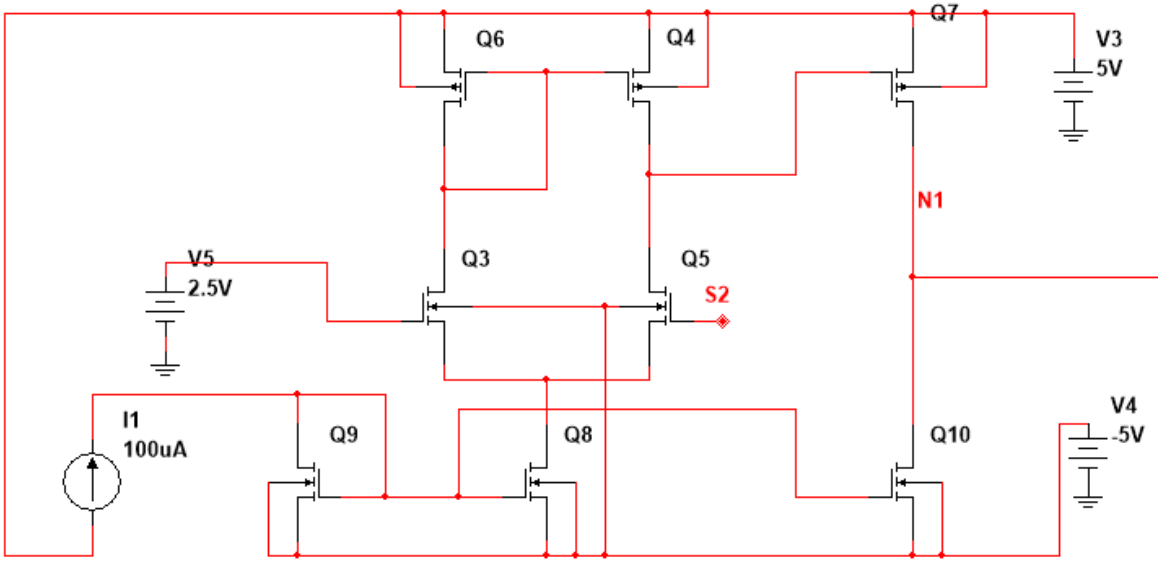

Fig 4.14 Voltage level shifter circuit

The op-amp has a PMOS differential pair with a NMOS current source. The inverting input is referenced to +2.5V and the non-inverting terminal receives the signal S2. The supply voltages are +5V and -5V. When the signal S2 is logic 1, voltage in non-inverting terminal is higher than inverting terminal which turns on the PMOS Q7 hence producing +5V on the output terminal. Similarly, when S2 is logic 0, NMOS Q10 is turned on producing -5V on the output. The MOSFET models used are 5µm level 1 models taken from Sedra and Smith [20]. The output of the voltage level shifter is displayed in the Fig 4.15 below.

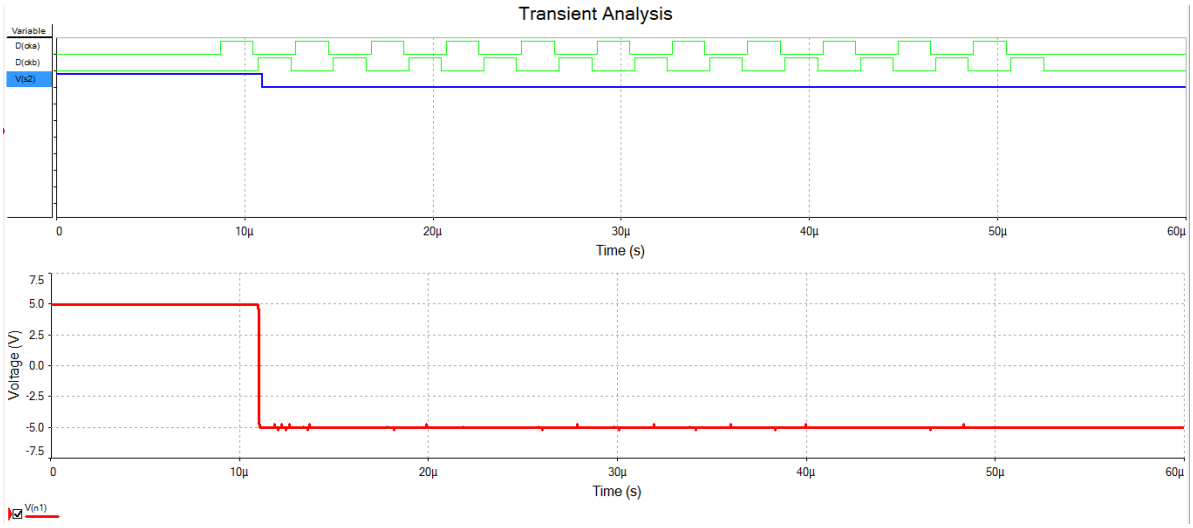

Fig 4.15 Output of the voltage level shifter

4.7 Op-Amp/Comparator

For comparator, another two-stage op-amp was implemented using the 5µm MOSFET models. The differential pair and the current mirror was implemented using PMOS and the current sink using NMOS. The supply voltage is +5V and – 5V. For the output stage, a common source amplifier was included. The compensation capacitor and resistors used here are 747Ω and 0.5pF respectively. Fig 4.16 displays the circuit diagram of the op-amp.

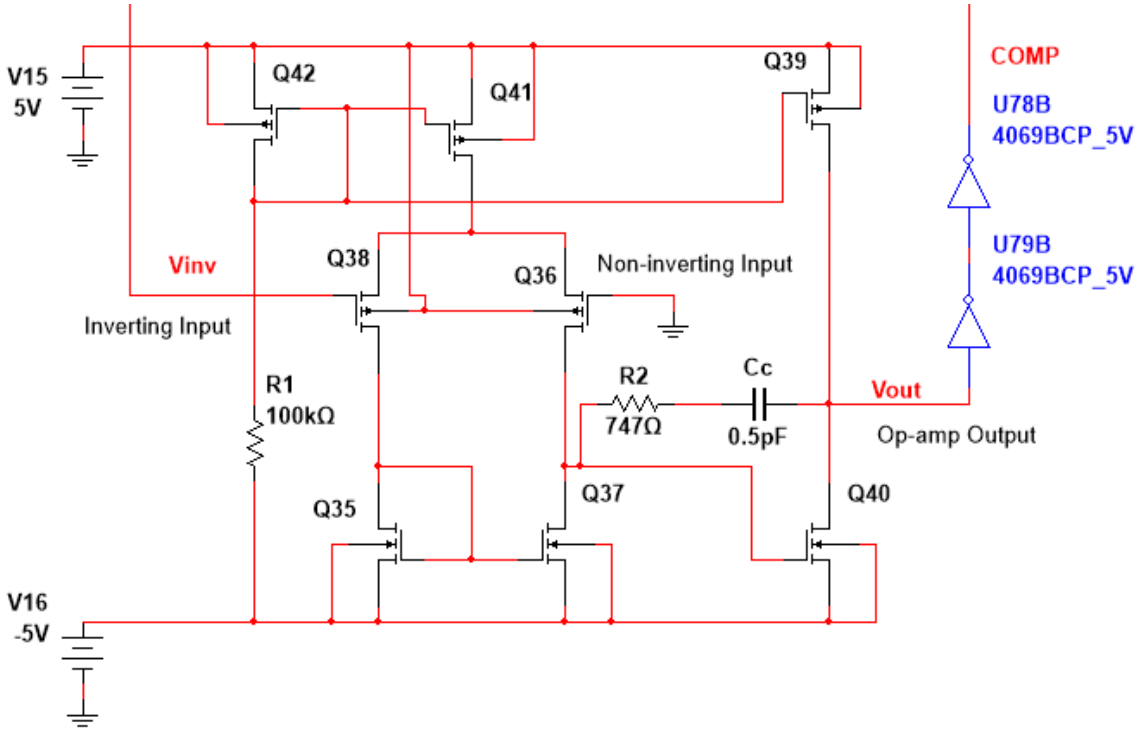

Fig 4.16 Comparator circuit

The inverting terminal is connected to the output of the capacitor array, while the non-inverting terminal has been grounded. The output of the op-amp goes to two inverters in series acting as buffer stage, to give the final output of the comparator.

The dc open-loop gain obtained was 67.33dB. Open-loop gain dropped to 0dB at 94.8MHz at which frequency the phase of the open-loop gain was -138.14° giving a phase margin of 41.86°. Fig 4.17 shows a Bode plot of the ac open-loop gain.

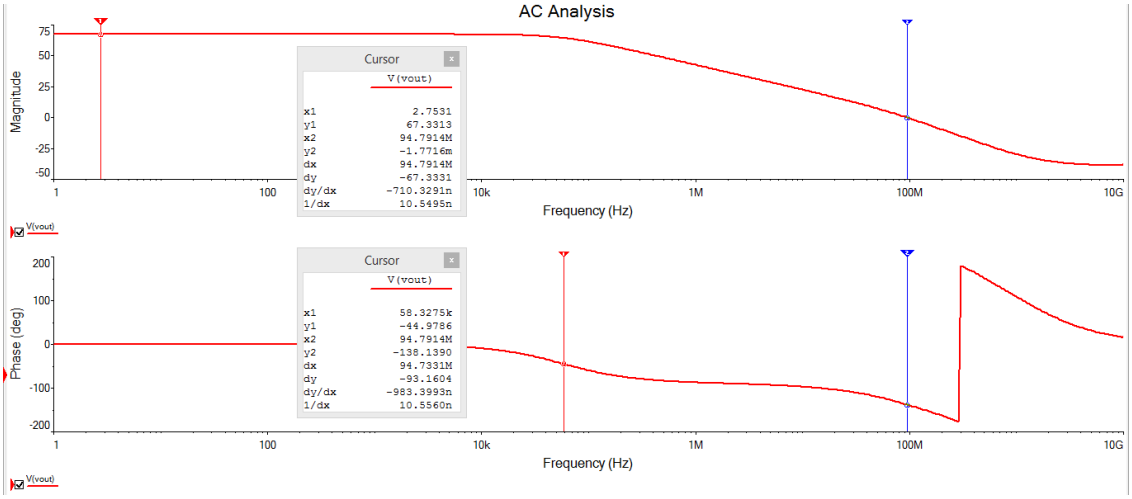

Fig 4.17 DC open loop gain and phase graphs of the comparator

The dc output swing obtained was between -4.45V to 4.05V as shown below in the Fig 4.18. The op-amp was configured as a voltage follower for this simulation.

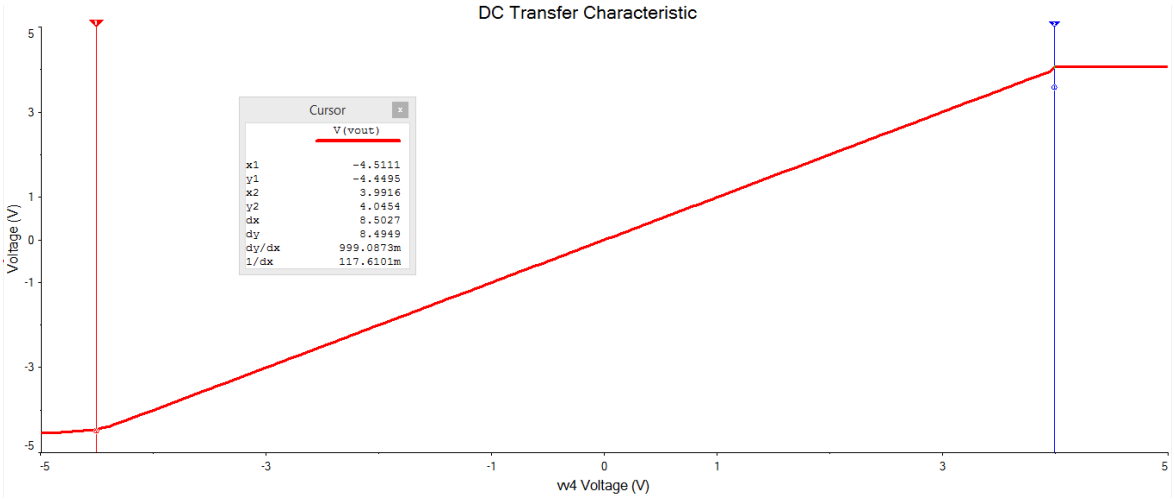

Fig 4.18 DC output swing of the op-amp

The positive and negative slew rates were found to be 246 V/us and 328.5 V/us respectively. The plots are shown in the Fig 4.19 and 4.20.

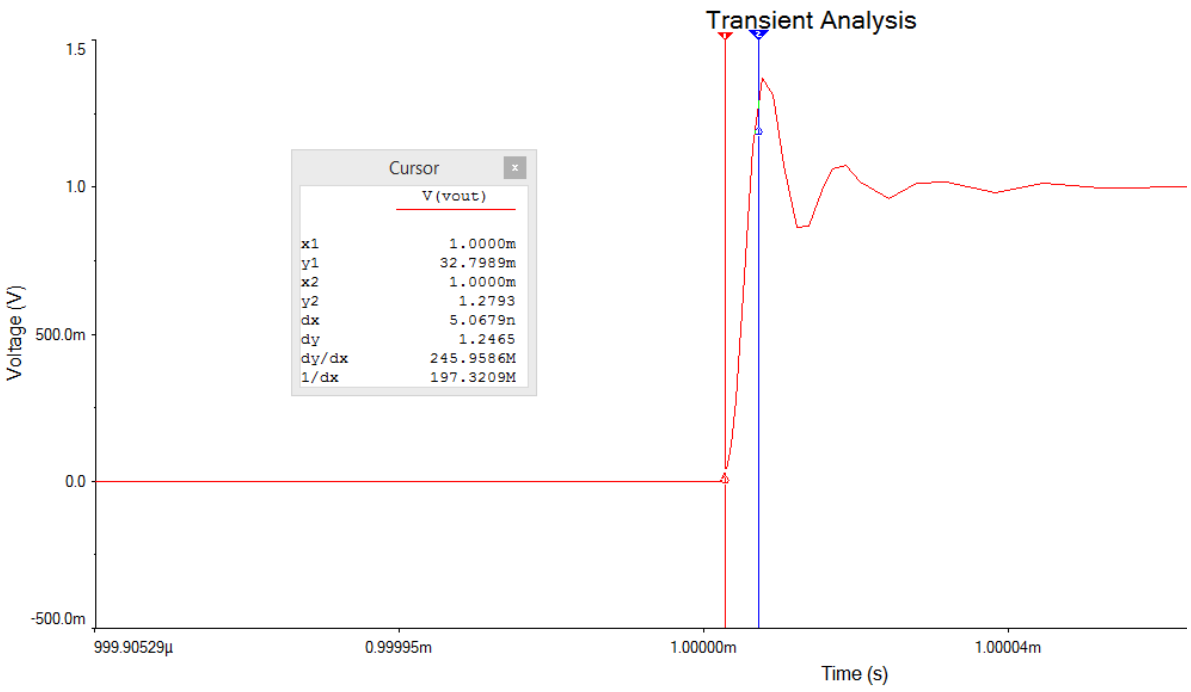

Fig 4.19 Positive slew rate of the op-amp

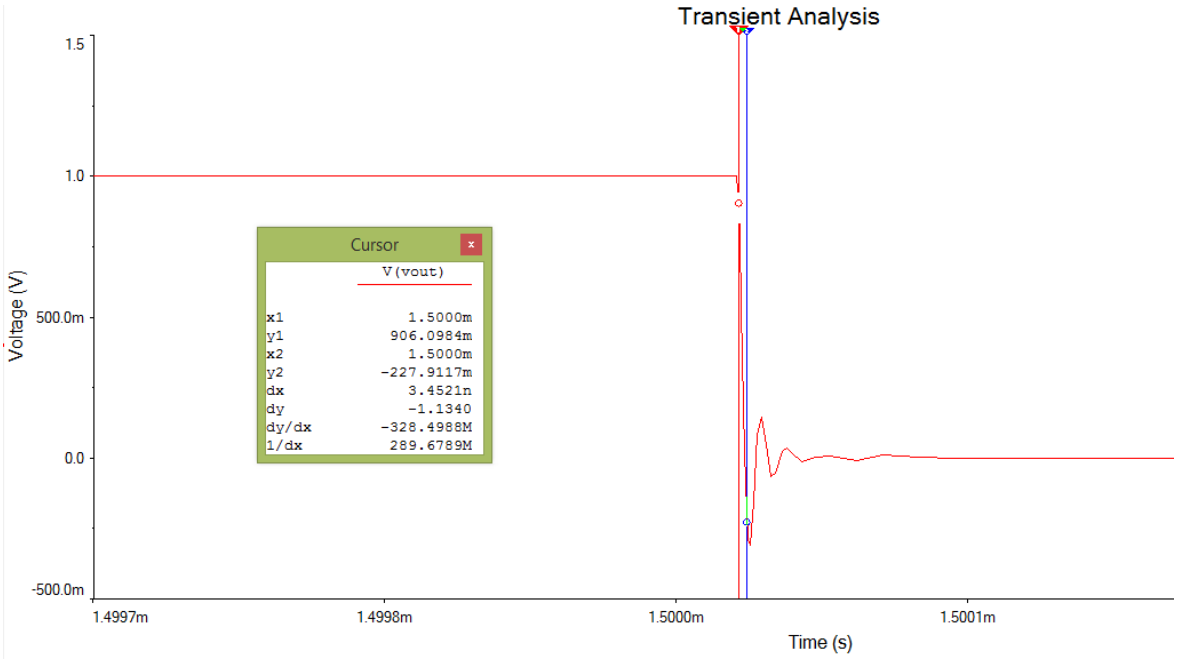

Fig 4.20 Negative slew rate of the op-amp

Chapter 5

Results

This chapter discusses the digital outputs obtained from the circuit with the help of examples. The later section estimates the power dissipated by the ADC during the operation cycle.

5.1 Digital output

The output code of the ADC is given by $(Vin \times 2^N)/Vref$, where N is the number of bits. For example, if the input is Vin = 2V and since, the value of N here is 8 and Vref is 5V, the output will come out to be $(2 \times 256)/5 = 102.4 \approx 102$. The digital code obtained from the ADC will be the 8-bit binary equivalent of 102 which is 01100110.
Three different input voltages were considered for testing the ADC and their corresponding outputs are presented below.

Fig 4.1 demonstrates the digital output corresponding to the input of 1.3V. The reference voltage Vref is 5V for all the cases. D7 is the MSB, D0 is the LSB and EOC is the end of conversion signal. When the START signal arrives the clocks CKA and CKB gets activated. These clocks start the conversion process. It can be seen that the bits D7, D5, D4, D3 and D0 gets high for a small period then gets low, whereas bits D6 and D1 gets high and remains as it is during the entire process. This signifies the output obtained in binary was 01000010 which is equivalent to 66 in decimal.
The output code for Vin = 1.3V should be $(1.3 \times 256)/5 = 66.56 \approx 66$. Hence, the accuracy of the ADC can be verified.

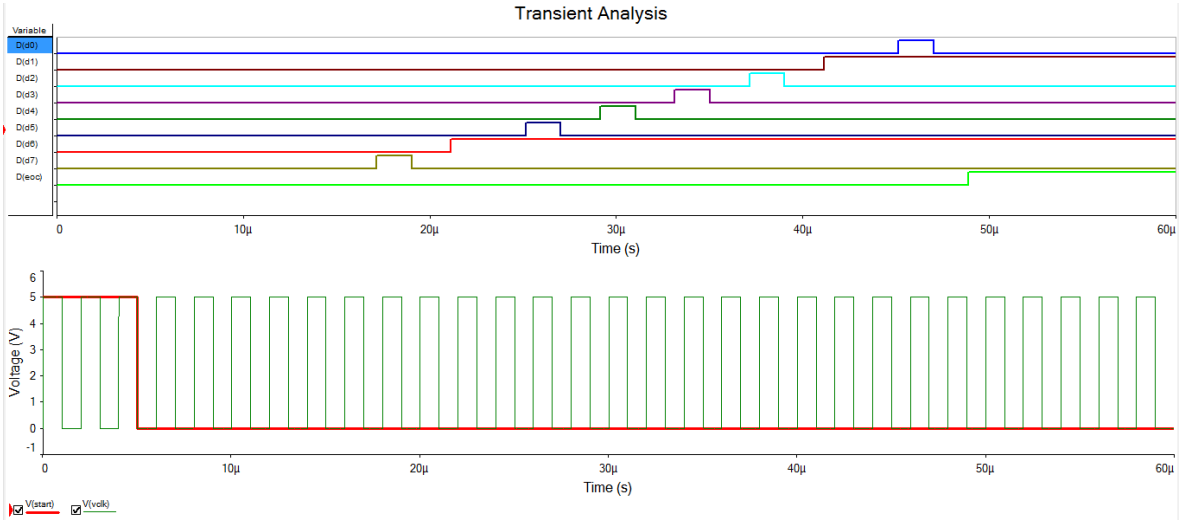

Fig 5.1 Digital output for Vin = 1.3V

Similarly, for the second case, Vin was taken to be 3V. The output obtained from the ADC was 10011001. For Vin = 3V, the output should be $(3 \times 256)/5 = 153.6 \approx 153$. 153 in 8-bit binary is 10011001 which matches with the ADC output as displayed in the Fig 3.2 below.

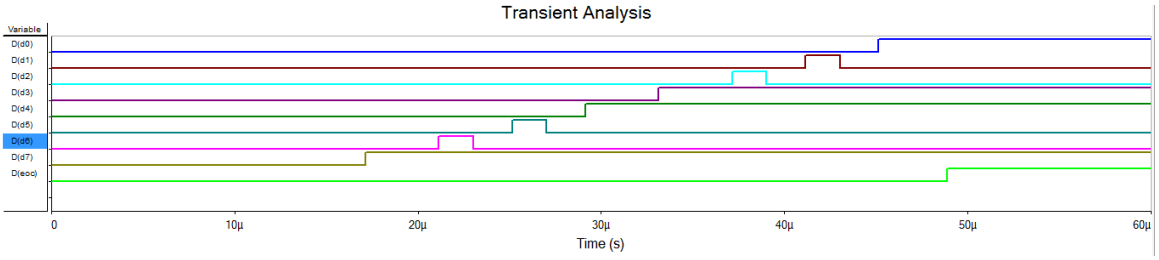

Fig 5.2 Digital output for Vin = 3V

Finally, for the last case, Vin was taken to be 4.26V. The digital output obtained was 11011010 as shown in the Fig 4.3. For Vin = 3V, the output should be $(4.26 \times 256)/5 = 218.112 \approx 218$ which is 11011010 when converted in 8-bit binary notation.

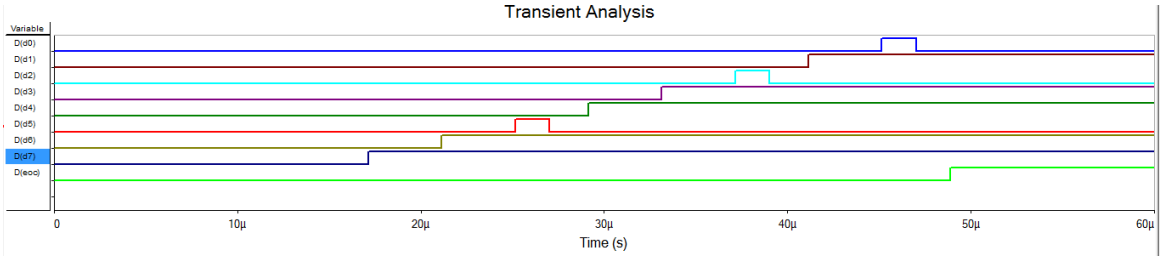

Fig 5.3 Digital output for Vin = 4.26V

5.2 Power Dissipation

The power dissipation for the circuit was calculated during the conversion period of the ADC. Most of power dissipated is in the clock generation circuit, the voltage level shifter and the comparator. Since, the bit-cycling circuit and the charge redistribution circuit are ON for a very short period, the power dissipated by them are negligible. Moreover, during the conversion period, the capacitors in the DAC are not being charged or discharged. Their respective charge is only being redistributed through the capacitor array making the net charge across the array to be constant. Hence, the power dissipation in the DAC during the conversion cycle remains zero.

For clock generation circuit, the capacitances of the D flip-flops and the logic gates were assumed to be 2pF. Since, the frequency of the main clock is 500 kHz, the clocks CKA and CKB are of 250 kHz. The clock CKA drives eleven devices in the circuit, therefore, the power dissipated due to CKA is:

$$P_{CKA} = \text{Freq} \times \text{Total Capacitance} \times V_{DD}^2$$

$$P_{CKA} = 250\text{kHz} \times 11 \times 2\text{pF} \times 5^2 = 137.5\ \mu\text{W}$$

Similarly, clock CKB drives ten devices, therefore, the power dissipated due to clock CKB is:

$$P_{CKB} = 250kHz \times 10 \times 2pF \times 5^2 = 125\ \mu W$$

Total power dissipation by the clock generation circuit is **262.5 µW**.

The power dissipation in the voltage level shifter and the comparator can be calculated by the currents generated in the circuit due to the supply voltage. These circuits don't depend on the frequency of the clock as they dissipate static power throughout the conversion period. The power in the voltage level shifter is calculated as:

$$P_{VLS} = (V_{DD} - V_{SS}) \times I_{Total}$$

The total current flowing through the circuit is the sum of the drain currents of the MOSFETs Q6, Q4, Q7 and I1 from the current source. Their values are given in the table 5.1 below

Table 5.1 Drain currents of the current source MOSFETs in the voltage level shifter circuit

MOSFET/Current Source	Current (µA)
Q6	48.24 µA
Q4	54.04 µA
Q7	108.04 µA
I1	100 µA
Total	**310.32 µA**

Therefore, $P_{VLS} = (5 - (-5))V \times 210.32\ \mu A =$ **3.10 mW**

Similarly, for the op-amp/comparator circuit, the total current flowing is the sum of the drain currents of Q42, Q41 and Q39 which is shown in the table 5.2 below:

Table 5.2 Drain currents of the current source MOSFETs in the op-amp/comparator circuit

MOSFET	Current (A)
Q42	68.38 µA
Q41	535.0 µA
Q39	1.11 mA
Total	**1.71 mA**

Therefore, $P_{COMP} = (5 - (-5))V \times 1.71mA =$ **17.1 mW**

Hence, the total current dissipated by the circuit during the conversion cycle is **20.46 mW**. The table 5.3 gives the percentage of power dissipated by individual blocks.

Table 5.3 Distribution of power consumption between different blocks of the ADC

Block	Percentage of power dissipation
Clock generation circuit	1.28 %
Voltage level shifter	15.15%
Op-amp/Comparator	83.57 %

Chapter 6

Conclusions and Future Work

In this thesis, an 8-bit charge redistribution SAR ADC was successfully implemented and tested. It operates at a supply voltage of 5V with a speed of 500KHz. The ADC consists of six modules namely- clock generator, charge redistribution DAC, two-stage comparator, bit-cycling circuit, switch logic and voltage level shifter. These modules were designed and tested individually on NI Multisim.

The comparator is one of the most critical part of the ADC. In this work, a two-stage op-amp was designed to function as the comparator. The circuit was built using complementary NMOS and PMOS devices on 5µm level-1 MOSFET models. The open loop gain obtained was 67.33dB, whereas the phase margin was 41.86°.

The bit-cycling logic was developed using the D flip-flops and inverter gates available in the Multisim. This logic requires two-phase non-overlapping clocks for its operation. Therefore, a clock generation circuit was also designed using the flip-flops and inverters with an appropriate delay.

The estimated dynamic power dissipation was also calculated and was found to be 20.46mW during conversion

Future work may be done on both the design level and the circuit level. The design can be further extended to higher number of bits by including more capacitors in the DAC and replicating the bit cycling circuit and the switches for the additional bits. This will increase the accuracy and the resolution of the ADC.

The circuit can be modified by designing the D flip-flops and the inverters using MOSFETs. The design must correctly include the propagation delay of the circuit. This will provide a more accurate calculation of the power dissipation.

Further improvement in the design can be made by replacing the MOSFET models to a lower technology. This will reduce the supply voltage and hence, decrease the power consumption and increase the conversion speed of the ADC.

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