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ANALYSIS OF DYNAMIC LOGIC CIRCUITS IN DEEP SUBMICRON CMOS TECHNOLOGIES

by

RAHUL C. MUPPASANI

A thesis submitted in partial fulfillment

of the requirements for the degree of

Master of Science in Electrical Engineering

Department of Electrical Engineering

David H. K. Hoe, Ph.D., Committee Chair

College of Engineering and Computer Science

The University of Texas at Tyler

November 2012

The University of Texas at Tyler
Tyler, Texas

This is to certify that the Master's Thesis of

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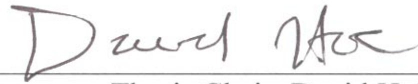

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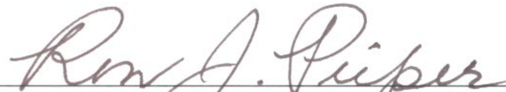

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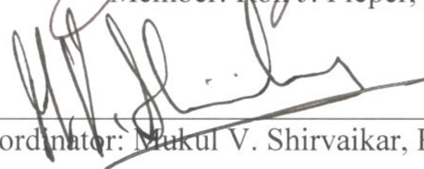

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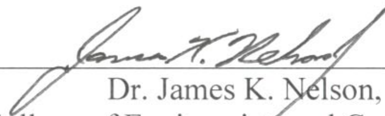

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Abstract

ANALYSIS OF DYNAMIC LOGIC CIRCUITS IN DEEP SUBMICRON CMOS TECHNOLOGIES

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Thesis Chair: David H. K. Hoe, Ph.D.

The University of Texas at Tyler

November 2012

Dynamic logic circuits are utilized to minimize the delay in the critical path of high-performance designs such as the datapath circuits in state-of-the-art microprocessors. However, as integrated circuits (ICs) scale to the very deep submicron (VDSM) regime, dynamic logic becomes susceptible to a variety of failure modes due to decreasing noise margins and increasing leakage currents. The objective of this thesis is to characterize the performance of dynamic logic circuits in VDSM technologies and to evaluate various design strategies to mitigate the effects of leakage currents and small noise margins.

In order to effectively simulate the performance of dynamic logic circuits at the nanoscale dimensions, the required interconnect scaling model is described and a transistor predictive technology model is utilized. The design optimization of the dynamic logic circuits is discussed and this method is illustrated via the design of full adder circuits using various dynamic logic families.

The effects of charge sharing and charge leakage are major concerns in the implementation of dynamic logic.

Weak pull-up transistors known as bleeder devices are used to compensate for the loss of charge from the dynamic storage node. The impact of these devices on the performance of dynamic logic was evaluated through the addition of a noise generator circuit to the simulations. It is concluded that increasing leakage currents in nanoscale technology will be a major concern but functional dynamic logic circuits can be implemented in VDSM technologies through the introduction of properly sized bleeder devices. However, some degradation in circuit speed is expected.

Chapter One
Introduction

The design optimization of processors used in modern electronic devices has several conflicting goals such as ever-increasing performance and ever decreasing energy consumption. Scaling down of the semiconductor process is one of the solutions to address these issues. This thesis examines the design issues with using dynamic logic in deep submicron processes.

1.1 Dynamic Logic

Dynamic logic is a circuit style that is well-suited for high-performance microprocessor implementations. It offers a significant performance advantage over static circuits with reduced area while avoiding static power consumption. The construction of a simple N-type dynamic logic gate is shown in Figure 1.1.

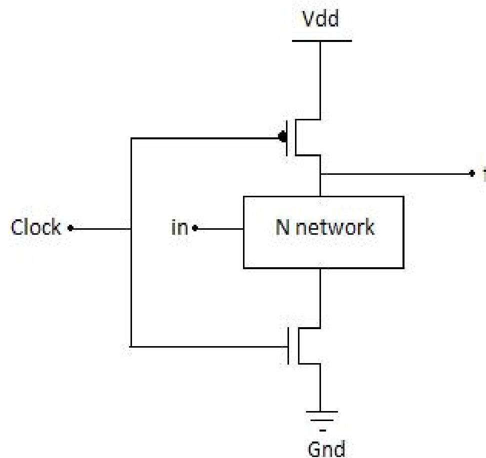

Figure 1.1: Basic dynamic logic circuit

1.2 Background

The inverter is the key component in all digital designs. Understanding the properties and operations of the inverter and extrapolating its results will enable the design of more complex logic gates which are used to construct adders and

microprocessors. The operation of a static CMOS inverter is explained with the help of a simple switch-level model. The schematic of the CMOS inverter is shown in Figure 1.2.

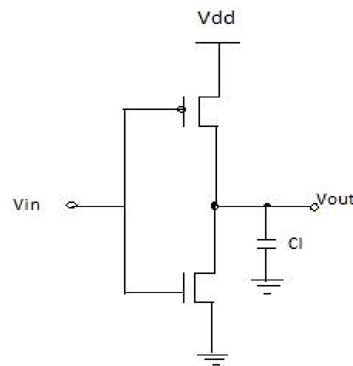

Figure 1.2: Schematic of a CMOS inverter

When Vin is high and equal to Vdd, the NMOSFET is on and PMOSFET is off, providing a direct path between Vout and ground, resulting in a steady-state value of zero volts. Subsequently, when the input voltage is low the NMOSFET turns off and the PMOSFET on. This provides a path between Vdd and Vout resulting in a high output voltage. Complementary CMOS circuits are a class of static circuit where at every point of time each gate output is either connected to Vdd or ground via a low resistance path. A static CMOS logic gate with a fan-in of N requires 2N devices.

In order to reduce the number of transistors required to implement a logic function, a number of approaches such as pseudo-NMOS, pass-transistor logic, etc., were developed. Pseudo-NMOS logic requires only N+ 1 transistor to implement an N-input logic gate, but unfortunately it has static power dissipation.

An alternate approach called dynamic logic was developed. When there is a choice to select dynamic logic over conventional static CMOS logic, the following factors are taken into consideration. In CMOS logic, both N and P logic blocks are necessary which contribute to the input capacitance. This has a direct impact on gate delay since this delay is directly proportional to the output load and inversely proportional to the device size. By contrast, in dynamic logic, a single logic block is needed. Therefore the input capacitance is only due to the NMOS devices (assuming all the logic is implemented in a pull-down logic block)

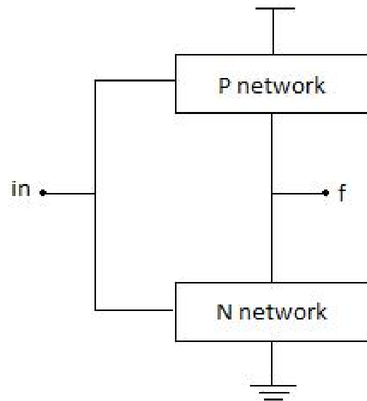

Figure 1.3: CMOS network

The dynamic logic style follows the NMOS logic tree style implementation. The two possible design styles are either using a p-type pull up network or by using an n-type pull down network. The addition of a clock input is necessary to create a sequence of precharge and conditional discharge phases. This eliminates the chance of any static power that might be consumed during the precharge period (static current would flow between the supplies if both the pull-down and the precharge device were turned on simultaneously). In practice, the NMOSFET type logic is preferred because the PMOSFETs are generally wider than NMOSFETs, which can become a major concern when a logic tree with a large depth is utilized.

Hence summarizing the properties of dynamic logic, the logical function in dynamic logic is implemented by the NMOS pull-down network and its construction is very similar to static CMOS but the number of transistors is substantially lower than in the static logic which is 2N versus only N+2 in dynamic logic.

The logic gates in dynamic logic have comparatively faster switching speeds because of two facts. The first reason is that there exists a low load capacitance attributed to the smaller number of transistors per gate and the single-transistor load per fan-in. This results in reduced logical effort. The second reason is that the dynamic logic gate does not have short circuit current during static operation (unlike pseudo-NMOS logic), hence making it a very desirable choice for high-performance circuits. The disadvantages to consider while implementing dynamic logic are the need of a clocking device and issues with charge sharing and charge leakage.

1.3 Scaling

A prediction was made by Gordon E. Moore that technology would advance and transistor sizes would be scaled to half their size every 24 months thereby doubling the number of transistors that can be placed on a microchip [1].

Circuit optimization not only is concerned with performance but also with the physical layout size and reliability of operation, but when it comes to dynamic logic, scaling plays a crucial role because the leakage in the circuit increases exponentially through scaling [2]. Hence, strict design methodologies and circuit guidelines must be followed to scale the device sizes when designing adders using dynamic logic. This includes analyzing their performance based on various metrics and understanding the effect of charge leakage and charge sharing.

1.4 Research Objective

The aim of this study is to evaluate the feasibility of using dynamic logic for deep submicron CMOS technologies. The focus is on the issues of charge leakage and charge sharing.

1.5 Research Method

The method in which the performances of the adder circuits under study are evaluated is discussed in this subsection. First, the schematic of full adder designs of the various dynamic logic styles are obtained from the literature and set as benchmarks. Then each adder is optimized for delay versus area at the 45 nm technology node to determine the transistor sizes. A physical layout is created for each adder design using the Electric software, which allows netlists to be extracted that include the parasitic capacitances. Various tests are then performed to evaluate the performance of the adder circuits at several submicron technology nodes. Performance is also evaluated against different scenarios by including bleeder devices of different sizes.

Susceptibility to noise increases exponentially with scaling which is discussed in the later chapters. The main advantage of the use of bleeder devices in the form of a PMOS pull-up FET is to compensate for the loss of charge in the pull-down leakage path. Bleeder resistances are made high to avoid the problems associated with ratioed logic.

A feedback configuration is implemented with the bleeder devices to eliminate static power dissipation.

1.6 Outline of Thesis

In Chapter 2, various scaling models are developed for submicron technology nodes and a predictive technology model is discussed. Chapter 3 discusses the delay performance of dynamic logic by means of a simple generic dynamic logic circuit. Chapter 4 analyzes the major issues with dynamic logic which are charge sharing and charge leakage. Improvements in noise immunity through the use of a bleeder device are analyzed with the aid of a simple noise generator circuit.

Chapter Two

CMOS Scaling Models

This chapter discusses interconnect scaling models and how the CMOS devices are characterized based on a predictive technology model. All the interconnect parameters used in simulating the dynamic gates in a deep submicron process, such as metal height, pitch, and thickness are explained.

2.1 Predictive Technology Model *(PTM)*

The two issues with scaling to submicron dimensions are power dissipation and process variation. This requires the development of new device and interconnect models which will perform accurately even when scaled down to very small geometries, allowing the adoption of dynamic logic techniques to be implemented in future technologies. Thus, this led to the development of a Predictive Technology Model (PTM) which enables us to accurately characterize a CMOS device when it is simulated with SPICE [7]. Scaling to submicron dimensions requires the development of a Predictive Technology model (PTM). To understand this better, the concept of a technology node is explained first. From the definition provided by the *International Roadmap for Semiconductors,* in a DRAM implementation, the minimum half-pitch between two metal lines defines the technology node**.** This is depicted in Figure 2.1 [9].

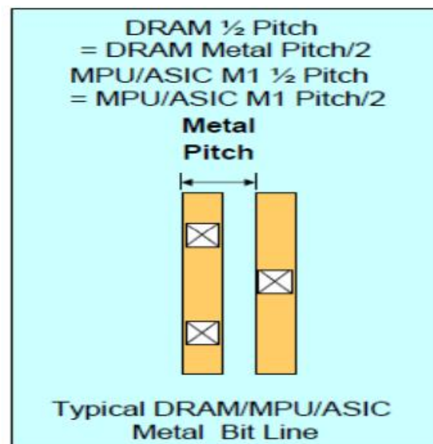

Figure 2.1: DRAM half pitch [3].

Once the reference technology node is selected, other new technology node values can be calculated by multiplying the value of the previous technology node by 0.7 as shown in Figure 2.2 [12]. A technology node will be scaled by approximately 0.5 after two subsequent technologies [13].

$$\text{New Technology Node} = \text{Technology Node (Reference)} \times 0.7$$

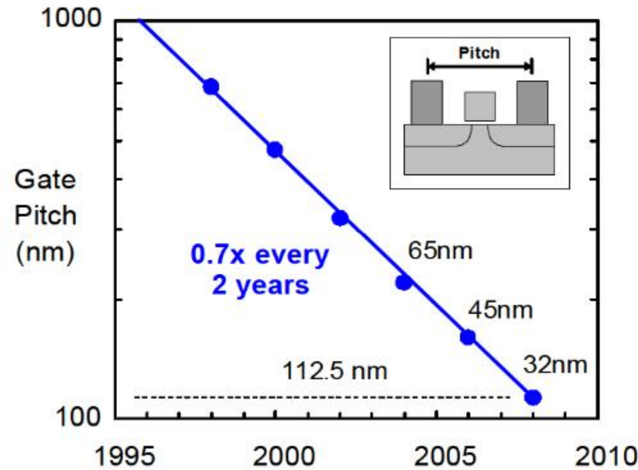

Figure 2.2: Evolution of gate pitch over the years [7].

There are challenges of scaling to submicron dimensions in a PTM. The effective length (L_{eff}), threshold voltage (V_{tho}) and oxide thickness (T_{ox}) can be scaled to submicron dimensions, but the behavior of MOSFET cannot be accurately predicted. The physical parameters have to be considered while developing an effective predictive model. To overcome this disadvantage a newer PTM model was developed [4], having improved smoothness and more accurate predictions. The figures in Appendix A help illustrate the PTM utilized in this thesis by simulating the IV curves of different technology nodes for both pMOSFETs and nMOSFETs.

Higher frequencies have been achieved by a microprocessor with each technology node. Intel has just released its "tri-gate transistors" on its 22 nm technology in the year 2011. There are two components which decide the speed of an IC. First is the transistor gate delay, which is switching the individual transistor and the other is wire delay or interconnect delay discussed in section 2.2.

2.2 Interconnect Delay

As technologies scale to the submicron regime, the delay due to interconnect becomes a larger fraction of overall gate delay. The performance of an on-chip interconnect depends on factors such as low dielectric materials and low wire resistance and capacitance.

Based on the extent of connection involved, there are three types of interconnects: local interconnects which are used for short connections between devices within the same cell, semi-global interconnects which are used to connect the devices in the same blocks, and global interconnects which are used to connect long connections between different blocks and power connections. Figure 2.3 illustrates the three types of interconnects [5].

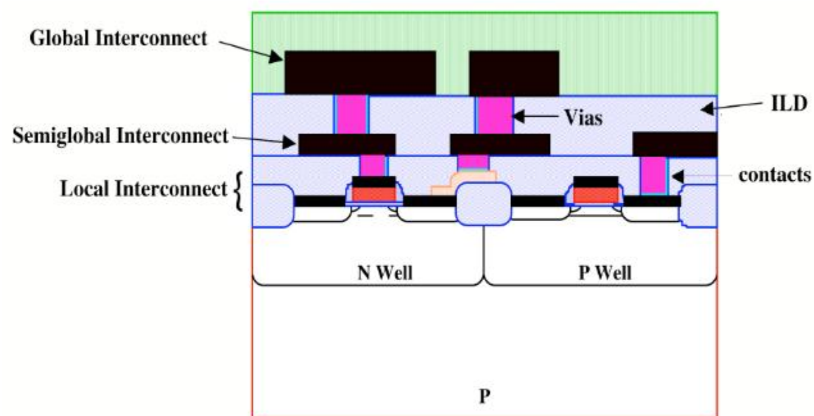

Figure 2.3: Local and Semi-global interconnects [5].

The short connections between the devices and the neighboring cells also known as the first level connections or the local interconnect are the subject of interest in this study. Several tradeoffs are made as interconnect scales with every technology generation. To reduce the line resistance, the metal thickness scales at a slower rate than the width.

These parameters will have an effect on propagation delay, power distribution, energy dissipation, and extra noise. The simulations will give an accurate result of the circuit performance, if all the above parameters, also called parasitic effects are considered.

Capacitance is one of the parameters to be considered when scaling the interconnects. This parameter is a function of the shape of a wire characterized by width (W), length (L), thickness (T), distance from surrounding wire (S), height (T), and spacing (with respect to neighboring wires).The parasitic values are calculated from the following equations. The literature [6] shows their derivations and how to obtain them.

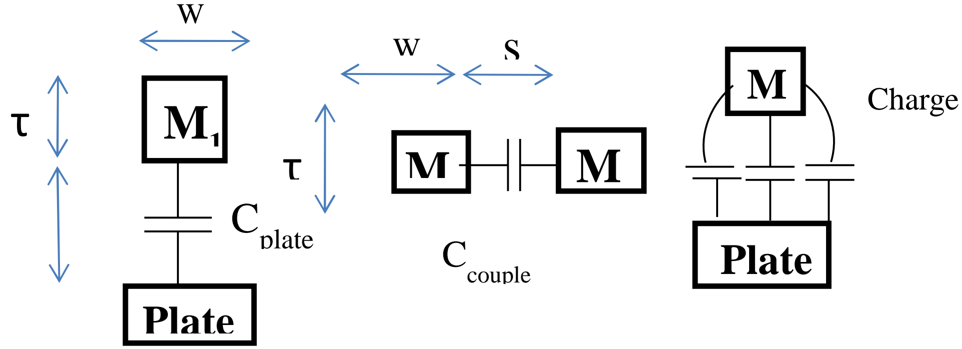

Figure 2.4: Types of capacitances associated with a metal line.

The parasitic capacitances mentioned in Figure 2.6 are calculated and are included in the following chapters. The parasitic values can be calculated from the formulae obtained from [17] as shown in the equations 2.1-2.5.

Plate Capacitance: $C_{plate}/\mu m^2 = \varepsilon/H$ (2.1)

Fringe Capacitance: $C_{fringe}/\mu m = \frac{2}{\pi}\varepsilon \ln\left[1 + \frac{T}{H}\right]$ (2.2)

Couple Capacitance: $C_{couple}/\mu m = \left\{\frac{T}{S} + \frac{2}{\pi}\ln 1 + \frac{2w}{s}\right] + \frac{3}{\pi} + \frac{1}{\pi}\ln\left[1 + \frac{T}{2(1+\pi)(s/2+w)}\right]\right\} \times \varepsilon$

(2.3)

Total Capacitance: $C_{total} = 2 \times C_{fringe}/\mu m + 2 \times Ccouple/\mu m$ (2.4)

Since the metal2 layer is used sparingly in the layout, its coupling capacitance is not calculated. The other parameter considered for interconnect scaling is the inter-layer dielectric.

Capacitance $C = {}^{\varepsilon}/_{t_{ox}}$ (2.5)

where t_{ox} is the thickness of the oxide layer and ε is the dielectric permittivity.

As illustrated by equation 2.6, a lower capacitance value will be obtained from a lower dielectric value, which depends on the material used. SiO_2 with a dielectric

constant of 3.9 is commonly used, but with scaling down of t_{ox}, some other materials with lower dielectric constants are preferred. Reducing the dielectric will improve interconnect delay, and decrease the dynamic power consumption. Using a good dielectric material will usually cause a reduction in the value of the parasitic capacitance by a factor which depends on how it compares with that of SiO_2 [8]. Some of these required properties are good adhesion force between dielectric layer and metal, good stability under high temperature processing, and the ability to fill in the gap or narrow space between metal lines. Figure 2.5 shows that by reducing the dielectric constant the interconnect delay is lowered.

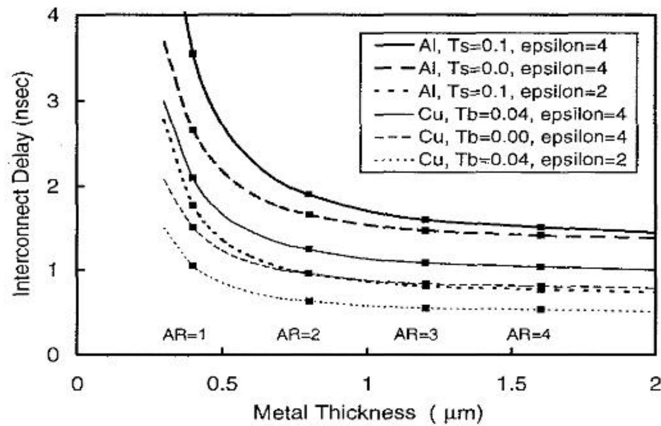

Figure 2.5: Interconnect RC delay vs thickness of metal for 0.8 µm pitch and 10 mm length. [9]

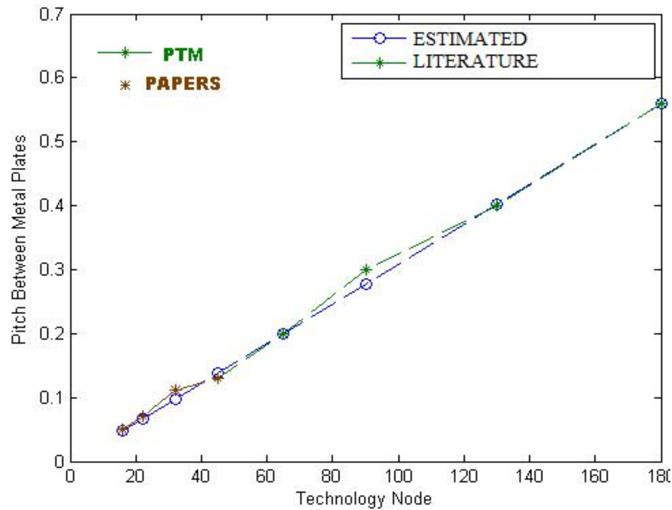

Figure 2.6: Trends of metal pitch from both literature and estimated data versus technology node. [18][19][20-21]

Table 2.1: Data values of metal pitch based on technology node.

Tech Node (nm)	180	130	90	65	45	32	22	16
Literature data (nm)	560	400	300	200	130	112.5	70	50
Estimated data (nm)	560	403	277.9	200	137.9	97.7	66.9	48.5

Another parameter considered while scaling is metal pitch. The figure above shows trends of metal pitch with respect to technology node. Calculation of estimated data is performed by using a reference node value which is scaled according to the *1/S* scaling method, where *S* is the scaling factor. For example, S=2 means that the new node has half the dimension of the reference node [8-12].

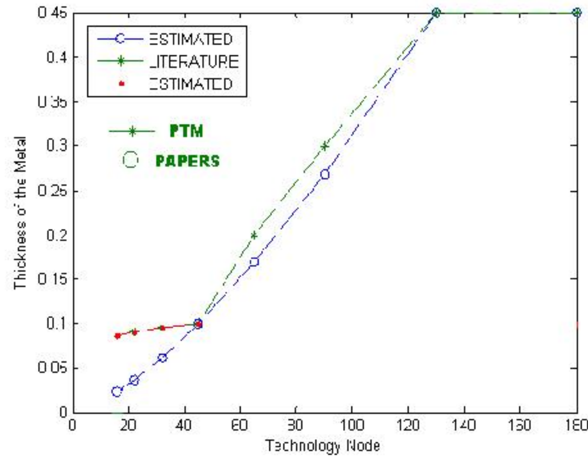

Figure 2.7: Trends of metal thickness from, literature and estimated data versus technology node.

Table 2.2: Literature and estimated values of metal thickness based on technology node [7].

Tech Node (nm)	180	130	90	65	45	32	22	16
Literature data (nm)	450	450	300	200	100	95	90	-
Estimated data (nm)	450	450	267.2	168.4	100	61.7	36.3	23.1
Estimated data (nm)	-	-	-	-	100	95	89.8	85.6

The parasitic capacitances are calculated for each node from the dimensions taken from Table 2.3 and by using equations (2.1-2.5).

Table 2.3: Data values used for finding parasitic capacitances.

Technology Node (nm)	**90**	**65**	**45**	**32**	**22**	**16**
Bulk K	2.8	2.2	2.5	2.3 -2.7	2.1 – 2.5	1.9 – 2.3
Metal Pitch (nm)	300	200	200	112.5*	70*	50
Metal Width (nm)	150	100	50	49	33.5	24.2
Metal Thickness (nm)	300	200	100	95*	90	85.6
Metals Spacing (nm)	150	100	50	49	33.5	24.2
Metals Height (nm)	300	200	100	88	57	39.5

Table 2.4 shows the tabulated values of parasitic capacitances of each technology node for metal and polysilicon. Similarly, Table 2.5 shows the summarized values of parasitics used in this research.

Table 2.4: Parasitic capacitance and thickness of polysilicon based on the technology nodes.

	Technology Node (nm)	**90**	**65**	**45**	**32**	**22**	**16**
Metal_1	**Plate Capacitance**	82.6	97.3	221.3	251.5	357.27	470.73
	Fringing Capacitance	10.9	8.59	9.76	10.3	12.28	13.64
	Coupling Capacitance	93.8	73.7	83.7	82.3	91.76	100.31
Metal_2	**Plate Capacitance**	55.0	64.9	147.5	167.6	238.18	313.82
	Fringing Capacitance	8.06	6.33	7.19	7.63	9.32	10.58
Polysilicon	**Thickness (nm)**	180	130	90	62.0	59.10	56.59
	Plate Capacitance	165.2	194.7	442.7	503.0	714.55	941.46
	Fringing Capacitance	12.4	10.3	14.5	12.3	14.55	16.00
	Coupling Capacitance	61.9	48.6	55.3	54.5	58.45	61.88

Table 2.5 Parasitic capacitance values according to the technology nodes used in this research.

	Technology Node (nm)	**90**	**65**	**45**	**32**	**22**	**16**
Metal_1	**Plate Capacitance**	82.6	97.3	221.3	251.5	357.2	470.7
	Total Fringe Capacitance	209.5	164.6	187.0	185.3	208.0	227.9
Metal_2	**Plate Capacitance**	55.0	64.9	147.5	167.6	238.1	313.8
	Total Fringe Capacitance	16.12	12.6	14.3	15.2	18.6	21.1
Polysilicon	**Plate Capacitance**	165.2	194.7	442.7	503.0	714.5	941.4
	Total Fringe Capacitance	148.7	117.9	139.6	133.9	146.9	155.7

Note: Plate Capacitance $(aF/\mu m^2)$ Fringing Capacitance $(aF/\mu m)$

Coupling Capacitance $(aF/\mu m)$ Total Fringe Capacitance $(aF/\mu m)$

2.3 MOSFET Model

A summary of the MOSFET saturation drain-to-source current obtained from the PTM model for different technology nodes is given in the table below.

Table 2.6: Values of current flowing through PMOS NMOS based on technology node.

		Technology Node (nm)	90	65	45	32	22	16
		Vdd (Volts)	1.3	1.2	1.1	1.0	0.95	0.9
I-V Curves	PMOS	Width (nm)	180	130	90	64	44	32
		I_{ds}(μA)	-100.08	-76.59	-25.07	-18.07	-10.58	-8.48
	NMOS	Width (nm)	180	130	90	64	44	32
		I_{ds}(μA)	84.99	163.65	43.04	30.53	18.49	14.55

The transistors W/L ratio is 2:1. Due to relatively high values at the 65 nm node, the current values are non-monotonic. The reason for this is that the 90 nm, 65 nm, and the 45 to 16 nm models originated from different versions of the PTM model.

2.4 Conclusion

To summarize, this chapter has discussed the various parameters and dimensions of interconnect that are very important and should be considered when designing a new model for scaling to submicron dimensions. The parasitic capacitances for metal and polysilicon are also determined as a part of this chapter. The summarized parasitic capacitances are used in next chapter for finding the delay and optimized size of transistors used in the full adder circuits implemented with different logic styles.

Chapter Three
Dynamic Logic

This chapter discusses the design and simulations of various dynamic logic circuits in advanced submicron processes.

3.1 Dynamic Logic Gate design

The information from the previous chapter is used to determine parasitics for different technology nodes and sizes. As discussed, to reduce the number of transistors required to generate a given logic in a static CMOS logic, which requires 2N devices, various other logic families were developed, such as pseudo-NMOS and pass transistor logic. The problem with the other logic families is power dissipation. To overcome this, dynamic logic was developed. Dynamic logic circuits require a clock to generate a sequence of precharge and evaluation cycles. The construction of a dynamic circuit is shown in Figure 3.1 below.

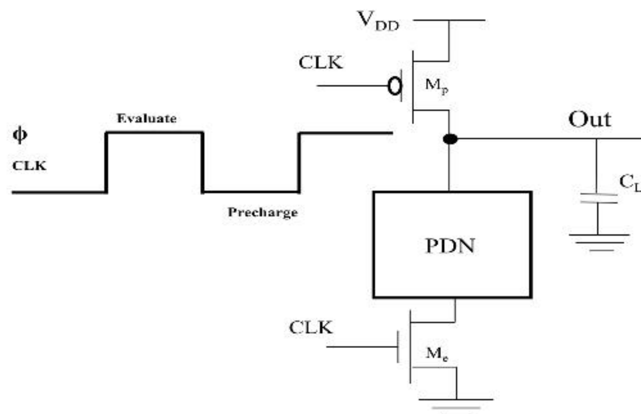

Figure 3.1: Dynamic logic circuit

There are two main phases in the operation of a dynamic gate: precharge and evaluation, as determined by the clock signal CLK. During the precharge, CLK = 0, and the output node Out is precharged to V_{dd} by PMOS M_p. The pull-down network (PDN) is disabled during this time due to footer device M_e. The FET ensures there is minimal

static power during this period. During the evaluation phase, the PDN conditionally discharges the output node depending on the input values and PDN topology. When the PDN is turned off, the precharged values are stored on the output capacitance C_L (i.e., a combination of junction, wiring and input capacitance). Thus when the output is discharged it can be charged again only in the next precharge cycle. The schematic of a 6 input dynamic CMOS gate is shown in Figure 3.2.

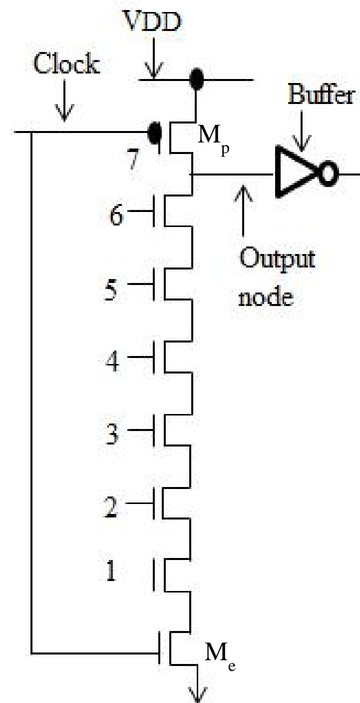

Figure 3.2: Schematic of a 6 input CMOS gate.

Electric software was used to create the layout which is shown in the Figure 3.3.

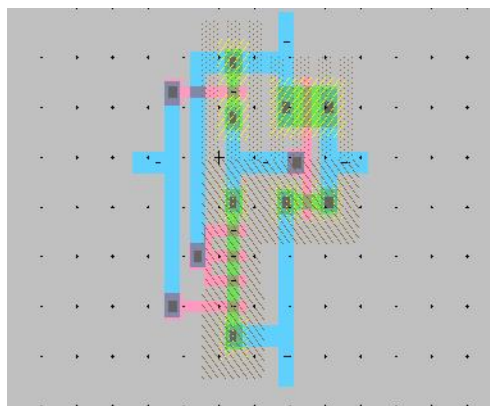

Figure 3.3: Layout of Figure 3.2

The schematics and physical layouts of all the adder logic styles used in this chapter are constructed after studying the literature. The Electric design tool is used to prepare these layouts. This is a tool used to extract the parasitics. A netlist is formed with all the parasitic capacitance linked to the interconnect, after the parasitic capacitance of different technology nodes, used in the previous chapter are included.

All the simulations were performed using the SPICE netlist extracted from the layout which includes the parasitic capacitances associated with the FETs and interconnect. Lines of codes for SPICE for supply voltage connection, type of analysis and constants used were added to the netlist. While manually adding the connections to the netlist, extra care was taken to ensure no changes were made to the circuit topology.

The input voltage lines of the SPICE netlist are known as input stimulus waveforms. The input stimulus waveforms are a sequence of three bits from (0,0,0) to (1,1,1) used to test the functionality and delay of the adders. The input stimulus is used to verify the functionality of the adder circuits obtained from the netlist, and also to estimate delays from input to output. The delays obtained are used to calculate the transistor sizes. The values for different delays in the simulations are tabulated in the Appendix. The least delay corresponding to minimum area of logic circuit are used to calculate the final sizes of transistors. The values are tabulated in Table 3.1 below.

Table 3.1: Device sizes in   dimensions in generic dynamic logic circuit.

Device	Size	Device	Size
MP1	5/2	MN_4	6/2
MPMOS@1	3/2	MN_5	6/2
MN_1	6/2	MN_6	6/2
MN_2	6/2	MN_7	6/2
MN_3	6/2	MNMOS@1	3/2

3.2 Delay analysis of the pull-down path

Since most of the delay of dynamic gate is incurred by the discharge of the dynamic node through the pull-down path, this delay is analyzed in detail in this section. The delay values for the dynamic logic circuit are obtained for two different scenarios, i.e. with 4 NMOS pull-down devices and 7 NMOS pull-down devices, respectively, and the values are compared to justify the device size finalized in the previous section. The results from these simulations are tabulated in Appendix C. The goal of this analysis was

to obtain an estimate for the on-resistance of the FET and the capacitance values in the dynamic network under study.

The drain-to-bulk capacitance C_{db} was calculated using the formula,

$$C_{db} = AD \cdot CJ \left[1 + \frac{V_{db}}{PB}\right]^{-MJ} + (PD - W) \cdot CJDW \left[1 + \frac{V_{db}}{PBSW}\right]^{-MJDW} +$$

$$W \cdot CJSWG \left[1 + \frac{V_{db}}{PBDWG}\right]^{-MJDWG} \quad (3.1)$$

The values from the corresponding BSIM files are substituted in to the above equation to get the value of the drain-to-bulk capacitance. Similarly the values of various capacitances are calculated in the process of determining the junction capacitance using the following equations.

C_{out} : derived from spice netlist

$C_{gb} = W_{eff} \times L_{eff} \times C_{ox}$ (3.2)

$C_{ox} = {}_{ox} / t_{ox} = {}_{SiO2} \times {}_{o} / t_{ox}$ (3.3)

t_{ox} : derived from SPICE netlist

${}_{SiO2}$: 3.9

${}_{o}$: 8.85×10^{-12} F/m

$C_1 = 2W \times CJSWG + 2Z \times CJSW + W \times Z \times CJ$ (3.4)

The values from the above equations are tabulated in Table 3.2 below.

Table 3.2: Tabulation of values used in C_{ox} calculations

Tech node (nm)	C_{ox} (fF/μm^2)	C_{out} (fF)	C_{gb} (fF)	C_1(fF)
16	28.75	0.166	0.028	0.052
22	31.3	0.21	0.027	0.073
32	21.5	0.276	0.015	0.107
45	19.17	0.398	0.013	0.15

The load capacitance is calculated using the formula,

$C_L = (C_{db})_{NMOS} + (C_{db})_{PMOS} + C_{out} + 2\, C_{OX}$ (3.5)

and the values are tabulated in Table 3.3.

Table 3.3: Tabulation of load capacitance

Tech node (nm)	C_L (fF)	$(C_{ds})_{NMOS}$ (fF)	$(C_{ds})_{PMOS}$ (fF)
16	0.364	0.078	0.080
22	0.480	0.1079	0.109
32	0.606	0.1558	0.144
45	0.763	0.96	0.243

In order to estimate the resistance values, the value of V_{ds} and I_{ds} are determined at $V_{DD}/2$ from the I-V plots for the corresponding technology node. Shown below in Figure 3.4 is the I-V plot for the 16 nm technology node plotted using LTSpice. The I-V plots used for the remaining technology nodes in this section are in Appendix B.

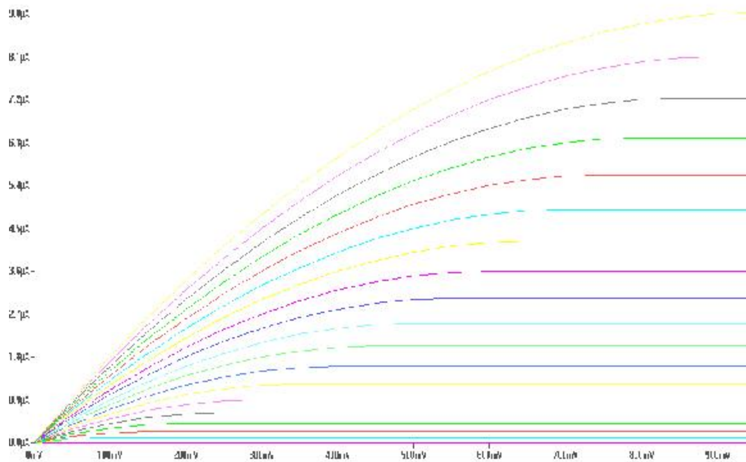

Figure 3.4: I-V plot for 16 nm technology.

V_{DS1} was calculated as,

$$V_{DS1} = V_{DD} / 2 \tag{3.6}$$

where V_{DD} is the supply voltage.

The value of the on-resistance is estimated by substituting the values into the equation $R=V_{ds}/I_{ds}$. The resistance values for different technology nodes are shown in Table 3.4.

Table 3.4: Tabulation of resistance R calculations.

Tech node (nm)	V_{DD} (V)	V_{DS1} (V)	I_{DS1} (μA)	R (K)
16	0.9	0.45	6.070	90
22	0.95	0.475	6.71	70.07
32	1	0.5	7.5	66.5
45	1.1	0.55	9.09	60

The Elmore [24] delay is calculated from the equivalent circuit of the schematic of a dynamic logic circuit with 7 NMOS pull-down devices as shown below,

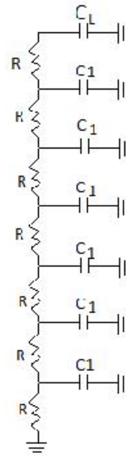

Figure 3.5: Equivalent RC network

$= (RC_1 + 2RC_1 + 3RC_1 + 4RC_1 + 5RC_1 + 6RC_1 + 7RC_L) \times K$

$$= K \times (21\ RC_1 + 7\ RC_L) \quad (3.7)$$

where K is a semi-emperical fitting parameter.

The values of resistance and capacitance calculated above are substituted and the value of   derived from the simulation is substituted to obtain the value of K. The values are tabulated in Table 3.5.

Table 3.5: Table of K values for 7 NMOS- pull down

Tech nodes (nm)	K values
16	0.38
22	0.40
32	0.42
45	0.48

Similar calculations were performed for a dynamic logic circuit with 4 NMOS devices and the values are shown in Table 3.6.

Table 3.6: Table of K values for 4NMOS- pull down

Tech nodes (nm)	K values
16	0.40
22	0.44
32	0.31
45	0.34

Table 3.7: Step response of lumped and distributed RC networks

Voltage range	Lumped RC Network	Distributed RC Network
0 to 50 % (tp)	0.69 RC	0.38 RC
0 to 63% (tp)	RC	0.5 RC
10 to 90 % (tp)	2.2 RC	0.9 RC
0 to 90 %(tp)	2.3 RC	1.0 RC

The literature [13] states that the delay of a distributed network is approximately 0.38RC, where R is the total capacitance of the network and C is the total capacitance of the network. The K values derived from the calculations prove the fact that they are consistent with the estimations in the literature, down to the K value for the 16 nm technology simulations for the 7 NMOS pull-down circuit.

3.3 Delay of Adders

This section deals with the study of two single bit full adder cells implemented with the dynamic logic style. One of them is hybrid CMOS logic and the other is NPCMOS logic. Both structures are optimized and validated separately. The dynamic mode causes the speed of cells to be much higher than the conventional static full adders in all voltages under study.

The hybrid CMOS circuit design is essentially a differential implementation of the traditional dynamic domino full adder. Since it exhibits low delay, it is usually used in high performance circuits. Its topology in Figure 3.6 is based on an NMOS pull down network and a PMOS precharge, driven by the clock, that brings the gate into precharge or evaluation mode. The output inverters ensure that no race condition occurs, while the weak feedback PMOS transistors help in reducing the charge redistribution problem, thereby increasing the noise immunity

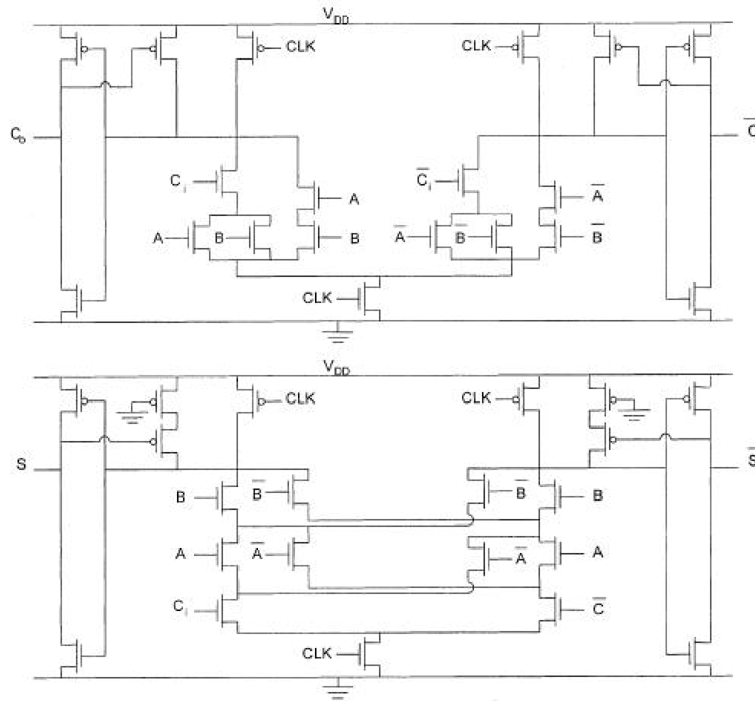

Figure 3.6: Schematic of a hybrid domino logic circuit, i.e. Sum and Carry blocks [23]

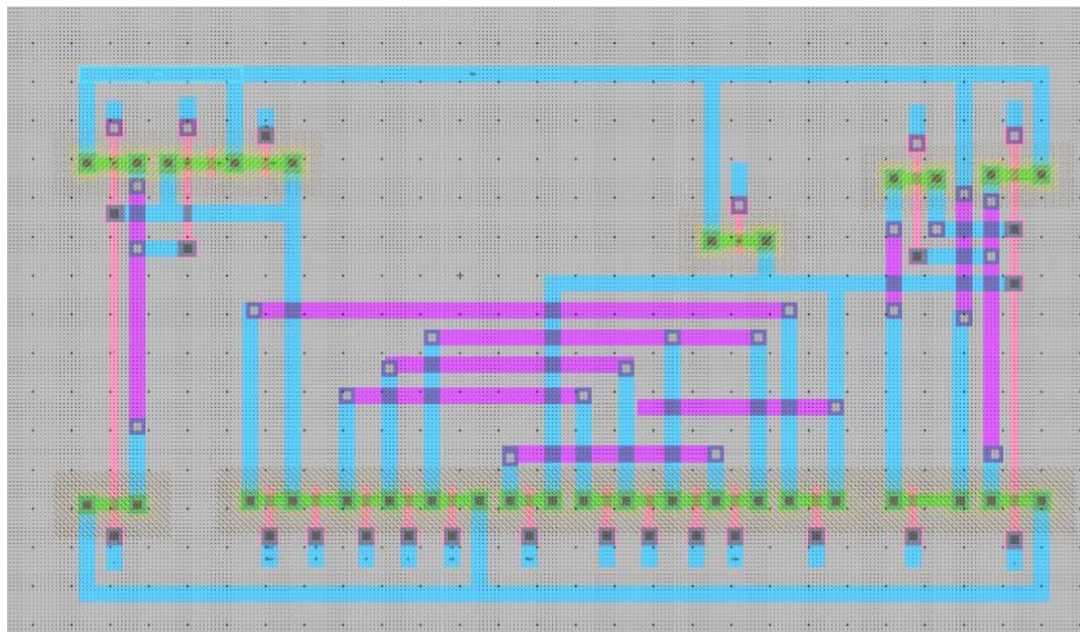

Figure 3.7: Electric layout of Sum block

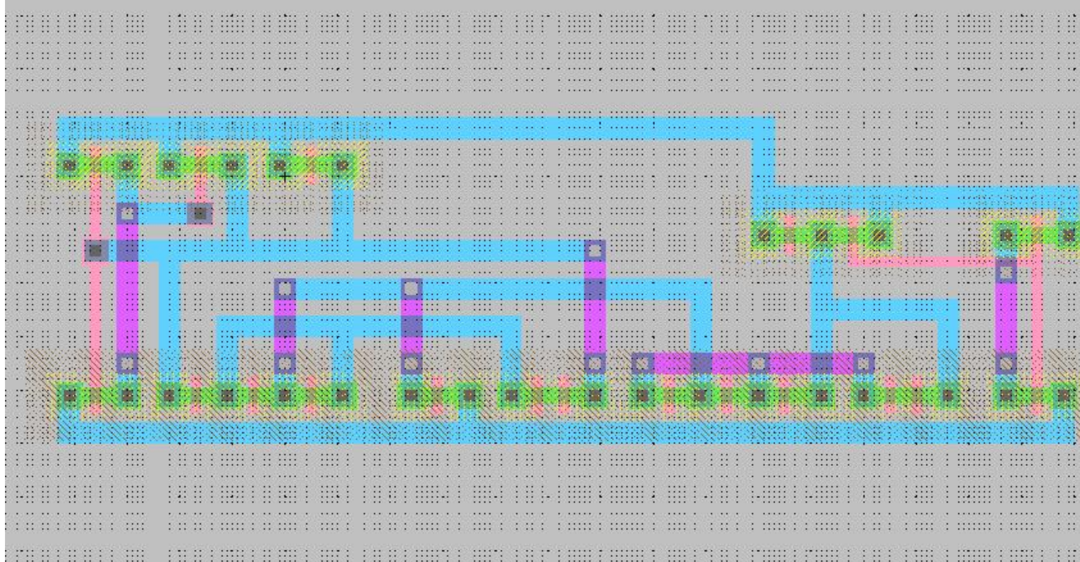

Figure 3.8: Electric layout of Carry block

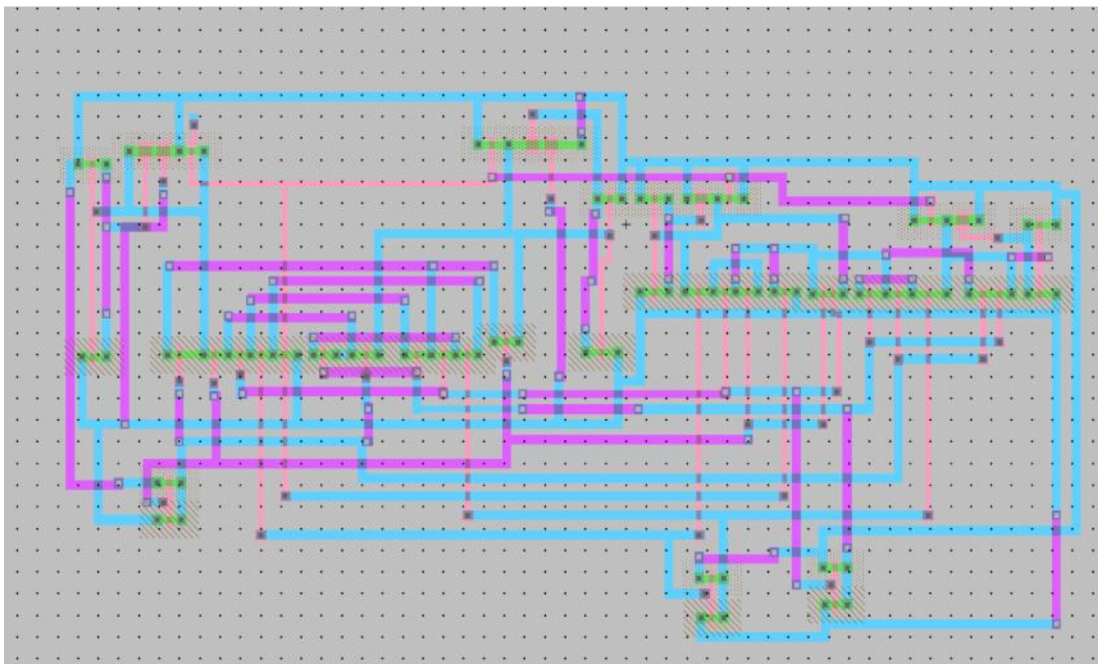

Figure 3.9: Electric layout of hybrid domino full adder

Another approach which uses dynamic logic is the NP-CMPS logic style, where at the first stage the $\overline{C_{out}}$ function is obtained using the bridge style [17]. At the second stage the $\overline{Sum}$ function is gained according to the equation $Sum = C_{out} \times (A + B + C_{in}) + A \times B \times C_{in}$. This design has full swing voltage levels. Clock and clock' signals

ensures that both stages enter the evaluation phase simultaneously. The schematic is depicted in Figure 3.10.

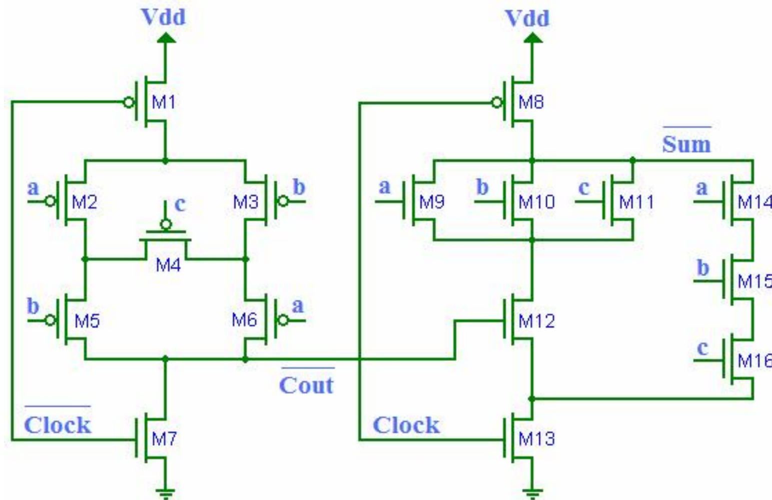

Figure 3.10: Schematic of NPCMPS

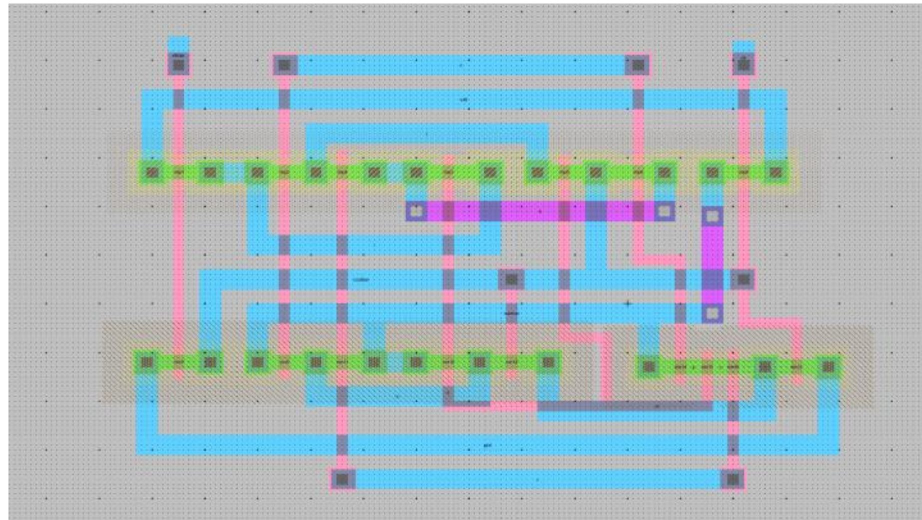

Figure 3.11: Electric layout of NPCMPS circuit.

3. 4 Adder (Full bit adder)

3.4.1 DCVSL

Dynamic CVSL is basically a dynamic gate and its complimentary gate together which makes it possible to merge the two complimentary trees to have one common pull-down path. The schematic of full adder, shown in Figure 3.6 is obtained from the

literature [18] and set as a benchmark. The adder circuit is optimized for delay versus area at the 45 nm technology node to determine the transistor sizes. Several simulations were run for worst case delay while changing the device sizes. The values obtained from the simulations are tabulated in Table 3.8. Based on the delay versus device size analysis, the device sizes are finalized. The simulations for worst case delay against the two possible paths are tabulated.

The layouts for all the technology nodes under study, (i.e. 16 nm, 22nm, 32nm, 45nm and 65nm) are optimized by changing the device sizes to the final values. The final device sizes of the PMOS devices and the NMOS devices are shown in Table 3.9 and Table 3.10. All the devices are sized based on lambda ( ) design rules, which allow ease of scaling to different technology nodes which is the approximation of deep submicron process. Based on the worst case delays, the sizes X=6 ; y= 12 are utilized. The device sizes are changed in the layout and thereby changing the parasitic to get the layout for specific technology nodes

A physical layout of the adder design is created using the Electric Software, which allows corresponding netlists to be extracted that include the parasitic capacitances. Various tests were then performed to evaluate the performance of circuits in the corresponding technology nodes. Performance is also evaluated for different scenarios by including bleeder devices of different sizes. The delay values from the optimized layouts of different technology nodes are tabulated in Table 3.10.

Table 3.8: Table of sizes of PMOS devices in dimension.

Device	Size	Device	Size
M_{p1}	3/2	M_{p8}	3/2
M_{p2}	4/6	M_{p9}	12/2
M_{p3}	4/6	M_{p10}	4/6
M_{p4}	3/2	M_{p11}	3/2
M_{p5}	4/6	M_{p12}	3/2
M_{p6}	4/6	M_{p13}	4/6
M_{p7}	3/2	M_{p14}	12/2

Table 3.9: Table of sizes of NMOS devices in dimension.

Device	Size	Device	Size
M_{n1}	3/2	M_{n14}	3/2
M_{n2}	3/2	M_{n15}	12/2
M_{n3}	3/2	M_{n16}	12/2
M_{n4}	3/2	M_{n17}	12/2
M_{n5}	3/2	M_{n18}	12/2
M_{n6}	3/2	M_{n19}	6/2
M_{n7}	3/2	M_{n20}	6/2
M_{n8}	3/2	M_{n21}	12/2
M_{n9}	3/2	M_{n22}	12/2
M_{n10}	3/2	M_{n23}	12/2
M_{n11}	3/2	M_{n24}	3/2
M_{n12}	3/2	M_{n25}	3/2
M_{n13}	3/2	M_{n26}	3/2

Table 3.10: Final delay values of DCVSL.

Tech Node(nm)	16	22	32	45	65
Delays(ns)	0.1213	0.1361	0.0988	0.06876	0.027

3.4.2 NP-CMPS

The schematic of full adder, Figure 3.10 design is obtained from the literature [19]. Based on the worst case delay, the device size 9 λ is chosen to be optimal. Hence the layout is optimized, i.e., the device sizes are changed accordingly. The final device sizes in the layout are tabulated in Table 3.11. The netlists are extracted with corresponding parasitics included and delay values are calculated for each technology node under study, which are in Table 3.12. The same steps are repeated as in the hybrid CVSL and the delays for determining sizes are obtained accordingly.

Table 3.11: Device sizes for NPCMPS in dimensions.

Device	Size	Device	Size
M_{p1}	9/2	M_{n9}	3/2
M_{p2}	9/2	M_{n10}	3/2
M_{p3}	9/2	M_{n11}	3/2
M_{p4}	9/2	M_{n12}	3/2
M_{p5}	9/2	M_{n13}	3/2
M_{p6}	9/2	M_{n14}	3/2
M_{p7}	3/2	M_{n15}	3/2
M_{p8}	9/2	M_{n16}	3/2

Table 3.12: Final delay values for NPCMPS.

Tech nodes (nm)	16	22	32	45	65
Delays (ns)	0.2161	0.2317	0.1164	0.777	0.065

The delay versus technology nodes for the DCVSL and NPCMPS gates are plotted in Figures 3.12 and 3.13, respectively. For both gates, the delay increases with decreasing technology nodes. This is to be expected because the same width-to-length ratios were used in the pull-down paths for all the dynamic gates that were characterized. A similar effect was seen in the characterization of static CMOS gates versus technology node [17].

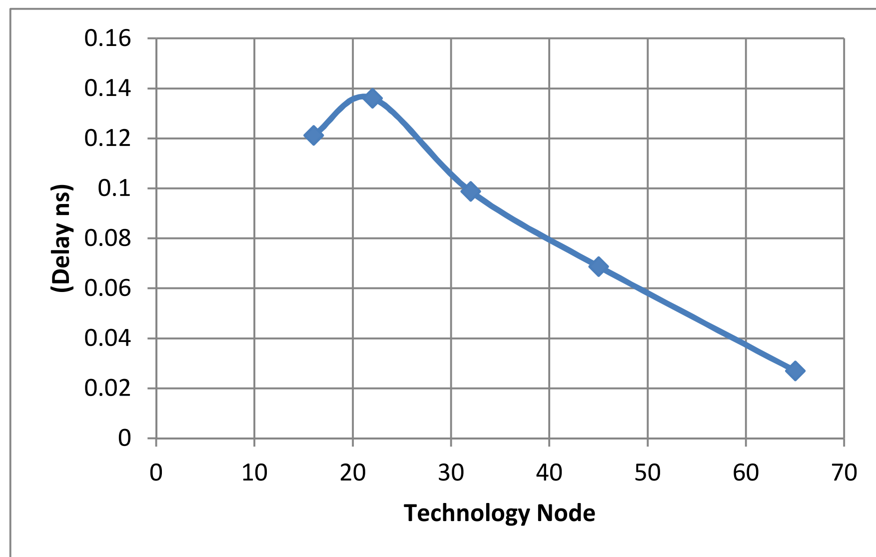

Figure 3.12: Delay versus technology node plot for DCVSL

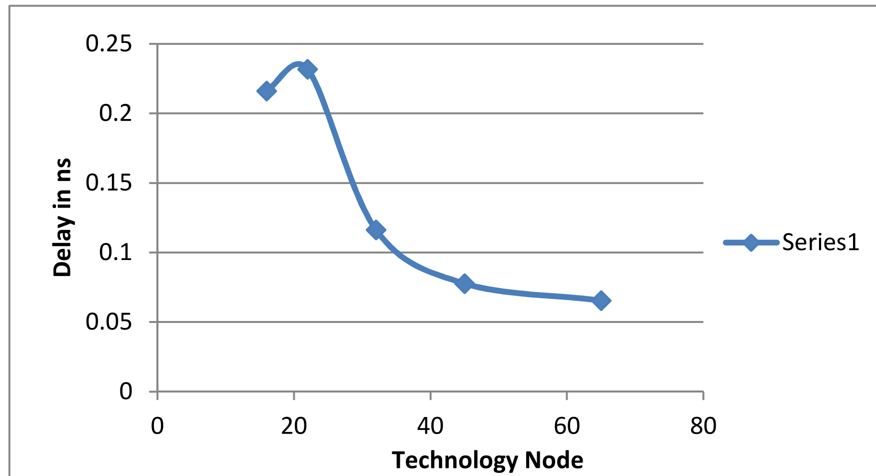

Figure 3.13: Delay versus technology node plot for NPCMPS.

3.5 Summary

The delay characterization of dynamic gates in deep submicron technologies was studied in this chapter. The use of the Elmore delay to estimate the time constant of the pull-down path in a dynamic gate has been validated. The design and layout of the dynamic gates have been described. Extracted SPICE netlists from the physical layout provided the parasitic capacitance information. The interconnect model and FET predictive technology models discussed in the previous chapter were utilized to obtain accurate simulations of the delay characteristics for the dynamic gates.

Chapter Four

Major issues in Dynamic Logic Implementation

Dynamic logic results in high performance solutions but some problems which have to be taken into account are charge sharing and charge leakage. These two issues are discussed and ways to avoid or minimize the effects of charge leakage and charge sharing with the aid of several simulations are discussed in the following sections.

4.1 Charge leakage

Leakage in a dynamic circuit is a concern when the pull-down path is in a high-impedance state and the charge storage node needs to maintain a high state. The operation of a dynamic gate is basically dependent on the dynamic storage of the output value on a capacitor. If the pull-down network is off, ideally, the output should remain at precharged state of V_{dd}. However this charge gradually leaks away due to leakage currents causing the gate to not function properly. Figure 4.1 shows the sources of leakage inside a MOS transistor.

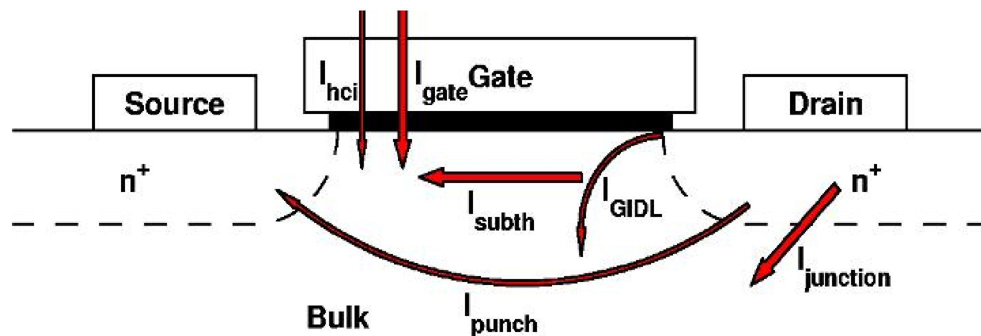

Figure 4.1: Sources of leakage in a transistor. [23]

As the scaling of devices enters the deep submicron ranges, the resistance values change in such a way that drastically influence the transistor's functional behavior. The more significant leakage mechanisms in MOS transistors are discussed below.

Table 4.1: Prediction of the I_{sub}, $I_{pn\text{-}jun}$ and I_{gate} obtained from literature [23].

Generation	Year	I_{sub}	$I_{pn\text{-}jun}$	I_{gate}
90 nm	2004	840 pA	25 nA	13 nA
50 nm	2010	21 pA	3.0 nA	52 nA
25 nm	2016	260 pA	120 nA	510 nA

The kind of leakage which has the most impact on the overall static power consumption of a MOS transistor is called the subthreshold current [23]. In practical scenarios, even when the gate voltage is considerably below the threshold voltage, the current passing through the channel is not literally zero because a transistor is not a simple switch but should be viewed as a complex analog component. Hence, a potential difference between the source and drain will result in a subthreshold current through the channel. In the case of deep submicron device sizes, this effect is substantially amplified because the scaling of a device to such sizes reduces the length of the device drastically. Drain induced barrier lowering (DIBL) due to greater interaction of the drain potential with the channel, results in a lowering of the threshold voltage. This results in increased drain-to-source current as well.

Based on the predictions derived from [23], gate leakage current is almost negligible today, as the subthreshold has become exponentially high. It needs to be noted that as the subthreshold current will rise by a factor of 25 from 90 nm to 50 nm technology, gate leakage will rise by a factor of 4000 at 90 nm. According to [19], gate leakage alone will contribute to 15% of the total power consumption. The above predictions are validated by further calculating the values for 45 nm and 22 nm. The calculations are as below:

$$t_{sub} = \frac{C_l \Delta V}{I_{leak1}} \tag{4.1}$$

$$\text{Where, } \Delta V = \frac{V_{DD}}{2} \tag{4.2}$$

$$I_{leak1} = 2I_{sub} \tag{4.3}$$

$$t_{pn-jn} = \frac{C_l \Delta V}{I_{leak2}} \tag{4.4}$$

$$\text{Where } I_{leak2} = I_{pn\text{-}jn} \tag{4.5}$$

$$t_{gate} = \frac{C_l \Delta V}{I_{leak3}} \tag{4.6}$$

$$I_{leak3} = 2I_{gate} \tag{4.7}$$

$$t_{total} = \frac{C_l \Delta V}{I_{leak4}} \tag{4.8}$$

$$I_{leak4} = I_{leak1} + I_{leak2} + I_{leak3} \tag{4.9}$$

The results from the calculations are summarized in Table 4.2.

Table 4.2: Delta_t calculation results.

45 nm technology		**22 nm technology**	
Delta_tsub	9.99ns	Delta_tsub	0.43ns
Delta_tpn-jn	34ns	Delta_tpn-jn	0.45ns
Delta_tgate	4.02ns	Delta_tgate	0.21ns
Delta_tTotal	2.65ns	Delta_tTotal	0.1ns

It needs to be noted that the value of Delta_tTotal is estimated to be only 0.1ns for the 22 nm technology node and all the values are less than 1 ns.

The leakage issue can be counteracted by adding a bleeder device or a bleeder transistor (Mb1) as shown in Figure 4.2. The only function of the PMOS pull-up device is to compensate for the charge lost due to pull-down leakage paths. This allows the stronger pull-down devices to lower the OUT node significantly below the switching threshold of the next gate when the pull-down network turns on.

More commonly, the bleeder device is implemented in a feedback configuration, as shown in Figure 4.3, to eliminate the static power dissipation altogether.

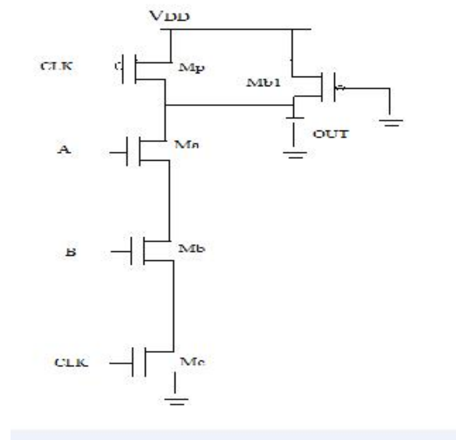

Figure 4.2: Bleeder device implementation.

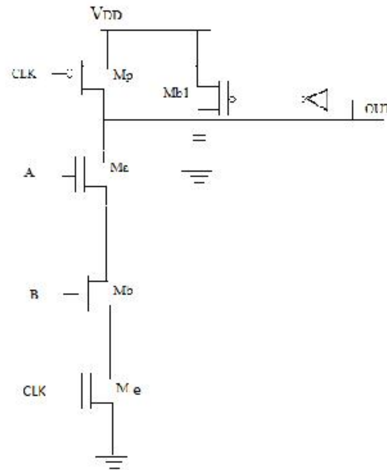

Figure 4.3: Bleeder device practical implementation in feedback configuration.

4.2 Charge sharing

Another major concern in dynamic logic is the impact of charge sharing. Consider the circuit in Figure 4.4 which is obtained from [24]. During the precharge phase the output node is precharged to V_{DD}. Assume that all inputs are set to 0 during precharge, and that the capacitance C_a is discharged and also that input B remains 0 during evaluation. When input A makes 0 to 1 transition, M_a is turned on. The charge initially stored on capacitance C_L is redistributed over C_L and C_a. This causes a drop in output voltage which cannot be recovered due to the dynamic nature of the circuit. When the output voltage drops below the switching threshold of the gate it drives, charge sharing becomes a major concern.

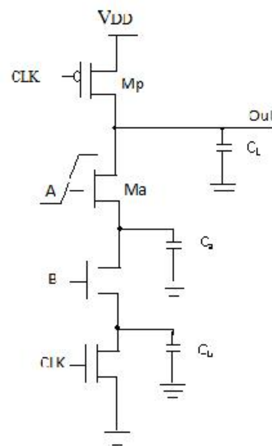

Figure 4.4: Charge sharing in dynamic network

The layout of the above schematic was generated using Electric software and the respective capacitance values were obtained from it. The values for different technology nodes are tabulated in Table 4.3.

Table 4.3: Values of C_L and C_a derived from the electric layout.

Technology Node	C_L	Ca
45 nm	0.243 fF	0.763 fF
32 nm	0.606 fF	0.1158 fF
22 nm	0.1079 fF	0.4809 fF

When $V_{out} < V_{Tn}$, the final value of V_x equals $V_{DD} - V_{Tn}\ (V_x)$. Charge conversation then yields,

$$C_L V_{DD} = C_L V_{out}\ (final) + C_\alpha\ [V_{DD} - V_{Tn}\ (V_x)] \tag{4.10}$$

$$\Delta V_{out} = V_{out}\ (final) + (-V_{DD}) = \frac{C_\alpha}{C_L}\ [V_{DD} - V_{Tn}\ (V_x)] \tag{4.11}$$

If $V_{out} > V_{Tn}$, V_{out} and V_x reaches the same value $\Delta V_{out} = -V_{DD}\left(\frac{C_\alpha}{C_\alpha + C_L}\right)$ (4.12)

The boundary conditions between two cases can be determined by setting V_{out} equal to V_{Tn} , yielding

$$\frac{C_\alpha}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}} \tag{4.13}$$

It is desirable to keep ΔV_{out} below $|V_{Tp}|$. The output of dynamic gate might be connected to a static inverter, in which case the low level of V_{out} would cause static power consumption.

4.2.1 Noise generator

With the continued scaling of CMOS technology and increasing performance requirement, deep submicron noise is becoming an issue. Noise can be defined as anything that deviates the voltage at the evaluation node from ground rails or nominal rails when it should have a stable low or high value [22]. In a modern CMOS processor as the interconnects are packed more closely, the amount of capacitive coupling between the nets increases. To maintain the drive strength the threshold voltage is scaled lower resulting in lower noise margins and increased leakage noise. Noise can be characterized

by peak magnitude relative to nominal supply and ground rails in time domain. Some of the noise sources most common in digital design are leakage noise, power supply noise, charge sharing noise and crosstalk noise. The major reason for extensive use of digital systems is because of its property of noise immunity. Digital systems operate over a range of voltages which may fall out of range due to noise. But a CMOS inverter restores these logic values by means of a nonlinear voltage transfer, which reduces the noise in low and high voltage rails.

The schematic of the noise injection circuit is derived from [22] and is shown in Figure 4.5. The noise injection circuit is designed to produce a noise waveform, i.e. induce a noise pulse of desired amplitude and width into a logic gate and several simulations are run to quantify the noise immunity of a network which in other words is to evaluate how tolerant is a gate to noise. It is important to understand the gate's noise immunity in the study of dynamic logic because dynamic logic gates are susceptible to glitches. This is not a major concern in static logic as it has both active pull-up and pull-down devices to aid with the recovery, i.e. even though the output might go down momentarily but it gets restored but whereas in dynamic logic, if we get a glitch and the charge at the output discharges; a bleeder device is required to recharge the output capacitance.

A glitch is introduced using the noise injection circuit shown below. This causes the output node to discharge due to charge leakage and then a bleeder device is added to the output of the circuit in an effort to compensate for the charge lost.

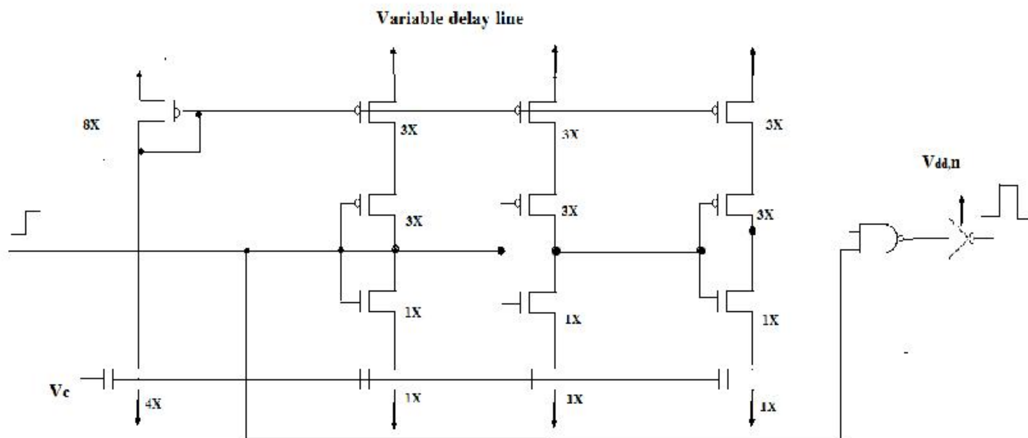

Figure 4.5: Schematic of a noise injection circuit.

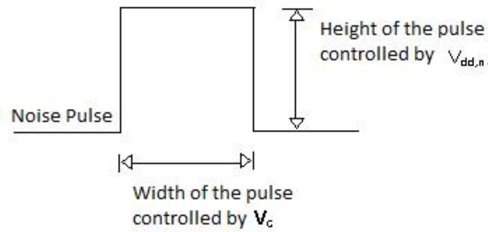

Figure 4.6: Noise pulse controls.

The width of the noise pulse generated by the noise injection circuit is controlled by the value of voltage V_c and the height of the pulse is varied by a change in the value of $V_{dd,n}$ as seen above in Figure 4.5.

Various simulations are generated using LTSPICE by varying the width of the noise pulse and the response time, i.e. how long before the output is restored with the help of the bleeder device. In other words, the whole point of these simulations is to analyze which bleeder device size results in the fastest recovery time when subjected to noise waveforms of different widths. The simulations are in Appendix B. The fastest recovery time was observed for $V_{nx} = 0.9V$ for all the three bleeder sizes simulated. The values are tabulated in Table 4 .4.

To understand the simulations, the following part of the above schematic is used to show the nodes, at which the waveforms are simulated,

Table 4.4: Recovery time for the bleeder sizes at V=Vnx.

Bleeder device sizes	$L=2\times L_p$	$L=3\times L_p$	$L=5\times L_p$
Recovery time	0.136 ns	0.172 ns	0.231 ns

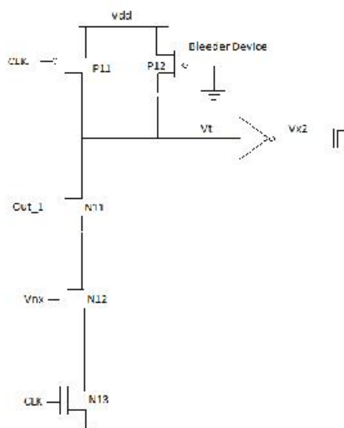

Figure 4.7: Bleeder circuit.

Electric software is utilized to generate the layout of the above schematic, from which the corresponding netlists are obtained. The netlists in turn are used to derive the parasitics which are used in running the simulations using LTSPICE software. Several simulations were performed by varying the bleeder device size. The results from the simulations are tabulated in the appendix.

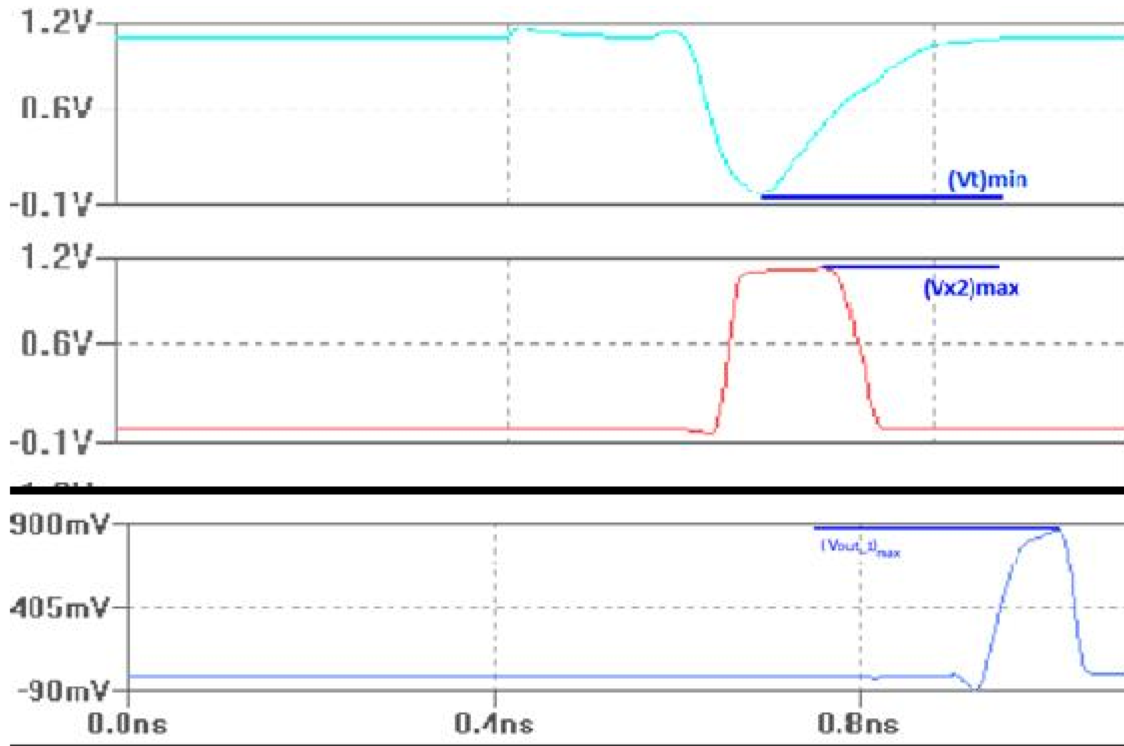

Figure 4.8: Explanation of bleeder device simulations.

where, V_{nx} is the voltage used to control the width of the noise pulse.

Recovery time is the time delay in ns for the output Vout to approximately reach its original high value because of the bleeder device, i.e. the delay between the 90% point of V_{out} and $V_{t.}$

$(V_t)_{min}$ is the minimum value to which the output of the bleeder circuit drops because of the noise pulse.

$(V_{x2})_{max}$ is the maximum value to which the output of the circuit recovers because of the bleeder device.

Similarly, simulations are run for bleeder sizes 3×Lp and 5×Lp and the results are tabulated in Appendix A.

Based on the observations made from the simulation results, it is validated that the bleeder device does help in the charge recovery at the output. It was observed that the response times are proportional to the size and strength of the bleeder device, i.e. the stronger the bleeder device, the faster was the recovery time. Hence the noise immunity of the dynamic logic circuit under study is dependent on the size and strength of the bleeder device.

Chapter 5
Conclusions and Future Work

5.1 Conclusion

The objective of this thesis is to characterize the performance of dynamic logic circuits in VDSM technologies and to evaluate various design strategies to mitigate the effects of leakage currents and small noise margins as they are a major concern when the technology is scaled to deep submicron dimensions and lower.

The design and layout of the dynamic gates have been described. Extracted SPICE netlists from the physical layout provided the parasitic capacitance information. The interconnect model and FET predictive technology models discussed in Chapter 2 were utilized to obtain accurate simulations of the delay characteristics for the dynamic gates. The parasitic parameters for each technology node were calculated based on the interconnect dimensions obtained from the literature. The design optimization of the dynamic logic circuits was discussed and this method is illustrated via the design of full adder circuits using various dynamic logic families. The method for adder circuit optimization included the analysis of the schematic of each full adder circuit and the construction of physical layouts.

In the analysis of the effects of charge sharing and charge leakage mechanisms, weak pull-up transistors known as bleeder devices were used to compensate for the loss of charge from the dynamic storage nodes. The impact of these devices on the performance of dynamic logic was evaluated through the addition of a noise generator circuit to the simulations.

It is concluded that increasing leakage currents in nanoscale technology will be a major concern but functional dynamic logic circuits can be implemented in VDSM technologies through the introduction of properly sized bleeder devices. However, some degradation in circuit speed is expected.

5.2 Future Work

This work has paved a way for implementing dynamic logic in more complex circuits like datapaths and microprocessors at submicron technology levels. Further research is required to explore the possibility of implementing these adders with future nanotechnologies, such as carbon nanotubes. The robustness and fault tolerance of the circuits need to be studied as these are critical factors for future technologies where the small transistor dimensions are likely to make the devices more prone to failure.

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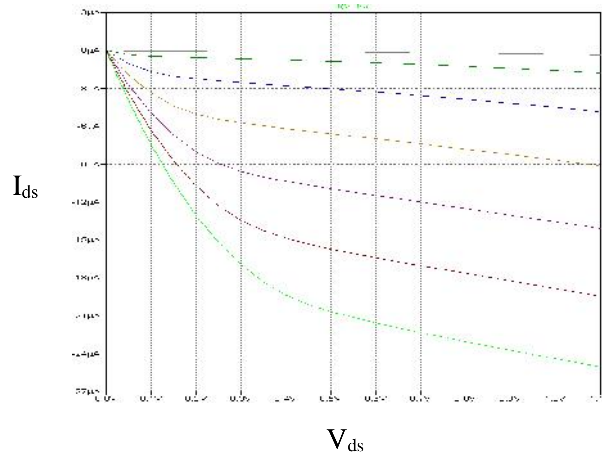
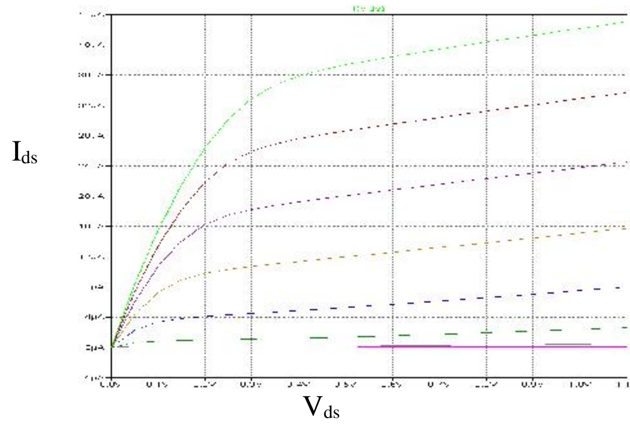
Appendix A: I-V plots of technology nodes

1. I-V curves for pMOSFET and nMOSFET for all the technology nodes.

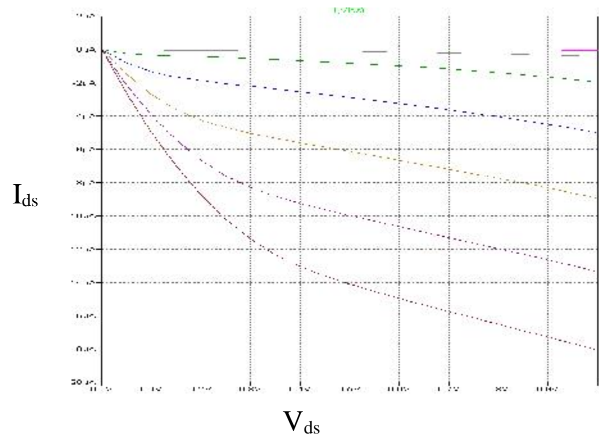
a) I-V plot for 16 nm technology node.



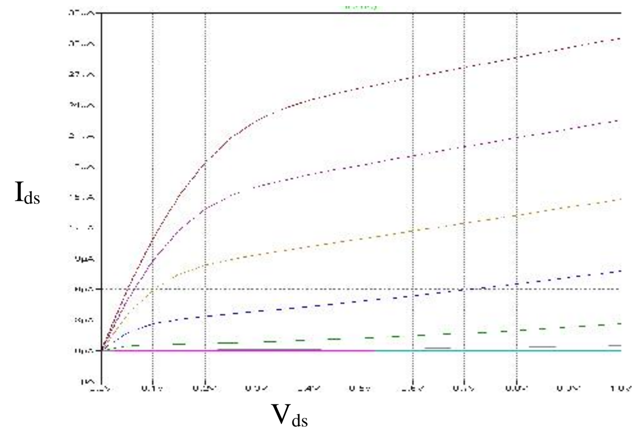
b) I-V plot for 32 nm technology node.



c) I-V plot got 45 nm technology node.



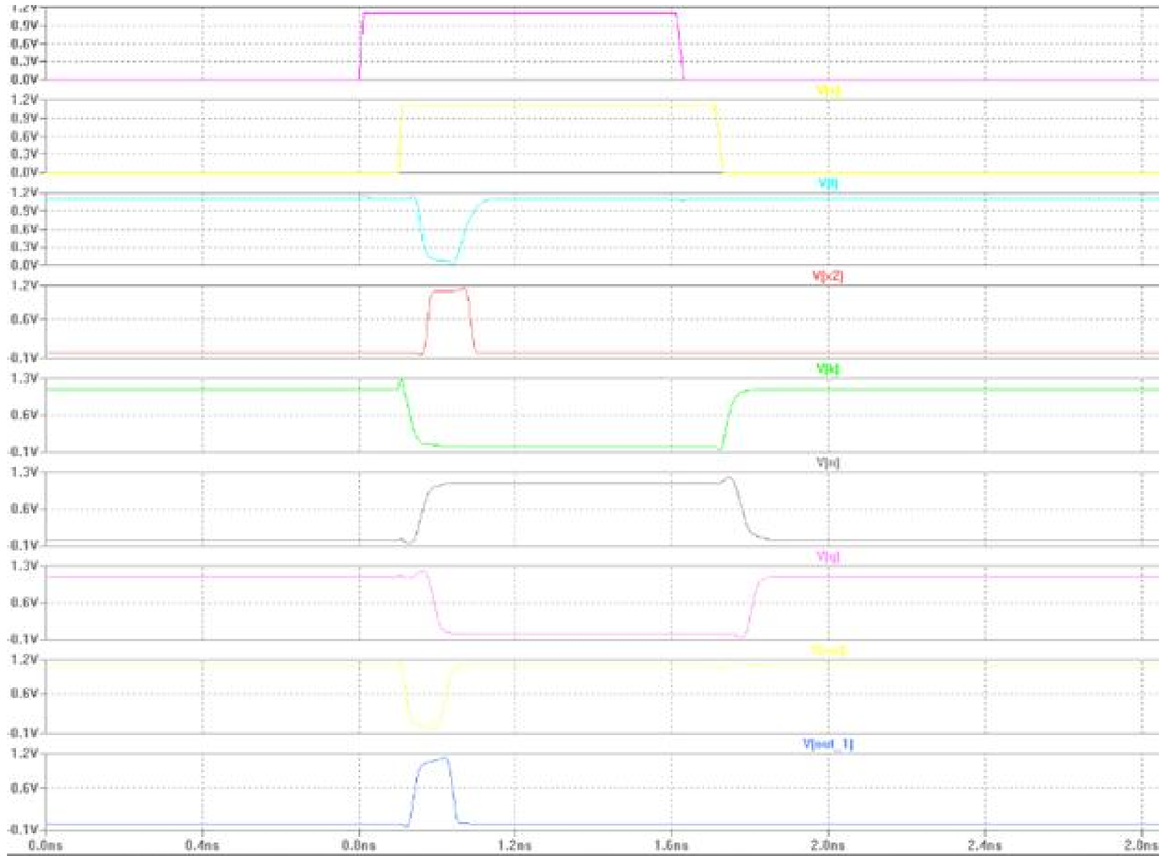
d) I-V plot got 64 nm technology node.



Appendix B

SPICE simulations for different bleeder device sizes i.e. 2×lp, 3×lp, 5×lp:

SPICE simulation for bleeder size 2×lp:



SPICE simulation for bleeder size 3×lp:

SPICE simulation for bleeder size 5×lp: