A Non-Electrolytic-Capacitor Low-Power AC-DC Single-Stage SEPIC-Flyback LED Converter

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***Abstract*—This paper presents an isolated single-stage SEPIC-flyback ac-dc converter for supplying light emitting diode (LED) that can eliminate electrolytic capacitor adoption. The Single Ended Primary Inductor Converter (SEPIC) converter performs the power factor correction (PFC) function, while the flyback converter regulates the DC stage and provides circuit isolation for LED protection. This paper analyses the operation of the proposed LED topology and verifies the performance of the circuit using PSCAD simulation. The converter achieved a high power factor, low total harmonic distortion and low output voltage ripple. The proposed circuit also obtained voltage below 450 V across the storage capacitor, allowing low voltage rating components employment.**

***Index Terms*—AC-DC Converter; Non-Electrolytic Capacitor; SEPIC-Flyback; Single-Stage Led Converter.**

I. INTRODUCTION

Recently, light emitting diode (LED) has succeeded in placing itself as a promising light source for general solid-state lighting applications. One of the most significant features of the LED as compared to the conventional lightings such as incandescent lamp and fluorescent lamp is its longevity. By comparison, a fluorescent lamp exhibits five times longer operating lifetime than the incandescent lamp, between 7,500 and 30,000 hours but still much lower as compared to the minimum lifetime of the LED which is between 35,000 and 50,000 hours [1].

The LED lighting connected to the ac main requires an ac-dc power converter because the LED operates on dc voltage. A conventional diode rectifier however causes poor power factor and high harmonics at the input current. Therefore, power factor correction (PFC) is necessary to ensure that the power factor comply with standards such as the Energy Star that specifies a power factor of more than 0.9 for commercial of the LED driver [2].

Table 1
Harmonics Limit for Class C [3]

Harmonics [n]	Class C [% of Fundamental Wave]
2	2
3	30* λ
5	10
7	7
9	5
11	3
13≤n≤39 (Odd Harmonics Only)	3

λ is the circuit power factor

Table 2
Comparison of Capacitors [7]

Capacitor Type	Lifetime at 500C ambient temperature (hours)	Available Range
Electrolytic	<10,000	1μF – 12mF
Polyester Film	>100,000	10pF - 80μF
Ceramic	>100,000	10pF - 10μF

Table 1 shows the limits for various low order harmonics up to 39th order harmonics, which are based on IEC-6100-3-2 Class C standard regulation for lighting equipment [3]. Reviews from [4-6] show that a unity power factor and low THD can be achieved through a single-stage LED driver solution. The drivers are particularly attractive for their compact size and implement only one semiconductor switch. However, an electrolytic capacitor is adopted inside the system in order to prevent the unbalanced power between the sinusoidal input power and constant output power over half the line cycle.

Table 2 shows the comparison for three types of dc-link capacitors, which are the electrolytic, polyester film, and ceramic capacitors [7]. Installing an electrolytic capacitor that has a lifetime of less than 10,000 hours will eventually reduce the lifetime of the LED system. Moreover, an increase at 10^{o}C in operating temperature will shorten the electrolytic capacitor lifetime to half [8]. This justifies the motivation to eliminate an electrolytic capacitor from the LED driver. The polyester film or the ceramic capacitor is favourable as it has a longer lifetime than the electrolytic capacitor. However, the available capacitance range is limited. A cascaded dc-dc converter is usually employed on the second stage of the driver to obtain ripple-less output voltage so that lower capacitance value could be used, and polyester film or ceramic capacitor can be selected. However, it compromises on the controller scheme complexity, low conversion efficiency and increases the driver volume [9,10].

A non-electrolytic capacitor has been employed in a single-stage structure integrating the power factor corrector (PFC) stage and dc-dc output voltage regulation stage in a single power conversion stage [11-15]. In [11], the single-stage ac-dc converter output voltage ripple is reduced by intentionally distorting the input line current. As a consequence, the output dc-link capacitance is lowered. However, a complex third harmonic injection control method need to be implemented to achieve the power factor of unity. The other method is to use the feedforward control as proposed in [12] and [13], however

the overall cost of the LED driver is expensive due to the microcontroller adoption. Authors in [14] use analogue devices to achieve the feedforward function with reduced complexity and price. The output current ripple is approximately 15%-20%. Nevertheless, there is trade- off between the output capacitor value and THD. The converter contains THD more than 20% if the output capacitor is less than 10μF. Another single-stage non-electrolytic ac-dc converter which integrates boost converter with half- bridge resonant inverter can achieve maximum efficiency of 93.14% [15]. However, two switches on the half-bridge inverter and four extra diodes at the resonant output side increase the converter size and decrease the system reliability.

In this paper, a simple isolated single-stage single-switch SEPIC-flyback converter as shown in Figure 1 is proposed. The proposed converter topology draws a high power factor line current, has a low THD and low dc voltage ripple even with a small capacitance value. The next section presents the configuration of the proposed circuit and describes the operating modes. Section 3 explains the components design and Section 4 presents the calculation of the component value for an 18 W LED driver. Finally, the verification of the converter circuit using PSCAD simulation is presented in Section 5.

II. Circuit Configurations and Operating Modes

The proposed isolated single-stage SEPIC-flyback converter in Figure 1 can be treated as two independent circuits where the PFC takes place in the SEPIC-like circuit and the regulated dc output stage occurs at the flyback-like circuit. The PFC stage consists of a filter inductance, L_f, an input rectifier, a coupling capacitor, C_f, and an input inductor, L_1. When inductor L_1 behaves in discontinuous conduction mode (DCM), the converter can naturally draw near-unity power factor during a constant duty cycle switching and gives low THD at the input line. However, high current stress exists across the circuit components. In order to avoid high components cost and maintain reliability in the circuit system, the current in inductor L_1 is designed to be in continuous conduction mode (CCM) and still obtain a high power factor. A small filter inductor, L_f and coupling capacitor, C_f are employed to remove the high frequency current harmonics at the input line.

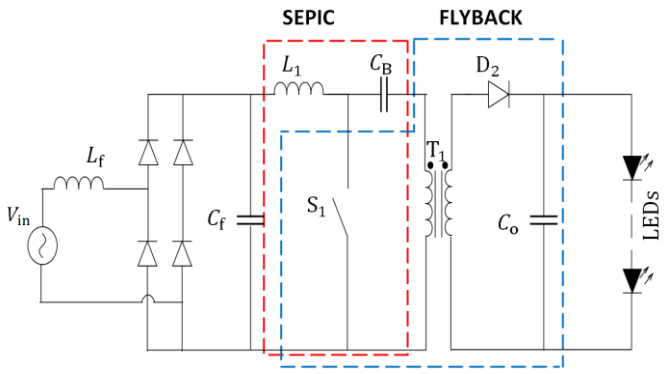


Figure 1: Proposed SEPIC-flyback converter.

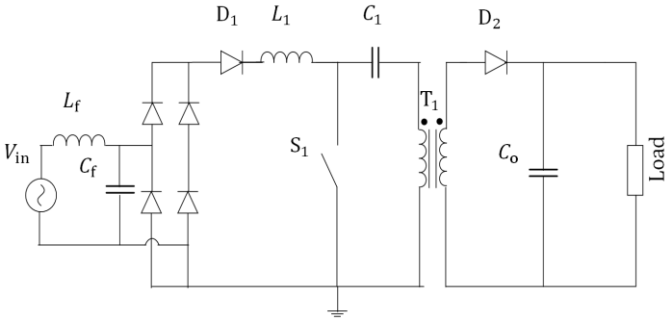


Figure 2: BIFRED converter.

In Figure 1, the flyback dc-dc conversion stage involves a switch S_1, an energy storage capacitor C_B, an isolation transformer T_1, an output capacitor C_o, and an output diode, D_2. The proposed circuit configuration is somewhat similar to the boost-integrated flyback- rectifier energy- storage dc-to-dc converter (BIFRED) as shown in Figure 2. The difference in the proposed SEPIC-flyback circuit with the BIFRED is that the proposed converter eliminates diode, D_1 .

According to [16], if the dc-dc stage of the BIFRED converter operates in CCM, the energy storage capacitor voltage V_{C_1} is strongly dependant on the line voltage and load current variations. Simply put, the capacitor C_1 exhibits high voltage stress at light load and high input voltage. It is possible to keep the voltage across capacitor C_1 at the range below 450V if the dc-dc stage operates in DCM because the voltage is independent of the output current and becomes dependent on the inductor instead. However, the DCM operation results in a high current stress problem in the switch S_1.

In the proposed circuit, the flyback side is allowed to operate in CCM. In fact, output current ripple is lower in CCM if compared to DCM [17]. The energy storage capacitor, C_B and transformer magnetizing inductance is properly designed to obtain voltage lower than the commercial capacitor rating of 450V or 600V especially during light load. Also, an appropriate value selection of the capacitor C_B and transformer magnetizing inductance results in a less–distorted less-ripple input and output current enabling the usage of non-electrolytic capacitor to prolong the lifetime of the LED system.

Figure 3 describes the key waveform of the proposed circuit during half-line cycle of input frequency. Two steady-state operation modes exist for the proposed converter, which depends on the state of the power switch, S_1 and the output diode, D_2 as shown in Figure 4. For simplifying the analysis, the following assumptions are made:

(a) The input voltage is an ideal sinusoidal wave, $V_{in}(t) = V_m \sin \omega t$ where V_m is the peak input voltage and ω is the angular frequency. The diode rectifier is ideal and $V_{rec}(t) = V_m|\sin \omega t|$.

(b) The switching frequency, f_s is much higher than the ac line frequency and the ac source is regarded as a constant voltage source during one switching period,

(c) The transformer winding ratio, $\left[\frac{N_2}{N_1}\right]$ is one.

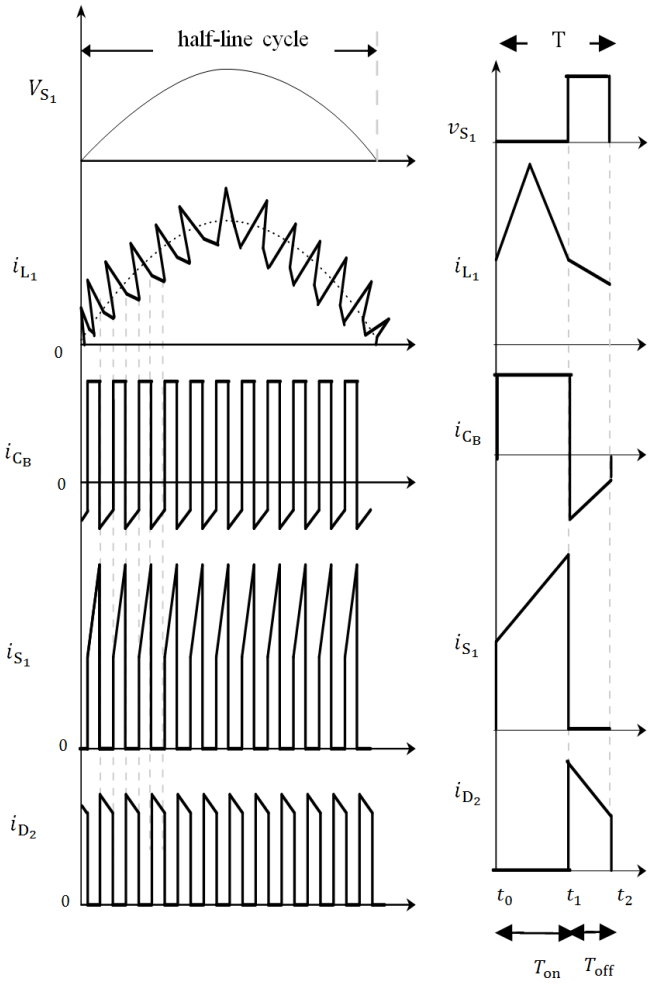


Figure 3: Operating waveforms of the proposed SEPIC-flyback converter.

A. *Mode I [$t_0 \leq t < t_1$]*

Mode I happens when switch S_1 is turned on at time $t = t_0$. The rectified voltage, v_{rec} is imposed across the inductor L_1. The increasing energy associated with inductor current i_{L_1} is obtained from the input line and the change of current is:

$$\frac{\Delta i_{L_1}}{\Delta t} = \frac{V_{rec}(t)}{L_1} \quad (1)$$

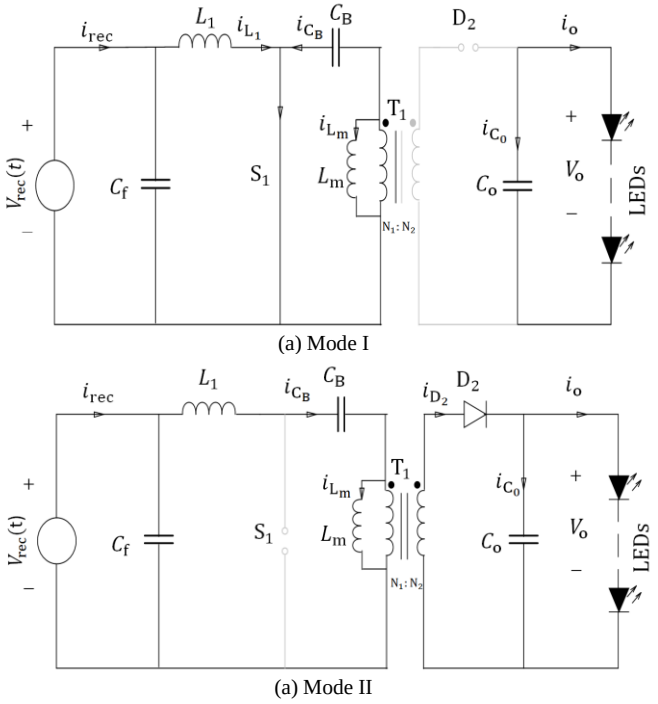
At the same time, the energy stored in the magnetizing inductance of transformer T_1 is discharged to capacitor C_B in the direction of i_{C_B} as portrayed in Figure 4. Thus, current and voltage across C_B are:

$$V_{C_B}(t) = V_{L_m}(t) \quad (2)$$
$$i_{C_B}(t) = -i_{L_m}(t) \quad (3)$$

Switch S_1 then carries the total current across inductor L_1 and capacitor C_B.

$$i_{S1}(t) = i_{L_1}(t) + i_{C_B}(t) \quad (4)$$

At this mode, since the output diode is in reverse biased, the output capacitor C_o solely provides current to the load.



(a) Mode I

(a) Mode II

Figure 4: SEPIC-flyback topological modes

$$i_{C_o}(t) = -\frac{V_o(t)}{R_\delta} \quad (5)$$

where R_δ is the resistance parameter for the LED lamp equivalent circuit.This mode terminates when S_1 is switched off and voltage at D_2 is more than zero commencing the next interval.

$$V_{D_2}(t) = V_{C_B}(t)\left[\frac{N_2}{N_1}\right] - V_o(t) < 0 \quad (6)$$

B. *Mode II [$t_1 \leq t < t_2$]*

The output diode is forward biased when switch S_1 is turned off, indicating the start of Mode II. Assume that the magnetizing inductance is large enough and i_{L_m} is negligible, then the current in the output diode D_2 can be expressed as

$$i_{D_2}(t) = i_{C_B}(t)\left[\frac{N_1}{N_2}\right] = i_{C_o}(t) + i_o(t) \quad (7)$$

During this mode, the energy in inductor L_1 and capacitor C_B are discharged and the magnetizing inductance, L_m is charged.

$$i_{L_1}(t) = i_{C_B}(t) = \frac{V_{rec}(t) - (V_{C_B}(t) + V'_o(t))}{L_1} \quad (8)$$

where V'_o is the primary side referred output voltage. The changes of secondary current, Δi_{sec} is in proportion to the changes of primary current, Δi_{pri} and the transformer winding ratio in order to charge the output capacitor, C_o and power up the LED. Assume an ideal diode, where the voltage drop in D_2 is zero. Therefore, the primary (V_1) and secondary (V_2) voltages is written as:

$$V_1(t) = V_2(t)\left[\frac{N_1}{N_2}\right] = V'_{\mathrm{o}}(t) \quad (9)$$

III. Design Analysis

A. Capacitor C_B Design

The energy storage capacitor, C_{B} is employed between the power switch and transformer for balancing the input and output power. The value for capacitor C_{B} should be properly selected so as the rise time for voltage $V_{\mathrm{C_B}}$ is not too slow as compared to the rise time for voltage across the filter capacitor, C_{f}. If value for capacitor C_{B} is too big, then the reset time for inductor L_1 will be longer and the current will eventually go to the negative value. This current will flow to the capacitor C_{f} and the input line waveform will be distorted.

By using the magnitude of charge in capacitance definition:

$$\Delta V_{\mathrm{cB}} = \frac{\Delta Q_{\mathrm{C_B}}}{C_{\mathrm{B}}} = \frac{i_{\mathrm{C_B}} DT}{C_{\mathrm{B}}} \quad (10)$$

where T is the switching period and D is the duty cycle. The capacitor charge balance for output capacitor is zero in one switching period. Using equations (5) and (7), the charge balance equation is written as:

$$D\left(-\frac{V_{\mathrm{o}}}{R_\delta}\right) + D'(i_{\mathrm{C_B}}\left[\frac{N_2}{N_1}\right] - \frac{V_{\mathrm{o}}}{R_\delta}) = 0 \quad (11)$$

where D' is $(1-D)$. Equation (11) is simplified and the current in capacitor C_{B} is:

$$i_{\mathrm{C_B}} = \frac{V_{\mathrm{o}}}{D'.R_\delta}\left[\frac{N_1}{N_2}\right] \quad (12)$$

The voltage second balance in Modes I and II of inductors L_1 and L_{m} are considered in the representation of the voltage across capacitor C_{B}. Equations (1) and (8) are used to solve the voltage second of L_1.

$$D.V_{\mathrm{rec}} + D'\left(V_{\mathrm{rec}} - V'_{\mathrm{o}} - V_{\mathrm{C_B}}\right) = 0 \quad (13)$$

The voltage across capacitor C_{B} is

$$V_{\mathrm{C_B}} = \frac{V_{\mathrm{rec}}}{D'} - V'_{\mathrm{o}} \quad (14)$$

Moreover, Equations (2) and (9) are used to express the voltage second balance of inductor L_{m} as:

$$D.V_{\mathrm{C_B}} - D'.V'_{\mathrm{o}} = 0 \quad (15)$$

The voltage across capacitor C_{B} is also written as:

$$V_{\mathrm{C_B}} = \frac{D'V'_{\mathrm{o}}}{D} \quad (16)$$

Equations (14) and (16) are rearranged so that the primary-side-referred output voltage is defined as:

$$V'_{\mathrm{o}} = \frac{DV_{\mathrm{rec}}}{D'} \quad (17)$$

By substituting Equation (17) into Equation (16), the voltage across capacitor C_{B} can be expressed as:

$$V_{\mathrm{C_B}} = \frac{D'}{D}\left(\frac{DV_{\mathrm{rec}}}{D'}\right) = V_{\mathrm{rec}} \quad (18)$$

The value for capacitor C_{B} can be obtained by substituting equations (12) and (18) into equation (10), thus

$$C_{\mathrm{B}} = \frac{i_{\mathrm{C_B}}\mathrm{DT}}{\Delta V_{\mathrm{cB}}} = \frac{V_{\mathrm{o}} DT}{D' R_\delta \Delta V_{\mathrm{rec}}} \quad (19)$$

B. Input Inductor Design

An input inductor, L_1 gives a smooth continuous input current waveform that leads to a small line input filter adoption. The variation of voltage across L_1 is found from equation (1) where:

$$V_{\mathrm{L_1}}(\mathrm{t}) = V_{\mathrm{rec}}(t) = L_1\left(\frac{\Delta i_{\mathrm{L1}}}{\Delta t}\right) = L_1\left(\frac{\Delta i_{\mathrm{L1}}}{DT}\right) \quad (20)$$

Rearranging Equation (20),

$$L_1 = \frac{V_{\mathrm{rec}}.D}{\Delta i_{\mathrm{L_1}}.f_{\mathrm{s}}} \quad (21)$$

To solve for the current across inductor L_1, the charge balance theory at capacitor C_{B} and C_{o} is used. Thus, from Equation (3) and (8), an equation for charge balance at C_{B} is obtained.

$$-D.i_{\mathrm{L_m}} + D' i_{\mathrm{L_1}} = 0 \quad (22)$$

and the current across inductor L_1 is:

$$i_{\mathrm{L_1}} = i_{\mathrm{L_m}}\frac{D}{D'} \quad (23)$$

On the other hand, the current across capacitor C_{o} during on-state and off-state of switch S_1 to be expressed using the charge balance theory based on Equation (5) and (7) is:

$$-D.\frac{V_{\mathrm{o}}}{R_\delta} + D'\left(i_{\mathrm{L_1}} + i_{\mathrm{L_m}} - \frac{V_{\mathrm{o}}}{R_\delta}\right) = 0 \quad (24)$$

The current across inductor L_1 is also expressed as:

$$i_{\mathrm{L_1}} = \frac{V_{\mathrm{o}}}{R_\delta D'} - i_{\mathrm{L_m}} \quad (25)$$

Equaling both Equation (12) and (14), thus:

$$i_{\mathrm{L_m}}\frac{D}{D'} = \frac{V_{\mathrm{o}}}{R_\delta D'} - i_{\mathrm{L_m}} \quad (26)$$

By simplifying Equation (26) and substituting it into Equation (17),

$$i_{\mathrm{L_m}} = \frac{V_{\mathrm{o}}}{R_\delta} = \frac{V_{\mathrm{rec}}.D}{R_\delta.D'} \quad (27)$$

Therefore, the current i_{L_1} can be expressed as:

$$i_{L_1} = i_{L_2}\frac{D}{D'} = \left(\frac{V_{rec}.D}{R_\delta.D'}\right)\frac{D}{D'} = \frac{V_{rec}.D^2}{R_\delta.D'^2} \quad (28)$$

C. Boundary Working Condition

The boundary between the continuous and discontinuous behaviour is reached when the magnetizing inductor current falls to zero right at the end of the commutation cycle. The boundary expression for the duty cycle can be interpreted as:

$$D_{\text{boundary}} = 1 - \sqrt{\frac{2f_s L_m}{R_\delta L_m}} \quad (29)$$

If the DC-flyback side is operating in CCM, the duty cycle must stay lower than D_{boundary}. As mentioned earlier, if the dc-dc stage operates at CCM, large energy is being dumped at the capacitor C_B especially during light loads and high input line because the duty cycle cannot change instantaneously. This leads to a high voltage stress across the storage capacitor to balance the input-output power. It is reported in [18] that the voltage across the energy storage capacitor could reach 900 V at 0.5 A output current with input voltage of 120 V_{rms}.

D. Capacitor C_o Design

The variation in the output capacitor C_o is computed from the capacitance charge theory where:

$$|\Delta Q| = C_o \Delta V_o = \left(\frac{V_o}{R_\delta}\right) DT \quad (30)$$

and ΔV_o is the output voltage ripple. Expressing the output capacitance in terms of output voltage ripple yields to:

$$C_o = \frac{D}{R_\delta\left(\frac{\Delta V_o}{V_o}\right)f_s} \quad (31)$$

IV. Design Example

An 18W SEPIC-flyback circuit design is calculated based on the following parameters:

1. AC input line voltage (V_{ac}) : 230 V_{rms};
2. Switching frequency (f_s) : 100 kHz;
3. Duty cycle (D) : 0.2;
4. Total forward voltage of LED (V_o) : 30 V;
5. LED current (i_o) : 0.6 A.

The main objectives are to get the power factor more than 0.9, keep the harmonics within the IEC standard, to ensure capacitor C_B has a low voltage rating; and to regulate the output ripple so that a non-electrolytic capacitor output can be employed.

As the switching frequency is much higher than the input line frequency, rapid transitions in switching signal may interact with the power line signal, conducting noises in the circuit. To comply with the specified harmonic current emission standard in IEC6100-3-2 Class C, adding an inductor L_f helps to raise the impedance of the current path from the power source. The conducted interference noise is suppressed, thus resulting in lower harmonics distortion. In accordance to [19], the inductance reactance can be calculated as:

$$X_{Lf} = \frac{V_{rec}}{i_o} - \frac{V_o\pi}{2i_o} \quad (32)$$

where $X_{Lf} = 2\pi f_s L_f$. Then, the filter inductor, L_f is solved to be 0.76 mH. A small resonant capacitor is added at the front end of the rectifier in order to effectively shunt the noise. To calculate for the filter capacitor, C_f, the attenuation of 24 db at the switching frequency of 100 kHz is assumed [20]. So, the corner frequency is:

$$f_c = f_s 10^{\left(\frac{-24}{40}\right)} = 25,118 \text{ Hz} \quad (33)$$

It can be seen that the corner frequency is sufficiently less compared to the switching frequency, f_s. So, the filter will essentially pass only the dc part of $v_{in}(t)$. Now, solving for the filter capacitor,

$$C_f = \frac{1}{4\pi^2 f_r{}^2 L_f} = 52 \text{ nF} \quad (34)$$

The inductor L_1 value is calculated by first determining the current across inductor L_1 by using Equation (28).

$$i_{L_1} = \frac{V_{rec}.D^2}{R_\delta.D'^2} = 0.4 \text{ A} \quad (35)$$

Assuming the inductor L_1 peak-to-peak current is half the averaged i_{L_1}, thus the inductor value based on Equation (21) is:

$$L_1 = \frac{V_{rec}.D}{\Delta i_{L_1}.f_s} = 3.25 \text{ mH} \quad (36)$$

Assuming that the ripple voltage is 1% and the transformer ratio is one, the value of C_B is:

$$C_B = \frac{i_{C_B}DT}{\Delta V_{cB}} = \frac{V_o DT}{D'R_\delta \Delta V_{rec}} = 0.4 \text{ µF} \quad (37)$$

To calculate the output capacitor value, assuming that the desired output ripple voltage is 1%, therefore from (31), the output capacitor is:

$$C_o = \frac{D}{R_\delta\left(\frac{\Delta V_o}{V_o}\right)f_s} = 4 \text{ µF} \quad (38)$$

V. Simulation Results

In order to verify the proposed converter, the simulation of an 18W SEPIC-flyback circuit model was carried out using PSCAD software in accordance to the design example discussed before. Table 3 summarizes the parameters of the components for the proposed circuit configuration.

Figure 6 shows the waveforms of input voltage, V_{in} and input current, i_{in} when the input line voltages is 240 V_{rms} at 50 Hz line frequency. It can be observed that the input current waveform is a smooth sinusoidal and follows the input voltage closely. The power factor achieved is more than 0.9 with a THD of 7.88%. By assuming that the power factor is unity,

Figure 5 compares the harmonics content of the input current with standard IEC 6100-3-2 Class C regulation for input power less than 25W. It can be seen that the proposed converter satisfies the standard IEC harmonics limit with only about 7% harmonics spectrum obtained at third order harmonics.

Table 3
Circuit parameters

Parameter	Value
Duty cycle	0.2
Capacitor C_B	0.4 µF
Filter capacitor, C_f	52 nF
Output capacitor, C_o	4 µF
Inductor L_1	3.25 mH
Filter inductor, L_f	0.76 mH
Capacitor C_B	0.4 µF

From Figure 7, the switching peak voltage of 383 V at 30 V voltage output is observed. Meanwhile, peak voltage of 365 V across capacitor C_B is observed during the same interval as in Figure 8. Figure 9 shows the overvoltage stress across capacitor, C_B as a function of the load variation at different input voltage with 50 Hz line frequency. The proposed converter maintains voltage below than 450 V from 4 W to 20 W output power, entailing a low cost 450 V/600 V capacitor rating adoption.

Figure 10 and Figure 11 illustrate the detailed output voltage and output current waveforms. The average output current is 0.59 A with approximate 3% peak-to-peak ripple. An average of 29.6 V output voltage with approximate 3% peak-to-peak ripple is observed at the load side. Generally, LED manufacturers recommend about ±5% to ±20% of the DC output current ripple [21]. This proves that the proposed circuit could implement a 4 µF non-electrolytic capacitor at the DC-bus side to produce a stable DC output power with only 3% ripple. This will maintain the projected lifetime of the LED.

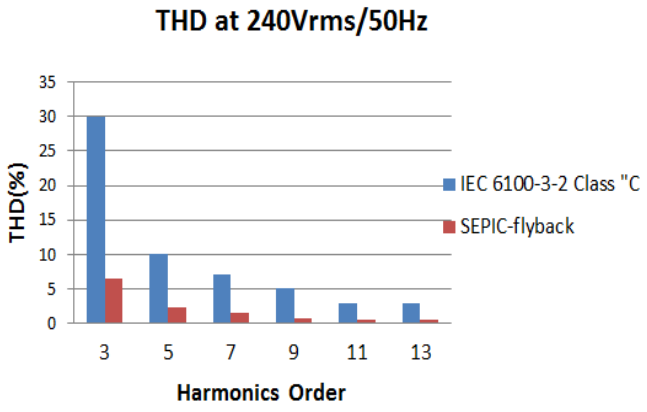


Figure 5: Harmonic content of input current compared with IEC 6100-3-2 Class C.

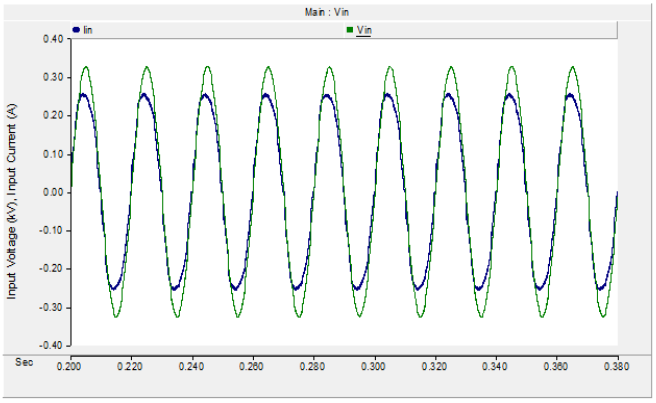


Figure 6: Simulated waveforms of input voltage (V_{in} = 230 Vrms) and input current (i_{in} =0.24 Arms)

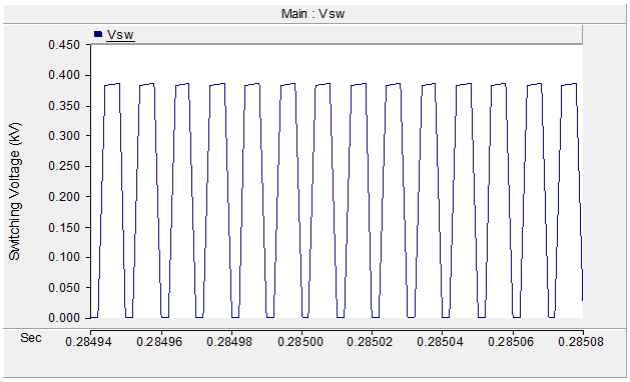


Figure 7: Simulated waveforms of switch S_1 ($V_{S1,max}$ =383V).

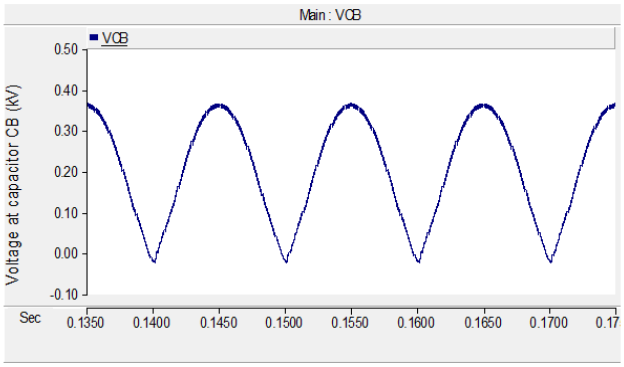


Figure 8: Simulated waveforms of capacitor C_B voltage ($V_{CB,max}$= 365 V).

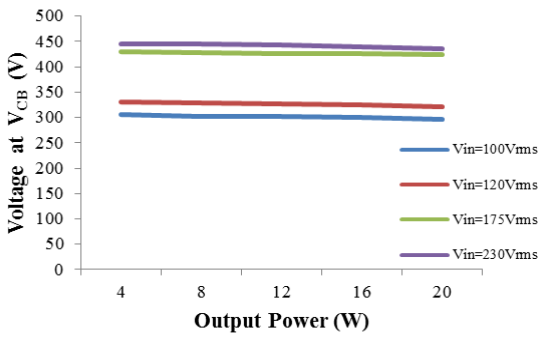


Figure 9: Capacitor C_B voltage over load variation.

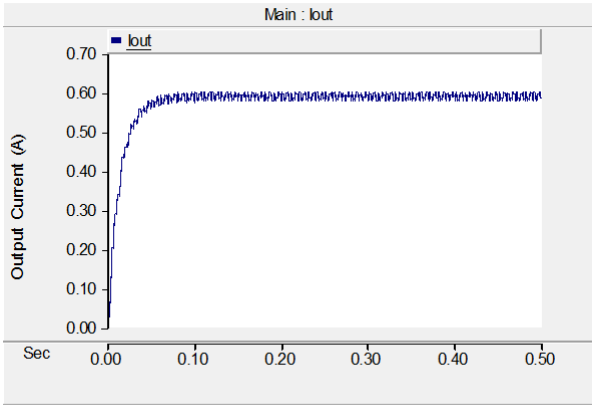


Figure 10: Simulated waveforms of output current (I_o = 0.59A)

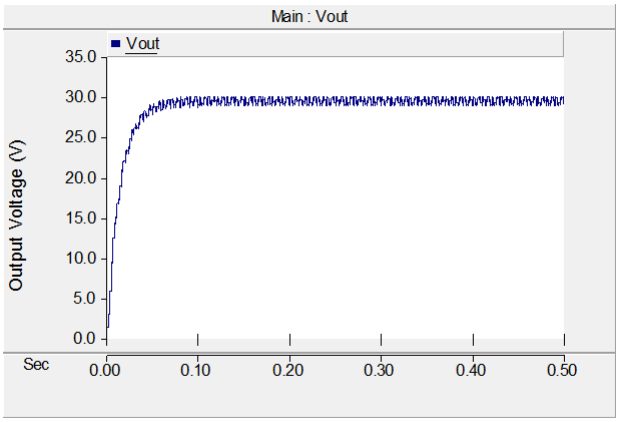


Figure 11: Simulated waveforms of output voltage (Vo = 29V).

VI. CONCLUSION

This paper presents the design of an 18W SEPIC-flyback converter. The proposed circuit is validated using PSCAD software and the results obtained are presented. The proposed circuit has a power factor more than 0.9, THD of 7.88% and a maximum output ripple voltage of 3%. There is no high voltage stress at the storage capacitor as can be seen from results where voltages below than 450 V are obtained. The proposed circuit can also preserve the lifespan of the LED because a non-electrolytic capacitor can be used. Additionally, the proposed converter provides protection for the LED lights through the transformer isolation. The authors intend to carry out experimental verification on the proposed converter.

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