Optimisation of Fine Pitch Contactor and Test Board for QFN Package

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***Abstract*—Fine pitch contactor describes a contactor with smaller air gap between the contact pins. It is used for testing small portable devices. This work presents the optimised way of designing the 0.4 mm pitch contactor and test board for QFN package. The signal integrity of fine pitch test contactor has become a concern due to the small air-gap between the pins that leads to signal crosstalk and impedance mismatch issues. The same challenge had been seen when designing the fine pitch test board because of the requirement to meet 0.4 mm pitch for typical hand-held devices. It restricts the trace routing with typical design rules at the contactor mounting area due to the limited spaces. This would bring to impedance discontinuity and crosstalk effect. Therefore, optimised design rules on the fine pitch contactor and test board are necessary. Full-wave modelling and system level simulation were demonstrated to study the fine pitch design rules. While the full-wave modelling was to construct the contactor and test board components, the system level simulation was intended to study the signal transmission when propagating from one component to another. Overall, designing the fine pitch contactor requires extra study on the signal integrity and layout design. This paper presents a method to study and design the fine pitch contactor design. It reports the test board to achieve minimum losses and distortion test system for functional testing. Our simulation results for fine-pitch contactor model show that the return loss is less than −12 dB at 4 GHz.**

***Index Terms*—Fine Pitch Contactor; Impedance; QFN Package; Signal Integrity; Test Board.**

I. INTRODUCTION

Test contactor provides the electrical connection between package and test board [1]. It is an important component in high volume manufacturing (HVM) to enable millions of device being tested [2]. Most often, this manufacturing testing is implemented on the package with system level function, such as the processor and Field-Programmable Grid Array (FPGA). The complex design of these packages requires a robust test tooling that offers minimum losses and able to emphasise the performance of package to be used by consumers. Signal integrity designer plays an important role in designing the high accuracy test tooling.

Generally, fine pitch contactor is used to describe the contactor design with smaller air gap between pins. Design with 0.5 mm or smaller pitch can be categorised as a fine pitch. This work focuses on the fine pitch contactor at 0.4 mm with Quad-Flat No-Lead (QFN) package because of its popularity with good electrical and thermal performances. It is due to the large ground island in the middle of the package that provides a better signal return path. In the following section, it addresses the challenges of creating the design rules for both fine pitch test contactor and test board.

Designing a fine pitch contactor experiences more signal integrity challenges comparing to a larger pitch of contactor [3]. The major challenge is drawn from the additional mutual inductance between the pins because of the closer distance between the pins. When the current is switched on in the device, the voltage is induced with the factor of mutual inductance and creates the Simultaneous Switching Noise (SSN) effect [4]. SSN is a common signal integrity issue caused by transistor switching activities where it could result in a system failure. A model of a surface mounted socket parasitic using Ansoft's 3-dimension (3D) method has been developed by Figueroa et al [5]. Further, a de-embedding process and a unique test fixture were applied to measure the socket parasitic with a good agreement with their model. The pogo pin structures for test socket in single-ended and differential signalling system, modelled with an equivalent transmission line model was developed by Sun et al [6]. In their work, a simple quasi-static simulation tool Q3D was used to construct the test socket model and verified by full-wave HFSS software. They found the return loss was −15 dB at the frequency range from dc to 10 GHz for the pin radius-to-pitch ratio of 0.20. Recently, a new package-on-package interconnect technology that offers a very fine pitch (less than 0.2 mm) for high bandwidth between the processor and memory in multi-core CPU was published by Ilyas et al [7]. This work shows that more than 1000 interconnects can be formed with the same footprint as the current package. Tunaboylu et al. [1] designed a new spring contactor for wafer-level interposer and high-speed package test system applications. Their experiment results show −1 dB bandwidth of 3.73 GHz for 0.8 mm pitch, measured by the direct contact method.

This work starts with the component level 3D-modelling on fine pitch contactor and test board for QFN package designs using full wave simulation tool from ANSYS HFSS. The objective is to monitor the signal performance changes when sweeping the design parameters, which is followed by the system level simulation, where fine pitch test contactor and test board s-parameter files extracted from the 3D-modelling were cascaded in series to form the functional testing system. The simulation intends to mimic the actual hardware design and monitor the integrity of signal transmitted from one component to another [5].

II. Modelling of Fine Pitch Contactor and Test Board

A. Fine Pitch Contactor Modelling

There are various types of test contactor pin, such as pogo pin and stamped pin used in manufacturing testing [8]. Pogo pin is found to be more reliable and easy to implement in many contactor designs for functional testing. It is also known as spring probe due to the mounting of spring inside the barrel of pin [3]. The spring enables the contact with device under testing (DUT) and test board using the mechanism of spring compression.

Designing a fine pitch test contactor requires analysing the loss of signal caused by interference between pins [6]. To predict the signal performance using a 3D modelling analysis, it is recommended that the construct should be as close as possible to the actual hardware design. The accuracy of result could be varied if the analysis is conducted with different modelling skill. Therefore, this work will demonstrate the reliable method of building the 3D fine pitch contactor model. Using the 3D modelling tool, it allows different structure of contactor and board models to be simulated. ANSYS HFSS tool is an industrial recognised 3D modelling tool for electromagnetic simulation [9, 10] applied in this work.

The simplified pogo pin model is formed by barrel, top tip and bottom tip. Barrel is the body of the pin and typically used as the basic part to start the pogo pin modelling. The spring inside the barrel can be excluded from the modelling because the presence of the spring in the model does not bring any effect to the result. This phenomenon is known as the skin effect, where signal will transmit on the barrel in high frequency that has lower resistance [11]. The total length of the barrel should be the compressed length of actual pogo pin under testing condition. This is critical to study the losses of pin because the inductance is varied by the length of the pin.

Constructing the barrel is as simple as using the cylinder shape. However, adding the probe tips on both ends of barrel may require additional steps. It is because a direct option of the shape can represent the design of the probe tips. Therefore, this work recommends a simplified probe tip with 2-dimension (2D) trapezium and sweep across the z-axis to transform into 3D part. This will create a smaller diameter of probe tip in comparison to the barrel. The design of the pogo pin is completed, once the top and bottom probe tips are constructed, Figure 1 shows the illustration of creating the 2D trapezium model and transforming it into 3D probe tip.

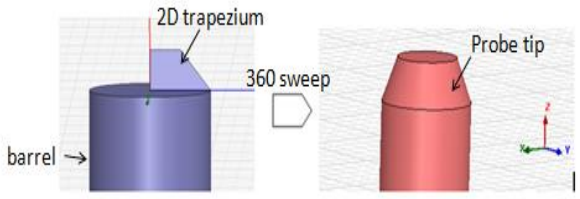

Figure 1: Construction the pin-tip of the pogo pin

To complete the fine pitch contactor, the constructed pogo pin must be duplicated with multiple pins at pitch 0.4 mm. This work analysed 3 × 3 pin matrix of fine pitch contactor. Therefore, a total of 9 pogo pins were required in this work. The pogo pin allocated in the middle was assigned as the signal pin and surrounded by 8 ground pins in the outer row. Figure 2(a) is the example of fine pitch contactor model where the blue pin is the signal pin and the brown pins are the ground pins. Figure 2(b) is the model after building the housing body using dielectric material Semitron ESd520. It is commonly used in electronic industrial as a housing material. Air-gap is required to provide the physical isolation between the pogo pin and the housing material. This is to mimic the mechanical design of an actual contactor, where air gap is necessary in between the pins and housing to allow the compression of the pogo pin.

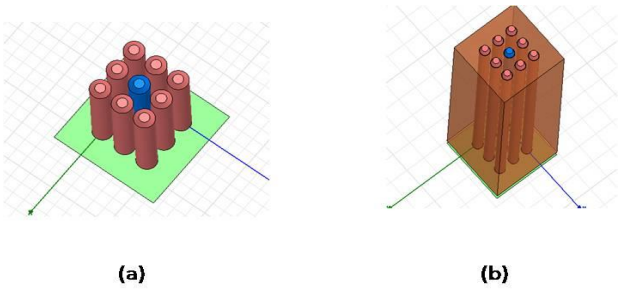

Figure 2: (a) 3 × 3 pin matrixes of fine pitch contactor model and (b) contactor model with housing material

The model of fine pitch contactor is completed at this step. It is followed by port setup to instantiate the magnetic field into the signal pins. The red circle on top of the signal pin in Figure 3(a) is the port that leads to the electromagnetic wave into the signal pin. Figure 3(b) shows the Perfect-E plane that shorted all the ground pins together. Perfect-E plane is a tool setting to define the part that becomes a perfect conductor. By adding this step, the losses from the Perfect-E plane will be minimised and the performance from the contactor pin can be truly assessed. The port is in between the probe tip and the Perfect-E plane. Similar port assignment method is implemented at the bottom side of the contactor.

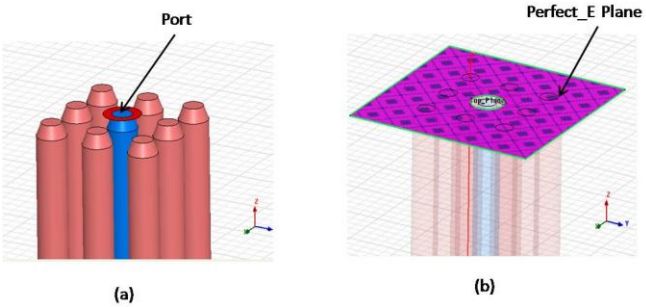

Figure 3: Port assignments on signal pinto define the input and output nodes of voltage source instantiated into channel

A vacuum box is required to isolate the contactor model from the conductive environment. Without the vacuum box, the entire contactor model will be electrically shorted together. The size of the vacuum box must be larger than the model and the allocation for the extra air-gap. Analysis setup is the last step of contactor modelling before proceeding to the system simulation.

B. Test Board Modelling

Fine pitch test board is required to enable the fine pitch contactor to be mounted on top and provides the electrical path at the same time for electrical functional testing. Because of the close distance between the contactor pins, the test board must be carefully designed to interface with the fine pitch contactor. The typical board design rules are no longer applicable to accommodate the challenges of fine pitch test board because of their limited spaces for trace routing.

The board trace routed out from landing pad can be either a microstrip or stripline. Microstrip was routed on the board surface, but it is more restrictive on the fine pitch design because of its narrow space in between the landing pads. In comparison to the stripline, it provides more flexibility for trace routing. Smaller via diameter is required to transit the signal from the top layer to the inner layer.

Figure 4 illustrates the 0.4 mm landing pad and the microstrip model. The demonstration of the microstrip model helps to show the challenges of board design at 0.4 mm pitch. Yellow landing pads are connected to the ground planes through the ground. The yellow landing pads will interface with the test contactor of the ground pins. The violet landing pad is the signal pad united with the microstrip. The radius of the landing pad is 0.127 mm with copper thickness of 1.4 mils to benchmark the fabrication standard with 1 oz (0.0347 mm) copper.

The test board topology was aligned with test contactor designed earlier. Therefore, it has one signal pin in the middle and surrounded by eight ground pins in the outer layers. To simplify the board design, only a single layer of dielectric material and a single layer of ground plane were considered. Typical dielectric material used in the industry, such as standard epoxy FR4 (Flame Retardant 4), Nelco 4000-13 and Roger4350 Hydrocarbon ceramic laminates were applied in the model. These dielectric materials are commonly used for printed circuit board (PCB) fabrication.

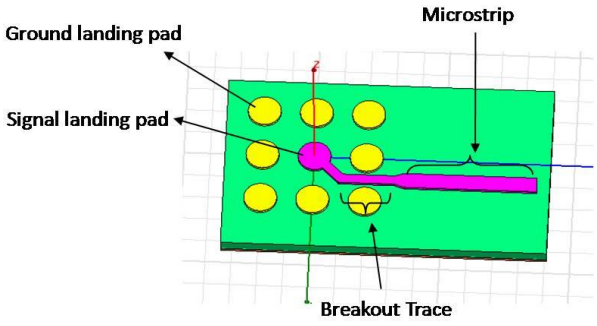

Figure 4: Fine pitch PCB design with microstrip

As illustrated in Figure 4, the microstrip passed through the landing pads that are narrower than the typical trace width. This is to avoid the trace from being shorted electrically with landing pads that is conductive. The landing pads were designed with 5 mils of radius at 0.4 mm pitch. It remains only the 10.75 mils for trace routing. By considering the minimum air-gap between the breakout trace and the landing pad, the allowed trace width is required to keep at around 3 mils. It leads to higher impedance than the typical microstrip at 5 mils trace width that controls the impedance at 50 Ω. Therefore, it is recommended to shorten the breakout trace in order to minimise the signal reflection.

The full channel schematic constructed with Advanced Design System (ADS) tools are shown in Figure 5(a) and (b). It is a system and circuit simulator used for compiling the electromagnetic models [12, 13], such as the model built to evaluate QFN and FPGA. The s-parameter files exported from HFSS were imported into the ADS circuit environment. These two full channel simulations were setup to compare the signals of Nelco 4000-13 and FR4. From the pin radius analysis, it is recommended to keep the radius to not exceeding 0.12 mm. Therefore, these two full channel simulations were using the same 0.12 mm fine pitch contactor model built with Semitron ESd520 housing material.

In Figure 5(a) and (b), SNP1 and SNP4 are the 2-port black boxes with the fine pitch contactor models. SNP2 and SNP5, on the other hand are the black boxes with imported model from the PCB landing pad simulation. The inclusion of TL1 and TL2 added to the extended microstrip with 100 mils channel length. They need the MSub to define the material properties of the PCB. For instance, the MSub1 defines the material properties of Nelco 4000-13, while the MSub2 defines the material properties of FR4. To form the 50 Ω microstrip, the dimension of the trace, such as the trace width at 8 mils and trace thickness at 1.4 mils for FR4 PCB dielectric material at thickness 5 mils can be calculated with any free impedance calculation tool. Termination (Term) is compulsory at both ends of the channels for signal integrity purpose. Otherwise, it will cause the reflection and signal distortion. The termination impedance in Figure 5(a) and (b) is 50 Ω to match the impedance of the channel.

When cascading the components in series, the polarity of the port connection must be correct. For instance, the output of the fine pitch contactor must be attached to the input of the PCB landing pad. If the polarity of the connection is incorrect, it will not cause the signal totally collapse and the graph plotted may not correlate to the performance of the components.

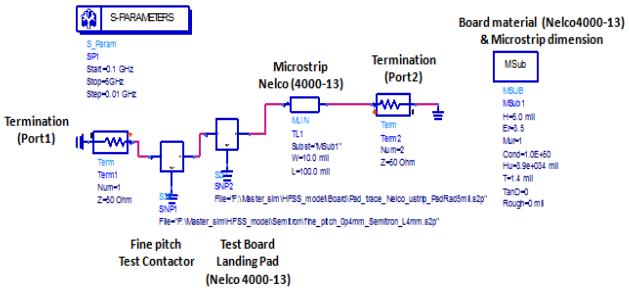

Figure 5 (a): Full channel simulation1: Fine pitch contactor with 0.12 mm pin radius and Semitron ESd 520 housing material; PCB landing pad constructed with Nelco 4000-13 material and pad radius at 5 mils

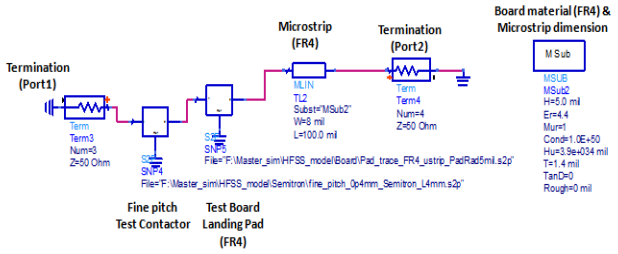

Figure 5 (b): Full channel simulation2: Fine pitch contactor with 0.12 mm pin radius and Semitron ESd 520 housing material; PCB landing pad constructed with FR4 material and pad radius at 5 mils

III. Results And Discussion

This section analyses the simulation result of system level simulation for QFN. To understand the signal behaviour of the system level with multiple electrical components, a full channel simulation is necessary. It is closer to the real hardware implementation, typically constructed by multiple passive, such as the trace and the active electrical components that are the relay or the transformer. In other words, the signal analysis of the full channel simulation is more realistic to represent the hardware functionality when it is powered up [14].

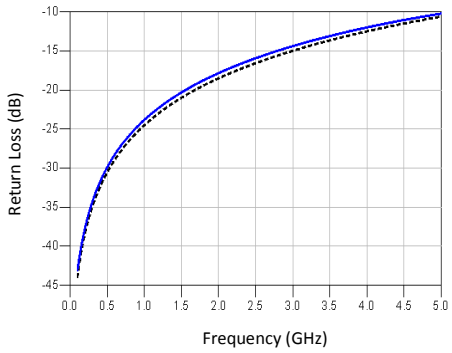

Figure 6(a): Full channel simulation – Return loss at fine pitch contactor (Dotted-line: Simulation 1 (S(1,1) = –16.567 dB at 2.5 GHz and –10.604 dB at 5 GHz) and solid-line: Simulation 2 (S(3,3) = –15.932 dB at 2.5 GHz and –10.221 dB at 5 GHz))

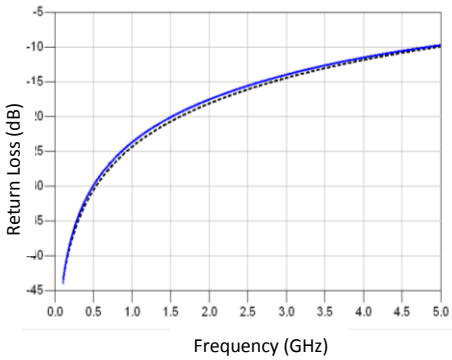

Figure 6(b): Full channel simulation – Return loss probed at board trace (Dotted-line: Simulation 1 and solid-line: Simulation 2)

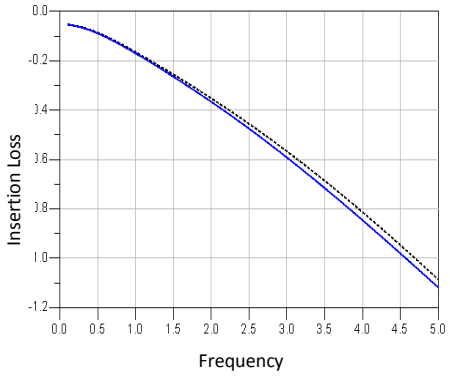

Figure 6(c): Full channel simulation – Insertion loss (Dotted-line: Simulation 1 (S(2,1) = –0.456 dB at 2.5 GHz and –1.087 dB at 5 GHz) and solid-line: Simulation 2 (S(4,3) = –0.476 dB at 2.5 GHz and –1.119 dB at 5 GHz))

Figure 6(a) shows the graph of the return loss plotted near the fine pitch contactor input terminal. The S(1, 1) represents the input node to the full channel with Nelco 4000-13 material while S(3,3) represents the input node to the full channel with FR4 material. Both lines in Figure 6 (a) show the return loss increases linearly up to 5 GHz. Because of the dielectric permittivity of FR4 at 4.4 is slightly higher than the Nelco 4000-13 at 3.5, the return loss of FR4 is relatively higher as well. These results are consistent to the work of Sigalov et al. [15] for QFN package with the lead pitch of 0.5 mm. The return loss of –10 dB at 5 GHz for the contactor was reported in reference to [15].

Figure 6(b) is the return loss plotted near the extended microstrip. S(2,2) represents the output termination of the full channel with Nelco 4000-13 microstrip, while S(4,4) represents the termination of the full channel with FR4 microstrip. Because of the non-symmetrical design between input and output terminals of the full channel, the observed return loss is slightly different in Figure 6(a) and (b). Nevertheless, the relationship of Nelco 4000-13 and FR4 are consistent, as shown in Figure 6(a) and (b).

Figure 6(c) is the insertion loss of the full channel simulation, as shown in Figure 5. They are measuring the full channel loss of signal at the termination point by referring to the signal instantiated into the full channel. S(2,1) measures the insertion loss of full channel with Nelco 4000-13 material, whereas the S(4,3) measures the insertion loss of full channel with FR4 material. As expected, the loss of FR4 is higher in comparison to Nelco 4000-13 as the dielectric permittivity of FR4 is higher. Figure 6(c) is consistent to the hypotheses made on Figure 6(a) and (b).

The results of the full channel simulation at 2.5 GHz and 5 GHz are summarised in Table 1. The return loss specification for the typical industrial standard is normally kept below –12 dB. Our simulation results for the design model of fine-pitch contactor show good agreement with the industrial standard at 4 GHz.

Table 1
Full Channel Simulation with ADS Schematic Simulator to Compare the PCB Material with Nelco 4000-13 and FR4

Model	Full Channel A (dB)		Full Channel B (dB)	
Frequency	2.5 GHz	5 GHz	2.5 GHz	5 GHz
Return Loss (contactor)	–16.567	–10.604	–15.932	–10.221
Return Loss (board trace)	–16.105	–9.953	–15.586	–9.752
Insertion loss	–0.456	–1.087	–0.476	–1.119

IV. CONCLUSION

This work emphasise the design of fine pitch test contactor and the fine pitch test board for QFN package. It is helpful to develop a robust test tooling with minimum signal losses in order to test the DUT correctly. Constructing the 3D models with high accuracy method is equally important. It ensures the hardware developed is within the design intent. System simulation should be performed to evaluate the signal interfacing when the electrical parts are formed together. It is closer to the actual hardware design. Our simulation results for fine-pitch contactor model fulfil the industrial applications, where the return loss is less than −12 dB at 4 GHz. By implementing early assessment during the design development, it helps to minimise the risk of getting system failure, which may consume unnecessary hardware cost and development time in the microelectronic industry.

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