A Multiband, Low Power and Low Phase Noise CMOS Voltage-Controlled Oscillator with NMOS Varactor for UWB Applications

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***Abstract*—A multiband low power and low phase noise LC-tank Voltage Controlled Oscillator (VCO) is designed for low band channels of the standard IEEE 802.15.4a. The LC-VCO uses the structure of complementary cross-coupled differential negative resistance and tank circuit, which contains varactor arrays for frequency fine-tuning and a spiral inductor. A method that uses resistor tail biasing for reducing the phase noise and the power consumption has been adopted. The circuit is fully designed in TSMC's 180 nm technology process. The oscillator output provides three center frequencies of 3.5, 4, 4.5 GHz with good phase noises of -113.784, -116.703 and -126.753 dBc/MHZ at 1 MHz offset, while it dissipates 9mW power energy. The proposed LC VCO not only set a good balance between low phase noise and low power consumption, but it is also a highly desired circuit for multiband wireless transceiver systems, which are the major contributions of this proposed design.**

***Index Terms*— LC VCO; Phase Noise; Multiband; Varactor; Low Power.**

I. INTRODUCTION

With the wide variety of wireless communication technologies, multi-standard communication systems have received an increased interest among researchers. In this context, the Ultra-wideBand (UWB) technology has defined the IEEE 802.15.4a as a multi-standard, which splits the overall frequency band into UWB sub-band whose bandwidth is 528 MHz [1]. It allows designing transceivers with low power consumption, low complexity and high speed transmission by taking the benefits from the Impulse Radio (IR) technique [2].

This approach requires circuit designers to adopt a more compact and cost effective multiband oscillator, which is a key building block in any multiband transceiver used for carrier frequency synthesizes for up-convert and down-convert signal. To design multiband VCO, several methods have been developed, such as using switched differential inductor as proposed in [3] that generates multibands of 0.9, 1.8, 2.4 and 4.5 GHz. However, this technique increases the chip area and the power consumption due to the use of extra passive inductors.

Another way to achieve multiband LC VCO is to use switchable varactors and switchable capacitors block as reported in [4]. The proposed multiband VCO establishes a wide tuning range frequency from 4.5 to 6.5 GHz. with an average phase noise performance.

Recently, [5] proposes a wide tuning LC VCO using a tunable active inductor to generate an output frequency of 5.5GHz. Obviously, it is a compact VCO with easy integration; however, it has unsatisfactory phase noise of -81dBc/MHz.

In designing the LC VCO, the phase noise appears as the most challenging task because it reflects the quality and performance of information transfer. It is generally recognized that the major contributor to overall phase noise in LC VCO is the tail current source [6]. Thermal noise, which is added by the biasing circuit, is down converted and flicker noise is up converted during the mixing action resulting in increasing the phase noise. Thus, removing the tail biasing source seems as a solution to improve the phase noise criterion as reported in [7] although it considerably increases the power consumption in nominal conditions.

In turn, the strong combination of low power and low phase noise surges circuit designers to create a spectacular field of research toward the techniques used to enhance these metrics.

[8] uses the harmonics filter technique to filter out the second harmonic of the tail current noise. This approach incorporates a LC network in between switching transistors common node and tail current source. Hence, it allows the output noise to be reduced significantly to-130 dBc/Hz without increasing the power consumption. However, it presents the drawback of an increased chip area due to the use of additional inductors, and the lack of control circuit to widen the frequency tuning range.

Another approach based on using the tail current shaping method is demonstrated in [6]. It consists of current injection and two paths for current disconnection to reduce strongly the phase noise. This circuit proves as a good phase noise performance of-127 dBc/Hz from the carrier frequency of 1.65 GHz at the expense of increased circuit complexity and limited number of frequency bands.

Furthermore, [9] develops a novel biasing technique for LC VCO based on using a feedback loop and LD to generate an output current. This solution ensures the regulation of the bias current in order to eliminate the current source, as a consequence improving the phase noise performance. It works at around 2.25 GHz carrier frequency and achieves-127.2 dBc/Hz phase noise. However, this circuit suffers from increased complexity design and inability to generate various carrier frequencies.

Another alternative solution depicted in [10] consists of using a cross-coupled series LC resonator instead of using

parallel LC resonator. This technique generates a rectangular shaped voltage at the drain nodes of the switching pair. Thereby, it enhances the spectral purity output by amplifying the fundamental frequency and removing the noise and harmonics components. The proposed LC VCO enhances significantly the phase noise which is -126 dBc/Hz at 3.56 GHz carrier frequency without degrading the power consumption. The main drawback of the proposed method is that it is not able to provide several carrier frequencies.

Obviously, these structures meet the stringent requirements of low phase noise and low power consumption; however, they are not able to support a variety of wireless communication systems.

To overcome this bottleneck, the proposed LC VCO uses varactors bank in the tank to maximize both the tuning range and operating frequency. Moreover, it replaces the tail current source by a tail resistor biasing to reduce both phase noise and power consumption.

The resistor tail biasing serves as a source damping device to eliminate excess 1/f noise caused by the differential pair transistor when it is carefully chosen [11]. Furthermore, an adequate adjustment of this resistor can control the current consumption to avoid the oscillator from drawing current as much as it can.

This paper proposes the differential cross coupled LC VCO uses switched varactors banks structure and a resistor tail biasing to achieve a wide frequency tuning range, low phase noise and low power consumption. Following Section I, Section II presents the basic concepts about the proposed complementary cross-coupled LC oscillator topology and the C-V characteristics of an MOS varactor. In Section III, simulation results of the proposed circuit and comparison with other related works are presented. Finally, conclusions are drawn in Section V.

II. CIRCUIT DESIGN

A. Basic Concept

A complementary cross-coupled LC CMOS voltage controlled oscillator is shown in Figure 1. This structure is characterized by a good phase noise performance and easy start-up [12] condition by reducing the output signal amplitude. It is made up of active circuit, switched varactors block, passive inductor and tail resistor biasing. In this configuration, the active circuit consists of cross coupled pair NMOS and PMOS devices that are (Mn1, Mn2) and (Mp1, Mp2). This topology allows transistors to share the same bias current, which consequently leading to doubling the negative resistance for the same power consumption.

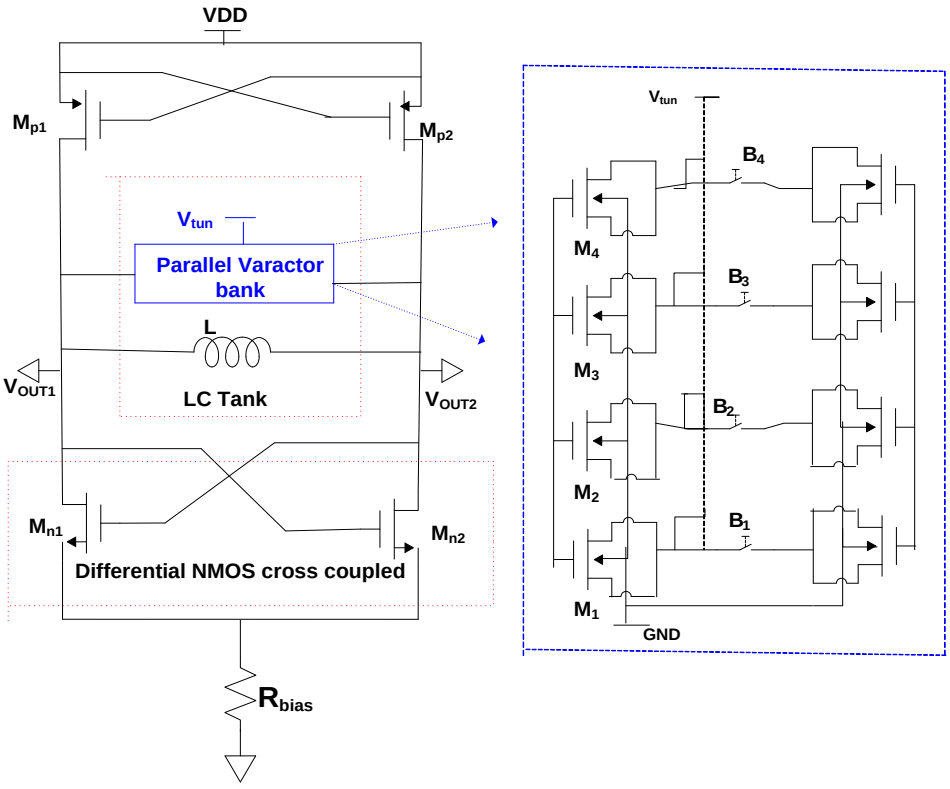


Figure 1: The circuit schematic of the proposed LC VCO

To guarantee that the circuit can enable sustained oscillation, the total negative resistance should be able to compensate the losses in the LC tank. The latest can be expressed as a parallel combination of the NMOS and PMOS pair's negative resistance, $R_{in,n}$ and $R_{in,p}$ as [13]:

$$R_{negative} = R_{in,n} // R_{in,p} = -\frac{2}{G_{mn} + G_{mp}} \quad (1)$$

Taking account that these devices operate in the saturation region, the drain current will be given as below:

$$I_{dc} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right)^2 \quad (2)$$

Where μ_n , C_{ox}, V_{gs} and V_{th} are the surface mobility of electron, the gate oxide capacitance, the gate to source voltage and the threshold voltage of NMOS transistor,

respectively. Thus, the transconductance of each transistor can be expressed as:

$$G_m = \frac{\partial I_{dc}}{\partial V_{gs}}\Big|Q_{point}\Big\rangle = C_{ox}\mu_0\left(\frac{W}{L}\right)\left(V_{gs}-V_{th}\right) \quad (3)$$

In this proposed design, the tail current source is completely suppressed to improve the phase noise. Adding a tail biasing resistor at the common source point is used as an alternative solution to meet the issue of increased power consumption. This technique has great effect on enhancing the VCO performances.

First, the added resistor allows a flexible control of impedance at the common source to maintain the circuit working in current limited region, resulting in decreasing the overall power consumption.

Second, this technique eliminates extra noise generated by biasing circuit. Consequently, this technique provides great features for improving both phase noise and power consumption. As a result, this circuit can achieve lower power consumption and generates sufficient negative resistive to compensate the losses of LC tank core.

B. Proposed Switched Varactor Bank

Integrated voltage controlled capacitance (varactor) is a key building block of the VCO used to generate the fine tuning frequency. PMOS varactors are widely used for linear devices like amplifiers. However, for nonlinear devices like mixers and oscillator, NMOS varactors are more desirable because they work faster due to their mobility of electrons, which is nearly two times more than the mobility of holes [14]. As a result, N- channel device has lower size and lower impedance of an equivalent P- channel device. Hence, NMOS varactor is selected in this work for a good start-up condition and high performance. By connecting the three terminals of MOS transistor drain, source and bulk (D, S, B) together, a variable capacitance appears depending on the voltage between bulk and gate. The characteristic C-V of NMOS varactor, which is formed with 67 gate fingers, each finger having a gate length of 0.18 µm and a gate width of 1.5 µm, is illustrated in Figure. 2.

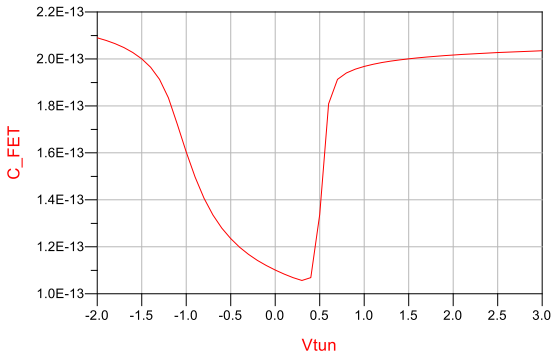


Figure 2: Characteristic C-V of NMOS varactor

Thus, three major regions are displayed including accumulation, depletion and inversion.

Inversion mode is the best candidate due to its superior performance in terms of maximum capacitance value, phase noise characteristic and easy implantation, which is done by connecting together the remaining drain and source, while the bulk is connected to the ground.

This proposed design includes multi-symmetrical body-bias varactors connected in parallel to increase the tenability of the proposed oscillator. The amount of capacitance is changed by varying the control voltage Vtun. To work under a precise frequency, the varactor block is digitally controlled by a binary array of autonomous control signals.

Hence, the resonance frequency of the tank is given as:

$$f_0 = \frac{1}{2\pi\sqrt{L_{\tan k}C_{\tan k}}} \quad (4)$$

where $L_{\tan k} = L$ and $C_{\tan k} = \frac{C_{\text{var}}}{2} + C_p = C'_{\text{var}} + C_P$,

in which C_p and C_{var} are the total parasitic capacitance and varactor capacitance.

Moreover, the tuning range (TR) criterion can be expressed as [4]:

$$TR = 2\times\frac{f_{\max} - f_{\min}}{f_{\max} - f_{\min}}\% \quad (5)$$

where $f_{\max}$ is the maximum oscillation frequency and $f_{\min}$ is the minimum oscillation frequency.

By using (4) and (5), the tuning range is given by:

$$TR = 2\times\frac{\left(\sqrt{C'_{\text{var,max}}+C_p}\right)-\left(\sqrt{C'_{\text{var,min}}+C_p}\right)}{\left(\sqrt{C'_{\text{var,max}}+C_p}\right)+\left(\sqrt{C'_{\text{var,min}}+C_p}\right)} \quad (6)$$

It is noted from equation (6) that the tuning range depends on the highest value and the lowest value of the MOS varactors. To determine accurately this great influence, TR expression can be simplified as:

$$TR = 2\times\frac{\left(\sqrt{\frac{C'_{\text{var,max}}}{C'_{\text{var,min}}}+\frac{C_P}{C'_{\text{var,min}}}}\right)-\left(\sqrt{1+\frac{C_P}{C'_{\text{var,min}}}}\right)}{\left(\sqrt{\frac{C'_{\text{var,max}}}{C'_{\text{var,min}}}+\frac{C_P}{C'_{\text{var,min}}}}\right)+\left(\sqrt{1+\frac{C_P}{C'_{\text{var,min}}}}\right)} \quad (7)$$

Hence, to maximize the tuning range it is demanded to increase the varator ratio $C'_{\text{var,max}} / C'_{\text{var,min}}$ and reduce the parasitic capacitance C_P.

According to the above expression, we can conclude that the oscillation frequency is fixed by MOS varactors and inductor in LC resonator.

Table 1 shows the amount of transistors and values of passives elements.

Table 1
Values for Passive Elements and Transistor's Aspect Ratio

Components	Specifications
$M_1;(W/L)_1$	30µm/0.18µm
$M_2, M_3, M_4;(W/L)_{2,3,4}$	100µm/0.18µm
$M_{n1}, M_{n2};(W/L)_{n1,n2}$	30µm/0.5µm
$M_{p1}, M_{p2};(W/L)_{p1,p2}$	90µm/0.5µm
R_{bias}	200Ω
L	2 nH

III. SIMULATION RESULTS

The multiband low-phase-noise VCO has been implemented in 0.18µm CMOS technology. The center frequencies are about 4.5, 4 and 3.5 GHz, which can be simulated with Advanced Design System (ADS) software by using transient analysis, DC simulation, phase noise simulation and HB simulation.

To generate the three center frequencies, the inductance value is 2nH, and the total equivalent capacitance is in the range of 1.033pF to 0.625pF.

Figure 3 (a), (b), (c) and (d) show the simulated output waveform and its spectrum at frequency 3.5 GHz. It proves that the proposed circuit can enable sustained oscillation with an acceptable start-up time of 8ns.

For the lower frequency, it is needed to use the largest capacitance value; consequently, the four parallel varactors are used with an adequate control of Vtun voltage, which is fixed at 0.5V.

The amount of output power spectrum is -1.569 dBm and the phase noise is about -113.784 dBc/Hz at 1 MHz offset from carrier frequency f_{osc} of 3.5 GHz.

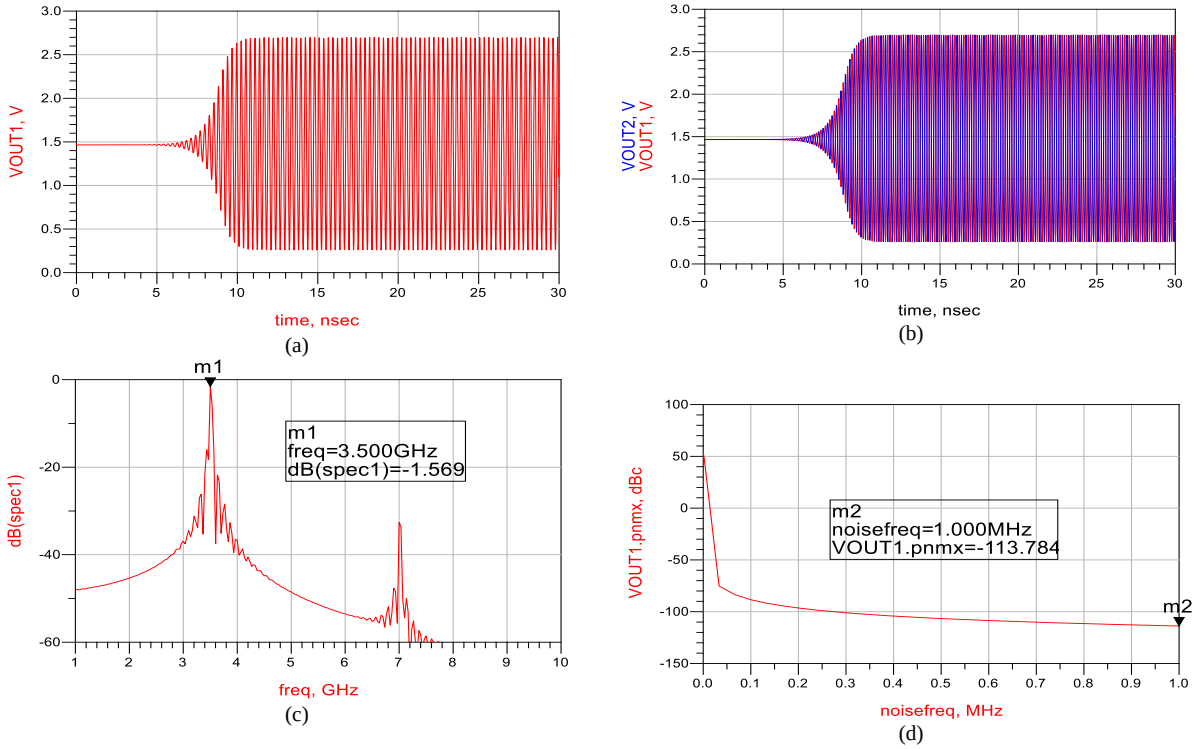
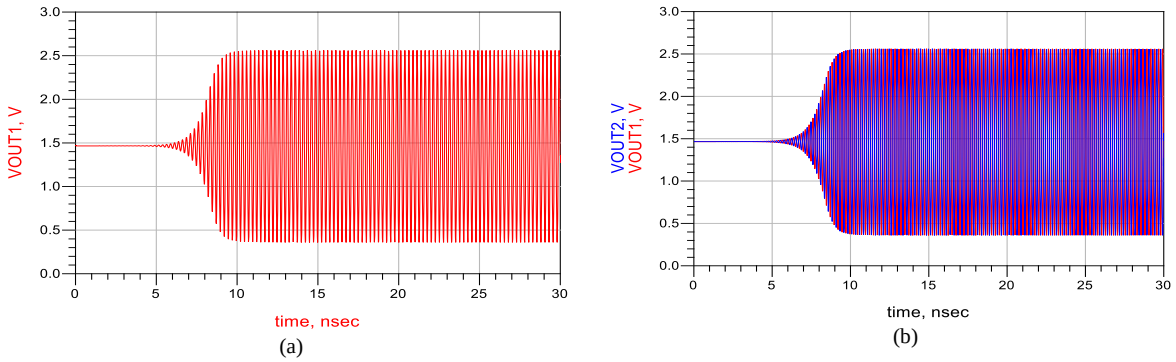


Figure 3: (a) Single ended transient response of VOUT1, (b) differential transient response, (c) phase noise response, (d) frequency spectrum of the LC-VCO at frequency 3.5 GHz.



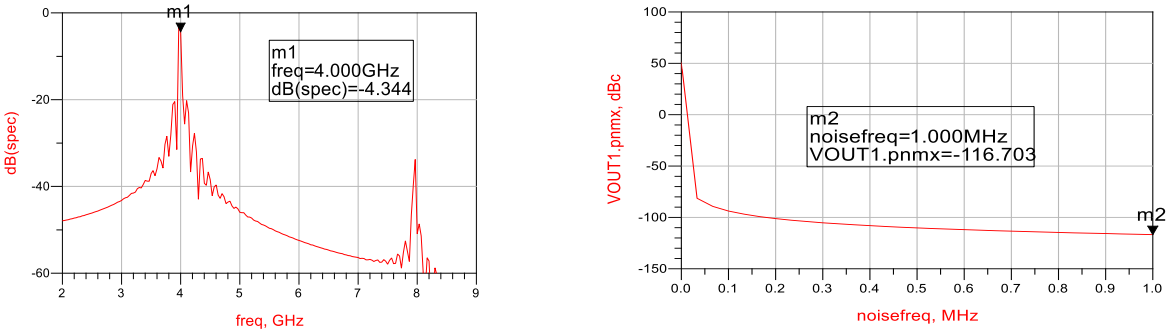


Figure 4: (a) Single ended transient response of VOUT1, (b) differential transient response, (c) phase noise response, (d) frequency spectrum of the LC-VCO at frequency 4 GHz.

As shown in Figure 4, the oscillations are able to sustain to guarantee the easy start up criterion at the center frequency of 4 GHz. To generate this desired frequency, only two NMOS varactors are used by setting the Vtun voltage of the last varactor at 1V. The amount of output power spectrum is -4.344 dBm and the phase noise is about -116.703 dBc/Hz at 1 MHz offset.

For the higher frequency of 4.5 GHz, it is demanded to use the smallest capacitance value. Hence, only one NMOS varactor is used with a settled Vtun at 2V. The amount of output power spectrum is -3.152 dBm and the phase noise is about -126.753 dBc/Hz at 1 MHz offset, as illustrated in Figure 5.

Notably, the phase noise increases as the number of varactors decreases and as the varactor gain decreases.

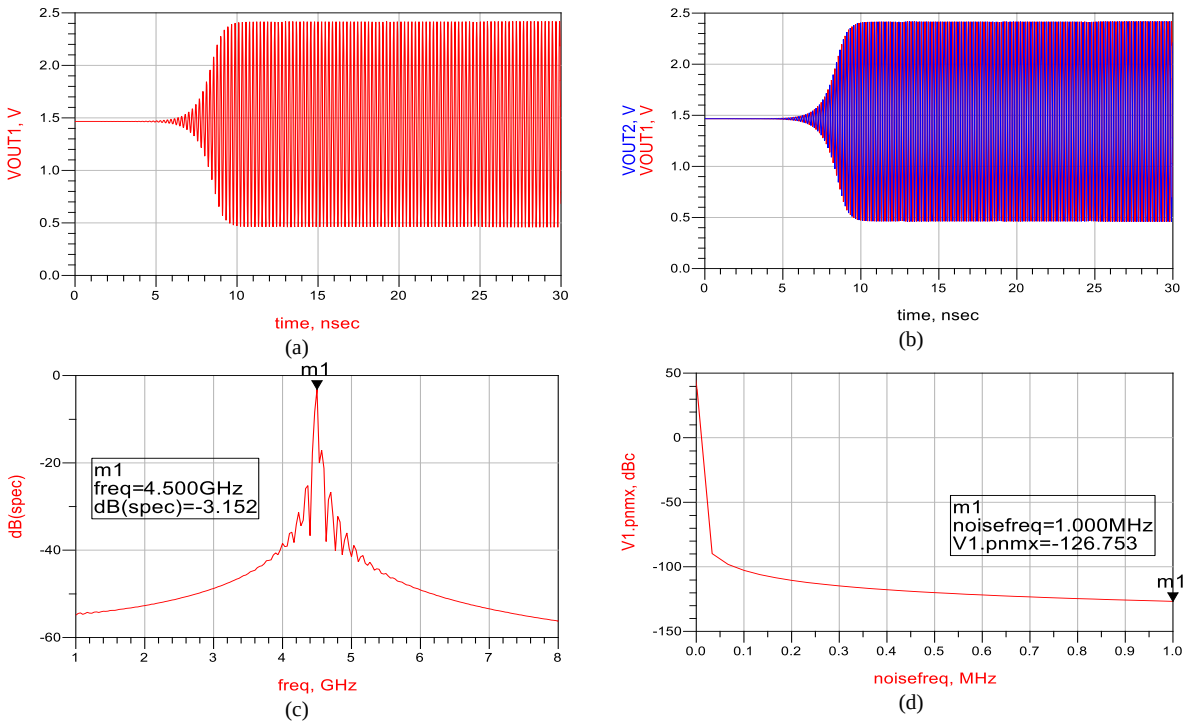


Figure 5: (a) Single ended transient response of VOUT1, (b) differential transient response, (c) phase noise response, (d) frequency spectrum of the LC-VCO at frequency 4.5 GHz.

The significant improvement in both phase noise and power consumption resulting from the resistor biasing has a sharp effect in enhancing Figure of Merit (FOM). This metric measures the VCO performance and is defined as [6]:

$$FOM = L\{f_{offset}\} - 20\log\left(\frac{f_c}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (8)$$

where L {foffset}, PDC, are the phase noise at offset frequency (*foffset*) from the carrier frequency of *fc* and the DC power consumption of VCO in mW.

Table 2 summarizes the performance of the proposed LC VCO with recently published works. It shows good performances in terms of low power consumption, good phase noise and wide band tuning. Moreover, it fulfills the stringent requirement of miniaturization by reducing the number of circuit components.

Table 2
Performance Comparison of Multiband LC VCO

REFERENCE	Technology (µm)	Frequency range (GHz)	Phase noise at 1MHz offset (dBc/Hz)	Power consumption (mW)	FOM (dBc/Hz)	YEAR
This work	0.18	3.5 4 4.5	-113.784 -116.703 -126.753	9	-175.2 -179.2 -190.2	2018
[3]	0.18	0.9 1.8 2.4	-133 -135 -125	16.2	-180 -188 -181	2018
[6]	0.18	4.5 1.65	-127 -127.7	4.1	-188 -186	2018
[9]	0.065	2.25	-127.2	5.6	-183.8	2017
[15]	0.18	0.9 1.8 2.4	-104.7 -107.7 -101.7	5.3	-156.3 -164.5 -160.3	2017
[16]	0.18	10.6	-107.779	9.8	--	2017
[10]	0.065	3.56	-126	5.6	--	2014

VI. CONCLUSION

This paper presents a low power, low phase noise multi-band LC VCO using a switched Varactor bank in a standard TSMC 0.18µm CMOS technology. The proposed LC VCO is achieved to operate at 3.5, 4, 4.5 GHz center frequencies. The phase noises are about -113.784 dBc/Hz, -116.703 dBc/Hz and -126.753 dBc/Hz at 1 MHz offset from carrier frequency *f*osc of 3.5GHz, 4 GHz and 4.5 GHz, respectively, while consuming 9mW of energy. Since the proposed LC VCO uses a switched varactors bank, which covers from 3 to 4.5 GHz, it can be used as a crucial block of multi-standard application. This work complies with the current debate to produce multifunction wireless device; hence, making the proposed LC VCO design as a challenging block for multiband and low power consumption wireless transceiver.

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