Invited paper

Advanced compact modeling of the deep submicron technologies

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Abstract — The technology of CMOS large-scale integrated circuits (LSI's) achieved remarkable advances over last 25 year and the progress is expected to continue well into the next century. The progress has been driven by the downsizing of the active devices such as MOSFETs. Approaching these dimensions, MOSFET characteristics cannot be accurately predicted using classical modeling methods currently used in the most common MOSFET models such as BSIM, MM9 etc, without introducing large number of empirical parameters. Various physical effects that needed to be considered while modeling UDSM devices: quantization of the inversion layer, mobility degradation, carrier velocity saturation and overshoot, poly-depletion effects, bias dependent source/drain resistances and capacitances, vertical and lateral doping profiles, etc. In this paper, we will discuss the progress in the CMOS technology and the anticipated difficulties of the sub-0.25 μm LSI downsizing. Subsequently, basic MOSFET modeling methodologies that are more appropriate for UDSM MOSFETs will be presented as well. The advances in compact MOSFET devices will be illustrated using application examples of the EPFL EKV model.

Keywords — ultra deep submicron (UDSM) technology, compact modeling, EKV MOS transistor model, MOSFET, matching, low power and RF applications.

1. The ultra deep submicron CMOS technology developments

Over the last 25 years, technology of CMOS large-scale integrated circuits (LSI's) has achieved advances stage. However, even before the downsizing of the LSI devices reaches its fundamental limits this process is expected to encounter severe technological and economic problems when the minimum features of the active devices are being shifted to dimensions below sub-quarter micron, the so-called ultra deep submicron (UDSM) technology. The downsizing allowed minimizing geometry of transistor. The number of the transistors in a chip increases and the functionality, switching and operation speed of the LSI's circuit is improved. Indeed, these continuous technology improvements are correctly predicted according the Moore's law [1]. Moreover, at the research level, many institutions have already reported successful fabrication of sub-0.1 μm MOSFET devices operation at room temperature. As indicated in Fig. 1, for most aggressively scaled DRAM, the integration scale will reach 256 Gbit by the year 2010. There seems to be no physical limitation for feature size down to 25 nm. Furthermore, there are no apparent fundamental limits for Si, in terms of tunneling and other quantum mechanical effects

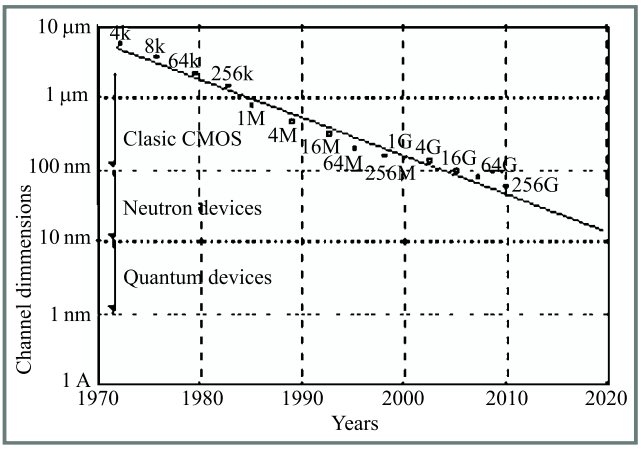


Fig. 1. Trends of the MOSFET gate length scaling in advanced LSI technologies.

for the features size. The challenges to surmount these problems encompass almost all aspects of the device physics, processing, and integration including interconnection and patterning technologies. In the long term, as the semiconductor feature size reaches the atomic limit, alternative means for computation will be needed to further increase the information throughput.

The great success has been achieved with the scaling methods in miniaturizing MOSFETs down to gate lengths of 0.18 μm at the LSI product level and 0.01 μm at the research level, respectively. However, the actual scaling of the parameters has been different from that originally proposed [3] and is shown in Table 1. The major difference is the supply voltage reduction. The supply voltage was not reduced in the early stage of the LSI generation in order to keep a compatibility with the supply voltage of conventional systems and to obtain higher operation speed at higher electric fields. The supply voltage started to decrease at the level of 0.5 μm CMOS processes because the electric field across the gate oxide would have exceeded value of 4 MV/cm, which has been regarded as the maximum limitation in terms of time-dependent dielectric breakdown and hot-carrier induced degeneration for short channel transistors, generally speaking reliability issues of the MOSFET devices. Now, however, it is not easy to reduce supply voltage because of the difficulties in reducing the threshold voltage of the MOSFET. Too small threshold voltage leads to significant large subthreshold leakage current and forcing designers to design IC operating in subthreshold (moderate inversion) regime. The supply voltage higher then expec-

Table 1
Main EKV v2.6 intrinsic model parameters for first and second order effects

Name	Description	Default	Unit
COX	Gate oxide capacitance	0.7E-3	F/m^2
XJ	Junction depth	0.1E-6	m
VTO	Nominal threshold voltage	0.5	V
GAMMA	Body effect factor	1.0	$V^{1/2}$
PHI	Bulk Fermi potential (2)	0.7	V
KP	Transconductance parameter	50E-6	A/V^2
E0	Mobility reduction coefficient	1E12	V/m
UCRIT	Longitudinal critical field	2E6	V/m
DL	Channel length correction	0.0	m
DW	Channel width correction	0.0	M
LAMBDA	Depletion length correction	0.5	-
LETA	Short channel effect coefficient	0.1	-
WETA	Narrow channel effect coefficient	0.1	-
Q0	RSCE peak charge density	0.0	A s / m^2
LK	RSCE characteristic length	0.3E-6	m
IBA	First impact ionization coefficient	0.0	1/m
IBB	Second impact ionization coefficient	3E8	V/m
IBN	Saturation voltage factor for impact ionization	1.0	-

ted form the original scaling is one of the reasons for the increased distributed power.

An increase of the number of transistors in a chip by more than factor of K^2 is another reason for the power increase. In fact, the transistor size decreased by a factor of 0.7 while the transistor area decreased by factor of 0.5 for every generation. Present complex digital designs cannot wait for the downscaling and thus the actual chip size increased by a factor of four, more than predicted by standard scaling rules. Introducing new technologies such as multilayer interconnections, double polysilicon and further complicated cell structures for the memories partially solves the problem of insufficient IC area.

Recent progress in the CMOS scaling has been achieved using improved DUV lithography tools. Originally, targeted at the 0.35 μm devices, these tools were successfully introduced at 0.25 μm level and are being used in the current 0.18 μm generation. The use of these tools is projected at least for 0.15 μm devices. Further progress is required to adapt popular reticle enhancement technique (RETs), proximity correction and phase shift mask (OPC/PSM) to obtain improved packaging densities. ¿From the extrapolation of traditional scaling, UDSM devices are expected to have excellent drive current and the projected performance suggests circuits operating at frequencies up to 10 GHz. On the other hand, one should remember that there are serious technological and economic limitations of further, accelerated improvements of the standard CMOS technologies and the transistor performance could be, to some extent, compromised. In aggressively sized technologies, oxide scaling leads to rapidly increased gate currents, regardless of the oxide quality. Further improvements in the reduction of the gate tunneling currents require the use of alternative gate dielectric materials. High-k materials are good candidates to replace standard gate oxides. Similarly, potential solutions (e.g. low energy implantation) for advanced source/drain extension engineering, which would approach the physical limit of ultra-shallow but low-resistance junctions, have been discussed in the literature. Table 2 lists scaling problems of the advanced LSI devices and possible technology and architecture solutions.

2. Challenges of the compact modeling

As previously mentioned, in aggressively scaled UDSM technologies, the gate oxide thickness is approaching the inversion layer thickness resulting in high fields at the silicon surface. These high electric fields at the surface cause various physical effects such as quantization of accumulation/inversion layers (QM effect), carrier saturation velocity and velocity overshoot that must be taken into account while developing UDSM transistor model. Other physical effects, which are additional to the short channel effects are polysilicon gate depletion effect, impact of nonuniform channel doping profile on threshold voltage, bias dependent source/drain resistances and capacitances, drain induced barrier lowering (DIBL) are relevant to UDSM modeling, as well.

First of all, the regional approach, which is the most frequently used that combines different equations for different regions of device operation and then piece them together by smoothing function to avoid eventual discontinuities. There are a number of advantages. Firstly, it allows for a simple implementation of the short channel effects using empirical relations. Then it offers relatively fast computation time, which is not always true for other models like BSIM3. Nevertheless, it has some disadvantages such as ignoring the

Table 2
Parameter scaling

Ideal Scaling Rules		Limiting factor	Example values
Parameter	Scale		
Gate length (L_g)	$1/K$	Lithography	0.18 µm
Gate width (W_g)	$1/K$	Lithography	
Gate area (A_g)	$1/K^2$	Lithography	
Oxide thickness (t_{ox})	$1/K$	Defects, direct tunneling	5 nm
Gate capacitance ($C_{ox} \sim A_g/t_{ox}$)	$1/K$		
Gate charge ($Q_g \sim C_{ox}V$)	$1/K^2$		
Propagation delay (t_{pd})			20 ps
Clock frequency ($f \sim 1/t_{pd}$)	K	Power consumption, circuit speed	600 MHz
Channel doping (N_{sub})	K	Junction leakage current	10^{18}cm^3
Junction depth (x_j)	$1/K$	Sheet resistance	0.04 µm
Threshold voltage (V_{th})	$1/K$	Off leakage current	0.4 V
Supply voltage (V_{dd})	$1/K$	Lower V_{th}, circuit speed	2.7 V
Number of transistors (n)	K^2	Power consumption, Circuit speed	3-22 M
Chip size ($\sim nA_g$)	1	Yield	3 cm^2
Power ($1/2fnCV^2$)	1	Heat generation	10 W

inversion layer thickness and consequently the quantization of the inversion layer. This leads to wrong deduction of the non-physical gate oxide thickness which in turn results in inaccurate capacitance simulations. The model scalability over full range of available device geometries (W, width/L, length) is rarely possible without so-called parameter binning. The binning is artificially introduced into the model structure and usually generated discontinuities across the boundaries. Most common way of including L and W dependence on a parameter P is:

$$P = P_0 + \frac{P_1}{L} + \frac{P_2}{W}$$

assuming that the model parameters are inversely proportional to L and W. However, a better binning scheme have been proposed in [4]:

$$P = P_0 + P_1\left[\frac{1}{L} - \frac{1}{L_{ref}}\right] + P_2\left[\frac{1}{W} - \frac{1}{W_{ref}}\right] + \\ + P_3\left[\frac{1}{L} - \frac{1}{L_{ref}}\right]\cdot\left[\frac{1}{W} - \frac{1}{W_{ref}}\right],$$

where L_{ref} and W_{ref} are large reference device length and width, respectively.

To model UDSM technology processes, more and more parameters are introduced into models based on the regional approach. The increased number of adjustable parameters complicated the parameter extraction process and model usage.

Most of above mentioned shortcomings of the regional based models are solved using surface potential approach. The full operation range of the MOSFET device from weak inversion through moderate to strong inversion is described in a physical and continuous way. Artificial smoothing functions and parameter binning are not necessary. This physical description of the MOSFET characteristics is also most accurate because gate bias dependence of the surface potential is taken into account in the continuous manner. Unfortunately, the biggest disadvantage is that the surface potential needs to be solved at each bias point interactively due to the implicit nature of the bias dependence of the surface potential. Thus, the drawback of this approach is computation time because of the iteration procedure.

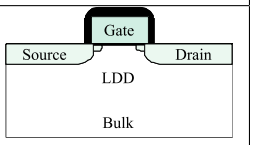
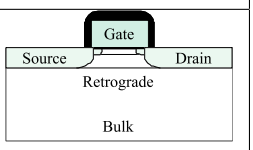
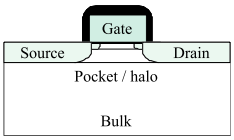
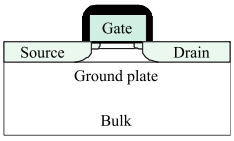
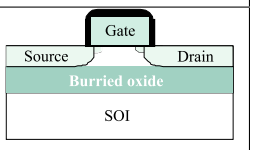
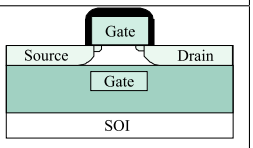
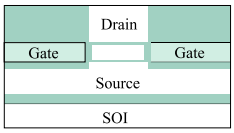
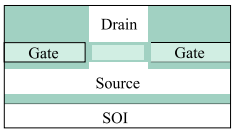
The third approach is the hybrid approach, which combines regional and surface based methods to take advantages of both. The hybrid methodology allows the incorporation of all the essential physics of scaled UDSM MOSFET devices such as short channel and narrow width effects, reverse short channel effect (RSCE), bias dependent source/drain resistances, and channel length modulation (CLM). Successful modeling of UDSM devices with channel length of 0.1 µm has been reported.

Growing complexity of the most commonly used compact models (including recent versions of BSIM [5], MM9 [6] and EKV [7]) can be clearly visible in Fig. 2, which shows also the increase of the number of the intrinsic DC parameters. This figure indicated that models are becoming more and more empirical rather than physical in the their description.

3. The EPFL EKV MOSFET model

A detailed description of the EKV v2.6 model formulation can be found in [7–10]; for reference some basic model equations are presented here. One of the main features of the EKV model is the continuity of the large- and small-signal characteristics and its derivatives from weak through moderate to strong inversion. The model accounts for many of the important second order effects, by using only a small set of the intrinsic parameters (see Table 3), most of which have similar meanings as in well-known Spice models.

Table 3
Scaling problems and possible technology solutions

Scaling problem	Solution	Technology	Architecture
Hot electrons degenerate gate oxide and reduce device reliability	Reduction of the high electric potential drops in drain region	Additional lightly doped drain (LDD) ion implantation	
Subsequent increase of the channel doping increase S/D capacitancs	Decuppling of both parameters thru additional vertical implantation in the substrate	The retrogate well using additional implantation in the substrate	
Parasitic leakage currents in the substrate (punch through). The potential barrier at S/D junction is reduced by high potential (DIBL)	Higher doping concentration increases S/D potential barrier	Introduction of the pocked/halo implantation step	
Complex and difficult to control implantation steps introduces large variations of the process related device parameters	Substitution of the ion implantation by well controlled thin layer deposition	Improved MBE and/or CVD process steps	
Bulk MOSFET are difficult to scale because of very complex implantation profiles	Substitution of the classic pn-junction by a insulator barrier	Bulk Si wafers are replaced by SOI wafers with buried oxide	
Limit of the optical photolithography (alternative lithography systems are not ready)	Introduction of the 3D planar processes (Double Gate MOST)	Buried Si-SiO_2 interface as additional channel region	
Lithography of the planar structures are not more possible (constant channel length)	Lithography independent channel scaling using thin atomic layers	Vertical Double Gates are defined channel by thin atomic layers	
Classic MOST are not scalable. MOST operation is dominated by quantum effects	New quantum level devices (i.e. based on the tunnel barrier)	Multi tunnel junction (MTJ) technologies	
Atom level scaling (?)	Optimum of the Si technology is reached	Additional improvements of the IC performance are possible only on an algorithmic level.	

Referring the gate, source and drain voltages, V_G, V_S, and V_D respectively, to the local substrate preserves the intrinsic device symmetry. The model uses a threshold voltage VTO corresponding to the gate voltage such that the inversion charge forming the channel is zero in equilibrium ($V_D = 0$ and $V_S = 0$). A pinch-off voltage V_P corresponds to the value of the channel potential for which the inversion charge becomes zero in a non-equilibrium situation (Fig. 3). The pinch-off voltage is directly related to the gate voltage:

$$V_P = V'_G - PHI - \gamma' \left[\sqrt{V_G + \left(\frac{\gamma'}{2} \right)^2} - \frac{\gamma'}{2} \right], \qquad (1)$$

$$V_G = V'_G - VTO - \Delta V_{RSCE} + PHI + GAMMA \sqrt{PHI}. \qquad (2)$$

The pinch-off characteristic measured at constant specific current in the transistor biased in saturation is a kernel of the EKV v2.6 parameter extraction [11, 12]. In the current formulation of the EKV v2.6 model the modified body effect factor accounts for both short and narrow channel effects:

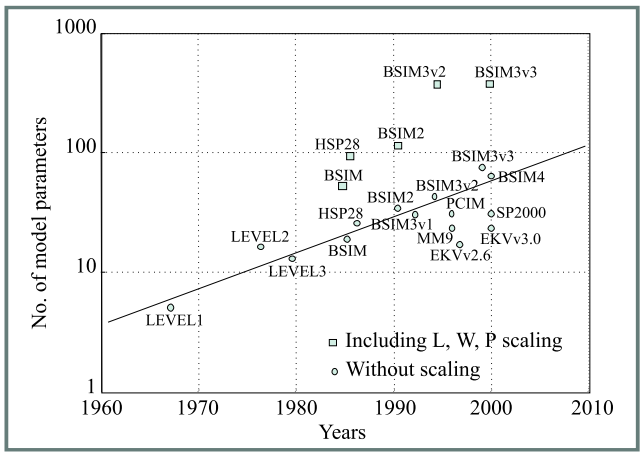


Fig. 2. Number of DC current parameters versus the year of the model introduction. Most recent versions of the BSIM, MM9 and EKV models are included.

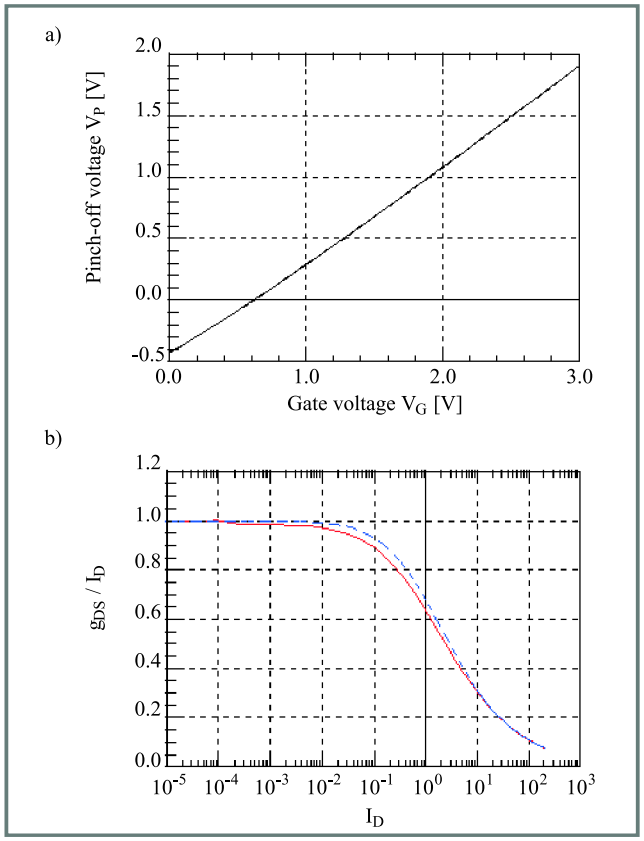


Fig. 3. (a) The pinch-off voltage (V_P vs V_G) characteristic for a NMOS transistor of a 0.5 µm technology. (b) Measured and simulated transconductance to normalized drain current (g_{DS}/I_D) ratio from weak through moderate to strong inversion.

$$\gamma' = GAMMA + \frac{\varepsilon_{Si}}{COX}\left[\frac{3\cdot WETA}{W+DW}\sqrt{PHI+V_S} + \right.$$
$$\left. -\frac{LETA}{L+DL}\left(\sqrt{PHI+V_D}+\sqrt{PHI+V_S}\right)\right]. \qquad (3)$$

The slope factor n is defined as the inverse of the derivative of the pinch-off V_P vs V_G characteristic and therefore is a function of the same parameters: *VTO*, *GAMMA* and *PHI*.

The drain current is derived under typical assumptions for charge-sheet models, including drift and diffusion components [9], and is normalized to the specific current I_S:

$$I_D = I_F(V_P - V_S) - I_R(V_P - V_D), \qquad (4)$$

where

$$I_{F(R)}\left(V_P - V_{S(D)}\right) = I_S\, i_{f(r)}, \qquad (5)$$

$$I_S \equiv 2nU_t^2\, \mu\, COX\, W_{eff}/L_{eff}, \qquad (6)$$

$i_{f(r)}$ are normalized forward and reverse currents expressed by a simple function. The specific current I_S depends essentially on W/L and μ, where μ is the mobility accounting for vertical and lateral electric fields in the transistor channel.

Both components, the forward and reverse currents, have the same asymptotic behavior, which is exponential in weak inversion and quadratic in strong inversion. The intermediate region of moderate inversion is described by an interpolation function derived from physics. The expression for the drain current of an ideal long channel transistor requires only four parameters: the mobility related parameter *KP*, the threshold voltage *VTO*, the substrate effect parameter *GAMMA* and the surface potential in strong inversion at equilibrium *PHI*. Second order effects such as mobility reduction due to the vertical field, velocity saturation and short- and narrow-channel effects are taken into account with additional model parameters. Another parameter, *COX*, is required so that charges and transcapacitances necessary for dynamic operation can also be expressed.

The reverse short channel effect (RSCE) is included in the pinch-off voltage V_P, in addition to the charge-sharing concept, to extend range on the EKV v2.6 model applications. The RSCE is described using simple expression [9]:

$$\Delta V_{RSCE} = \frac{2\cdot Q0}{COX}\,\frac{1}{\left[1+0.5\left(\xi+\sqrt{\xi^2+C_\varepsilon}\right)\right]^2}, \qquad (7)$$

where $\xi = C_1\,(10\ L_{eff}/LK - 1)$, C_1 and C_ε are constants. The parameters are the peak charge density at the source/drain ends $Q0$ and the characteristic length of charge distribution *LK*.

The substrate (impact ionization) current effect, which requires three model parameters, is modeled using the following expression [8]

$$I_{DB} = I_{DS}\frac{IBA}{IBB}\,V_{ds'}\,\exp\left(\frac{-IBBL_C}{V_{ds'}}\right), \qquad (8)$$

where $V_{ds'} = V_D - V_S - IBN\ V_{DSS}$ and V_{DSS} is the drain to source saturation voltage. The substrate current is treated as a component of the total extrinsic drain current, flowing from the drain to the bulk. The total drain current is therefore expressed as $I_D = I_{DS} + I_{DB}$. Consequently, the substrate current affects the total extrinsic conductances, in particular the drain conductance.

The static DC model is completed with a continuous dynamic model, in which intrinsic charges and capacitances are expressed as continuous functions of the normalized forward and reverse currents, which are valid in all regions of operation. This implementation does not require additional model parameters. The same holds for the noise model. The thermal noise expression is continuous and valid from weak to strong inversion. A first order non-quasi-static (NQS) model for transadmittances is used for AC and transient analysis at high frequencies. Temperature behavior of the intrinsic model can be adapted using four parameters. Finally, many analog circuit applications are limited by the matching properties of the devices, which depend mainly on geometry and bias conditions. Unlike other MOS transistor models, the EKV v2.6 model also allows for geometry and bias-dependent matching analysis using Monte-Carlo statistical circuit simulation. The EKV v2.6 requires only three dedicated matching parameters.

Extrinsic model elements: series resistances, junction currents and capacitances, overlap capacitances along with temperature dependencies are implemented into model in conventional manner similar to many other models. Series resistances usually add two extra nodes. However if this should be avoided to increase efficiency, the following scheme allows to explicitly account for series resistance in drain current and conductances as discussed in [12]

$$\frac{I_D}{I_{D0}} = \frac{g_m}{g_{m0}} = \frac{g_{ms}}{g_{ms0}} = \frac{g_d}{g_{d0}} \cong \frac{1}{1 + g_{ms0} R_S + g_{d0} R_D}, \quad (9)$$

where the subscript „0” denotes currents or conductances calculated without series resistances.

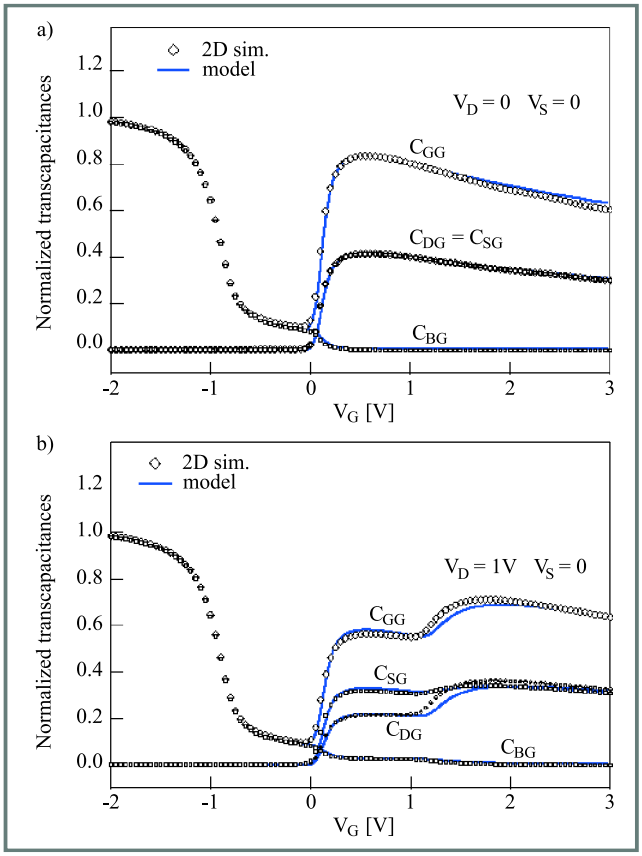


Fig. 4. Normalized transcapacitances versus gate voltage for n-channel device showing polysilicon depletion: (a) $V_D = V_S = 0$ V, (b) V_D = 1 V, V_S = 0 V. The new analytical model (lines) is compared to 2D numerical devices simulation (markers).

4. New polysilicon depletion model

The continuing increase of the channel doping concentration when scaling deep submicron CMOS technology using dual polysilicon gates accentuates the impact of the polysilicon depletion effect [16, 17] on all device characteristics. The new model, which correctly predicts transcapacitances as well as drain current and includes mobility reduction, has been published [18].

New compact modeling results are compared to the characteristics obtained from a 2D numerical device simulator. In Fig. 4, the normalized transcapacitances versus gate voltage are shown at various drain-to-source voltages, namely $V_D = 0$, 0.5, 1 V and V_S = 0 V. The new analytical model is compared to the numerical device simulation, and shows an excellent match for all bias conditions for all transcapacitances: C_{GG}, C_{DG}, C_{SG}, and C_{BG}. A single set of parameters is used in the analytical model for all bias conditions. The flat-band voltage has been adapted to match the measurement, and all other parameters match those underlying the 2D device simulation to within a few percent, i.e. to about the accuracy of the estimate of the doping concentrations in the gate and the substrate. The agreement at $V_D = V_S = 0$ V is excellent, $C_{DG} = C_{SG}$ is correctly predicted, and the value of $C_{DG} = C_{SG} = C_{GG}/2$ is correctly reached in strong inversion. At non-equilibrium conditions, the agreement is slightly degraded in the transition regions from saturation to non-saturation. Nonetheless, the overall qualitative behavior for an analytical model using only physical parameters remains excellent. Similar results have also been found with different levels of substrate and gate doping concentrations. Correct asymptotic behavior is found for all transcapacitances, including the ones not shown here, and is found to be further improved with respect to the previous linearization. Note that e.g. the correct behavior of $C_{BG} \to 0$ in strong inversion non-saturation, is due to the higher-order development of the bulk charge used, while its first-order counterpart would indeed lead to an incorrect asymptotic behavior of C_{BG}.

The effect of polydepletion on drain current versus gate voltage characteristics is shown in Fig. 5, for two values of drain voltage, V_D = 0.5 V and V_D = 1 V corresponding to the same cases as in Fig. 4. Two cases of polysilicon doping concentrations are shown, $N_p = 1 \cdot 10^{19}$ cm^3 corresponding to the same devices as used in Fig. 4, and $N_p = 9.1 \cdot 10^{20}$ cm^3 showing no polydepletion as a result. The same parameter set is used for the analytical model in both cases, except for the change in polysilicon doping concentration and a slight change in the flat-band voltage, due to a changed work function difference between the polyga-

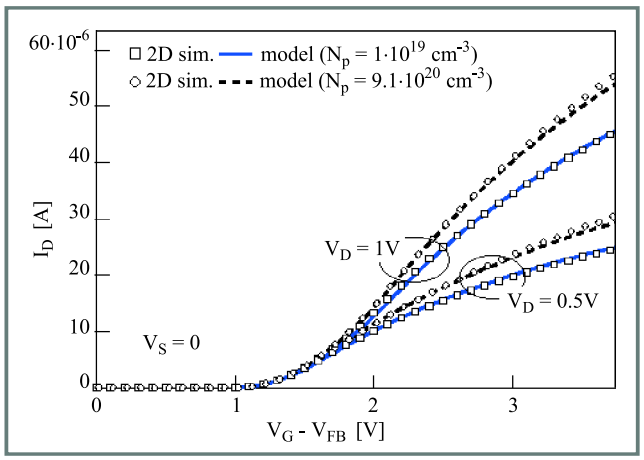


Fig. 5. Drain current versus gate voltage, for two drain voltages, V_D = 0.5 V; 1 V; V_S = 0 V, for two cases of polysilicon doping concentrations. 2D simulation (markers) and analytical model (lines). The model uses one set of parameters in all conditions except for changed gate doping concentration.

te and the substrate. The mobility model parameters have been chosen to match the case with polydepletion. As can be seen, the case without polydepletion is reasonably well matched without adapting model parameters further, confirming the coherence of the model. The slight difference observed may also stem from different processing circumstances for each cases.

5. New NQS charge based model

Despite various efforts devoted to high frequency and transient modeling of the MOS transistor, using both numerical and analytical approaches [19, 20], only incomplete sets of first-order NQS expressions were proposed for the kind of model discussed here [21]. The new model offers exact analytical of small signal NQS MOS transistor behavior, which is valid in all modes of operation and from DC to high frequencies, and was published in [22]. This is derived from a general charge based approach and uses the framework of the EKV model. It has been demonstrated that only four independent transadmittances are needed to fully characterize the small signal operation of the device. All quantities in the model are expressed in terms of normalized variables, which are independent of the process parameters. Only six independent real parameters (four transcapacitances and two transconductances) are needed to fully describe the low frequency, small signal, behavior of the intrinsic MOS transistor. It is also important to note that the intrinsic transcapacitances are nonreciprocal but satisfy the charge conservation condition.

In order to validate the model, experimental data taken from the literature have been used. These high frequency measurements were performed on PMOS transistors with 10 and 30 lm channel length and have been published [23]. The normalized y_{DG} data are plotted in Figs. 6a (magnitude) and 6b (phase). The set of curves, in both figures, depicts the normalized transconductances for the three channel lengths, in saturation mode. The corresponding theoretical characteristics, calculated in terms of Bessel functions, are also shown (note that, in Fig. 6, ny_{DG} is plotted instead of y_{DG}).

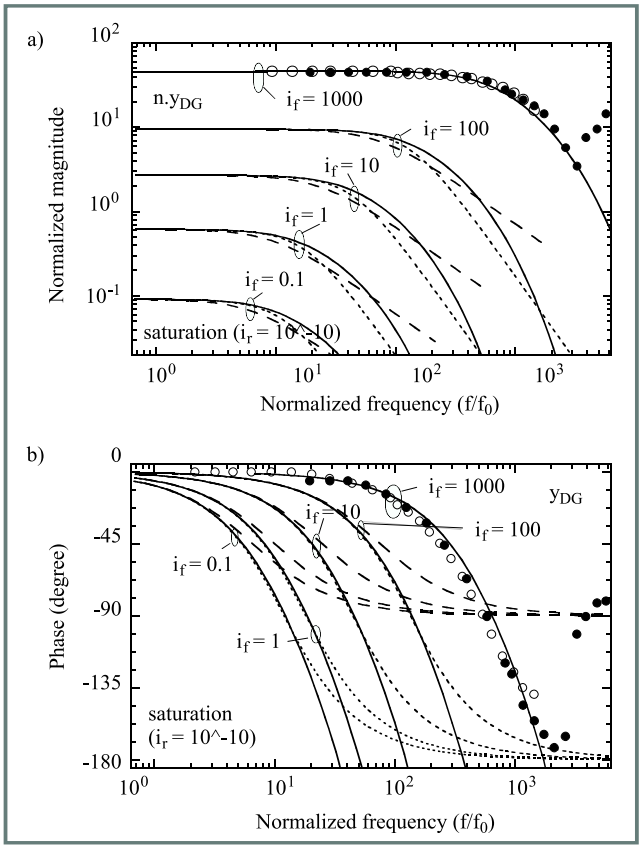


Fig. 6. Normalized plots of measured and simulated y_{DG} data: (a) magnitude and (b) phase.

A very good agreement between theory and experiment can be observed for both; the magnitude and phase characteristics, even for submicron devices. It can be noted that the phase shift appears well before the decrease in the magnitude of y_{DG}. This supports the accuracy of the model, as phase shift is difficult to predict precisely, especially over a large range of variation, as in the present case. The complete evaluation of the magnitude and phase characteristics of the model in saturation mode, from weak to strong inversion is possible. As expected, the accuracy of the second-order expressions is far better than the first-order one and appears to be sufficient for most practical applications. The agreement is fairly good for phase lags lower than 110°. On the contrary, the accuracy of the first-order expansion already degrades rapidly for phase shifts exceeding 30°.

6. RF characterization

The goal of the on-the-wafer MOSFET devices characterization is to obtain the electrical behavior of the intrinsic device, i.e. the transistor characteristic without the parasitic components associated with bond pads and interconnec-

tions. In order to achieve this goal proper vector network analyzer (VNA) calibration and MOSFET device parameter deembedding have to be performed.

6.1. VNA system calibration

Advanced VNAs offer number of the calibration options and standards. A full calibration of all parameters must be used to ensure the high accuracy needed for precise 2-port RF measurements. The calibration procedure removes most of errors including directivity, source match, load match, reflection tracking, transmission tracking and crosstalks.
The most commonly used calibration method is SOLT (short-open-load-thru) calibration available on every commercially available VNA. This calibration is the combination of two single-port SOL calibrations with additional measurements of a „thru" standard to complete the two port calibration. The SOLT standards are reasonably good modeled using simple lumped elements.

6.2. MOSFET parameters deembedding

The parasitics surrounding the transistor can be characterized by measuring two DUT pad frames after VNA system calibration. The measurements begin with the „open" test structure providing Y-parameters and with „short" test structure providing corresponding Y-parameters. The layout of both pad frames is based on a typical GSG (ground-signal-ground) pattern for on-the-wafer RF characterization. First measurements determine the interconnect parasitics which are assumed to be parallel to DUT. The second measurement is used to determine losses and phase rotation in the interconnect line. Once „open" and „short" pads frames are characterized, a large range of device geometries can be measured using the same de-embedding set. In order to demonstrate the advantages of the two-step de-embedding procedure, two experiments were performed over a wide frequency range up to 110 GHz to measure a short-channel MOSFET current gain characteristic from the Y-parameters (Fig. 7). The difference between the corrected curves applying the „open" and „open-short" de-embedding procedures is clearly seen for frequencies above 10 GHz. The simulation performed using the EKV v2.6 model with the extracted parameters from DC measurements and the factory default AC model parameters exhibits a qualitatively correct behavior, but shows the need for more a precise extraction of all intrinsic and extrinsic capacitances. The measurement data acquisition, calibration and de-embedding were performed using commercially available software packages [24, 25].

6.3. RF parameter extraction

Several approaches were proposed to improve RF performance of compact models by simple modification of the MOSFET equivalent circuit. Modifications that use additional substrate resistances along with bulk diodes and series gate resistances were studied [14]; these are implemented

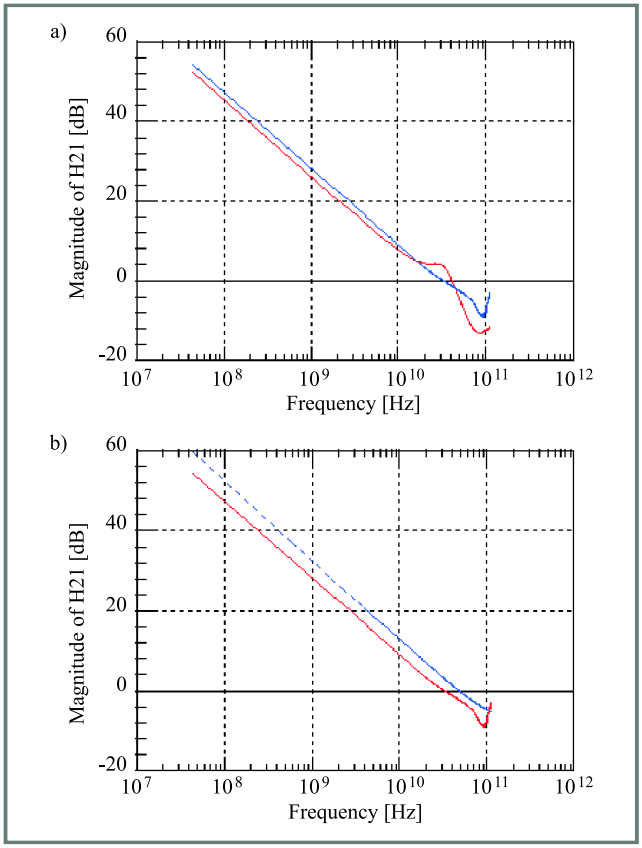


Fig. 7. (a) Open. (b) Open-short de-embedding and simulation current gain data up to 110 GHz (n-channel MOSFET device: 30 × 20 µm/0.35 µm). Bias: V_{gs} = 1.0 V, V_{ds} = 1.0 V.

as a simple equivalent. Elements such as gate resistance R_g and bulk resistance R_b cannot be neglected in RF operation because they are essential in forming the real part of the Y-parameters. Note that in some simulators, R_g and R_b are already parts of the MOSFET model, so that a subcircuit definition specific to RF is not needed.
The equivalent gate resistance R_g takes into account the sheet resistivity of the polysilicon gate layer and the gate contact resistance. It can be estimated from the device geometry and plays a major role in the phase characteristics of the input Y11 and transfer admittances Y12 & Y21 of short channel devices.
The addition of the substrate equivalent resistance R_b allows a simple but reasonably accurate modeling of the output characteristics Y22. It may be bias-dependent in order to include the variations of the depleted regions close to the source and drain junctions.
As Y11, Y12 & Y21 are very weakly dependent on R_b, a first estimate of R_g can be obtained from Re{1/Y11}. The total gate capacitance C_{gg} is extracted from Im{Y11} while Im{Y12} provides a precise evaluation of the gate-to-drain overlap capacitance C_{gd} . The extraction of R_b is based on Y22 data. The values of these additional parameters, as well as of other AC model parameters are then globally optimized.
Using EKV v2.6 for the intrinsic device, it is shown from

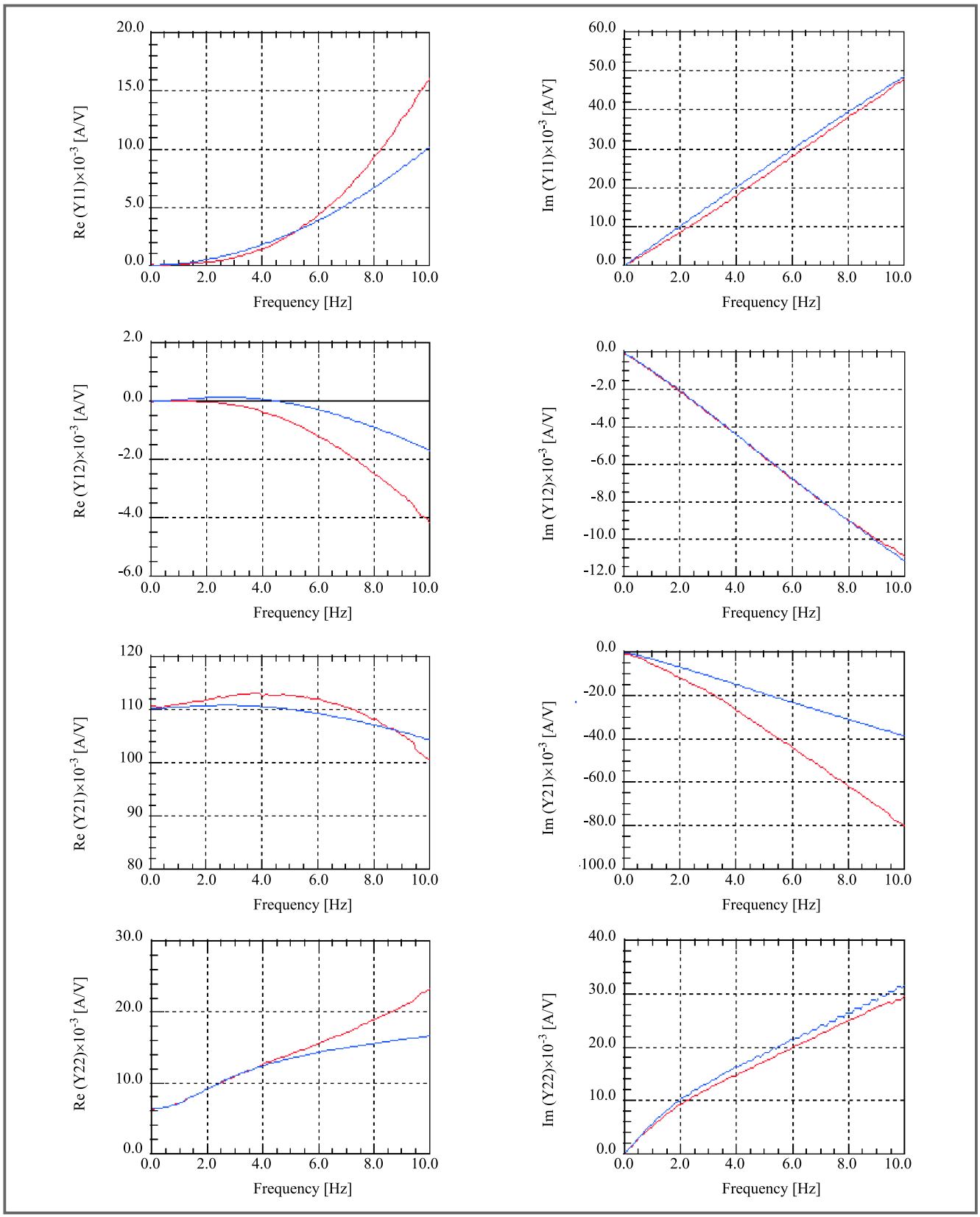


Fig. 8. Comparison between measured and simulated Y parameters for an n-channel MOSFET (30 × 20 µm/0.35 µm), $V_{gs} = V_{ds} = 1$ V. Frequency span is 0÷10 GHz.

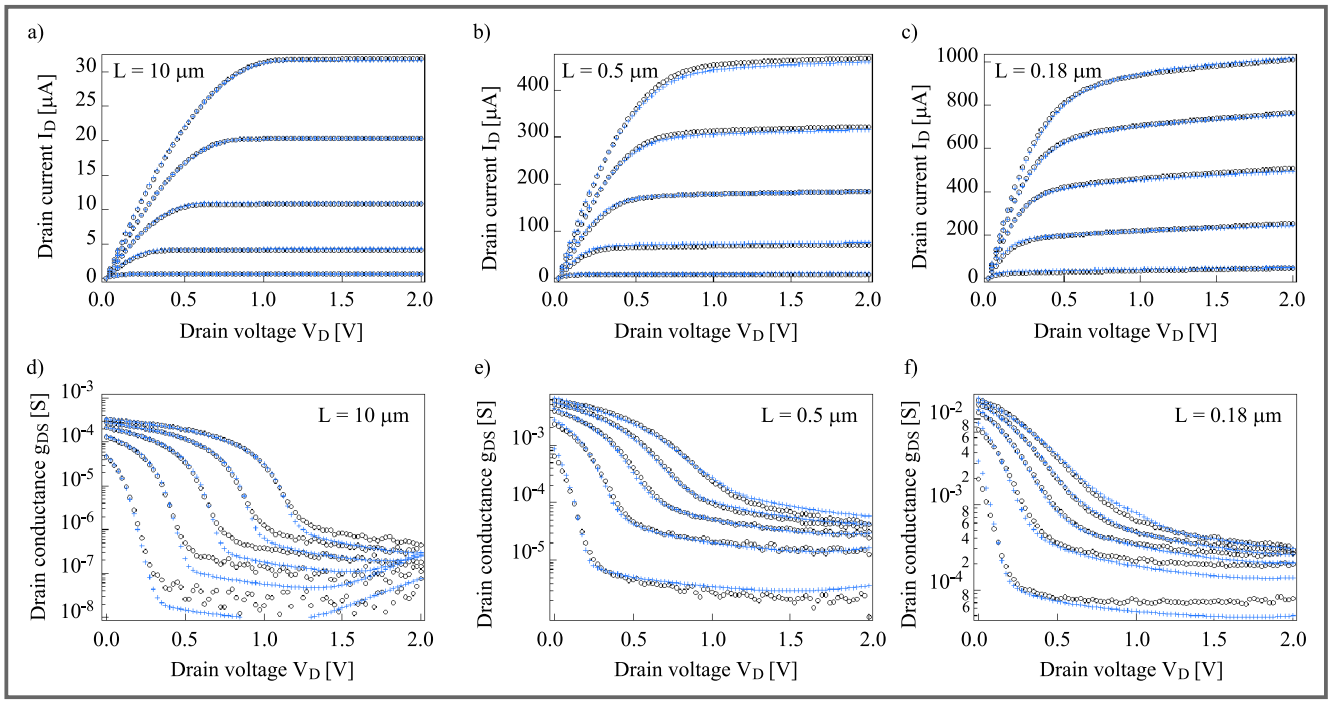


Fig. 9. The simulated (o) and measured (-) output current (I_D) (a), (b), (c) and conductance (g_{DS}) (d), (e), (f) for n-channel devices of a standard 0.18 µm CMOS process.

Fig. 8 that the resulting model validity typically covers DC to 5 GHz for 0.35 µm devices. The values for R_g and R_b were found to be 5 Ω and 50 Ω, respectively. This shows that losses associated with the bulk connection come into play already at 1 GHz. The imaginary part of the Y parameters is accurately predicted except for the Y21 transcapacitance. The latter discrepancy is attributed to short-channel effects not accounted for in the channel charge calculation. This is consistent with the noticeable difference between the measured and simulated of the current gain characteristics for this particular MOSFET transistor.

For medium- and long-channel MOSFETs, R_g can be neglected compared to the bias-dependent, nonquasistatic (NQS) effects due to the distributed nature of the channel. Although any charge-based MOS model intrinsically pro-vides a first-order fit of the transadmittance (through the so-called transcapacitances), a consistent modeling of the NQS effects requires more specific extensions of the compact model, for which the EKV MOSFET model formulation is particularly suitable [22].

7. Model applications

7.1. DC circuits evaluation

The scaling model performance with the channel length is presented using a standard 0.18 µm CMOS process. Figure 9 shows the measured and simulated output characteristics (I_D vs V_D and g_{DS} vs V_D) at different V_G for the devices with $W = 10$ µm and L = 10, 1 and 0.5 µm, respectively. The output conductance is adequately modeled using one unique parameter set for all geometries in conduction as well as in saturation.

The next example shows the benchmark results of D/A converter circuit analysis using the EKV v2.6 model. The insert of Fig. 10 shows a typical current divider circuit used in D/A converters. The circuit designed is based on the principle of an R-2R ladder circuit. Each stage divides the reference current by a factor of 2. Simulation results show expected behavior of the perfect current divider over several decades of reference current. The estimated error is less than 5% for LSB.

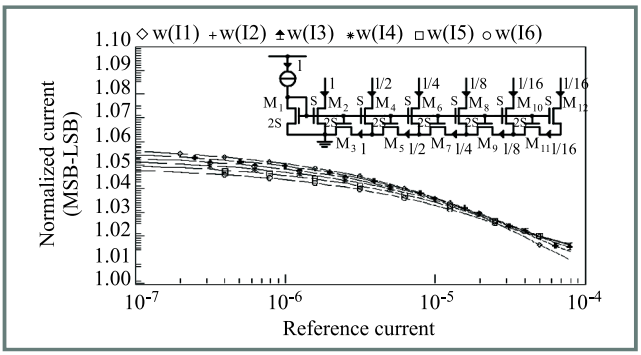


Fig. 10. The normalized branch currents versus reference current for typical current divider circuit used in D/A converters (the insert shows divider stages).

7.2. RF circuits evaluation

To test the performance to the EKV v2.6 model, a circuit level evaluation was performed using two different RF

chips. As a first example, a simple power amplifier (PA) well suited for RF MOSFET model evaluation has been chosen to illustrate the use of the new subcircuit model. The core of the PA is an interdigitated 0.35 mm NMOS transistor, encapsulated into a SO-8 package. The circuit operates at 900 MHz as an overdriven class B PA. Output power vs input power characteristics (Fig. 11) were measu-

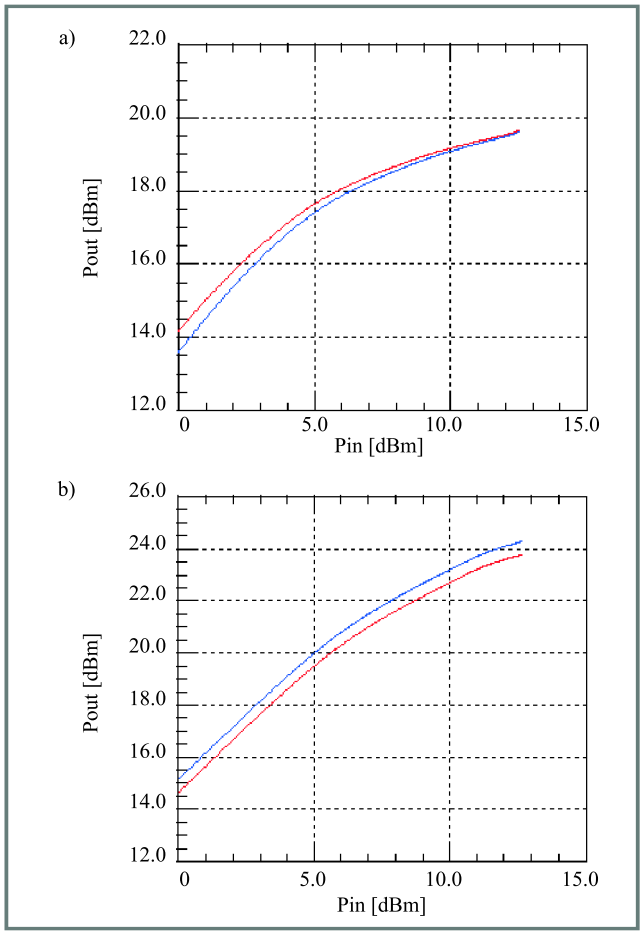


Fig. 11. Output power vs input power characteristics of the PA. Supply voltage is: (a) 1.5 V and (b) 2.7 V.

red and simulated at two different supply voltages, 2.7 V and 1.5 V, respectively. A good agreement for broad power range has been achieved. In the second example, a harmonic oscillator was designed and fabricated in the same 0.35 mm CMOS technology. The oscillator operates at 900 MHz and with 3 V power supply has phase noise of −101 dBc/Hz 25 kHz. Figure 12 shows basic characteristics of the oscillator. Performed simulations based on the EKV v2.6 model accurately predict the circuit performance.

Acknowledgments

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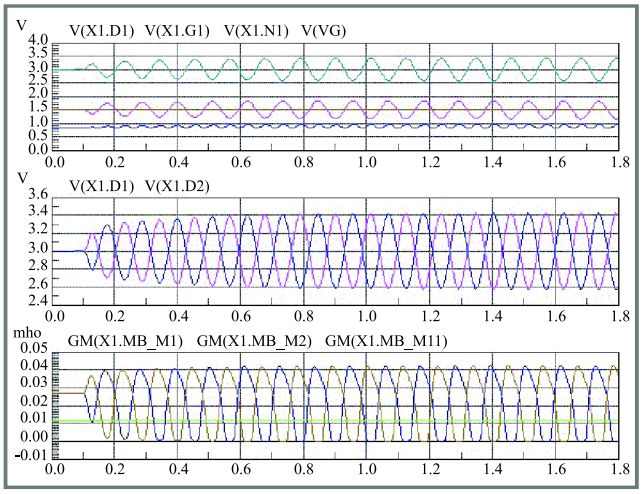

Fig. 12. Simulated characteristics of the 900 MHz harmonic oscillator.

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