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An impact of physical phenomena on admittances of partially-depleted SOI MOSFETs

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Abstract — An influence of the selected physical phenomena: impact ionization in silicon and time variation of internal electric field distribution in partially-depleted (PD) SOI MOSFETs on several C-V characteristics of these devices is presented. The role of avalanche multiplication in the so-called „pinch-off" region is discussed in a more detailed way. The analysis is done using a numerical solver of drift-diffusion equations in silicon devices and using an analytical model of the PD SOI MOSFETs. The calculations results exhibit the significance of proper modelling of the phenomena in the floating body area of these devices.

Keywords — SOI MOSFET, floating body, avalanche ionization, recombination, displacement current, admittance.

1. Introduction

It is well known, that I-V characteristics of partially depleted silicon-on-insulator (PD SOI) MOSFETs are determined by the balance of internal current components, which originate from different phenomena in intrinsic and extrinsic parts of the device. This was confirmed in several works and by numerical simulations. Obviously the same phenomena influence the C-V characteristics of the PD SOI MOSFETs [1, 2]. Due to the strong impact of these phenomena on the AC data reliable small-signal models of the PD SOI MOSFETs are relevant for the characterization and design purposes.
Below brief discussion of the influence of several phenomena on PD SOI MOSFETs capacitances is presented. It is based on preliminary numerical simulations and on computations made using an analytical small-signal non-quasi-static model of the PD SOI MOSFETs.

2. Numerical analysis of the PD SOI MOSFETs capacitances

Numerical simulation is a very valuable tool for detailed investigation of physical phenomena, which determine electrical characteristics of the semiconductor devices. One of the main advantages of this approach is a possibility of selective turning on/off the models of the particular phenomena. Owing to this an engineer may compare electrical characteristics of the device obtained with or without accounting for the given mechanism. Such approach is not possible when experimental data are analysed.

Impact ionization is very important for determining electrical parameters of the PD SOI MOSFETs. A role of impact ionization for I-V and C-V characteristics becomes more clear using the approach mentioned above. Figure 1 shows comparison of $C_{gfs}(V_{DS})$ and $C_{gfd}(V_{DS})$ data of the PD SOI MOSFET, calculated using ATLAS/SPISCES program [3] with avalanche ionization turned on and turned off. Parameters of the simulated device are as follows: L = 0.6 μm, $t_{Si} \approx 0.2$ μm, $t_{ox,b} \approx 0.4$ μm, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm^{-3}.

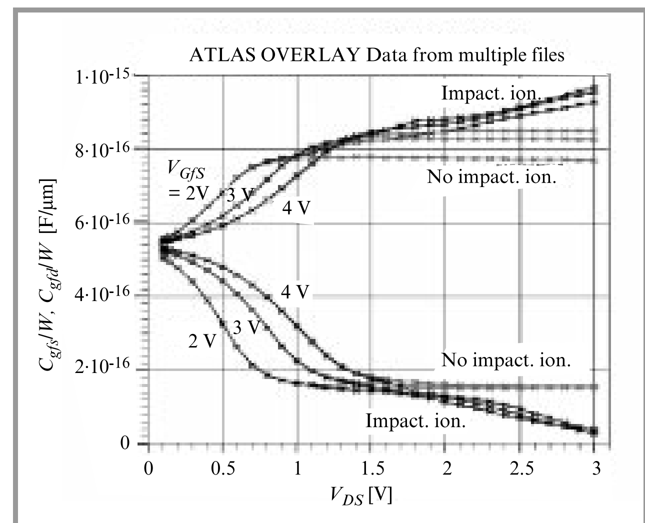

Fig. 1. Influence of the impact ionization in silicon on the front gate-to-source and front gate-to-drain capacitances of the PD SOI MOSFET obtained with numerical simulations [3]. Comparison has been done by switching on/off the impact ionization components in the drift-diffusion equations. The device parameters are mentioned in the text.

For impact ionization turned on the following effects may be distinguished, which may be observed neither in bulk MOSFETs nor in hypothetic PD SOI MOSFETs without avalanche multiplication:

- increase of the C_{gfs} capacitance in saturation range for increasing V_{DS} voltage;
- decrease of the C_{gfd} capacitance in saturation almost below zero farads for increasing V_{DS} voltage.

Of course C_{gfs} and C_{gfd} capacitances consist of intrinsic and extrinsic components [4]. Extrinsic parts are related

to overlap and fringing capacitances and are almost constant. Intrinsic parts result from variation of electric field below the gate. If extrinsic components were „subtracted” from the total $C_{gfd}(V_{DS})$ curve, then it would appear, that intrinsic component of C_{gfd} capacitance became negative. This result is not possible in the conventional MOSFETs, where C_{gfd} capacitances approaches zero farads in saturation range. Moreover Flandre estimated in [1], that a small „plateau” visible in C_{gfs} data (1 V ÷ 2 V, depending on the V_{GfS} value) corresponded to C_{gfs} value of ca. $0.72 \cdot C_{ox,f}$, where $C_{ox,f}$ denotes front gate voltage of the device analysed in [1]. Therefore it would considerably exceed value of $2/3 \cdot C_{ox,f}$, which is typical for bulk transistors. All the effects mentioned above are strictly related to the avalanche ionization in the depletion area of the drain-body junction. It is also worthwile to mention, that $C_{gfs}(V_{DS})$ characteristics of the PD SOI MOSFETs calculated with ionization turned off, differ from the same data obtained for the conventional MOSFETs. A V_{GfS}–controlled variation of the C_{gfs} value in the saturation range can be observed only in the hypothetic PD SOI MOSFETs. This effect is probably due to small variations of the body potential, even if a large number of excess holes generated by ionization do not enter the thin Si-film. This may induce appropriate change of width of front gate depletion area and finally a change of C_{gfs} intrinsic component related to coupling between front gate and source through the „pinch-off” region.

The simulator does not allow to switch multiplication on/off selectively, so the characteristics in Fig. 1 reflect the overall effect of the impact ionization in the space-charge regions, surrounding drain-body junction, where high electric field exists. However ionization in the „pinch-off” region is particularly relevant, because number of holes generated there and injected into the floating, quasi-neutral body area is several orders of magnitude higher, than the number of holes generated in the depletion region of the drain body junction. This results from the fact, that drift current component at the interface is much more higher, than the parasitic current flowing in the bulk part of the Si-film.

3. Role of displacement currents at the source-body and drain-body junctions

Displacement current components flowing through the extrinsic gate-source and gate-drain capacitances (for both gates) are connected in-parallel with the appropriate intrinsic capacitances. As has been mentioned earlier, they are almost constant, so their effect is self-evident. They simply increase the total capacitances. Moreover, as the currents flowing through them are purely capacitative, they do not influence the character of intrinsic admittances, i.e. they do not modify their partitioning between capacitance and conductance. Therefore for the simplicity it has been assumed here, that gates fringing capacitances may be neglected. Further brief analysis will be concerned with displacement currents at the junctions.

Figures 2 and 3 show fragments of $C_{gfs}(V_{GfS})$ and $C_{gfd}(V_{DS})$ characteristics of the PD SOI MOSFET, obtained using the model [5]. They were calculated for the device parameters, which are given in [6, Table 1]. Data presented in Fig. 2 correspond mainly to the accumulation range and transition between weak and strong inversion, which however is not modelled properly (in this model version subthreshold range is not accounted for). Data shown in Fig. 3 correspond to transition between non-saturation and saturation ranges.

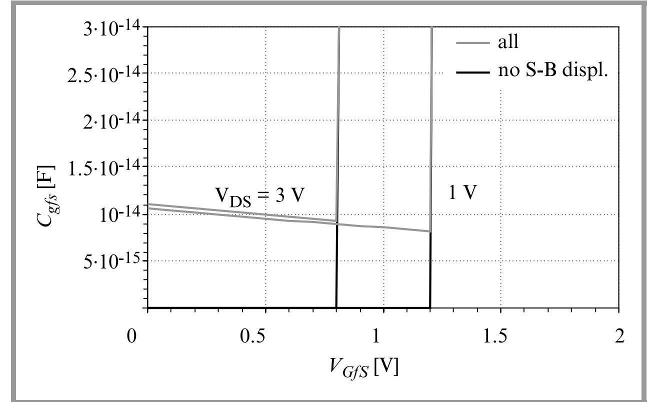

Fig. 2. The influence of the displacement current at the source-body junction for the C_{gfs} capacitances in the accumulation range.

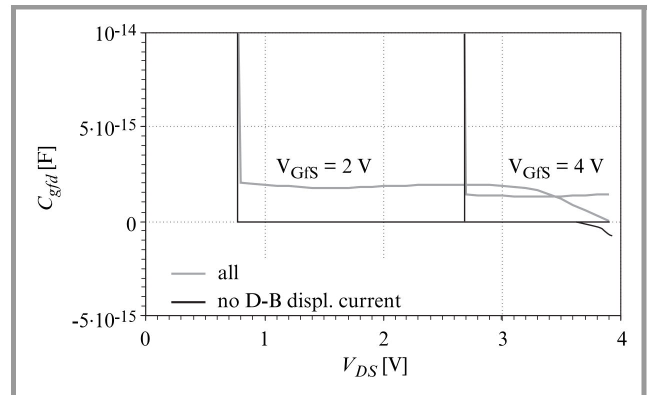

Fig. 3. The effect of the displacement current at the drain-body junction for the C_{gfd} capacitances in the saturation range.

In the accumulation range neglecting of the S-B junction displacement current causes, that C_{gfs} capacitance vanishes. It means, that in this way the only path (except of neglected fringing capacitance) for HF signal propagation from source to front gate becomes closed. Thus in accumulation S-B junction admittance is connected in parallel with other components of the front gate-source admittance. Figure 2 illustrates also decrease of the junction admittance for increasing front gate voltage. It is caused probably by the narrowing of the quasi-neutral part of the Si-film, as front-gate induced depletion region widens.

In the saturation range (Fig. 3) C_{gfd} capacitance calculated using the model [5] is also determined by parasitic compo-

nents related to fringing capacitances (neglected) and admittance of the drain-body junction. As expected in case of neglecting of displacement current component flowing through this junction C_{gfd} vanishes to zero farads. However for sufficiently large drain-source voltage and gate-source voltage equal 2 V decrease of C_{gfd} below zero may be observed. For V_{GfS} = 4 V saturation and „kink" ranges are shifted towards higher values of V_{DS}, so effect of impact ionization on C_{gfd} capacitance is not visible. Brief discussion of this effect based on results of numerical computations was presented in the previous section. Its analysis based on computations made using the analytical model is presented in the next section.

4. Role of phenomena in the „pinch-off" region

In the saturation range C_{gfd} capacitance calculated using the model [5] is determined by parasitic components related to fringing capacitances (neglected) and admittance of the drain-body junction. This is analogous to the case of conventional MOSFETs. However contrary to bulk devices the D-B junction admittance has not purely capacitative character. In the drain bias range beyond „kink" it behaves rather like RLC circuit [7]. As a result, current components flowing through areas of high electric field induce such phase shift between AC components of the drain voltage and body potential, that intrinsic component of C_{gfd} capacitance becomes negative. Figure 4 illustrates this effect. However turning off the appropriate AC component

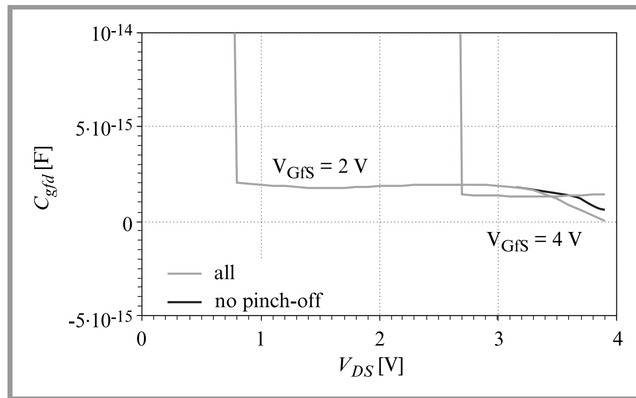

Fig. 4. The influence of the impact ionization in the „pinch-off" region upon the C_{gfd} capacitances in the saturation range. These data are consistent with Fig. 1.

of the drain current does not remove it completely. So a conclusion may be done, that a generally valid balance of all the AC currents in the PD SOI MOSFET makes, that their capacitances differ significantly from the appropriate capacitances of the bulk devices. Even a small difference in phases or amplitudes of currents AC components may induce unusual admittance behaviour.

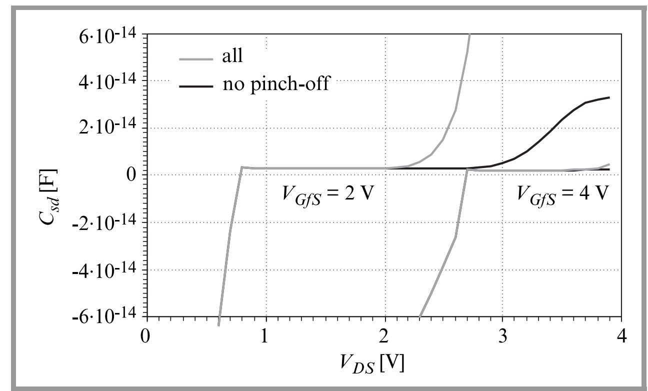

Fig. 5. The influence of the impact ionization in the „pinch-off" region upon the C_{sd} capacitances in the saturation range.

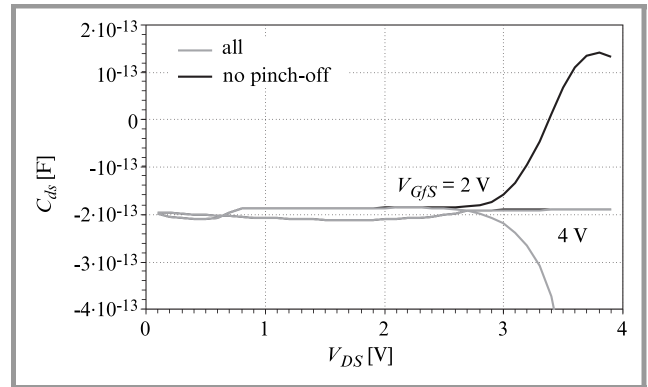

Fig. 6. The influence of the impact ionization in the „pinch-off" region upon the C_{ds} capacitances in the saturation range. The nonreciprocality of the C_{ds} and C_{sd} capacitances is obvious.

Figures 5 and 6 show also effect of impact ionization on C_{ds} and C_{sd} capacitances of the PD SOI MOSFET. It is very difficult to measure these variables, because during the measurement a large current flows between source and drain contacts. Such data are not available in the literature. Only simulated characteristics may be compared and discussed. The data presented in Figs. 5 and 6 show that in the saturation range switching the impact ionization off completely changes character of these capacitances. More detailed analysis of this effect is very difficult and will be presented in future together with comparison with characteristics obtained numerically. The eventual improvement of the model towards better modelling high-frequencies effects should be also considered. These data in Figs. 5 and 6 also illustrate, that both capacitances are non-reciprocal, which is typical for multi-port active devices.

5. Conclusions

The small-signal model of the PD SOI MOSFETs shows qualitatively the importance of the following phenomena for the proper modelling of C-V characteristics:

- displacement current at the source-body and drain-body junctions,
- avalanche multiplication of carriers within the „pinch-off" region.

Moreover it may be stated, that generation/recombination phenomena are less critical for the small-signal analysis of these devices.

Acknowledgment

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