Invited paper

High-temperature instability processes in SOI structures and MOSFETs

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Abstract — The paper reviews the problems related to BOX high-temperature instability in SOI structures and MOSFETs. The methods of bias-temperature research applied to SOI structures and SOI MOSFETs are analysed and the results of combined electrical studies of ZMR, and SIMOX SOI structures are presented. The studies are focused mainly on electrical discharging processes in the BOX at high temperature and its link with new instability phenomena such as high-temperature kink effects in SOI MOSFETs.

Keywords — SOI, MOSFET, high-temperature instability, ZMR, SIMOX.

1. Introduction

Devices fabricated on silicon-on-insulator (SOI) structures are very promising for high-temperature microelectronics [1]. Consequently, the high-temperature stability of SOI structures is the necessary condition for proper device operation. From this point of view, the main weakness of SOI structures is thick buried oxide (BOX), which can effectively accumulate a positive and a negative charge during the application of sufficiently low electric fields to SOI structures [2, 3].

Thus, the paper is devoted to review high-temperature instability phenomena in SOI structures and devices especially with respect to bias-temperature (BT) processes in the BOX.

2. Methods for electrical characterization of high-temperature instability processes

2.1. Capacitance-voltage method for SOI structures

The most widely used method to study the BT instability is the analysis of capacitance-voltage (C-V) curves. In this method measurements are performed at room temperature before and after application of the bias to the gate of SOI structure at high temperature. For SOI structures the C-V method is very useful, since it permits the potentials at BOX/substrate and at BOX/film interfaces (Fig. 1a) and, consequently, the total net charge, Q_{tn}, in the BOX and its centroid, X_0, to be determined. As it was proposed in [4, 5]

$$Q_{tn} = Q_f + Q_{sub} = \frac{C_d\left(V_{FB}^f - V_{FB}^{sub}\right)}{qS}, \qquad (1)$$

$$X_0 = \frac{\int_0^d \rho(x)x\,dx}{\int_0^d \rho(x)x\,dx} = \frac{|V_{FB}^f|\,d}{V_{FB}^f - V_{FB}^{sub}}, \qquad (2)$$

where V_{FB}^f, V_{FB}^{sub} are flat-band voltages related to the film/BOX and the substrate/BOX interfaces, respectively, $\rho(x)$ is the charge distribution in the BOX, d is the BOX thickness, C_d is the buried insulator capacitance. The centroid is determined with respect to the BOX/substrate interface (Fig. 1b).

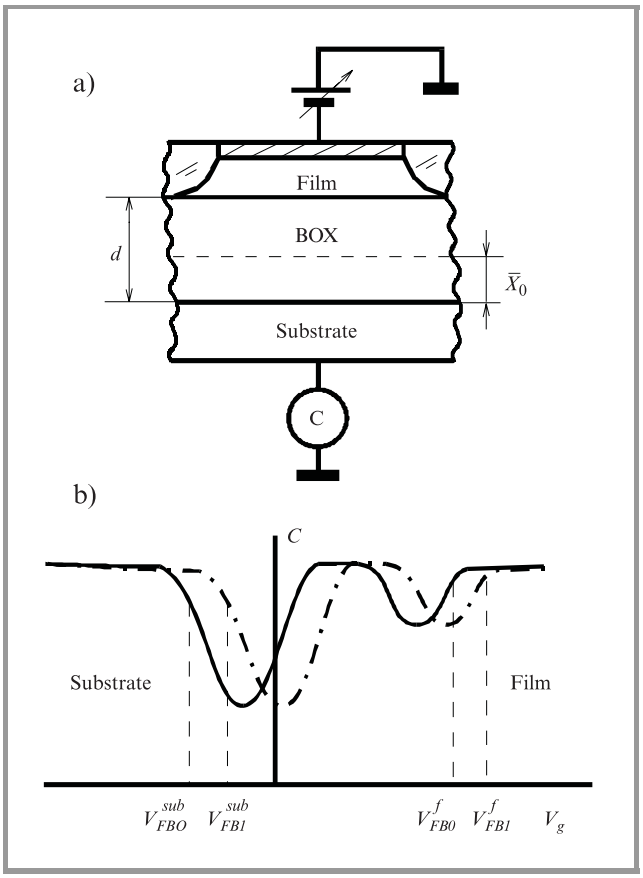

Fig. 1. A schematic diagram of a SOI capacitor (a) and low-frequency C-V characteristics before (bold line) and after (dotted line) BT stress (b).

The amount of the mobile charge related to the BOX/film interface, ΔQ_m^f, and to the BOX/substrate interface, ΔQ_m^{sub}, after BT stress can be calculated as

$$\Delta Q_m^f = \frac{C_d\left(V_{FB1}^f - V_{FB0}^f\right)}{qS} = \frac{C_d \Delta V_{FB}^f}{qS} \tag{3}$$

and

$$\Delta Q_m^{sub} = \frac{C_d \Delta V_{FB}^{sub}}{qS}\,, \tag{4}$$

where V_{FB1}, V_{FB0} are flat-band voltages after and before BT stress, respectively (see Fig. 1a). Thus, the change of the charge in the BOX is

$$\Delta Q_{tr} = \Delta Q_m^f - \Delta Q_m^{sub}\,. \tag{5}$$

If $\Delta Q_{tr} = 0$, we can consider the BOX/semiconductor interfaces as electrically blocking ones, if $\Delta Q_{tr} \neq 0$, interfaces are electrically unblocking.

2.2. Thermally stimulated polarization/depolarization currents

Thermally stimulated polarization/depolarization (TSP/TSD) current method is used to investigate the charge transfer processes in a dielectric during linear heating of the structure, holding a fixed voltage across the capacitors and measuring the resulting current (Fig. 2).

It has been shown that charge moving in the outer circuit during the polarization or depolarization processes, $Q_{TSP/TSD}$, is equal to the mirror charge at the blocking electrode [6]. Therefore:

$$Q_{TSP/TSD} = \frac{1}{\beta S}\int_{T_0}^{T} I(T)\,dT = \Delta Q_m^f\,, \tag{6}$$

if the BOX/film interface is blocking, or

$$Q_{TSP/TSD} = \Delta Q_m^{sub} \tag{7}$$

if the BOX/substrate interface is blocking, where β is the heating rate.

Thus, the comparison of C-V with TSP/TSD data allows to identify the electrically blocking interfaces and to determine the degree of blocking.

In addition, the TSP/TSD method gives the possibility of determination the activation energies of the polarization/depolarization processes and the frequency factor or capture cross section for traps involved in the processes (see, for instance [7]). In the case of energy distributed traps the fractional thermally cleaning method can be used in order to calculate the trap parameters [8].

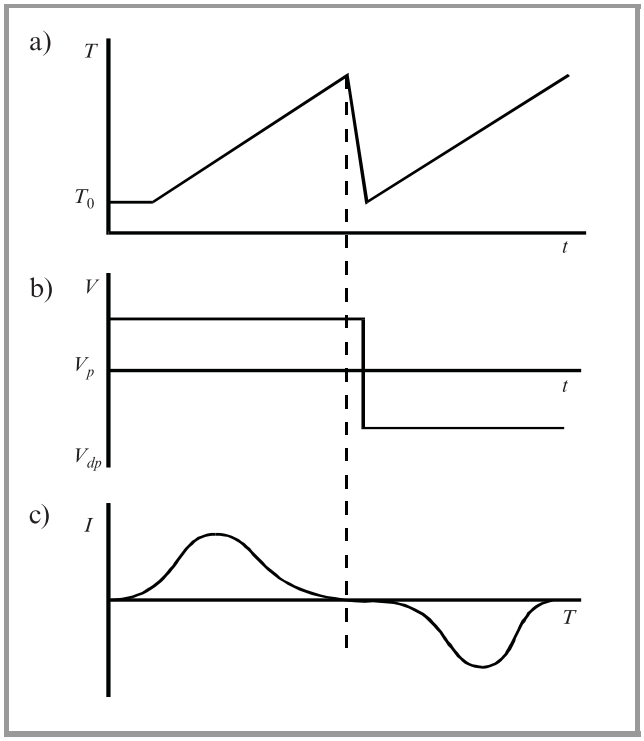

Fig. 2. Schematic time diagrams of temperature (a) and applied voltage (b), and TSP/TSD current (c).

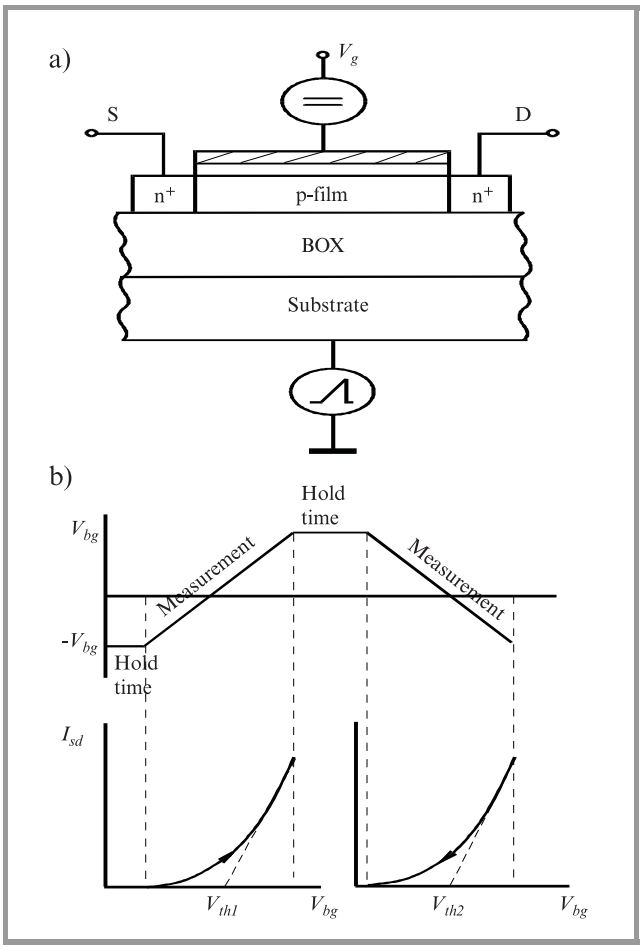

Fig. 3. A schematic diagram of a SOI MOSFET (a) and the applied voltage at the back-gate (b) for BT instability measurements using the drain-gate characteristic technique.

2.3. Source-drain current – gate voltage characteristics of MOSFETs

Source-drain current I_{sd} – gate voltage V_g, characteristics at high temperature enable the polarization parameters to be determined and the operation stability of the devices to be analysed. Measurement of the source-drain current, I_{sd}, in the back channel SOI MOSFET at high temperature, after holding the back-gate voltage positive or negative (Fig. 3), permits the change in the charge in the BOX layer relative to the BOX/film interface to be determined:

$$\Delta Q_m^f = C_d \frac{V_{th1} - V_{th2}}{qS} = \frac{C_d \Delta V_{th}}{qS} , \qquad (8)$$

where V_{th1}, V_{th2} are back-channel threshold voltages after negative and positive applied voltage to the back-gate, respectively.
Investigation of the threshold voltage shift as a function of temperature and hold time permits all main parameters of high temperature instability processes to be calculated.

2.4. Source-drain current relaxation

If at high temperature the polarity of the back-gate voltage is reversed and, as result, relaxation of the source-drain current occurs it is possible to determine the relaxation time of the processes, that links with the relaxation time of the charge changing in the BOX. This phenomenon is depicted schematically in Fig. 4. Indeed, as it was shown in [9] in the linear regime of the inversion mode (IM) SOI n-MOSFET operation, the source-drain current can be given by

$$I_{sd}(t,T) = \left(\frac{W}{L}\right) \mu_e C_d \left[V_{bg} - V_{thb}^* + Q_{BOX}(t,T)/C_d\right] V_{sd} , \qquad (9)$$

where W, L are the width and the length of the channel, μ_e is the electron mobility in the inversion channel, V_{bg} is the back-gate voltage, V_{thb}^* is constant with weak temperature dependence, Q_{BOX} is the total buried oxide charge, V_{sd} is source-drain voltage. That is, the source-drain current relaxation is directly linked with buried oxide charge changing.
If the BOX charge depends on the time and temperature as:

$$Q_{BOX}(t,T) = Q_{BOX}(t=0) \exp\left[-\frac{t}{\tau(T)}\right] \qquad (10)$$

the relaxation time, $\tau(T)$, can be calculated from slope angle tangent of the following dependence:

$$\ln \frac{I_{sd}(t) - I_{sd}(\infty)}{I_{sd}(0) - I_{sd}(\infty)} = -\frac{t}{\tau} , \qquad (11)$$

where $I_{sd}(0)$ and $I_{sd}(\infty)$ are the source-drain current at first and at final moment, respectively.
The measurement of source-drain current relaxation at different temperature allows the activation energy of the instability processes to be determined.
Thus, a combination of the C-V and the TSP/TSD current methods with I_{sd}-V_{bg} characteristics of MOSFETs fabricated on the same SOI wafer opens a wide range of possibilities for the study of high-temperature instability processes in the BOX.

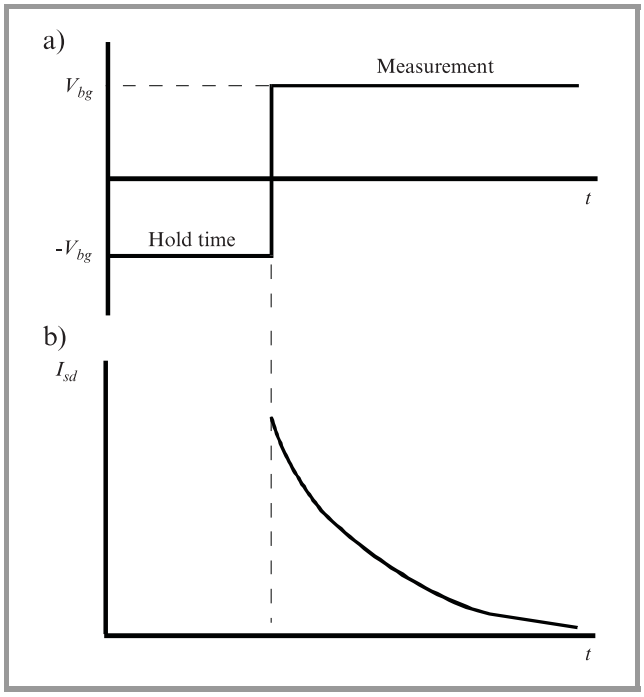

Fig. 4. A schematic diagram for (a) back-gate voltage switching and (b) measurement of the relaxation current.

3. High-temperature instability in buried oxide of SOI structures

3.1. Structure fabricated by zone-melting recrystallization technique

The SOI structures used in this study have been fabricated by the laser zone-melting recrystallization (LZMR) technique [10]. A linear melted zone was formed by a high-power CW YAG:Nd laser. A circular laser beam was transformed into a linear spot with thickness of 0.1 mm using special cylindrical lenses. In order to provide a low thermal gradient regime the wafer was heated up to 1300°C from the back side by a set of halogen lamps. Recrystallized structure was composed of a 400 nm thick poly-Si film deposited on silicon wafer thermally oxidized at high pressure ($d_{BOX} = 360$ nm) and covered by a SiO_2 cap layer to prevent agglomeration of the molten zone. SOI capacitors (Al-Si-SiO_2-Si-Al) were fabricated by LOCOS technique after recrystallization of polysilicon film.

Measurements of the C-V characteristics of LZMR SOI capacitors before and after TSP and TSD processes up to 400°C has led to the conclusion that the BOX/semiconductor interfaces in this material are almost blocking (Table 1) [11]. Bias application to the SOI structure at high temperature leads to charge movement from one interface to the other. During this movement only 10% of the charge is lost. Comparison of the total net charge in the BOX, obtained by C-V method, with moving charge in the BOX, obtained by TSP/TSD current method, helps us to conclude that almost all of the positive charge, which is trapped in the BOX, participated in the observed movement of charge.

Table 1
Total, Q_{tn} and mobile charges, Q_{TSP} and Q_{TSD}, and charge centroid in buried SiO_2 in ZMR SOI structures

Q_{tn} [cm^{-2}] (C-V)			$\overline{X}_0$ [Å] (C-V)			Q_{TSP}	Q_{TSD}
initial	after TSP	after TSD	initial	after TSP	after TSD	[cm^{-2}]	[cm^{-2}]
$1 \cdot 10^{12}$	$8.3 \cdot 10^{11}$	$9.4 \cdot 10^{11}$	1070	1900	380	$5 \cdot 10^{11}$	$7 \cdot 10^{11}$

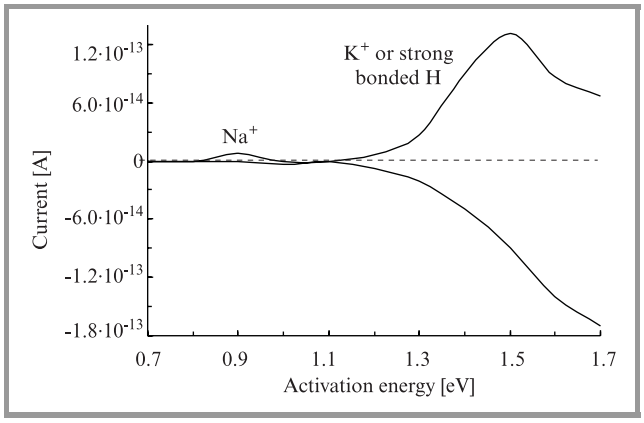

Fig. 5. TSP/TSD current spectra measured in ZMR mesa structures ($\beta = 0.3$°C/s).

Investigation of thermal polarization/depolarization processes (Fig. 5) [11] makes it possible to suggest that a small low-temperature current peak (located in temperature range from 50 to 100°C) with activation energy ranging from 0.75 to 0.9 eV can be related to Na^+ ions whilst the high-temperature current peak, located in the temperature range from 200 to 400°C with the activation energy from 1.2 to 1.7 eV is due to the movement of K^+ ions or to strongly bonded hydrogen.

3.2. SOI structures fabricated by single implanted SIMOX technique

The SOI structure used in this study has been fabricated by the standard single implanted SIMOX technique. The implanted dose was $1.8 \cdot 10^{18}$ O^+/cm^2, the energy of implantation was 200 keV, and the temperature of implantation was 600°C. Post-implantation annealing was performed at 1320°C in Ar + 2% O_2 for 6 hours. After wafer processing the thickness of the BOX was 360 nm.

Investigation of the high-temperature stability of the charge in the BOX layer in SIMOX SOI structures using C-V and TSP/TSD current methods has shown [12] considerable distinction of this material from LZMR SOI one.

It should be noted that at first measurement of TSP and TSD processes there is a significant difference between the values of the polarization and depolarization current in SIMOX samples which is greater than a factor of 5 (Fig. 6). Next, the current peaks are completely asymmetric, from which it is concluded that different processes are involved during polarization and depolarization. In addition, after thermal polarization when a negative voltage is applied to the substrate a positive charge buildup in the BOX is observed; whilst a positive voltage applied to the substrate leads to negative charge accumulation, which compensates the positive charge in the BOX. In each case a considerable variation in the charge close to the BOX/substrate interface is observed whilst a very small charge change occurs near the BOX/silicon film interface (Table 2).

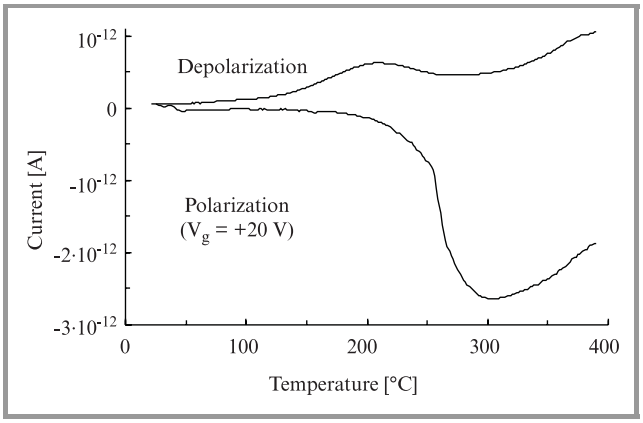

Fig. 6. The TSP/TSD current spectra measured in SIMOX mesa structures.

The important point is similar changing of total charge in the BOX obtained from C-V (ΔQ_m^{sub}, ΔQ_m^f) and TSP (Q_{TSP}) measurements at polarization up to 250°C, that can be considered as the BOX/semiconductor interfaces in SIMOX structure are almost electrically blocking in this temperature range. After thermal polarization up to 400°C the charge measured from TSP current is considerably higher than the transported charge determined from C-V measurements. This may be an evidence of electrical unblocking properties of the BOX/semiconductor interfaces in SIMOX structures at temperatures ranging from 250 to 400°C.

The activation energy of the main polarization process (observed at a negative bias applied to the substrate), determined by the fractional thermal cleaning method, is 1.2 eV. Charge movement during this polarization process at first measurement may reach the value of $1.1 \cdot 10^{12}$ cm^{-2} (see Table 2). In the case of depolarization at zero applied voltage we observed two small current peaks from which the activation energy can be only roughly estimated.

Table 2
The charges, obtained from C-V characteristics and from TSP current technique (Q_{TSP}) and charge centroid for SIMOX structures

Kind of treatment	Parameters							
	ΔQ_{sub} [cm^{-2}]	ΔQ_f [cm^{-2}]	ΔQ_{tn} [cm^{-2}]	$\overline{X}_0$ [Å]	Q_{TSP} [cm^{-2}]	ΔQ_m^s [cm^{-2}]	ΔQ_m^f [cm^{-2}]	ΔQ_{tr} [cm^{-2}]
Initial	$-3\cdot10^{10}$	$6.8\cdot10^{11}$	$6.5\cdot10^{11}$	3600				
Polarization (250°C)	$1.4\cdot10^{11}$	$6.2\cdot10^{11}$	$7.6\cdot10^{11}$	2680	$1.8\cdot10^{11}$	$1.7\cdot10^{11}$	$-5.8\cdot10^{10}$	$1.1\cdot10^{11}$
Polarization (400°C)	$9\cdot10^{10}$	$7.4\cdot10^{11}$	$8.3\cdot10^{11}$	3270	$1.1\cdot10^{12}$	$1.2\cdot10^{11}$	$6\cdot10^{10}$	$1.8\cdot10^{11}$

We think that the thermal polarization process at negative voltage applied to the substrate of SOI structure is associated with electron emission from traps located near the BOX/substrate interface. The capture cross section for these traps determined from TSP current peak is $8\cdot10^{-18}$ cm^{-2}. It should be noted that the flat-band voltage at the BOX/substrate interface is about zero, which is attributed to the complete compensation of the electrical charge located near this interface.

4. High-temperature instability of SOI MOSFETs

4.1. High-temperature kink-effect of back-channel SOI n-MOSFETs

The processes of charging and discharging in the BOX at high temperature can lead to some unusual effects in the MOSFETs. In the paper [3] a new high-temperature effect in the SIMOX SOI n-MOSFET named the high-temperature back-channel kink-effect has been described. This effect appears in fully depleted (FD) inversion mode (IM) n-MOSFETs, fabricated on single implanted SIMOX SOI wafer, when a negative voltage is applied to the substrate at a temperature above 200°C and thereafter the back-gate (substrate) voltage, V_{bg}, is rapidly swept to a positive value. Under these conditions and with a bias at back gate about zero it was observed that a jump occurs in the source-drain current (Fig. 7). This current jump increases with increasing temperature and hold time of negative voltage applied to the substrate prior to the back-gate voltage sweeping and tends to saturation for high-temperature measurements and for long hold times (Fig. 8a).

The current jump cannot be related to the floating-body effects in the SOI MOSFET because the drain voltage is low during the measurements (0.1 V) and the measurements are performed at high temperature, when the floating body effects have to be suppressed [13, 14]. In order to check that special experiments on the SOI MOSFETs with contact to silicon film have been performed. The source-drain current jump near zero back-gate voltage have been observed beginning from 200°C and have not disappeared when silicon film was grounded. Thus, it is believed that charging and discharging processes in the BOX of the SOI structure are responsible for the observed phenomenon [15, 16].

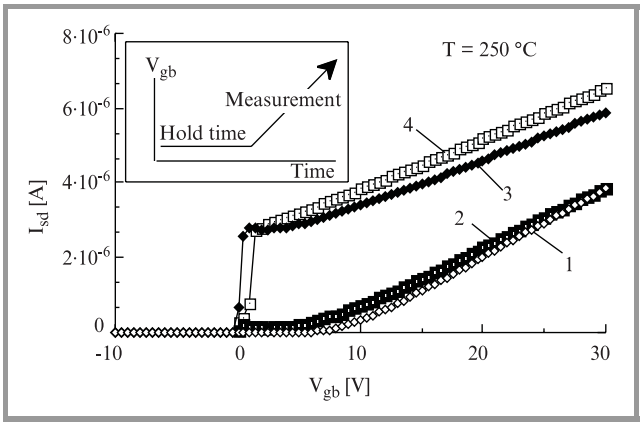

Fig. 7. Drain current versus back-gate voltage for different sweep rates: initial characteristic (sweep rate is 50 V/s) (*1*); the characteristics measured after keeping back gate at −30 V during 150 s and when a sweep rate equals to 1.7 V/s (*2*), 5 V/s (*3*) and 50 V/s (*4*).

The drain-current jump has been explained by the following processes taking place in the BOX of the SOI MOSFET. Firstly, when negative voltage is applied to the substrate at high temperature, a positive charge is accumulated in the BOX. Since this positive charge does not result in an increase of the channel current in the MOSFET, it has been concluded that this positive charge is compensated by a negative electron charge easily injected from the substrate (Fig. 8b). Accumulation of the positive charge has been suggested to be associated with electron extraction from traps located near the BOX/substrate interface. Secondly, when the back-gate voltage approaches to zero, the electrons, located in the vicinity of the BOX/substrate interface, recombine with the thermally generated holes in this region and cannot further compensate the positive charge in the BOX (Fig. 8c). Thus, a sharp increase of the drain current is observed. Thirdly, when a positive voltage is

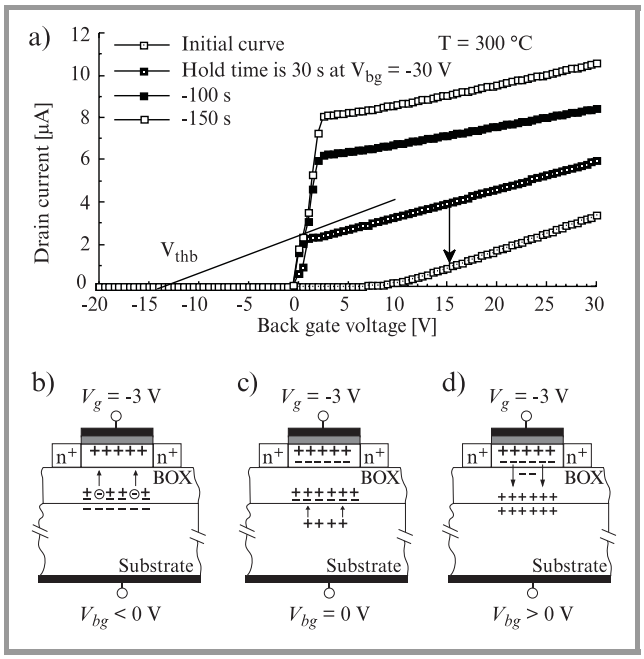

Fig. 8. Drain current versus substrate voltage for different hold times at −15 V (arrow signifies the direction of current relaxation) (a), schematic illustration of the positive charge accumulation in the BOX at $V_{bg} < 0$ V (b), electron recombination at $V_{bg} = 0$ V (c) and the neutralization of the positive charge at $V_{bg} > 0$ V (d).

applied to the substrate, the positively charged traps in the BOX are compensated by electrons injected from the channel of the MOSFET (Fig. 8d). In this case a change in the slope of the I_{sd}-V_{bg} – characteristic in dependence of the back-gate voltage sweep rate (Fig. 7) and of the magnitude of the current jump (that is the value of a positive charge accumulated in the BOX) (Fig. 8a) has to be observed.

Using the above considered model and studying the processes of positive charge accumulation (charging) and relaxation (discharging) in the BOX, the parameters of traps associated with these processes have been estimated.

4.2. BOX trap parameters extraction from high-temperature kink-effect of back-channel SOI n-MOSFET

It was shown [15], that the positive charge accumulation in the BOX can be investigated by measuring the magnitude of a drain current jump at different temperatures and hold times of a negative voltage applied to the substrate.

In order to estimate the threshold voltage in the presence of a high-temperature kink effect while taking into account the discharging effect it was suggested to draw the line parallel to the initial I_{sd}-V_{bg} – characteristic and passing through the point of the measurement characteristic where the jump is observed (Fig. 8a). The intersection of this line with the voltage axis gives the desired threshold voltage [15]. Using this method the values of positive charge accumulated in the BOX at different temperatures have been obtained (Fig. 9). From these dependences the maximum accumulated positive charge, Q_{BOXm}, activation energy of the process of

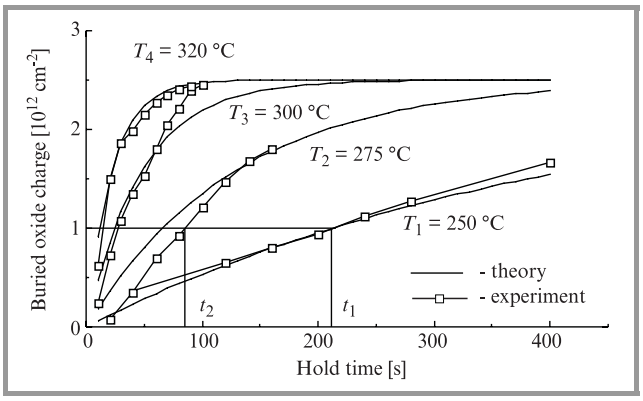

Fig. 9. Theoretical and experimental dependences of positive accumulated charge in the BOX on time at different temperatures.

electrons escaping from the trap, E_a, and capture cross section of the traps at room temperature, S_t, have been determined. It was found that Q_{BOXm} equals to $2.5 \cdot 10^{12}$ cm^{-2}, E_a is 1.1 ±0.1 eV and S_t is $2 \cdot 10^{-17}$ cm^2. These values are very similar to those obtained from TSP/TSD current measurements on the same SIMOX SOI structures (see part 3.2).

From studying the drain current relaxation (see part 2.4) at different temperature the activation energy of discharging process that has been equaled to 0.65 eV has been estimated [15]. It has been suggested that electron trapping is associated with multiphonon emission processes, which are an inherent feature of oxygen vacancy defect (E′-center) in dioxide [17].

Comparison of experimentally obtained trap parameters with the published ones [18÷21] leads to conclusion that the observed deep traps, responsible for high-temperature instability in the BOX are possibly related to oxygen vacancies which are capable to trap and release the electrons at high temperature [22, 23].

4.3. High-temperature kink-effect of front-channel FD SOI n-MOSFET

Positive charge accumulation in the BOX of FD SOI IM n-MOSFET can result in additional high-temperature instability of the MOSFET [24, 25]. This phenomenon is simply observed when the set of I_{sd}-V_g characteristics is measured in dependence of back-gate voltage changing at high temperature. If, at first, the back-gate voltage is negative, the I_{sd}-V_g curves show the jump of the current in the vicinity of the zero gate voltage when the back-gate voltage reaches the positive values (Fig. 10a). In the other case, when in the beginning of the set of measurements the back-gate voltage is positive, the I_{sd}-V_g curves have a usual form for all voltages at the substrate (Fig. 10b).

It is worthy noting that this current jump, as well as the high-temperature kink-effect of back-channel MOSFET, depends on the temperature of measurements and is created by the above mentioned condition at the temperatures higher than 200°C (Fig. 11). The observed phenom-

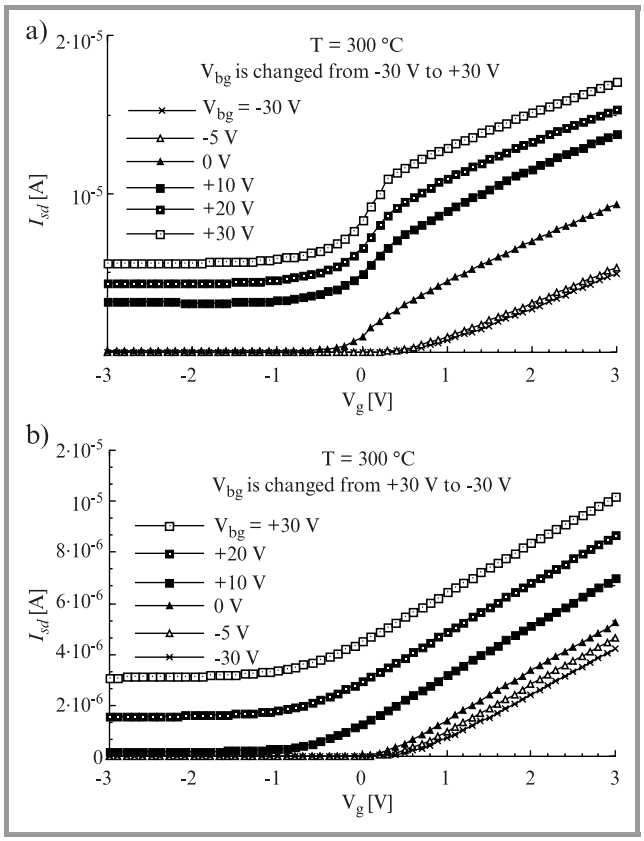

Fig. 10. Source-drain current versus gate voltage for different substrate voltages (V_{bg}) at 300°C when substrate voltage is swept from -30 V to $+30$ V (a) and from $+30$ V to -30 V (b).

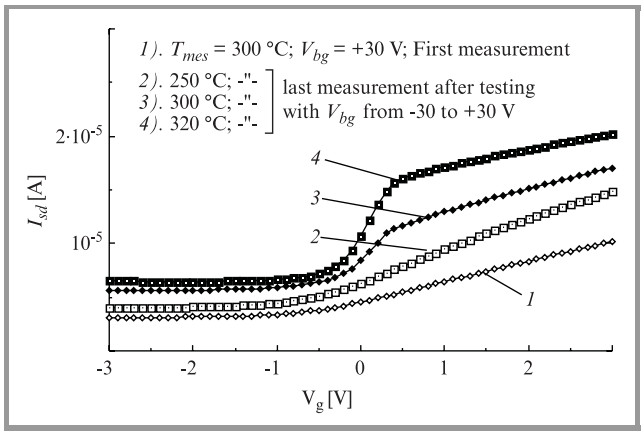

Fig. 11. Source-drain current versus gate voltage for different temperature and sequence of measurement.

ena were named as high-temperature kink-effect of front-channel MOSFET [24].

In the papers [24, 25] the direct link of the drain current jump in the front MOSFET and the positive charge creation in the BOX has been demonstrated. Indeed, the application of negative voltage to the substrate for 150 s at a temperature 250°C leads only to a small shift of the I_{sd}-V_g curve towards more negative gate voltage values, showing that some small positive charge is produced in the BOX

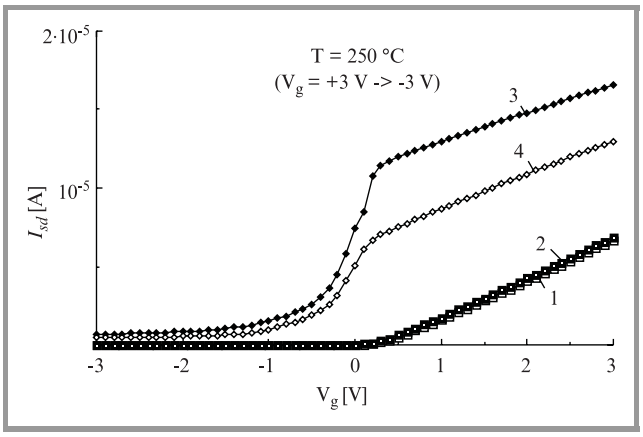

Fig. 12. Source-drain current versus gate voltage in dependence on conditions of the substrate: (*1*) $V_{bg} = -30$ V, hold time is 0 s; (*2*) $V_{bg} = -30$ V, hold time is 150 s; (*3*) $V_{bg} = -0$ V, hold time is 0 s after stressing at $V_{bg} = -30$ V for 150 s; (*4*) $V_{gb} = 0$ V, hold time is 150 s.

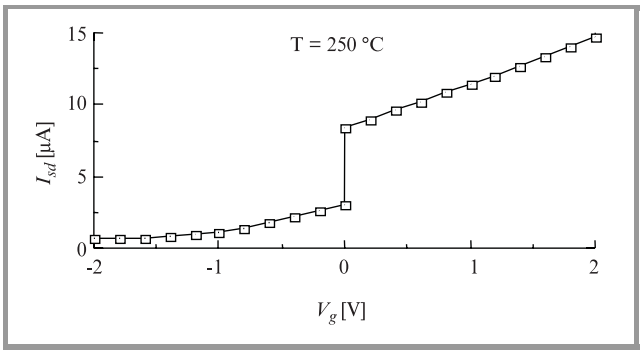

Fig. 13. MEDICI simulation of the drain current „jump". For $V_g > 0$ the curve was calculated for the case of a uniform positive charge distribution as a function of depth in the BOX. The positive charge $3.5 \cdot 10^{17}$ cm^{-3} is uniformly distributed within a distance of 200 nm from the BOX/substrate interface. For $V_g < 0$ the curve was calculated for the same positive charge distribution, but where $1.05 \cdot 10^{12}$ cm^{-2} electron charge is located in the BOX near the BOX/silicon film interface.

(curve *1* and *2* in Fig. 12). In this case as it was shown in [15] the positive charge, compensated by electrons from substrate, are accumulated in the BOX (see Fig. 8b). If the substrate voltage is switched to zero, the discompensation of the positive charge in the BOX (see Fig. 8c) takes place and considerable current increase and formation of a current jump appears (curve *3* in Fig. 12). After that, if the drain, the source and the substrate are shortened for 150 s, the values of the drain current and the magnitude of the current jump decrease (curve *4* in Fig. 12). This attests that the compensation of the positive charge in the BOX (the process is shown in Fig. 8c) leads to the decrease of the current jump in the I_{sd}-V_g characteristics.

The phenomenon can be due to simultaneous influence of two effects. The first one is related to gate voltage influence (due to charge coupling effect) on trapping of electrons from the back channel of the MOSFET into the electron

traps located in the BOX near the BOX/silicon film interface when the negative voltage applied to the gate. The second one is associated with considerable positive charge built-up into the BOX. At positive voltage applied to the gate an electric field at the BOX/silicon film interface decreases that leads to electrons release from the traps and increase of drain current. 2D MEDICI simulation [26] of this effect is presented in Fig. 13.

5. Conclusions

The developed complex of high-temperature methods for SOI capacitors and MOSFETs allows the processes of charge building up and neutralization in buried dielectrics of SOI structures and effect of this charge on SOI MOSFET operation to be studied.

In the LZMR SOI structures the BOX/semiconductor interfaces are almost electrically blocking up to 350°C, which leads to small discharging of internal BOX charge through these interfaces. The main processes of charge instability at high temperature in LZMR SOI BOX are linked with an ionic charge transport and determined by technological process cleanness.

In SIMOX SOI structures the BOX/semiconductor interfaces (especially the BOX/substrate interface) are electrically unblocking at temperatures above 200°C. This leads to considerable charge exchange through these interfaces at high temperatures. The building up of positive charge in SIMOX BOX and its neutralization is determined by charging processes of structural defects located near the BOX/substrate interface (for example, oxygen vacancies and oxygen vacancy complexes).

Positive charge incorporated into SIMOX BOX can lead to instability of the MOSFET high-temperature operation, which appears as uncontrolled MOSFET threshold voltage shift and drain current jump near zero gate voltage.

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