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Invited paper

Reliability of deep submicron MOSFETs

Francis Balestra

Abstract — In this work, a review of the reliability of n- and p-channel Si and SOI MOSFETs as a function of gate length and temperature is given. The main hot carrier effects and degradations are compared for bulk and SOI devices in a wide range of gate length, down to deep submicron. The worst case aging, device lifetime and maximum drain bias that can be applied are addressed. The physical mechanisms and the emergence of new phenomena at the origin of the degradation are studied for advanced MOS transistors. The impact of the substrate bias is also outlined.

Keywords — bulk MOSFETs, SOI devices, deep submicron transistors, reliability.

1. Introduction

It is well known that hot-carrier-induced device degradation (creation of interface states and/or positive and negative trapped charges by electron or hole injection) can limit the long-term reliability of deep submicron MOSFETs (reduction of transconductance and drain current, shift of the threshold voltage). The impact ionization phenomenon is one of the main hot carrier effects [$1 \div 6$]. We can distinguish two stress regimes, which depend on the electron energy. The first one corresponds to the primary impact ionization in maximal substrate current condition ($V_g \cong V_{d/2}$). The second stress regime corresponds to the secondary impact ionization in maximal gate current condition ($V_g \cong V_d$). The longitudinal electric field responsible for the primary impact ionization produces hot carriers with energy around 1.5 eV [3]. Monte Carlo simulations have shown that the secondary ionization generates hot carriers with energy values higher than $3 \div 3.5$ eV after a secondary heating in the drain/substrate junction. These energies correspond to the interface state threshold energy [4, 5]. The interface state creation is one of the major causes of device degradation. Nevertheless, several issues are still not clear up to now:

1. What is the worst case aging condition (maximum substrate or gate currents) as a function of gate length and temperature?
2. Which physical mechanisms are at the origin of the main degradation for advanced devices?
3. Is there some differences for the aging of bulk Si and SOI MOSFETs?
4. What are the lifetime and maximum drain bias which can be applied as a function of device architecture?

In this work, the hot carrier phenomena and degradation in various regimes of n- and p-channel bulk silicon and silicon-on-insulator MOSFETs are studied in a wide range of gate length down to deep submicron as a function of temperature.

2. Results and discussion

2.1. Bulk Si MOSFETs

Figure 1 shows the secondary impact ionization mechanisms. The first ionization leads to electron/hole pairs. The electrons flows towards the drain for a n-channel MOSFET and the holes are heated in the drain substrate junction where high electric fields exist for advanced MOSFETs due to high substrate doping. These holes gain high energies and can induce a second impact ionization leading to electrons/holes pairs. The holes constitute the substrate current and the electrons can be injected into the gate in particular for deep submicron devices realized with ultra-thin gate oxides leading to high transverse electric field. These electrons are at the origin of the gate current or can be trapped in this oxide.

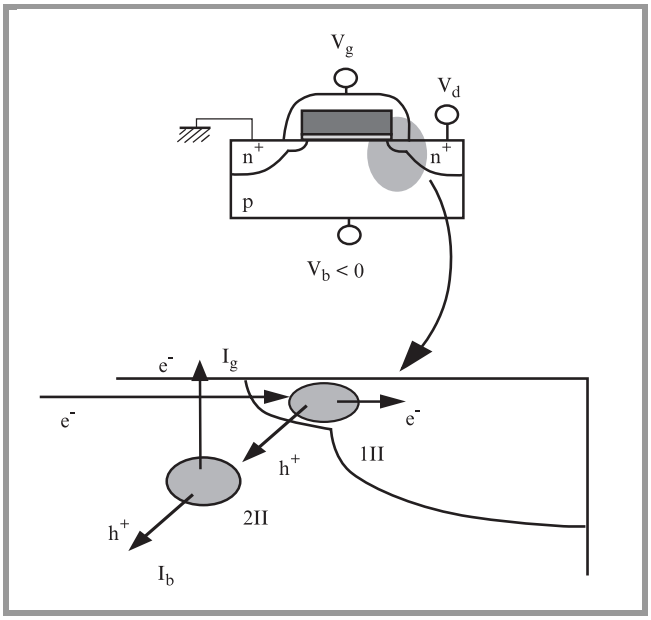

Fig. 1. Secondary impact ionization mechanisms.

Figure 2 exemplifies the gate current as a function of the substrate bias for a 0.45 μm MOSFET of a 0.1 μm technology with a 3.5 nm gate oxide [7]. The substrate bias is used in this experiment in order to enhance the electric field at the drain/substrate junction leading to a higher secondary impact ionization. The gate current induced by

this secondary heating obtained with a model based on the lucky electron concept is also shown in this figure. The good agreement observed between theory and experiment confirms the origin of this gate current. Therefore these additional hot carrier effects will play a major role for determining the worst case degradation and the reliability of advanced MOS transistors.

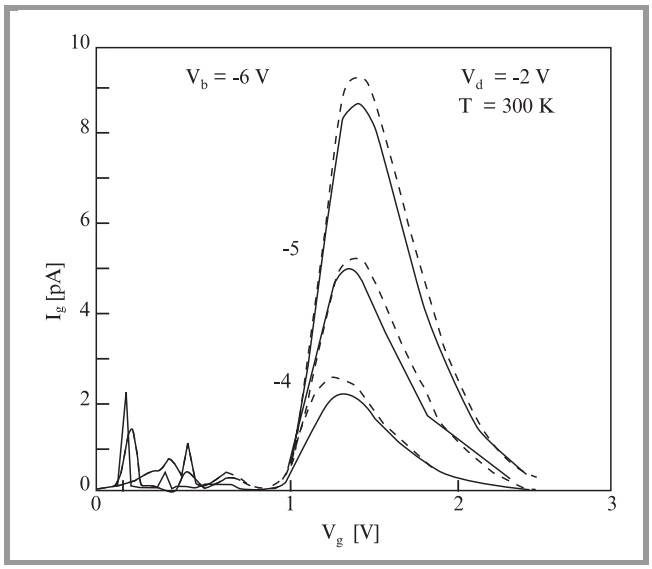

Fig. 2. Comparison between model and experimental data for the gate current of advanced bulk Si devices (0.45 μm N-MOSFET of a 0.1 μm technology with a 3.5 nm gate oxide) taking into account the secondary impact ionization.

Figure 3 is a plot of the impact of temperature on the gate current characteristics. I_g is substantially increased at low temperature even for a low drain voltage (2 V). The model taking into account the secondary impact ionization is also in good agreement with the experimental data.

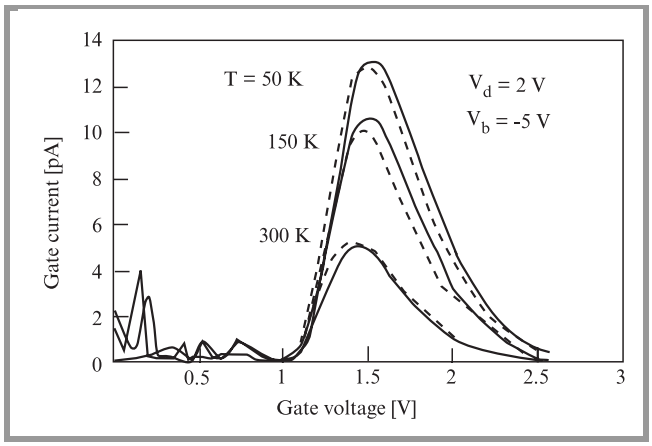

Fig. 3. Impact of temperature (experiment and modeling) on the $I_g\,(V_g)$ characteristics for a 0.45 μm bulk N-MOSFET of a 0.1 μm technology with a 3.5 nm gate oxide.

The number of emitted photons due to hot electrons as a function of energy is plotted in Fig. 4. The impact of the substrate bias on the light emission is also shown. For small energies ($1 \div 1.5$ eV) the substrate voltage has a very small impact. However, for high energies ($2 \div 3$ eV), the number of emitted photons substantially increases at high V_b due to the secondary heating at the drain/substrate junction. These hot carriers can lead to significant device degradation.

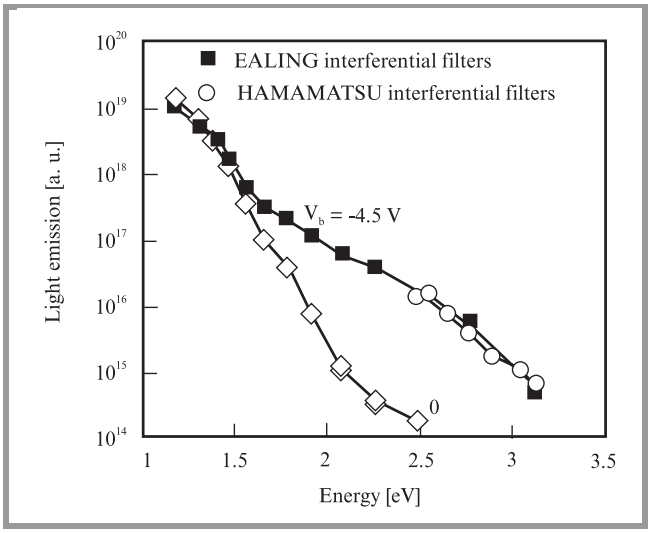

Fig. 4. Impact of the substrate bias on the light emission for deep submicron bulk MOSFETs.

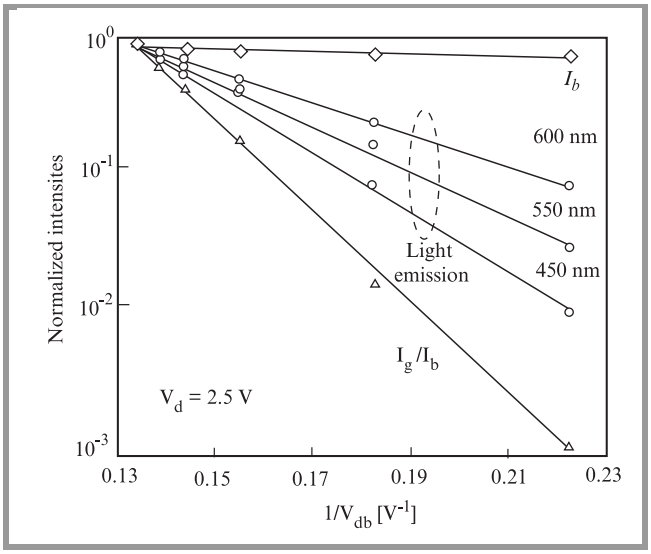

Fig. 5. Correlation between the normalized gate and substrate currents and the wavelength of emitted photons for bulk silicon n-channel MOSFETs.

Figure 5 presents the correlation between the light emission and the normalized gate and substrate currents. For long wavelengths, the variation of the light emission is similar to that of the substrate current (first heating), and for small wavelengths it is correlated with the gate current (second heating).

The impact of both the channel length and temperature on the worst case aging is exemplified in Fig. 6 [8]. For long devices, the worst case corresponds to the maximum substrate current ($V_g \cong V_{d/2}$) except for very low temperatures. However, for deep submicron devices (0.1 μm range) the limit between the two worst case regimes ($V_g = V_{d/2}$ or V_d) is observed in the room temperature range. Therefore, the maximum gate current ($V_g \cong V_d$) could become the worst case degradation even at 300 K. Furthermore, in the traditional operating range (between -50°C and 100°C) the worst case can shift from a regime to another one for advanced MOSFETs.

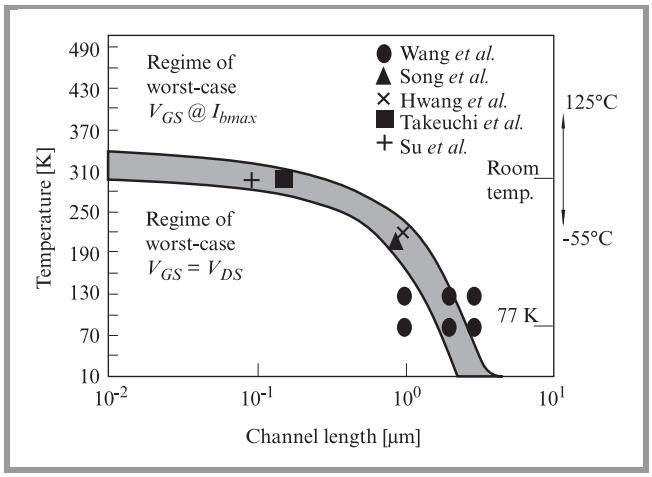

Fig. 6. Impact of channel length and temperature on the worst case degradation (bulk NMOS).

The influence of the substrate voltage for various temperatures is exemplified in Fig. 7. The significant impact of the substrate bias on the transconductance degradation both at 300 and 77 K demonstrates that the secondary heating plays a major role in the reliability of the devices. The maximum drain bias which can be applied in order to obtain a ten years lifetime (criterion: 10% transconductance degradation under static stress) is analyzed for 0.2 μm MOS transistors. The worst case aging leading to the minimum $V_{d\max}$ is obtained for a stress in $I_{g\max}$ condition both at room and liquid nitrogen temperatures (Fig. 8). In addition, a stronger degradation is always observed at 77 K as compared to 300 K, even in the case of $I_{b\max}$ stress (Fig. 8). In this regime, a smaller substrate current and impact ionization rate have been previously shown, but the enhancement of carrier trapping and the larger influence of a given degradation on the electrical properties at low temperature could explain this special behavior.

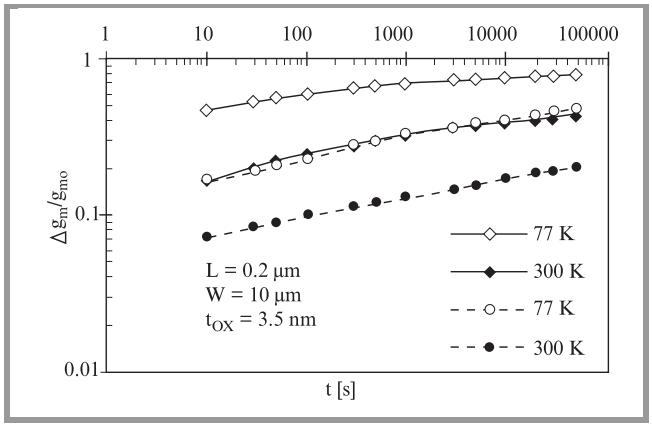

Fig. 7. Impact of substrate bias for bulk N-MOSFET devices on transconductance degradation for $I_{g\max}$ stress ($V_b = -3$ V full lines, $V_b = 0$ V dashed lines).

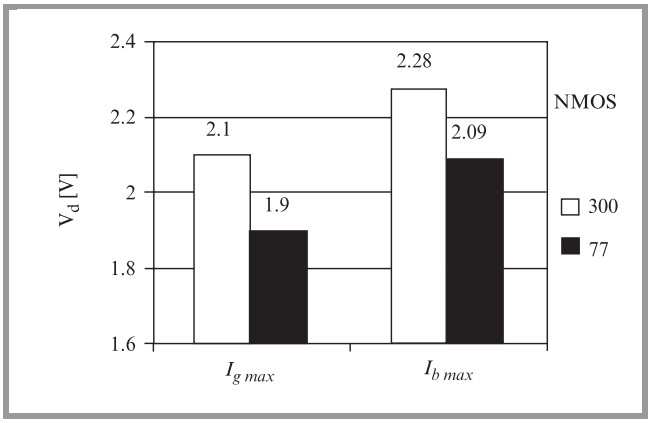

Fig. 8. Maximal drain voltage in order to obtain 10% transconductance degradation after 10 years for bulk N-MOSFET (W/L = 10/0.2, $t_{ox} = 3.5$ nm); static stress.

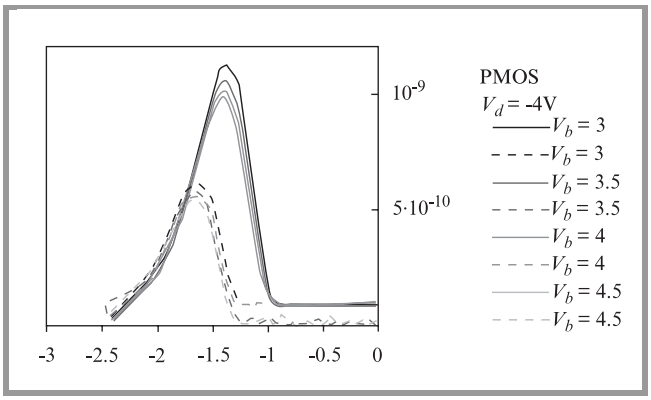

Fig. 9. Typical $I_g(V_g)$ characteristics obtained at $V_d = -4$ V for different substrate voltages at 300 K (full lines) and 77 K (dashed lines) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

Therefore, the impact of the secondary hot carrier effects is clearly demonstrated at room and low temperature for advanced n-channel MOSFETs.

Figure 9 exemplifies the typical gate current characteristics for a 0.2 μm p-channel bulk Si MOSFET. An electron current is found whatever the substrate and drain biases are. The substrate voltage has only a very low influence on the gate current level (small reduction with increasing the substrate bias). These results show that the influence

of the secondary impact ionization is negligible for PMOS devices. Furthermore, contrary to the case of n-channel MOSFETs, I_g is reduced for lower temperatures (Fig. 9).

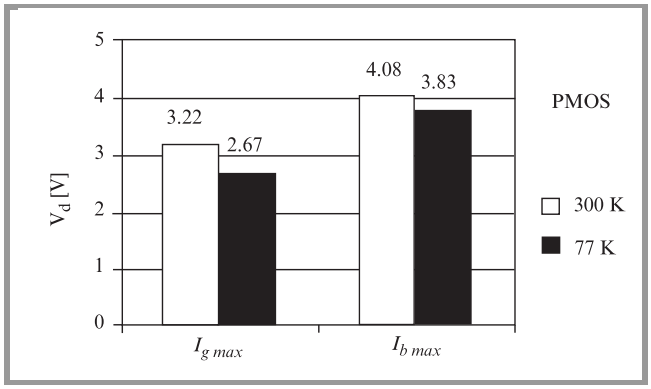

Fig. 10. Maximal drain voltage in order to obtain 10% transconductance degradation after ten years (static stress) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

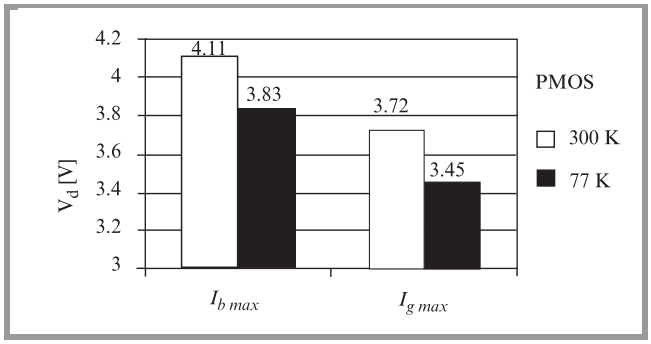

Fig. 11. Maximal drain voltage in order to obtain 100 mV threshold voltage degradation after ten years (static stress) (bulk PMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm).

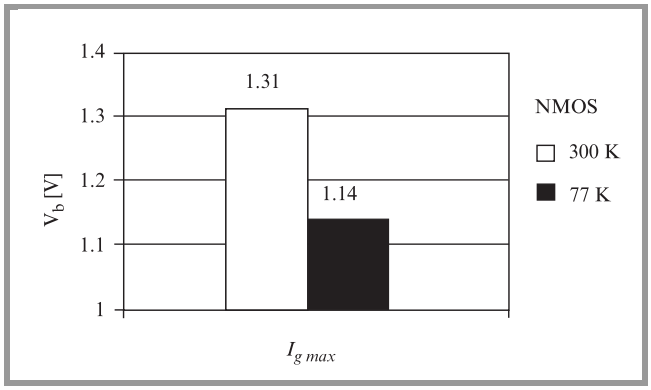

Fig. 12. Maximal substrate voltage in order to obtain 10% transconductance degradation after ten years (static stress) (bulk NMOS, W/L = 10/0.2, $t_{ox} = 3.5$ nm, $V_d = 2$ V).

The maximum drain bias which can be applied in order to obtain a ten years lifetime (criterion: 10% transconductance degradation under static stress) is shown in Fig. 10. The worst case aging is obtained for a stress performed at $V_g = V_d$ (noted „$I_{g\max}$"). However, it is worth noting that the maximum gate current is reached for a gate voltage substantially lower than the drain bias in the case of P-MOSFETs (see Fig. 9). The drain voltage $V_{d\max}$ for a 10 years lifetime is also reduced at 77 K as compared to room temperature operation, even if the substrate and gate currents are smaller at liquid nitrogen temperature. Therefore, for deep submicron devices, a stress at $V_g = V_d$ for a 77 K operation is always the worst case for PMOS and NMOS. A similar trend is observed for the threshold voltage degradation (Fig. 11).

The maximum substrate bias, which can be applied in order to obtain a 10 years lifetime for a 0.2 μm bulk Si N-MOSFET, is illustrated in Fig. 12. A nominal bias (2 V) is applied for this 0.2 μm technology. $V_{b\max}$ is around 1.3 V at 300 K and 1.1 V at 77 K, which shows that the applied substrate bias could become a limitation in some applications.

2.2. SOI MOSFETs

The SOI technology is well known for its advantages as compared to bulk devices, in particular in the field of low voltage/low power and high frequency applications [9, 10]. However, SOI MOSFETs can suffer from possible degradation of the front and the buried silicon/oxide interfaces. Furthermore, another hot carrier regime associated with the parasitic bipolar transistor triggered at high V_d can be harmful for deep submicron SOI devices. Therefore, it is necessary to perform a thorough evaluation of these effects as function of the SOI transistor architecture.

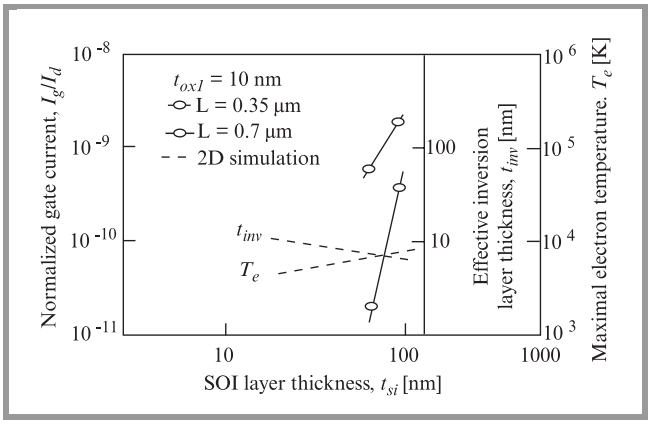

Fig. 13. Comparison between the variations of the normalized gate current, the inversion layer thickness and the electron temperature versus Si film thickness for fully depleted SOI MOSFETs.

In Fig. 13 the dependence of the normalized gate current versus the silicon film thickness is plotted [11]. The gate current is reduced for thinner films whatever the gate length is. This interesting behavior is partially attributed to the increase of the inversion layer thickness in fully depleted SOI films which is induced by the reduction of the transverse electric field. This phenomenon leads to a reduction of carrier temperature. However, another possible effect in order

to explain the decrease of hot carrier effects is the lowering of the secondary impact ionization. Indeed, in thin film SOI, the area of the drain/substrate junction decreases as compared to thick Si layers or bulk MOSFETs, and therefore a reduction of the number of high energy carrier is obtained. Moreover, the reduction of the transverse electric field also leads to a smaller injection probability into the gate.

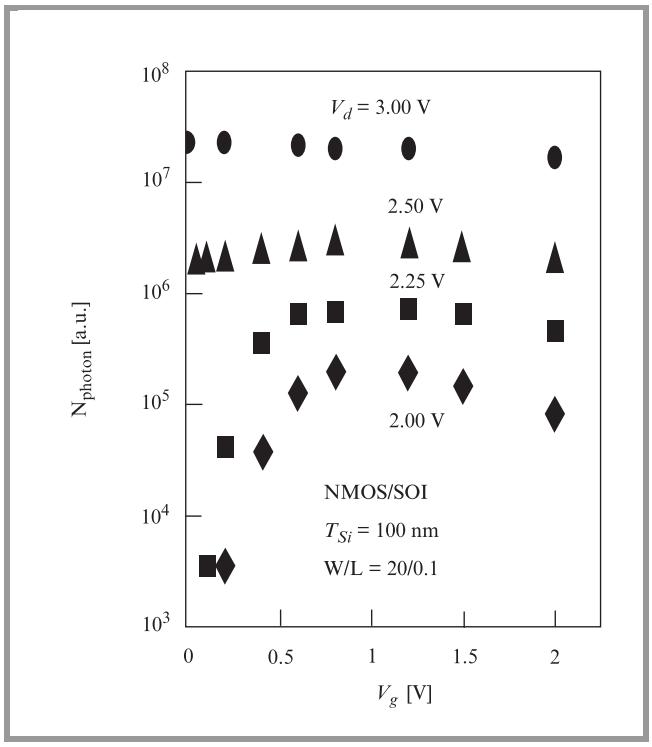

Fig. 14. Number of emitted photons in 0.1 μm n-channel SOI MOSFET versus gate and drain biases.

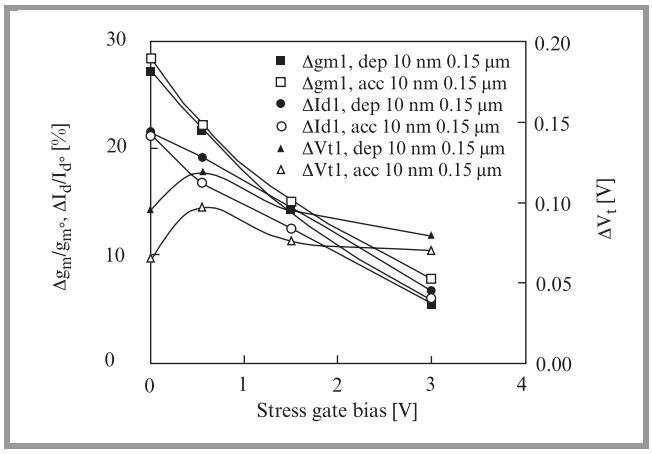

Fig. 15. Device parameter degradation as a function of gate bias for 0.15 μm n-channel SOI MOSFETs realized on an ultra-thin (10 nm) Si film thickness measured with accumulated or depleted opposite interface.

However, another typical SOI mechanism associated with the floating body has to be taken into account for long term device reliability. Figure 14 shows the number of emitted photons for a 0.1 μm SOI MOSFET versus gate and drain biases [12]. For small gate and high drain voltages, a large increase of the photon number is observed due to the parasitic bipolar transistor (PBT) action inducing high energy carriers. Contrary to the case of bulk Si MOSFETs, as illustrated in Fig. 15 for a 0.15 μm fully depleted SOI device fabricated on a 10 nm Si layer thickness, the worst case aging is obtained for small gate biases $(0 \div V_t)$ due to this PBT action [13].

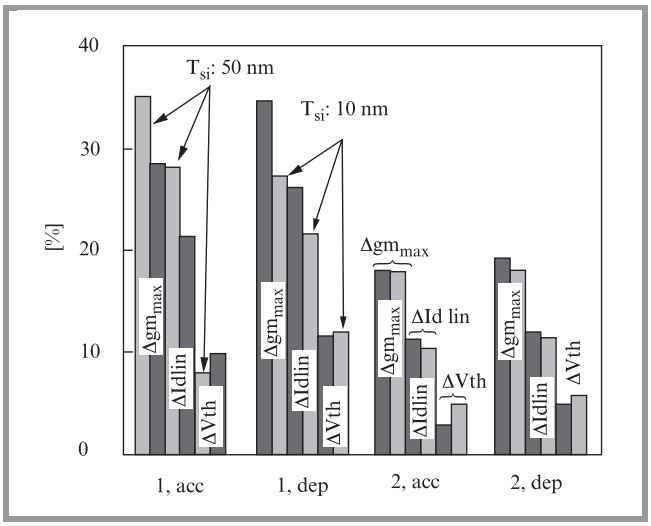

Fig. 16. Device degradation (I_d, gm, V_t) at the front (1) and back (2) interfaces as a function of Si layer thickness (10 and 50 nm) measured with accumulated or depleted opposite interface for n-channel fully depleted SOI MOSFETs.

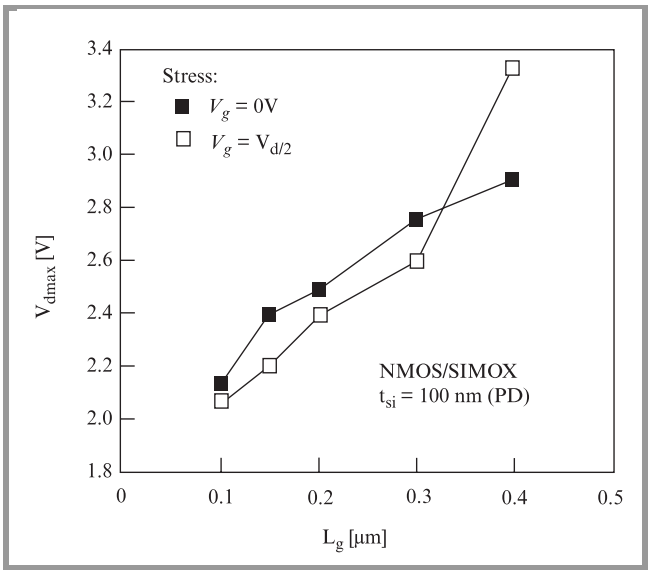

Fig. 17. Maximum drain bias that can be applied in order to obtain 10 years device lifetime (static stress) versus gate length for partially depleted (100 nm Si film thickness) n-channel SOI MOSFETs.

Figure 16 presents the impact of the Si film thickness on fully depleted SOI device degradation in the PBT regime [13]. It is clear that a reduction of the transconductance and drain current degradation is obtained with reducing the SOI layer thickness. In particular, a significant decrease of the front interface aging is observed, while similar degradations are observed for the back interface due to larger interface coupling in ultra-thin films.
The reliability of partially depleted SOI MOSFETs is exemplified in Fig. 17 [12]. The maximum drain bias which can be applied in order to obtain a 10 years lifetime is shown. For this device architecture, the worst case aging with a minimum $V_{d\max}$ is observed in the maximum substrate current condition $(V_g = V_{d/2})$ in the deep submicron range. Therefore, contrary to the case of bulk devices, the worst case aging is obtained for low gate voltages $(0 \div V_{d/2})$ in n-channel SOI MOSFETs whatever the device architecture is.

3. Conclusion

A review of the reliability of n- and p-channel bulk Si and SOI MOSFETs as a function of gate length and temperature has been given. The worst case aging, device lifetime and maximum drain bias that can be applied have been addressed. The impact of the substrate bias has also been outlined. The worst case degradation has been found at $V_g = V_d$ (which corresponds to the maximum gate current condition for n-channel) for deep submicron bulk Si MOSFETs whatever the temperature is and for long channel transistors at low temperature. The substantial influence of the secondary impact ionization on the degradation has been clearly demonstrated for very short channel N-MOSFETs. The interest of using ultra-thin film SOI MOS transistors for reducing the secondary impact ionization and device aging has also been pointed out. Contrary to the case of bulk MOSFETs, the worst case aging has been found for small gate biases $(0 \div V_{d/2})$ in all the n-channel SOI devices.

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