JOURNAL OF TELECOMMUNICATIONS AND INFORMATION TECHNOLOGY

Preface

Despite the fact that a range of limitations are beginning to appear as CMOS technology is being raised to ever higher levels of perfection, it is anticipated that silicon will be the dominant material of the semiconductor industry for at least the first half of the 21st century. The forecast for microelectronics development published in 2006 by Semiconductor Industry Association (SIA) reaches ahead to the years 2014–2020. Moreover, a comparison with former SIA forecasts indicates that they become more aggressive (that is more optimistic) with time.

While the development of silicon microelectronics in the past could be attributed mostly to the reduction of the feature size (progress in lithography), today it relies more on new material solutions, such as SOI, SON, SiGe or SiC. The combination of this trend with continuous miniaturization provides the opportunity of improving IC functionality and speed of operation.

Telecommunications and information technology are arguably the most powerful drivers behind microelectronics product development nowadays. Plenty of new applications are being created for fast analog and rf circuits, as well as for information processing ones. It is clear that with the anticipated peak $f_{\max} = 425$ GHz and $f_T = 385$ GHz to be reached by rf SiGe-base bipolar transistors in 2011, according to the 2006 issue of ITRS, a lot of effort must be put into the development of appropriate material, processing, characterization and modeling. While progress in the bipolar technology is impressive, the increase of MOSFET speed is even more so. The same issue of ITRS predicts on-chip clock of 73 GHz for 2020, which will require MOSFET internal switching speed of 12 500 GHz.

High-speed isn't, however, everything. Portable wireless products push, for obvious reasons, for low-power solutions. This trend requires new architectural solutions (e.g., channel thinning), and in consequence, new material, such as SOI (or its possible successor SON), where current driveability is considerably higher than in conventional MOSFETs.

In this issue the Reader will find papers devoted to fabrication (ultra-thin gate dielectrics, DLC and BN layers), characterization (influence of strain on the optical properties of the Si-SiO_2 system, non-uniformity of MOSFET electrical parameters over the gate area,

quality of the dielectric-semiconductor interface) and modeling (strained-Si, SiC MOSFETs) of semiconductor devices. Statistical modeling of process (Monte Carlo) and IC reliability is also addressed, as well as optical interconnects in future ICs.

We hope the Readers will find this issue of the *Journal of Telecommunications and Information Technology* useful and interesting.

Andrzej Jakubowski
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Guest Editors

Paper

Applying shallow nitrogen implantation from rf plasma for dual gate oxide technology

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Abstract—The goal of this work was to study nitrogen implantation from plasma with the aim of applying it in dual gate oxide technology and to examine the influence of the rf power of plasma and that of oxidation type. The obtained structures were examined by means of ellipsometry, SIMS and electrical characterization methods.

Keywords—CMOS, dual gate oxide, gate stack, oxynitride, plasma implantation.

1. Introduction

According to the ITRS roadmap [1] the reduction of the gate dielectric thickness is one of the ways to ensure the increasing level of packing and performance of silicon integrated circuits. In mixed logic/memory circuits manufactured as system on a chip, two different thicknesses of dielectric layers are required. The most advanced solution would be to form both dielectric layers simultaneously, in a single process. This may be possible if oxidation of a silicon layer is preceded with local nitrogen implantation, since the rate of oxidation depends on the nitrogen implantation dose and its profile (e.g., [2, 3]).

The experiments presented in this work are a part of a broader study that examines the possibility of fabricating very thin dielectric layers using ultrashallow nitrogen implantation from rf plasma. As opposed to the methods presented in the literature so far, where classical implanters or the IIIP technique were used for ultrashallow implantation, our process is performed in a typical Oxford plasma technology plasma enhanced chemical vapour deposition (PECVD) planar plasma reactor. The choice of nitrogen source and process parameters for plasma implantation was based on the results of previous studies [4–6].

In this work nitrogen implantation carried out from NH_3 plasma has been immediately followed by either thermal or plasma oxidation process. In this way the influence of oxidation type could be examined.

The aim of this work was to study the feasibility of dual gate oxide technology (Fig. 1) based on rf plasma implantation, as well as to investigate the influence of rf power during implantation and that of oxidation type (conventional versus plasma).

The thickness and nitrogen profile of the obtained layers were investigated by means of ellipsometry and secondary ion mass spectrometry (SIMS) measurements. Test structures were fabricated using NMOS technology with Al gate and electrical characterization was performed to determine selected electrophysical parameters, such as: effective charge and interface trap density, insulating properties and breakdown behavior.

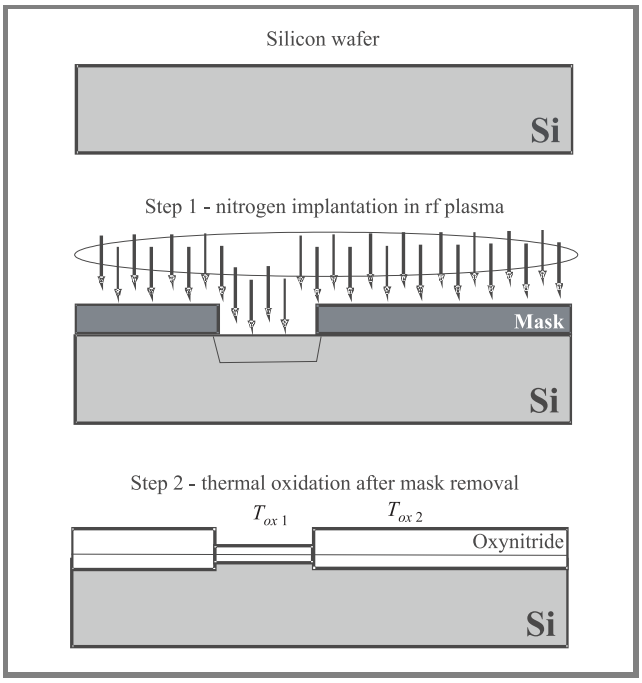

Fig. 1. Dual gate oxide technology – two oxynitride layers with different thickness obtained in a single oxidation process.

2. Experimental

The experiments in this study were carried out in two steps. In the first one, the process of nitrogen implantation from ammonia (NH_3) plasma was performed at 350°C in a PECVD system. The rf power was varied between 100 W, 200 W and 300 W. In the second step, the samples were oxidized either thermally or using a plasma process. Thermal oxidation was performed in dry oxygen diluted in argon (50 ml/min O_2 in 1 l/min Ar) at 1000°C (samples 2–4 in Table 1). Low temperature (350°C) plasma oxidation was performed in oxygen at rf power of 100 W (sample 6 in Table 1). The parameters of thermal and plasma oxidation were chosen based on the results of previous studies [4–6].

Table 1
Summary of process parameters

Parameters	Only thermal oxidation	100 W implantation + thermal oxidation	200 W implantation + thermal oxidation	300 W implantation + thermal oxidation	Only plasma oxidation	100 W implantation + plasma oxidation
Sample no.	1	2	3	4	5	6
Step 1 – nitrogen plasma ion implantation, 350°C, NH_3						
Implantation	no	yes	yes	yes	no	yes
Rf power [W]	no	100	200	300	no	100
Step 2 – oxidation						
Type	Thermal, dry oxygen diluted in Ar, 1000°C				Plasma, 350°C	

Table 2
Results of electrical characterization of NMOS test structures

Parameters	Only thermal oxidation	100 W implantation + thermal oxidation	200 W implantation + thermal oxidation	300 W implantation + thermal oxidation	Only plasma oxidation	100 W implantation + plasma oxidation
Sample no.	1	2	3	4	5	6
Optical thickness D_{ox_opt} [Å]	93	55	49	53	40	40
EOT from *C-V* (@1 MHz)	104	60	38	89	46	75
Effective dielectric constant ε_{eff}	3.4	3.4	4.6	2.2	3.3	2.0
D_{itmb} [1/eV cm^2]	$3.21 \cdot 10^{12}$	$4.93 \cdot 10^{12}$	$8.93 \cdot 10^{12}$	$4.11 \cdot 10^{12}$	$6.19 \cdot 10^{12}$	$3.12 \cdot 10^{12}$
Q_{eff}/q [cm^{-2}]	$4.82 \cdot 10^{11}$	$9.35 \cdot 10^{11}$	$3.12 \cdot 10^{12}$	$1.64 \cdot 10^{12}$	$1.34 \cdot 10^{12}$	$6.93 \cdot 10^{12}$
$Q_{eff}/q/D_{ox\_opt}$ [1/cm^2 Å]	$5.35 \cdot 10^{9}$	$1.70 \cdot 10^{10}$	$6.37 \cdot 10^{10}$	$3.10 \cdot 10^{10}$	$3.36 \cdot 10^{10}$	$1.73 \cdot 10^{11}$
Q_{eff} [C/cm^2]	$7.71 \cdot 10^{-8}$	$1.50 \cdot 10^{-7}$	$5.00 \cdot 10^{-7}$	$2.63 \cdot 10^{-7}$	$2.15 \cdot 10^{-7}$	$1.11 \cdot 10^{-6}$
U_{FB} [V]	–1.15	–1.20	–1.48	–1.60	–1.21	–3.34
E_{BR} [MV/cm] (50%)	13.2	11.3	12.0	19.2	13.8	13.8

To have the necessary reference data, two samples were subjected to either thermal (sample 1) or plasma (sample 5) oxidation only (no nitrogen implantation). The technological experiments performed in the course of this study are summarized in Table 1.

Thickness and composition of the obtained layers were then studied by means of ellipsometry, and ULE-SIMS (ultra-low-energy-SIMS), while electrophysical properties were evaluated based on electrical characterization (*C-V* and *I-V* characteristics analysis) of NMOS test structures with the investigated ultra-thin silicon oxynitride layers as gate dielectric.

3. Results

The results obtained in this work and summarized in Tables 1 and 2 confirm that nitrogen implantation does takes place even at very low rf plasma energies (even at 100 W – see Fig. 2). Subsequent thermal oxidation formed ultra-thin oxynitride layers with the composition and thickness dependent on the conditions of the implantation process.

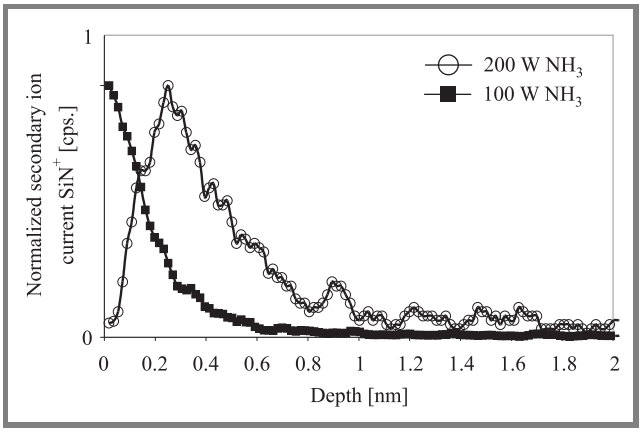

Fig. 2. Examples of nitrogen profiles of the layers formed by means of nitrogen implantation at different levels of rf power followed by plasma oxidation as obtained from ULE-SIMS [7].

During oxynitride layer formation two contradictory effects have significant influence upon the composition and final thickness of the layer.

Nitrogen implantation results in a significant decrease of the thermal oxidation rate, as can be seen in Table 2 (compare the thickness of all nitrogen implanted and thermally oxidized samples with that of sample 1).

Results obtained by ULE – SIMS (see Fig. 2) demonstrate that both, nitrogen profile and content may be controlled by rf plasma power used for implantation. Depending on this power the maximum of the nitrogen profile may be located just at the top surface of the layer or still within the layer – no further than 1.0 nm from its top (see Fig. 2).

A profile of this depth is difficult (if not impossible) to obtain by other techniques. The depth correlates well with the desired final thickness of the oxynitride layer. This means that when the formation of ultra-thin oxynitride layer is finished (that is after oxidation) the nitrogen profile will not extend into the device channel region.

Analysis of electrical characteristics of NMOS test structures indicates correlation between rf power used for nitrogen implantation and electrical properties of the Si/SiO_xN_y system.

Ellipsometric measurements indicate crucial difference between the thermal and plasma oxidation. For plasma oxidation no difference between the implanted and non-implanted samples was observed (see Table 2) while for thermal oxidation big difference between the implanted and non-implanted samples can be noticed. Almost no difference may, however, be noticed between the implanted samples despite varying rf power used. The whole picture changes if the electrical thickness is taken into consideration.

The equivalent oxide thickness (EOT) values (electrical thickness evaluated from the high frequency *C-V* characteristics assuming the dielectric permittivity is that of silicon dioxide) depend on rf power during implantation. The obvious and intuitive explanation to this observation is that this reflects the dependence of the efficiency of the nitrogen implantation (thus, the composition of the layer) on implantation conditions. In fact a comparison of the optical thickness and EOT leads to the conclusion that the effective dielectric constant of the layer is higher than that of thermal oxide only in one case (implantation at 200 W), which can be attributed to the significant presence of nitrogen in the layer (see Table 2). For the other cases, i.e., 100 W and 300 W, as well as the reference one, the effective dielectric constant values are lower than that of thermal oxide.

The case of thermal oxide proves that one should treat this comparison with highest care[1]. It is our strong belief that we should refer in our discussion to the observed trends in the effective dielectric constant values, rather than to the absolute values.

Following this approach one notices that the effective dielectric constant reaches maximum in the 200 W case. The dramatic drop of this parameter for 300 W could be interpreted as too much damage caused by nitrogen implantation during the first stage of layer formation. It is interesting, however, to realize that sample 4 has proved to be overall superior (as will be shown below) to all the other samples in terms of electrical properties (the lowest leakage current, highest critical electric field, well defined *C-V* curve and relatively low charge densities). The reason of this discrepancy is not yet known.

For plasma oxidized samples the situation is different. Although, as mentioned above, the optical thickness of the layer is the same, the EOT values differ significantly. Remembering the discussion presented above we may still state that some changes in the layer composition must take place as a result of nitrogen plasma implantation prior to plasma oxidation. Although such a drastic change in EOT would certainly be good enough to obtain satisfactory dual gate oxide technology, its value decreases instead of its required rise. Thus, instead of relaxing technological problems with formation of ultra-thin gate dielectric layer, application of this method to perform dual gate oxide technology would create even more serious difficulties.

Typical electrical characteristics of NMOS test devices manufactured for the purpose of this study are presented in Figs. 3–5. High frequency *C-V* curves are shown in Fig. 3. In general, the differences in maximum capacitance are the obvious consequence of different thickness and composition of the studied oxynitride layers and – to a certain extent – of different leakage currents. In order to

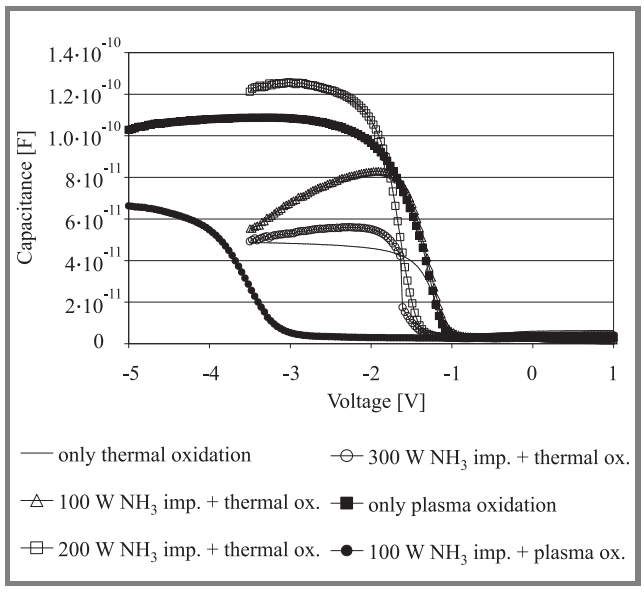

Fig. 3. High frequency (1 MHz) *C-V* curves of NMOS test structures with the gate dielectric layers produced under different plasma parameters (varied rf power and oxidation type – see Table 1).

[1]The optical thickness is evaluated from the ellipsometric measurements assuming silicon dioxide refractive index value, due to the low sensitivity of the ellipsometric curves for very low layer thickness. EOT, on the other hand, is evaluated assuming the dielectric constant of thick film thermal silicon dioxide. Neither of the two assumptions is true in the case of the examined samples, even for the reference sample 1 (this is only 10 nm layer). In fact, the significant decrease in the sensitivity of ellipsometric curves makes the former assumption certainly less critical than the latter. One should also keep in mind that for ultra-thin layers optical thickness tends to differ (is usually smaller) from electrical thickness (evaluated from *C-V* curves).

prevent the errors in EOT and all other electrical parameter calculations we used the estimation method of $C_{\max}$ as presented in [8]. A simple and intuitively obvious dependence has also been found between rf plasma power and the densities of the effective charge Q_{eff} interface traps at midgap D_{itmb}. Both parameters show maximum at 200 W. In fact, sample 4 (rf during plasma implantation 300 W) has superior trapping and effective charge density to all other samples subjected to the plasma implantation and only marginally worse than those of the reference thermal oxide. This result is promising for the dual gate oxide technology.

For plasma oxidation case, the situation is more complicated. Although the systems resulting from plasma nitrogen implantation and plasma oxidation are on a par with reference thermal oxide in terms of trapping properties, the effective charge density is certainly the highest among all samples studied (more than one order of magnitude higher than in the reference thermally oxidized gate oxide).

Typical *I-V* curves of individual samples studied in this work are shown in Fig. 4. The analysis of *I-V* curves yields a surprising result. Samples implanted at the highest rf power (300 W; sample 4) have the best insulating properties, better even than the reference thermal oxide (especially for high electric fields). Samples prepared using only plasma processes, that is plasma oxidation only (sample 5) or plasma implantation followed by plasma oxidation (sample 6) exhibit comparable *I-V* behavior, similar also to that of sample 1 (thermal oxidation only) for medium and higher electric fields, although their current is almost two orders of magnitude higher for low electric fields. Samples 2 and 3, implanted at 100 W and 200 W of rf power exhibit the highest leakage currents.

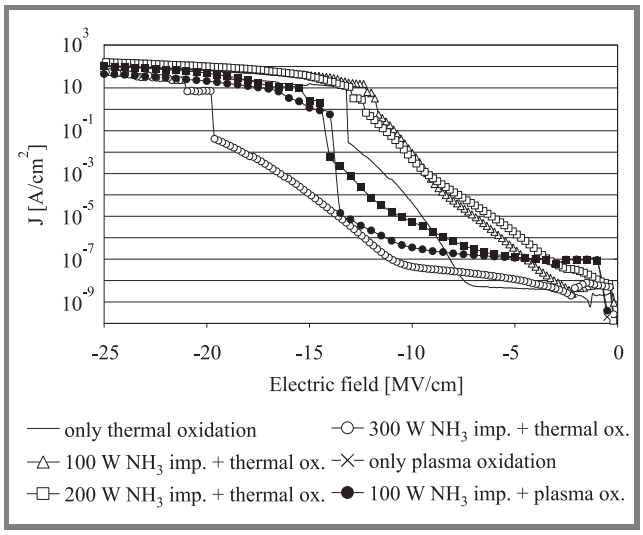

Fig. 4. The *I-V* curves of NMOS test structures; gate dielectric layers were produced with different process parameters (varied rf power and oxidation type – see Table 1).

In all studied samples breakdown events were well defined, thus the Weibull plots could be created for each sample (see Fig. 5). Oxynitride layer formed by means of implantation from NH_3 at 300 W and subsequent thermal oxidation (sample 4) was the best in terms of critical electric field with E_{BR} as high as 19 MV/cm. E_{BR} values of other samples vary between 11 MV/cm and 14 MV/cm (see Table 2). This means that in each case, the breakdown properties of the obtained SiON layers are superior to the defect free thermal oxides (10 MV/cm). It is interesting to realize that the plots for samples that underwent plasma oxidation are almost identical, whether they were or not subjected to nitrogen implantation.

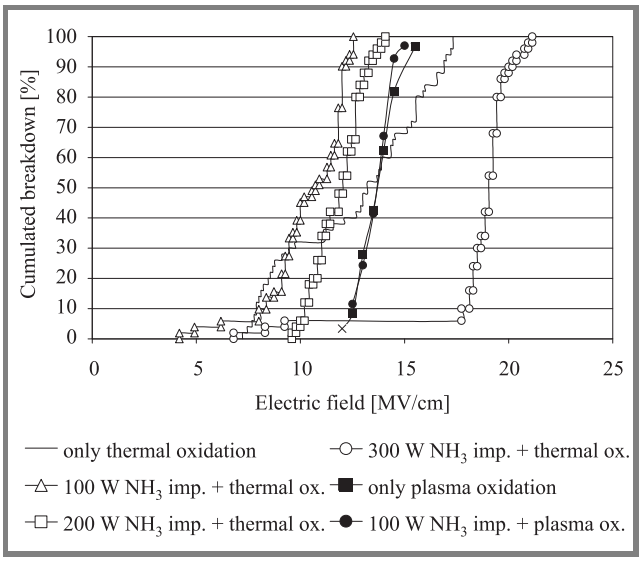

Fig. 5. Weibull plots of NMOS test structures; gate dielectric layers were produced with different process parameters (varied rf power and oxidation type – see Table 1).

Another interesting feature of the presented Weibull plots is their abruptness indicating that for each layer type all breakdowns took place under similar stressing voltage conditions. Therefore, it may be concluded, that we are dealing with intrinsic breakdown (characteristic of layers with almost no defects) or with one caused by one type of defects only (in the case where the intrinsic breakdown field is even higher for this type of material).

4. Summary

The experiments performed indicate that dual gate oxide technology based on ultrashallow implantation of nitrogen is feasible. From the two approaches to dual gate oxide technology studied in this work, the combination of nitrogen implantation with thermal oxidation is definitely more promising, because significant reduction of the final oxynitride layer thickness due to plasma implantation was observed.

Variation of rf power indicates that the highest investigated value of this parameter (300 W) results in a superior quality of the ultra-thin gate dielectric layer, comparable with that of non-implanted samples (trapping and effective charge density) and in certain aspects – leakage currents and critical electric field – even much better.

Although the plasma implantation does not degrade the properties in plasma oxidized samples (leakage currents, critical electric field, trapping) except for the effective charge density, the observed decrease in EOT seems to eliminate this method from the list of candidates for implementation for dual gate oxide technology in the future. On the basis of the results obtained in this study, it may be concluded that effective plasma implantation reduces the leakage current, especially at medium and high electric field, leading to significant improvement in breakdown properties (E_{BR} reaching 19 MV/cm). This effect may be of great value for future CMOS technologies, which suffer a lot from the leakage and reliability issues.

Acknowledgements

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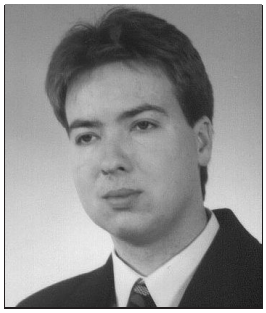

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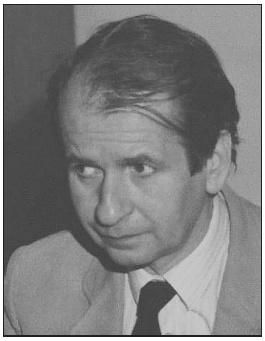

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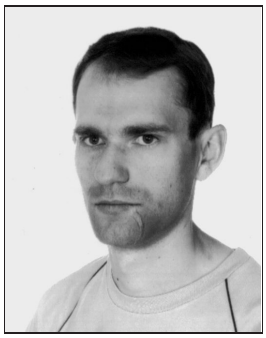

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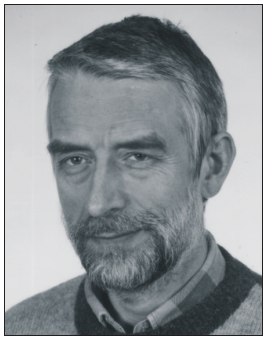

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Paper

Composition and electrical properties of ultra-thin SiO_xN_y layers formed by rf plasma nitrogen implantation/plasma oxidation processes

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Abstract—Experiments presented in this work are a summary of the study that examines the possibility of fabrication of oxynitride layers for Si structures by nitrogen implantation from rf plasma only or nitrogen implantation from rf plasma followed immediately by plasma oxidation process. The obtained layers were characterized by means of: ellipsometry, XPS and ULE-SIMS. The results of electrical characterization of NMOS Al-gate test structures fabricated with the investigated layers used as gate dielectric, are also discussed.

Keywords—CMOS, gate stack, oxynitride, plasma implantation.

1. Introduction

According to the ITRS roadmap [1] the thickness of the gate dielectric layer will be dramatically reduced in the near future to 6–8 Å in 2011. Such extremely thin layers generate, however, a lot of problems in terms of processing repeatability and reliability. This, in turn, creates a pressure to substitute silicon dioxide with a single layer of high-*k* material or – more probably – with a gate stack (a combination of high-*k* material and pedestal layer passivating silicon-dielectric interface).

Oxynitride layers seem to be very promising in this respect. This is mostly due to the fact that silicon nitride layers are known to be very resistant to diffusion and thus oxidation (vide their application for LOCOS), while oxide is undisputedly the best possible passivating layer for silicon surface.

Oxynitride layers can be produced with number of methods. The experiments presented in this work are a summary of the study that examines the possibility of fabrication of oxynitride layers for Si structures by nitrogen implantation from rf plasma (denoted hereafter as "as-implanted") or nitrogen implantation from rf plasma followed immediately by plasma oxidation process.

In contrast to the methods presented in the literature so far (e.g., [2, 3]), where the classical implanters or the ion immersion implantation in plasma (IIIP) technique were used for implantation, in this work we used a typical rf plasma planar reactor, usually applied for plasma enhanced chemical vapour deposition (PECVD) – Oxford plasma technology – PlasmaLab 80+.

2. Experimental

In this work ultra-thin oxynitride layers were formed during plasma processes. Ultrashallow plasma implantation of nitrogen ions and low temperature plasma oxidation were used to form the layers. Both these processes were performed, as already mentioned above, in a PECVD reactor. For the purpose of this study, the layers were formed under different conditions. The variable process parameters were: implantation time, rf power, nitrogen source gases, and temperature. A detailed process description may be found in [4–6].

Two-stage analysis of the studied ultra-thin oxynitride layers was performed. In the first stage, the layers formed using nitrogen plasma implantation only (as implanted) were characterized in order to understand the state of the silicon substrate right after plasma implantation. In the second stage, the layers formed using nitrogen implantation followed by plasma oxidation underwent similar analysis, to understand the consequences of the complex process.

Each stage included structural (i.e., optical – ellipsometry, chemical and physical X-ray photoelectron spectroscopy (XPS), secondary ion mass spectroscopy (SIMS) and electrical (electrical measurements of NMOS test structures with investigated layer used like a gate dielectrics) analysis. Structural analysis was aimed at independent determination of the chemical composition and thickness of the layers [7–9]. In order to perform electrical characterization of the layers, NMOS Al-gate test structures with ultra-thin dielectric layers formed using the studied method were fabricated. Al gate was chosen to avoid any thermal treatment after the gate dielectric was formed.

The NMOS test structures were then electrically characterized by means of *C-V* and *I-V* measurements in order to evaluate: leakage currents, effective charge density and trapping and breakdown behavior.

3. Results

3.1. Samples with nitrogen plasma implantation only (as-implanted)

In the first step, analysis of the correlation between the ultrashallow plasma implantation and composition and thick-

ness of the affected silicon layer was studied. The following parameters of plasma implantation were of interest: type of nitrogen source gas, rf plasma power, implantation time and sample temperature during implantation.

The XPS studies have revealed that despite using either nitrogen or ammonia plasma during implantation, the implanted substrate region consists mostly of silicon dioxide. This must be the result of a spontaneous oxidation upon the exposure of the samples to the atmosphere when removing them from the plasma reactor. Even though the implantation temperature is only 200°C or 350°C – the results prove that the implantation leaves the silicon surface very prone to oxidation even in such usually unfavorable conditions.

There are, however, small differences in the composition of the studied layers depending on the nitrogen source (see Fig. 1). Marginally higher content of nitrogen is observed for nitrogen implantation from ammonia plasma. Different nitrogen content and/or damage caused to the silicon surface during nitrogen implantation result in significantly different overall layer thickness – lower for implantation from ammonia than from nitrogen plasma. Thus, it seams reasonable to choose ammonia plasma for the purpose investigated in this paper and this choice has been adopted for the subsequent investigation.

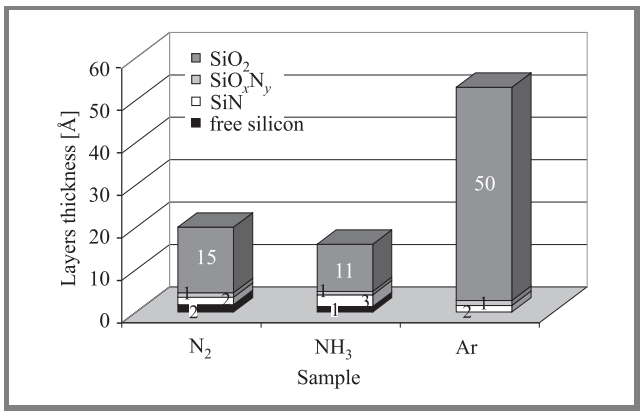

Fig. 1. Chemical composition and thickness obtained from XPS for layers formed in different plasmas (NH_3, N_2, Ar) – normalized to the optical thickness.

From the reference experiment in which the silicon sample was subjected to Ar plasma bombardment (for the same as in case of nitrogen and ammonia plasmas rf power – 100 W) one can evaluate the influence of substrate damage caused by bombarding ions. Comparison of the thickness of spontaneously oxidized layers after exposure to either Ar or nitrogen plasma clearly proves that the nitrogen presence in the surface silicon layer significantly slows down the oxidation rate.

This in turn proves that the presence of nitrogen-rich oxide at the silicon surface may be effectively used to prevent or at least to reduce oxide growth at the silicon interface during high-*k* dielectric deposition and/or source and drain dopant activation annealing.

The next correlation to investigate was the influence of implantation rf power. The analysis based on the example of NH_3 samples shows that rf power is a very important process parameter (see Figs. 2 and 3). Increasing implantation power results in a decrease of the layer thickness and in minor changes of its chemical composition (see Figs. 2a and 2b). It is not obvious if these changes are sufficient to cause the observed reduction of the layer thickness. The other possibility is that changing rf power affects the density of the plasma and thus also the implantation and substrate damage efficiency, which in turn can lead to a change in spontaneous oxidation rate. Additional data for this analysis may be obtained from ultra-low energy SIMS (ULE-SIMS).

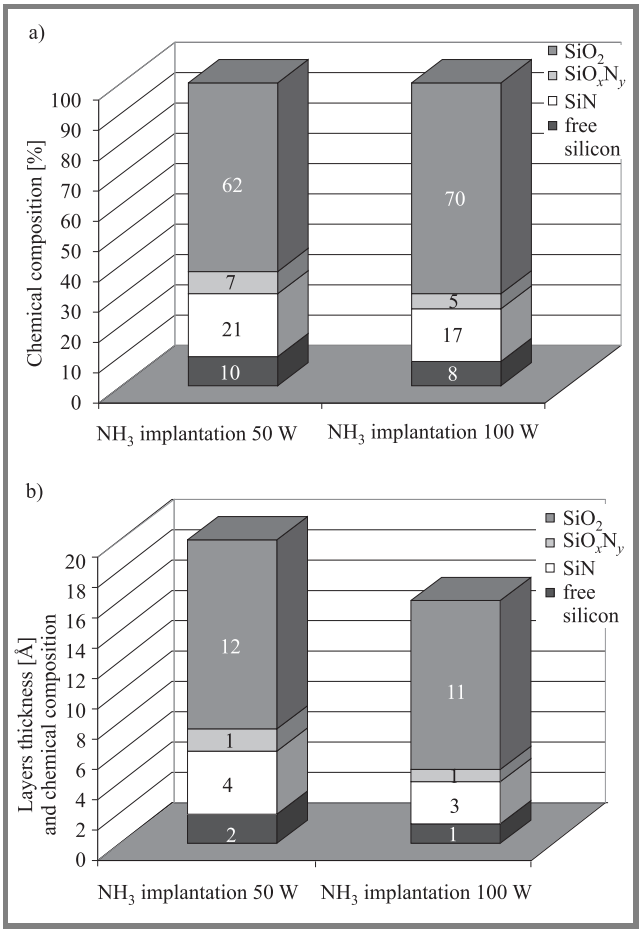

Fig. 2. Chemical composition and thickness obtained from XPS for layers formed in NH_3 plasma for two different levels of rf implantation power (50 W and 100 W) normalized to: (a) 100%; (b) to the layer thickness.

Analysis of ULE-SIMS data yielded similar results to the ones obtained from XPS. They prove that rf power used for nitrogen implantation is a crucial process parameter. Depending on rf power used, the maximum of the nitrogen profile may be located just at the top surface of the layers (for power not higher than 100 W) or within up to 1.0 nm from it (see Fig. 3). It seems, therefore, that the nitro-

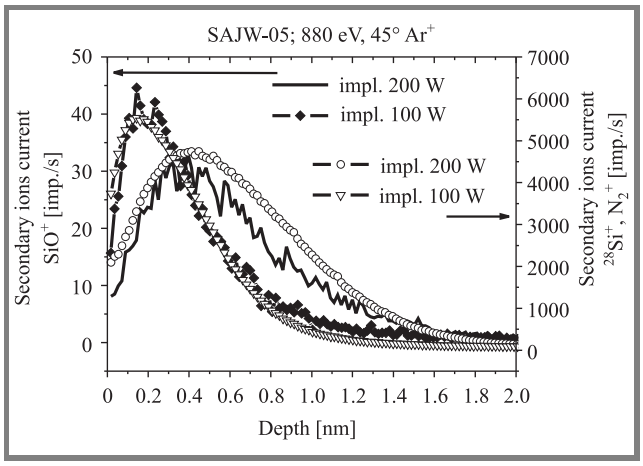

Fig. 3. Examples of ULE-SIMS results – secondary ion current for SiO^+, Si^+, N_2^+ for the samples implanted from NH_3 for two different rf power levels (100 W and 200 W).

gen profile may be optimized by choosing the appropriate rf power for nitrogen implantation.

A profile of this depth is difficult (if not impossible) to obtain by other techniques. The depth correlates well with the desired final thickness of the oxynitride layer. This means that when the formation of ultra-thin oxynitride layer is finished (that is after oxidation) the nitrogen profile will not extend into the device channel region.

The XPS study of the samples exposed to plasma implantation of nitrogen for different time (see Fig. 4) demonstrates that the amount of nitrogen rich phases (oxynitrides and nitrides) reaches a maximum at a certain implantation time. For the studied cases the highest content of nitrogen was observed in layers obtained by 10 min implantation. In practice, however, it may be difficult to use this parameter to optimize nitrogen content since the layer thickness is also dependent on implantation time.

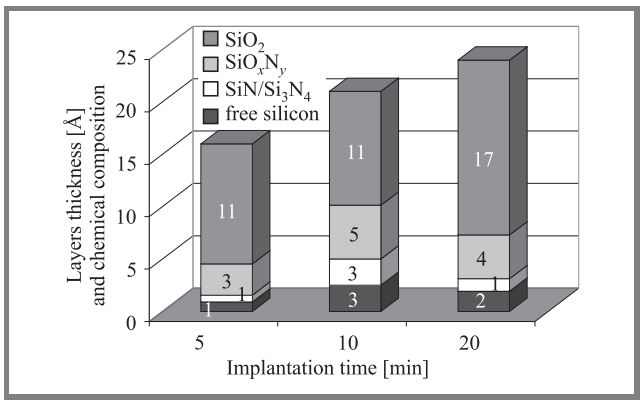

Fig. 4. Chemical composition and thickness obtained from XPS for different times of implantation (5 min, 10 min, 20 min) – normalized to the optical thickness.

The last parameter of nitrogen implantation to be studied was the temperature of the silicon substrate. The surprising result obtained in this study can be seen in Fig. 5a, which demonstrates that no differences in the chemical content are observed between the layer obtained at temperatures ranging from 200°C to 350°C. Interestingly enough higher temperatures promote layer growth (23 Å versus 45 Å for 200°C and 350°C, respectively – see Fig. 5b). The nature of this dependence is not clear. One might speculate

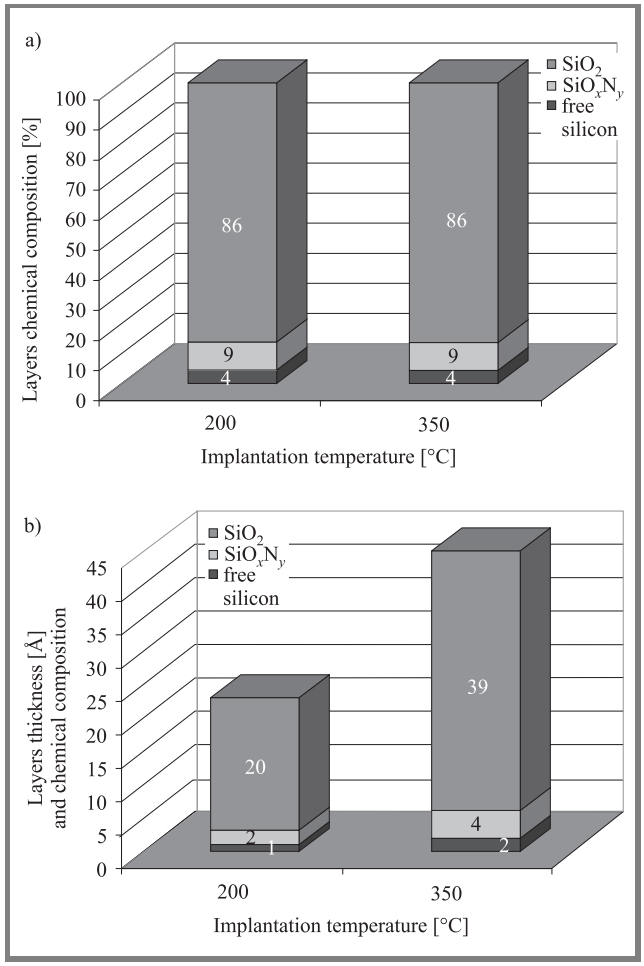

Fig. 5. Chemical composition and thickness obtained from XPS for layers formed at different implantation temperatures (200°C and 350°C) – normalized: (a) to 100%; (b) to the optical thickness.

that higher temperatures allow easier (and faster) formation of nitride bonds, which in turn increases the silicon substrate oxidation rate. Such an explanation would be, however, only true if silicon oxidation took place during implantation and not, as believed until now, exclusively during the exposure to the clean-room atmosphere.

3.2. Samples with nitrogen implantation followed by plasma oxidation

The next stage of analysis refers to the structural investigations of the layers formed using plasma implantation of nitrogen followed by plasma oxidation. Introduction of the second process step – plasma oxidation – has created new parameters to be decided upon. From previous studies

on plasma oxidation alone we have chosen the rf power of 50 W and oxygen pressure of 0.5 Tr for this process. Oxidation time was studied using XPS, similarly to the previous case. From the spectra presented in Fig. 6 we can clearly see that even half minute oxidation after nitrogen implantation is enough to form an oxynitride layer with high silicon dioxide content. Any oxidation, longer than 0.5 min, gives SiO_xN_y layer with similar oxygen content and profile. For the sake of this study, the plasma oxidation time was set to 2 min. The following experiments aimed at checking the influence of plasma oxidation on the composition of the final layer.

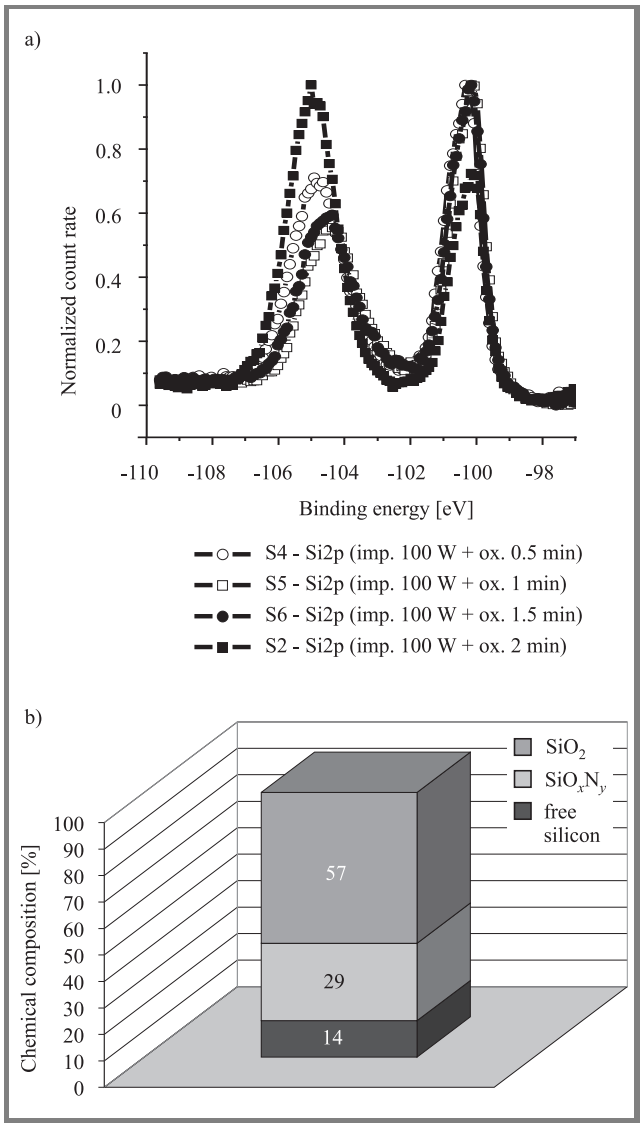

Fig. 6. Results of XPS measurements: (a) Si2p peaks for the samples implanted from NH_3 plasma at 100 W and plasma oxidized for different oxidation times (0.5; 1; 1.5, 2 min); (b) composition of the layer plasma oxidized for 2 min.

The XPS spectra shown in Fig. 7 prove that as a result of plasma oxidation we obtain almost the same composition of the oxynitride layer (as shown in Fig. 6b) regardless of the rf power used for nitrogen implantation.

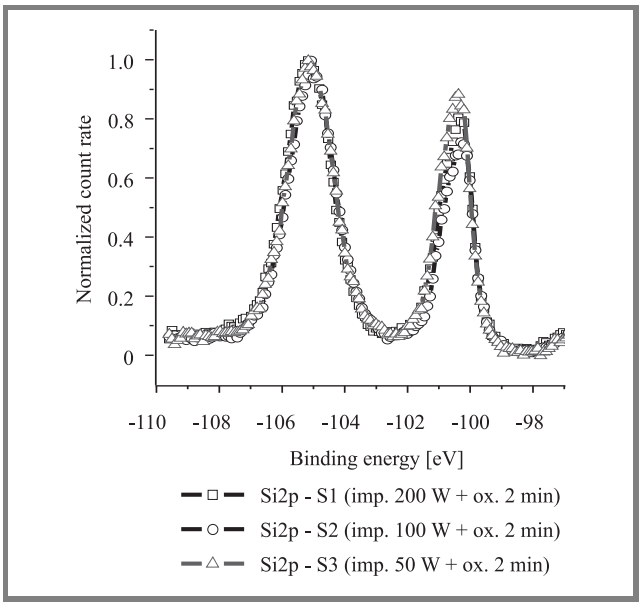

Fig. 7. Si2p peak for samples implanted from NH_3 plasma at three different levels of rf power (50 W, 100 W and 200 W) and oxidized in oxygen plasma for 2 min.

3.3. Electrical characterization

The test structures for the analysis of electrophysical properties were fabricated using different nitrogen implantation conditions. In order to establish the most sensitive relations between the properties of the layers and plasma process parameters the test structures were fabricated using different rf plasma power for plasma implantation. It should be remembered here that this parameter appeared to have the greatest influence on the properties of the layers directly after implantation. Two samples were fabricated using NH_3 as nitrogen source at different levels of rf power (sample 5–100 W and sample 6–50 W). For the sake of comparison, one sample was also produced with the layer formed using N_2 plasma (sample 4). Process parameters and characterization results are summarized in Table 1.

Analysis of electrical characteristics of NMOS test structures has shown strong correlation between plasma process parameters and electrical properties of the layers. This result was rather surprising since XPS analysis revealed that layer composition after plasma oxidation was the same regardless of the initial state after nitrogen implantation.

High frequency *C-V* curves shown in Fig. 8 form two clearly distinguishable groups. One curve (sample 1) is shifted towards negative voltage with respect to all the other curves (including also those obtained from as implanted samples 5 and 6). This voltage shift is the consequence of much higher effective charge concentration Q_{eff}/q (see Table 1). This confirms the results of the XPS analysis, which indicated that implantation at 200 W from NH_3 plasma created significantly more damage than processes carried out at lower values of rf power [4–6].

The differences in maximum capacitance C_{max} are the obvious consequence of the variation in layer thicknesses,

Table 1
The technological process parameters of oxynitride layer formation and the results of optical and electrical characteristics evaluation for NMOS test structures manufactured in this study

Parameters	Samples					
	1	2	3	4	5	6
Step 1 – nitrogen ions implantation (350°C)						
Power [W]	200	100	50	50	100	50
Gas/plasma	NH_3	NH_3	NH_3	N_2	NH_3	NH_3
Step 2 – plasma oxidation (350°C, 50 W, O_2)						
Optical characterization						
Layer thickness [Å]	33	24	24	52	45	32
Electrical characterization (from *C-V* curves)						
EOT [Å]	59	37	35	41	33	40
U_{fb} [V]	–2.2	–1.1	–1.0	–1.1	–1.2	–1.2
Q_{eff}/q [cm^{-2}]	$4.7 \cdot 10^{12}$	$9.0 \cdot 10^{12}$	$4.9 \cdot 10^{11}$	$7.0 \cdot 10^{11}$	$1.8 \cdot 10^{12}$	$1.1 \cdot 10^{12}$
Q_{eff}/q/optical thickness [cm^{-2}/Å]	$1.4 \cdot 10^{11}$	$3.8 \cdot 10^{10}$	$2.0 \cdot 10^{10}$	$1.3 \cdot 10^{10}$	$4.0 \cdot 10^{10}$	$3.4 \cdot 10^{10}$
D_{itmb} $1/eVcm^2$	$1.8 \cdot 10^{13}$	$1.5 \cdot 10^{13}$	$8.0 \cdot 10^{12}$	$1.2 \cdot 10^{13}$	$9.8 \cdot 10^{13}$	$7.7 \cdot 10^{12}$
Electrical characterization (from *I-V* curves)						
$E_{breakdown}$	17.8	20.4	19.6	10.6	10	–*

* No catastrophic physical breakdown could be detected for these devices.

compositions, as well as in leakage current for particular wafers. Leakage is related with oxide structure integrity, therefore should also be reflected in the effective dielectric constant of the studied oxynitride layers. These values obtained from C_{max} (oxynitride thickness was determined independently by ellipsometry) have confirmed the above mentioned relations between samples.

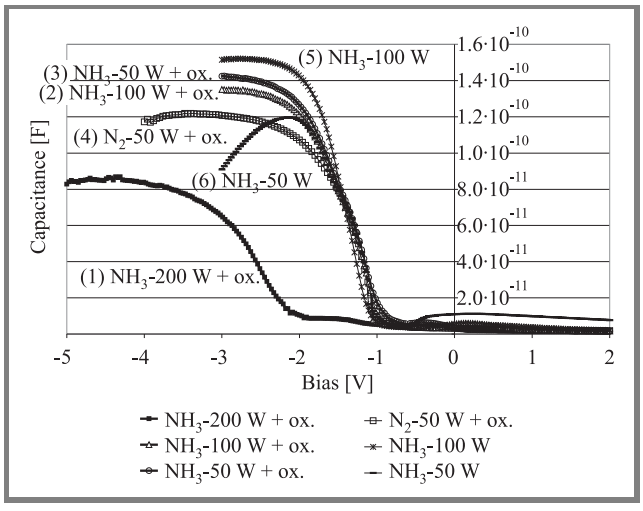

Fig. 8. Typical high frequency *C-V* curves for the studied NMOS test structures with the gate dielectric layers produced with different plasma parameters (varied rf power and nitrogen gas source) [6].

The *C-V* behavior of as implanted samples proves that a dielectric film (identified by XPS as oxynitride layer) is formed on top of the silicon substrate already after nitrogen implantation. This observation confirms that the exposure of the as-implanted silicon surface (please, keep in mind that the wafer temperature is 350°C before the plasma reactor is vented) to the atmosphere is enough to form an oxynitride layer. The quality of such layers (as-implanted) expressed in terms of charge and trap densities in the studied system is, amazingly, comparable to those formed by plasma oxidation only. The significant difference between these two groups (as-implanted and oxidized), as it will be shown below, exists in leakage currents and breakdown properties, which suggests that the main difference between them lays in the integrity of the dielectric layer.

Simple and intuitively obvious dependence between rf plasma power and the densities of the effective charge Q_{eff} and traps D_{itmb} has also been confirmed. The values of both of these parameters rise with the increase of rf power. Taking into consideration different final thickness of the oxynitride layers obtained under different conditions makes this dependence even stronger (see Q_{eff}/q normalized to the layer thickness in Table 1).

It is interesting to realize that although N_2 implanted samples exhibit relatively low Q_{eff}/q values (especially when normalized to the layer thickness) – their interface properties (expressed in D_{itmb}) are worse than those of the 50 W, NH_3-implanted sample.

The typical *I-V* curves (for the purpose of easier comparison drawn in the *J-E* scale) for individual samples studied in this work are presented in Fig. 9. In all of the examined cases (except of sample 6) the breakdown events were

well defined, thus, the Weibull plots could be constructed (see Fig. 10).

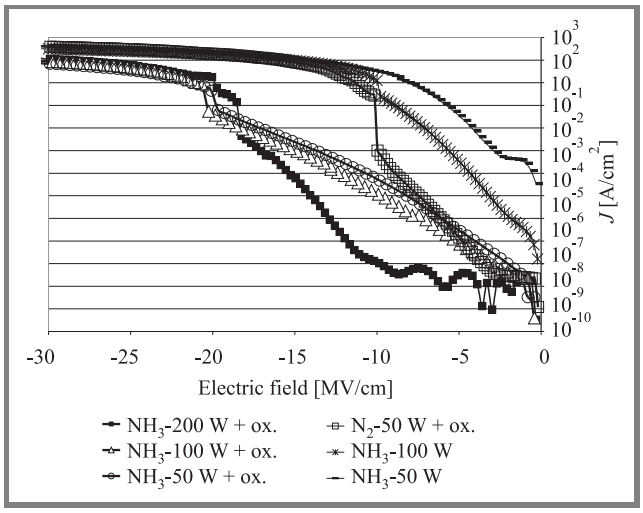

Fig. 9. Typical *J-E* curves for the studied NMOS test structures; gate dielectric layers were produced with different plasma parameters (rf power and nitrogen source gas) [6].

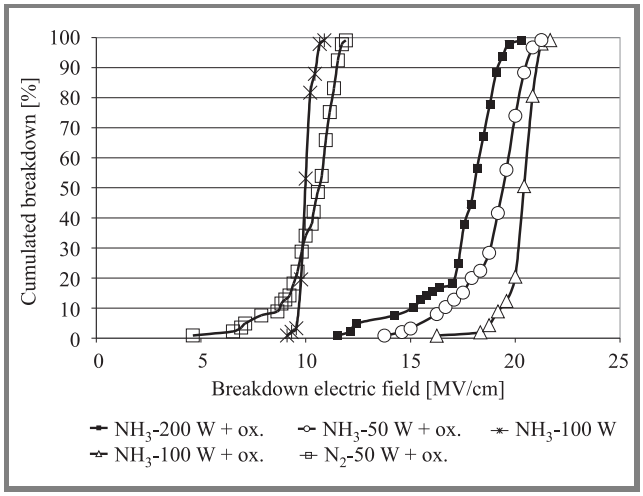

Fig. 10. Weibull's plots for the studied NMOS test structures; gate dielectric layers were produced with different plasma parameters (rf power and nitrogen gas source) [6].

The as-implanted samples (without plasma oxidation) exhibit obviously the highest leakage currents. In the case of the sample implanted at 50 W this current is approximately two orders of magnitude higher than that of the sample implanted at 100 W.

Among the samples which underwent plasma oxidation, N_2 implanted sample proves again to be inferior to the rest. Although its critical electric field is comparable to that typically achieved by thermal SiO_2 layers ($\sim$ 10 MV/cm), other samples exhibited much higher values. The best result (20 MV/cm) was observed in the oxynitride sample formed by implantation from NH_3 at 100 W.

It is interesting to realize that the lowest leakage current is observed for the sample implanted from NH_3 at 200 W, which is the worst among implanted and oxidized samples in terms of charge and trap density In the high electric field region the current for this sample was even a few (up to three) orders of magnitude lower than that for the samples implanted from NH_3 at lower rf power (100 W and 50 W).

The Weibull plots created from the results of *I-V* measurements are shown in Fig. 10. It is interesting to realize that all of them are very steep, proving practically single mode breakdown properties and no (or very little) early, defect related breakdowns.

4. Summary

The nitrogen implantation from rf plasma either alone or followed by plasma oxidation was studied as a potential method to fabricate ultra-thin oxynitrides layers.

It has been proved that nitrogen implantation from NH_3 can be more effective than from N_2. The rf power can be successfully used to control both, the thickness and composition of an ultra-thin oxynitride layer. It can also be used to control the nitrogen profile within the oxynitride layer. The nitrogen penetration depth can be less than 1.0 nm. Thus, no degradation of MOSFET carrier mobility in the device channel should be observed.

The implantation temperature and time are not sensitive parameters, therefore this method offers significant flexibility in this respect.

Plasma oxidation rebuilds the oxynitride layer, the final composition is practically the same regardless of the parameters of the preceding nitrogen implantation. The electrophysical properties of these layers are, however, different (implantation – parameter dependent).

The effective charge and interface trap densities are, so far, hardly acceptable, but no annealing has been used in this study. The breakdown properties of the studied layers are excellent and, hence, give hope for uniform and reliable gate stacks with pedestal oxynitrides formed by this method.

Acknowledgements

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Piotr Konarski and **Michał Ćwil** – for biographies, see this issue, p. 8.

Paper

The influence of annealing (900°C) of ultra-thin PECVD silicon oxynitride layers

Robert Mroczyński, Grzegorz Głuszko, Romuald B. Beck, Andrzej Jakubowski, Michał Ćwil, Piotr Konarski, Patrick Hoffmann, and Dieter Schmeißer

Abstract—This work reports on changes in the properties of ultra-thin PECVD silicon oxynitride layers after high-temperature treatment. Possible changes in the structure, composition and electrophysical properties were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization methods (*C-V*, *I-V* and charge-pumping). The XPS measurements show that SiO_xN_y is the dominant phase in the ultra-thin layer and high-temperature annealing results in further increase of the oxynitride phase up to 70% of the whole layer. Despite comparable thickness, SIMS measurement indicates a densification of the annealed layer, because sputtering time is increased. It suggests complex changes of physical and chemical properties of the investigated layers taking place during high-temperature annealing. The *C-V* curves of annealed layers exhibit less frequency dispersion, their leakage and charge-pumping currents are lower when compared to those of as-deposited layers, proving improvement in the gate structure trapping properties due to the annealing process.

Keywords—ultra-thin dielectrics, silicon oxynitride, PECVD, CMOS.

1. Introduction

According to the ITRS roadmap [1] SiO_2 gate dielectric will have to be replaced with by layers exhibiting higher dielectric constants. Ultra-thin silicon oxynitride (SiO_xN_y) seems to be a promising candidate as gate dielectric in future CMOS IC's (e.g., [2, 3]).

However, during standard CMOS self-aligned technology the implantation of source/drain regions is followed by a high-temperature annealing aiming at electrical activation of the implanted dopants. These processes occur after gate dielectric fabrication and may obviously influence its electrophysical properties.

This work reports on changes in properties of ultra-thin plasma enhanced chemical vapour deposition (PECVD) silicon oxynitride layers after high-temperature treatment. Possible changes in the structure, composition and electrophysical properties were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization.

2. Experimental

Non-self-aligned Al gate NMOS technology was used to fabricate test structures on 2" p-type ⟨100⟩ Si wafers. Oxynitride layers were deposited in a PlasmaLab System 80+ of Oxford plasma technology. The parameters of the PECVD process were optimized to allow repeatable formation of gate dielectrics. Split experiments with annealing of the obtained layers in argon at 900°C for 30 minutes were done. Process parameters are shown in Table 1.

Table 1
Process parameters allowing formation of ultra-thin silicon oxynitride layers

Parameters	Values
SiH_4 (2%): N_2 [sccm]	150
N_2O [sccm]	16
NH_3 [sccm]	32
Pressure [mTr]	500
Power [W]	10
Time [s]	20
Temperature [°C]	350
Time of annealing [min]	30
Temperature of annealing [°C]	900

The properties of the obtained layers were examined by means of: optical, electrical, XPS and SIMS measurements.

The thickness of the oxynitride layers was measured using a J. A. Wollam spectroscopic ellipsometer.

The X-ray photoelectron spectroscopy (XPS) analysis and ultra-low-energy-secondary ion mass spectroscopy (ULE-SIMS) profiles were used to observe the changes in chemical composition and component profiles due to the high-temperature treatment.

The XPS measurements were performed at the undulator beamline U49/2-PGM-2 supplying photons in the energy range of 80 eV – 1500 eV with a resolution above 7000 ($E/\Delta E$). An EA125 electron analyser (Omicron NanoTechnology GmbH) with a resolution of ∼200 meV was used.

The SIMS measurements were done using SAJW-05 system equipped with 06-350E Physical Electronics Ar^+ gun (ultra-low energy 880 eV Ar^+ beam) and Balzers QMA-410 quadrupole mass spectrometer. Quantitative atomic concentration of nitrogen and oxygen was calculated based on Si_2N^+, Si_2O^+ and Si_2^+ secondary ion currents.

Electrical measurements were performed with Hewlett-Packard 4061A Semiconductor Component Test System (*C-V* characteristics) and Keithley SMU (*I-V* characteristics). The metal-insulator-semiconductor (MIS) capacitors with gate area of $A = 1.7 \cdot 10^{-5}$ cm^2 were used to determine the basic electrophysical properties of the investigated layers. Moreover, charge-pumping currents of MISFETs ($W \times L = 10\ \mu\text{m} \times 10\ \mu\text{m}$) were measured to evaluate interface-trap density.

3. Results and discussion

Changes in the structure and composition of PECVD silicon oxynitride layers due to high-temperature annealing were studied by XPS measurements. To get the information about chemical bonds present in SiO_xN_y the measured spectra were analysed using line deconvolution. Every single line was attributed to the particular compound, due to its unique binding energy in the ultra-thin dielectric layer. Figure 1 shows a comparison of the chemical composition of the dielectric layers before and after annealing (expressed in terms of thickness and referred to the thickness obtained from the ellipsometric measurements) as determined from the Si2p line.

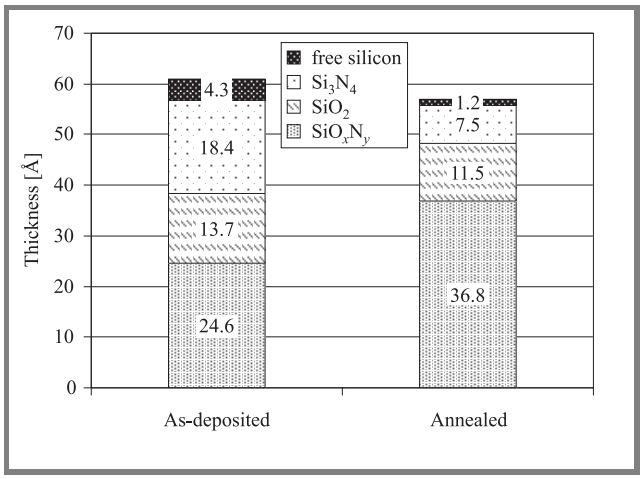

Fig. 1. Composition of PECVD ultra-thin silicon oxynitride layers (expressed as thickness), as determined from the Si2p line analysis.

From Fig. 1 a number of conclusions can be drawn. First – SiO_xN_y is the dominant phase in both as-deposited and annealed layers. Second – high-temperature annealing causes the amount of all phases other than oxynitride to decrease. These phases include oxide, silicon and, particularly significant, nitride (decreasing by almost 60%). It seems reasonable to expect that the growth of oxynitride takes place at the expense of nitride and oxide, while the decrease of the amount of free silicon resulting from annealing is probably due to the saturation of silicon dangling bonds during this high-temperature process. Third – the ultra-thin oxynitride layer can be considered thermally stable in terms of the total layer thickness, as no significant change in this parameter is observed after annealing at high temperatures. This is very important for application of such oxynitride layers in the self-aligned CMOS technology since post implantation high-temperature annealing must not result in any significant changes of the layer thickness. Such changes would obviously be detrimental to the overall integrity of the gate stack.

The SIMS profiles obtained for the same layers are shown in Fig. 2. It should be noticed that despite comparable physical thickness (as determined by ellipsometric measurements), sputtering of annealed dielectric layers during the measurement is much slower than that of as-deposited ones. Consequently, the location of the silicon/layer interface on the sputtering time scale is quite different for as-deposited and annealed layers (see Fig. 2). This difference in etching

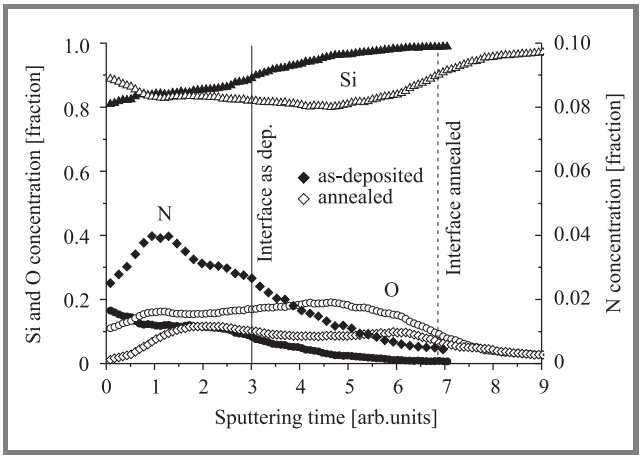

Fig. 2. The SIMS profiles of as-deposited and annealed silicon oxynitride layers.

rate has to be attributed to changes in physical and chemical properties (e.g., saturation of dangling bonds, densification of the layer) that must have taken place during high-temperature annealing of the oxynitride layers. A similar result has been observed during wet etching of ultra-thin oxynitride layers during formation of transistor gate. The wet etching time increased 18 times (from 10 seconds for as-deposited layers to 3 minutes for annealed ones)!

These observations indicate that annealed layers should exhibit better electrophysical properties than as-deposited ones. In fact, these expectations have been confirmed by the analysis of electrical properties of the studied ultra-thin dielectric/silicon system. The results of this analysis are presented below.

Another observation resulting from SIMS profiles is that nitrogen and oxygen are distributed more homogeneously in annealed layers than in as-deposited ones. In the case of the latter the maximum nitrogen concentration is located well within the layer (neither close to the top surface, nor to the interface).

The capacitance-voltage characteristics obtained from the test structures are shown in Fig. 3. It is clear that *C-V* curves of MIS capacitors with annealed oxynitrides exhibit smaller frequency dispersion in all regions (inversion,

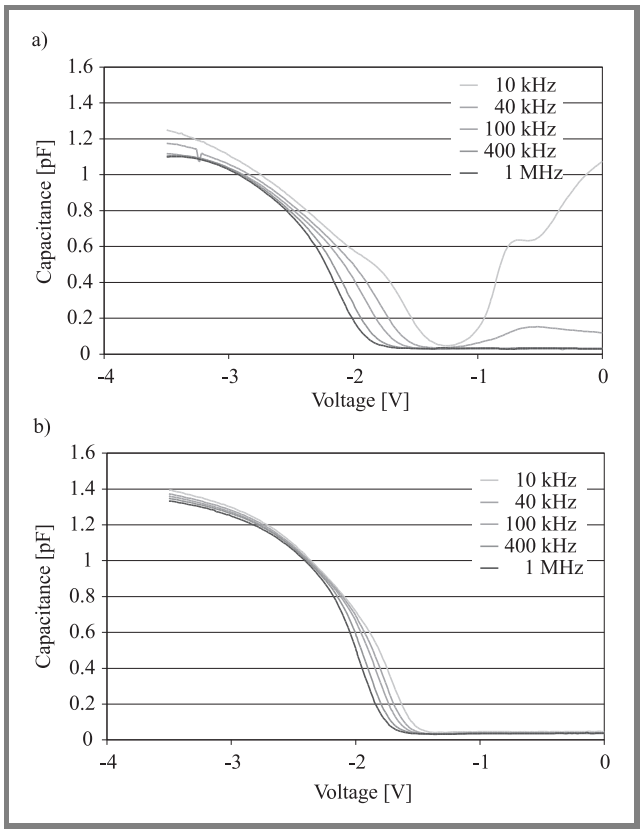

Fig. 3. Comparison of *C-V* characteristics of MIS structures with (a) as-deposited and (b) annealed silicon oxynitride layers.

depletion and accumulation). Moreover, the maximum capacitance $C_{\max}$ is higher in annealed structures. Since the total layer thickness (determined by ellipsometric measurements) is comparable for both annealed and as-deposited layers and $C_{\max}$ is stable over a wide voltage range we can conclude that the dielectric constant is increased as a result of annealing. The parameters presented in Table 2 confirm this assumption.

Table 2
Optical thickness and basic electrophysical properties of PECVD SiO_xN_y layers

Parameters	As-deposited	Annealed
Thickness [Å]	61	57
EOT [Å]*	50	42
Q_{eff}/q [cm^{-2}]**	$4.75 \cdot 10^{12}$	$4.82 \cdot 10^{12}$
D_{it} [cm^{-2}ev^{-1}]***	$1.2 \cdot 10^{13}$	$7.2 \cdot 10^{12}$
* EOT stands for equivalend oxide thickness (determined from *C-V* measurements), ** evaluated from *C-V* measurements, *** evaluated from *C-P* measurements.		

Table 2 compares the thickness and basic electrophysical parameters of the oxynitride layers, determined by means of spectroscopic ellipsometry, *C-V* and charge-pumping (CP).

The equivalent oxide thickness (EOT) is lower than physical thickness by 16% in the case of as-deposited layers and by 26% in the case of annealed ones. This is due to the fact that the dielectric constant of annealed layers is higher than that of as-deposited ones. The effective charge (as determined from *C-V* measurements) does not seem to be affected by annealing but the trap density determined from CP measurements is almost twice lower for annealed layers. It may be thus concluded that annealed oxynitride exhibits better electrophysical properties.

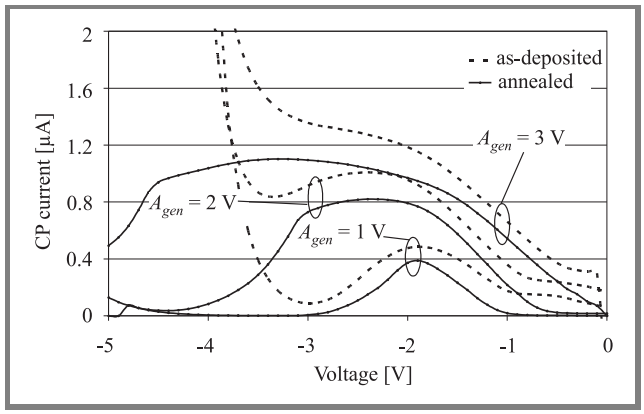

Fig. 4. Comparison of CP currents of MISFETs ($W \times L = 10\ \mu\text{m} \times 10\ \mu\text{m}$).

As seen in Fig. 4 only CP characteristics of MISFETs with annealed layers demonstrate classical behavior. Significantly higher CP currents of MISFETs with as-deposited layers at higher gate voltages are probably caused by higher leakage current (see Fig. 5) [4]. Additionally, CP currents of the MISFETs with annealed gate dielectric are clearly lower than these of as-deposited layers. This indicates that annealed layers have lower trap density (see Table 2).

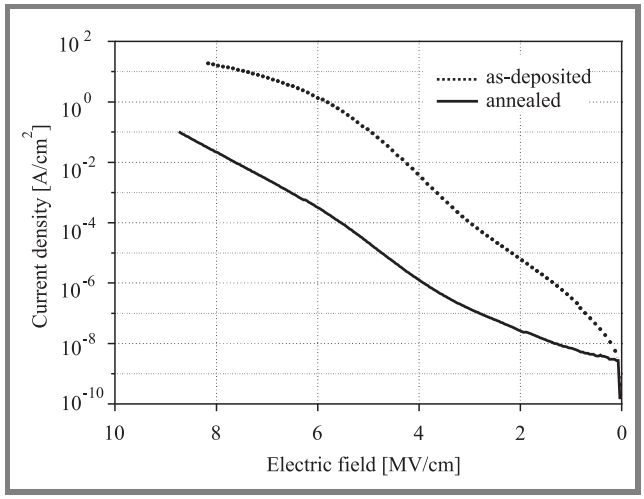

Fig. 5. Current density versus mean electric field within the dielectric layer.

The current-voltage characteristics were also measured in this study. To facilitate a comparison of the insulating properties of the investigated layers, these characteristics are

presented in Fig. 5 as current density versus mean electric field within the SiO_xN_y layer. It is clear that oxynitride layers exposed to high-temperature treatment show much better insulating properties – at intermediate electric fields current density of as-deposited layers is almost four orders of magnitude higher than that of annealed ones.

4. Conclusions

Ultra-thin PECVD silicon oxynitride layers were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization.

Ultra-thin PECVD silicon oxynitrides undergo complex changes in chemical composition due to thermal treatment (e.g., decreasing amount of oxide and nitride and increasing amount of SiO_xN_y). The amount of free silicon is lower in annealed layers – probably due to the saturation of free dangling bonds caused by annealing.

Oxygen and nitrogen are distributed more homogenously throughout annealed layers than as-deposited ones. In as-deposited oxynitride layers a maximum of nitrogen concentration is visible between the two interfaces.

Annealed silicon oxynitrides have better insulating properties (as evidenced by significantly lower leakage current). Additionally, annealed SiO_xN_y/Si system has better electrical parameters – lower frequency dispersion and lower interface traps density.

In view of all these results it is justified to conclude that high-temperature annealing improves electrophysical properties of silicon oxynitride layers. Moreover, oxynitride is thermally stable in terms of the total layer thickness, therefore high-temperature annealing may be applied (e.g., dopant activation after the implantation process) following the formation of the gate dielectric in self-aligned CMOS technology.

Acknowledgements

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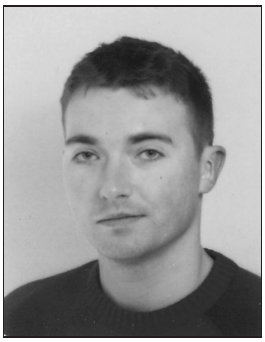

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Patrick Hoffmann and **Dieter Schmeißer** – for biographies, see this issue, p. 15.

Paper

Comparison of composition of ultra-thin silicon oxynitride layers' fabricated by PECVD and ultrashallow rf plasma ion implantation

Robert Mroczyński, Tomasz Bieniek, Romuald B. Beck, Michał Ćwil, Piotr Konarski, Patrick Hoffmann, and Dieter Schmeißer

Abstract—In this paper differences in chemical composition of ultra-thin silicon oxynitride layers fabricated in planar rf plasma reactor are studied. The ultra-thin dielectric layers were obtained in the same reactor by two different methods: ultrashallow nitrogen implantation followed by plasma oxidation and plasma enhanced chemical vapour deposition (PECVD). Chemical composition of silicon oxynitride layers was investigated by means of X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS). The spectroscopic ellipsometry was used to determine both the thickness and refractive index of the obtained layers. The XPS measurements show considerable differences between the composition of the fabricated layers using each of the above mentioned methods. The SIMS analysis confirms XPS results and indicates differences in nitrogen distribution.

Keywords—ultra-thin dielectrics, oxynitride, SIMS, XPS, PECVD.

1. Introduction

Silicon oxynitride has been investigated extensively for several years as an alternative for silicon dioxide (e.g., [1]). This is mainly due to the fact that the dielectric constant of oxynitride is slightly higher than that of SiO_2, the reliability of the oxynitride/silicon system is better and boron and phosphorus diffusion is reduced. Moreover, the diffusion of atomic hydrogen is also suppressed by silicon oxynitride (e.g., [2]).

Nowadays, as the thickness of the gate dielectric layers has reached the scale of a few nanometers, understanding the chemical composition of such thin layers is of extreme importance. For appropriate characterization of such ultra-thin layers ultra-low energy secondary ion mass spectroscopy (ULE-SIMS) and XPS can be used [3, 4].

In this paper ultra-thin silicon oxynitride layers were fabricated in a planar rf plasma reactor. The dielectric layers were obtained in the same reactor using two different methods: ultrashallow nitrogen implantation followed by plasma oxidation (referred to hereafter as implantation/oxidation) and plasma enhanced chemical vapour deposition (PECVD). The source of plasma used during nitrogen implantation was either ammonia (NH_3) or pure nitrogen (N_2).

Chemical composition of silicon oxynitride layers was investigated by means of XPS and ULE-SIMS. Spectroscopic ellipsometry was used to determine the thickness and refractive index of the obtained layers.

2. Experimental

Two-inch ⟨100⟩ p type silicon substrates of the resistivity 4–7 Ωcm were used in this study. The silicon oxynitride films were fabricated in an Oxford plasma technology PlasmaLab 80+ system. The silicon substrates were cleaned using the standard RCA method. A schematic view of the equipment used is shown in Fig. 1.

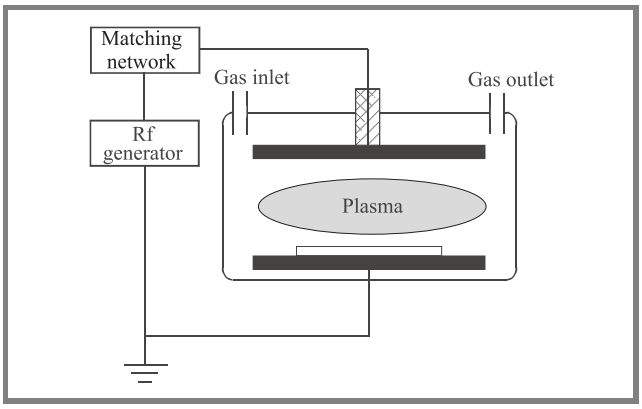

Fig. 1. Schematic view of the parallel plate reactor.

Process parameters necessary for ultra-thin oxynitride to be formed are presented in Table 1.

The properties of the obtained layers were studied by ellipsometric, XPS and ULE-SIMS analysis. A J.A. Woollam Co. ellipsometer allowing measurements at different angles with the wavelength ranging from 250 nm to 1400 nm was used to determine the thickness and refractive index of the investigated layers.

The XPS and ULE-SIMS measurements were used to investigate differences in the chemical composition and profiles of SiO_xN_y layers. XPS measurements were performed at 1254 eV at the Brandenburg University of Technology in Cottbus. SIMS measurements were done at the Industrial Institute of Electronics in Warsaw using

SAJW-05 system equipped with 06-350E Physical Electronics Ar+ gun (ultra-low energy 880 eV Ar^+ beam) and Balzers QMA-410 quadrupole mass spectrometer. Ar^+ beam (100 μm in diameter) was rastered over an area of 2 mm × 2 mm in order to get low ion current density and appropriate sputtering rate during ion bombardment. With this high in-depth resolution could be obtained.

Table 1
Process parameters allowing formation of ultra-thin dielectric layers

Parameters	Ultrashallow ion implantation		PECVD	
	Step 1 – plasma nitridation	Step 2 – plasma oxidation		
Power [W]	50		10	
Pressure [mTr]	500		300	500
SiH_4 (2%): N_2 flow [sccm]	–		150	
N_2O flow [sccm]	–		16	
NH_3 or N_2 flow [sccm]	50	–	32	
O_2 flow [sccm]	–	50	–	
Temp. [°C]	350		350	

Quantitative atomic concentration of nitrogen and oxygen was calculated based on Si_2N^+, Si_2O^+ and $Si_2{}^+$ secondary ion currents.

3. Results and disscusion

Thickness and refractive index of the obtained ultra-thin silicon oxynitride layers are presented in Table 2. These results combined with those of XPS measurements (to be discussed below) strongly indicate that the amount of silicon nitride phase is higher in the PECVD layers than in those fabricated using the implantation/oxidation technique. The refractive index of PECVD layers is significantly higher than that of implantation/oxidation ones. Additionally, its values are practically independent of process pressure (see Table 2). Moreover, the refractive index of oxynitride fabricated by means of implantation/oxidation depends on the plasma source used during implantation. In the case of pure nitrogen source the refractive index is very close to that of silicon dioxide ($N_{f\,\mathrm{layer}} = 1.44 \approx N_{f\,\mathrm{SiO_2}} = 1.46$) while the refractive index of layers obtained from ammonia source is between silicon dioxide and silicon nitride ($N_{f\,\mathrm{SiO_2}} = 1.46 < N_{f\,\mathrm{layer}} = 1.64 < N_{f\,\mathrm{Si_3N_4}} = 2$).

Table 2
Thickness and refractive index of ultra-thin silicon oxynitride layers evaluated from spectroscopic ellipsometry

Thickness [Å]	Ultrashallow plasma ion implantation		PECVD	
	NH_3 implantation	N_2 implantation	300 mTr	500 mTr
	36	36	30	38
N_f	1.63	1.44	1.95	1.98

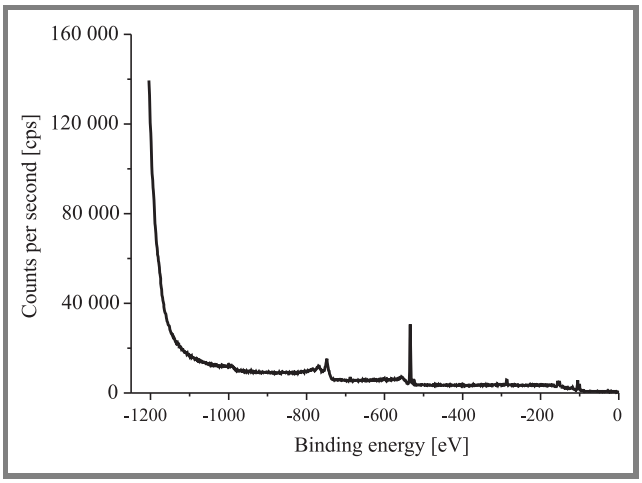

Fig. 2. The XPS spectrum of silicon oxynitride layer obtained by means of implantation/oxidation from ammonia source.

Comparison of composition and structure of ultra-thin silicon oxynitride layers was made using XPS analysis. Photoelectron spectra were taken at 1254 eV. In Fig. 2 a survey spectrum of an implantation/oxidation layer (ammonia source) is presented. Si2p (∼100 eV) and significant O1s (∼532 eV) peaks can be seen, while the N1s peak (∼398 eV) is not noticeable. It means that the nitride phase in this layer is practically absent.

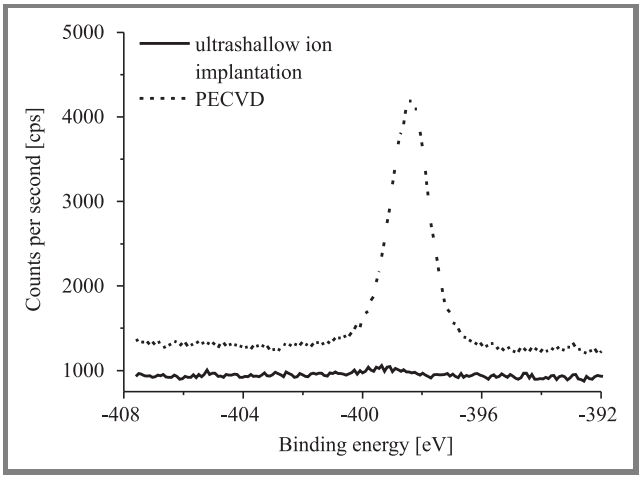

Fig. 3. Comparison of N1s spectra of PECVD and implantation/oxidation layers.

A comparison of N1s spectra obtained from PECVD and implantation/oxidation layers is shown in Fig. 3 confirming that the N1s peak of the implantation/oxidation layer is practically invisible, while it is very strong in the PECVD layer. This result might indicate that there is no nitrogen in the implantation/oxidation layers that consist of sil-

icon oxide only. One could argue then, that the implantation step failed at implanting nitrogen into the silicon subsurface region.

It is interesting to compare the nitrogen content in the fully formed implantation/oxidation layer with that directly after implantation [5]. We can clearly see that plasma oxidation, although taking place at low temperature, is extremely effective in removing nitrogen from the formed layer. Lower energy of nitrogen bonding with silicon than that of oxygen bonding with silicon is a well known reason for such an effect. However, this type of behavior has been so far reported in the case of high-temperature oxidation. In this work we have found evidence that this effect is also true for plasma oxidation at 350°C. As it will be shown below, some nitrogen remains in the oxide-silicon system.

In the PECVD layer, in turn, the amount of bonded nitrogen is significantly higher than implantation/oxidation layers – the nitrogen peak is clearly visible (see Fig. 3).

A comparison of O1s spectra of both types of ultra-thin silicon oxynitride layers is presented in Fig. 4. The concentration of bonded oxygen in implantation/oxidation layers is three times higher than in PECVD ones. These results will be discussed in more detail below using Figs. 6 and 7, where chemical composition of both types of silicon oxynitride is presented.

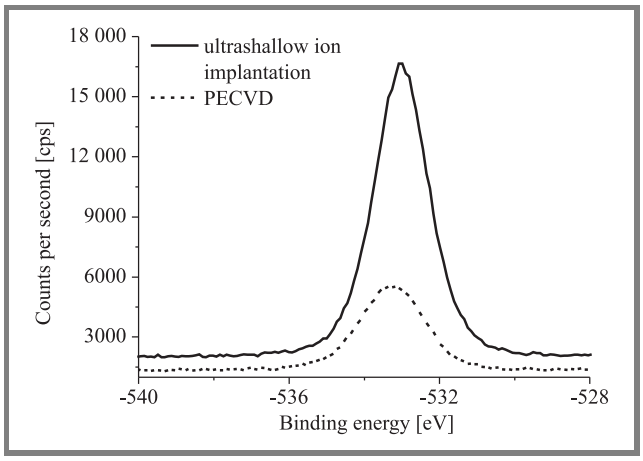

Fig. 4. Comparison of O1s spectra of PECVD and implantation/oxidation layers.

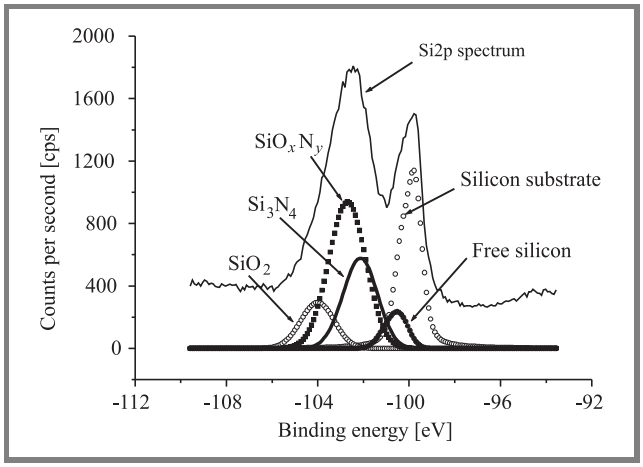

Fig. 5. Si2p line decomposition (PECVD sample, 500 mTr).

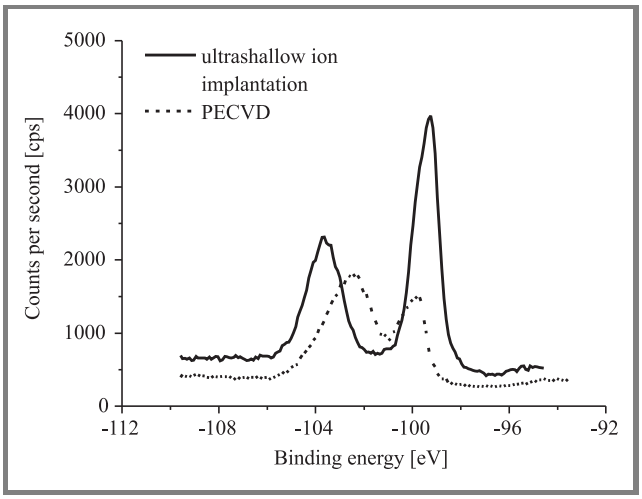

Fig. 6. Comparison of Si2p spectra of layers PECVD and implantation/oxidation layers.

The obtained emission lines were analyzed using curve-fitting procedure. An example of Si2p line deconvolution for a PECVD layer is shown in the Fig. 5. Since every single line may be attributed to a particular compound due to its unique binding energy, chemical composition of each layer may be determined.

The Si2p spectra of both types of ultra-thin silicon oxynitride layers are compared in Fig. 6. Si2p spectra of implantation/oxidation layers are characteristic for silicon dioxide layers. Similar spectra of thermal silicon dioxide may be found, e.g., in [6].

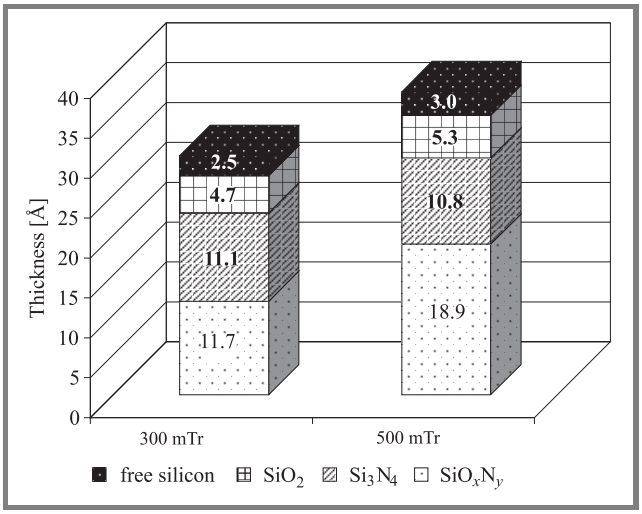

Fig. 7. Comparison of chemical composition (obtained from XPS spectra and expressed as thickness) of PECVD ultra-thin silicon oxynitride layers.

Chemical composition (as determined from the Si2p line) of PECVD and implantation/oxidation layers is shown in Figs. 7 and 8, respectively. The influence of process pres-

sure (300 mTr and 500 mTr) on the composition of PECVD layers is illustrated in Fig. 7. It should be noted that although SiO_xN_y and Si_3N_4 phases are the dominant compounds in the PECVD layer in both cases, increasing process pressure results in significant increase of SiO_xN_y only. The influence of nitrogen source (N_2 or NH_3) on the composition of implantation/oxidation layers is shown in Fig. 8. As seen, oxygen is present in implantation/oxidation layers in the form of silicon dioxide, which confirms the earlier conclusion that this type of oxynitride is almost classical silicon dioxide.

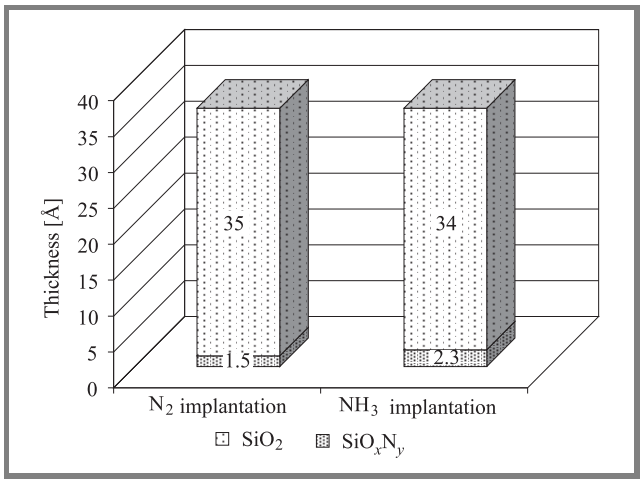

Fig. 8. Comparison of chemical composition (obtained from XPS spectra and expressed as thickness) of implantation/oxidation ultra-thin silicon oxynitride layers.

Comparison of Figs. 7 and 8 indicates that the composition of PECVD layers is more complex than that of implantation/oxidation ones. Furthermore, the chemical composition of the implantation/oxidation layers is characteristic of "classical" silicon dioxide.

The ULE-SIMS profiles of silicon, oxygen and nitrogen within the PECVD layers are shown in Fig. 9. No significant difference in the atomic profiles obtained from layers formed under different process pressure is observed. Moreover, the maximum concentration of both oxygen and nitrogen in the layers is almost the same for both PECVD conditions.

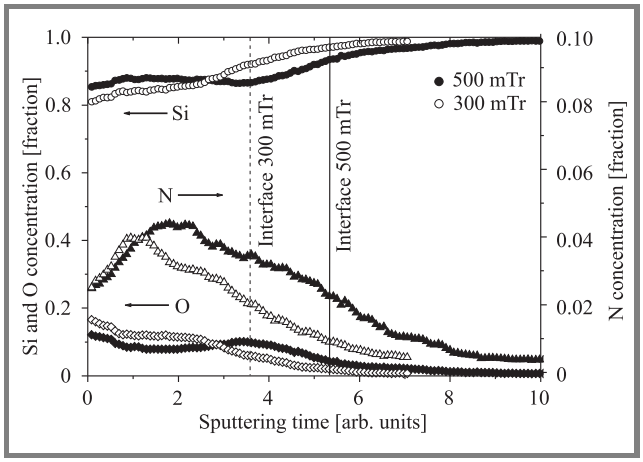

Fig. 9. Comparison of composition profiles (obtained by ULE-SIMS) of PECVD ultra-thin oxynitride layers.

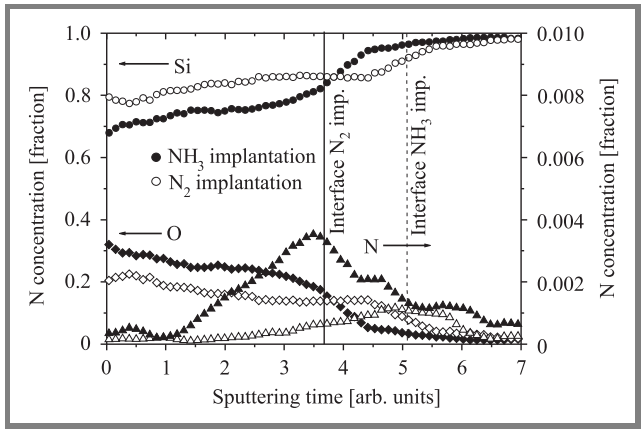

Fig. 10. Comparison of composition profiles (obtained by ULE-SIMS) of implantation/oxidation ultra-thin oxynitride layers.

Profoundly different conclusions may be drawn from Fig. 10, which shows profiles of silicon, oxygen and nitrogen in implantation/oxidation layers. Different profiles may be achieved depending on the source nitrogen ions. Maximum concentration of both oxygen and nitrogen is lower in oxynitride layers obtained by means of implantation from pure nitrogen plasma than in those formed using ammonia source. When the concentration of nitrogen in the bulk of the layer is taken into account, it becomes obvious that ammonia source is more effective than pure nitrogen source.

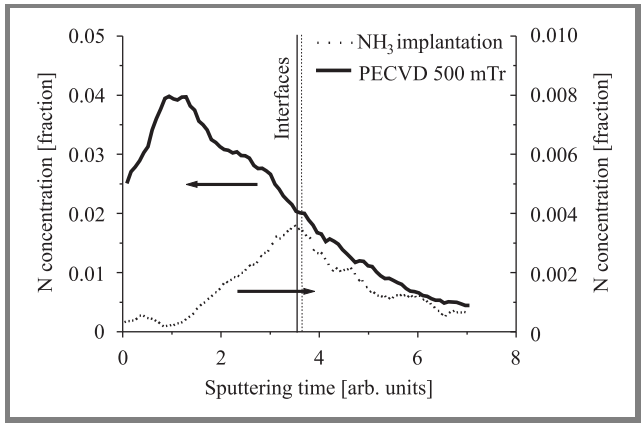

Fig. 11. Comparison of nitrogen profiles (obtained by SIMS) in oxynitride – silicon systems fabricated by means of PECVD and implantation/oxidation.

A direct comparison of nitrogen profiles obtained from PECVD and implantation/oxidation layers is shown in Fig. 11. It should be noted that nitrogen pile-up is observed at a certain depth in PECVD layers while the highest nitrogen concentration in implantation/oxidation is located near the dielectric-silicon interface. Moreover,

the nitrogen content in PECVD layers is one order of magnitude higher than implantation/oxidation layers. In the literature published so far it is commonly agreed that nitrogen incorporation not exceeding a certain limit (~ 0.1 at. %) at or near the Si channel interface improves device performance, while higher amounts of N near this interface make device properties deteriorate [7]. It is also known that introduction of nitrogen near the dielectric/poly-Si interface prevents boron penetration if the p^+-poly-Si gate is used [8]. Taking into account these findings and the results presented in this paper, it can be concluded that nitrogen profile may be engineered using a multi-stage process combining PECVD and implantation/oxidation steps. Moreover, unlike the approach of Mian and Flora [9], who demonstrated a technique to engineer the nitrogen profile in an ultra-thin oxide by changing the oxidation sequence in O_2 and N_2O by RTP, low temperature processing in the standard planar rf plasma reactor is compliant with the requirement to keep silicon nanotechnology thermal budget low.

4. Conclusions

In this paper differences in chemical composition of ultra-thin silicon oxynitride layers fabricated in standard rf planar reactor were studied.

The investigations carried out in this work showed that the two investigated methods of ultra-thin silicon oxynitrides fabrication result in completely different chemical composition.

The PECVD SiO_xN_y layer composition is more complex than that of oxynitride formed by means of implantation/oxidation. Moreover, ultra-thin silicon oxynitride obtained using the latter method is almost a "classical" silicon dioxide (SiO_2) which is proved not only by chemical composition but also by refractive index value.

The two studied methods result also in different nitrogen profiles. In the PECVD oxynitride the highest concentration of nitrogen is located near the metal gate/dielectric interface, while for the implantation/oxidation oxynitride – at the dielectric/Si interface. These differences may be used to our advantage in particular devices. Additionally, using a multi-step process combining both methods, the required nitrogen profile may be achieved. It should be remembered that this variety of nitrogen profiles may be obtained using very low temperature processes, which is of great importance to next generations of ULSI-CMOS technology.

Acknowledgements

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Tomasz Bieniek and **Romuald B. Beck** – for biographies, see this issue, p. 7.

Michał Ćwil and **Piotr Konarski** – for biographies, see this issue, p. 8.

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Paper

The role of fluorine-containing ultra-thin layer in controlling boron thermal diffusion into silicon

Małgorzata Kalisz, Romuald B. Beck, Adam Barcz, and Michał Ćwil

Abstract—We have investigated the influence of silicon dioxide reactive ion etching (RIE) parameters on the composition of the polymer layer that is formed during this process on top of the etched layer, and finally, the role of this layer in high-temperature thermal diffusion of boron into silicon. The polymeric layer formed on the etched surface appeared to consist of fluorine and silicon fluoride (SiOF and SiF). Concentration of these components changes depending on the parameters of RIE process, i.e., rf power, gas pressure and etching time. The composition of this polymeric layer affects, in turn, boron thermal diffusion into silicon. With increasing rf power, the depth of boron junction is increased, while increasing time of etching process reduces boron diffusion into silicon.

Keywords— fluorine, reactive ion etching, silicon fluoride, boron thermal diffusion, fluorocarbon plasma.

1. Introduction

When silicon dioxide or silicon are exposed to fluorocarbon plasma (e.g., CF_4) during reactive ion etching (RIE), an ultra-thin polymer layer consisting of fluorine and silicon fluoride (SiOF and SiF) is formed on the etched surface. In fact, etching and polymer deposition take place in parallel (e.g., [1, 2]). It is reasonable to expect that concentration of these components depends on the RIE process parameters, e.g., rf power, gas pressure and etching time.

On the other hand, for the past few years, fluorine and its chemical compounds have been investigated as a means to reduce boron thermal diffusion into silicon.

In this work we try to find correlations between the parameters of RIE applied to silicon dioxide, the chemical composition of the polymer layer and the rate of high-temperature boron diffusion into silicon through that polymer layer.

2. Experiment

N-type, phosphorus-doped (100)-oriented silicon wafers with resistivity of 4–10 Ωcm were cleaned using standard procedures prior to oxidation. After that 150 Å thick thermal oxide was formed.

In the next step, this oxide layer was etched off at constant room temperature by RIE in CF_4 (50 sccm) under various process conditions: rf power, gas pressure and etching time. Boron thermal diffusion was studied afterwards at two temperatures: 1000°C and 1100°C. The matrix of experiments is shown in Table 1.

The chemical composition of the thin polymer layer, formed on the etched surface of silicon dioxide during RIE in fluorocarbon plasma, has been evaluated by ultra-low-energy secondary ion mass spectrometry (ULE-SIMS). Ellipsometry was used to obtain the thickness of this layer.

Table 1
The matrix of experiments

Experiments	RIE parameters		Diffusion parameters		
	Time [min]	Power [W]	Pressure [mTr]	Temperature [°C]	Time [min]
1	1	80	200	1100	30
2	2	80	200	1100	30
3	7	80	200	1100	30
4	10	80	200	1100	30
5	10	120	200	1100	30
6	10	180	200	1100	30
7	2	80	200	1000	30
8	7	80	200	1000	30
9	10	80	200	1000	30
10	10	80	100	1000	30
11	10	180	200	1000	30

The depth of boron diffusion into silicon was determined by grooving and staining. Boron profiles in samples 1 to 6 were measured by means of high-energy secondary ion mass spectrometry.

3. Results and discussion

It has already been established (e.g., [1, 2]) that an ultra-thin polymer layer is formed on the etched surface of silicon dioxide or silicon during RIE process in fluorocarbon plasma. Surface chemical reactions during RIE process, depending on the etching process parameters, are responsible for this situation.

When SiO_2 surface is irradiated with CF_4 atoms, free fluorine ions penetrate the bulk of the oxide, displace atoms in dangling bonds and form new compounds like SiOF or SiF. Fluorine is accumulating in the polymer layer as free ions, too [3]. Da Zhang observed that during oxide etching the bombarding fluorine ions break O-Si-O bounds.

Dangling and unsaturated Si-O and Si bonds are formed on the surface. As a result of free fluorine ions reacting with broken bonds, SiOF and SiF species appear on the surface as chemical components of the polymer layer formed [3].

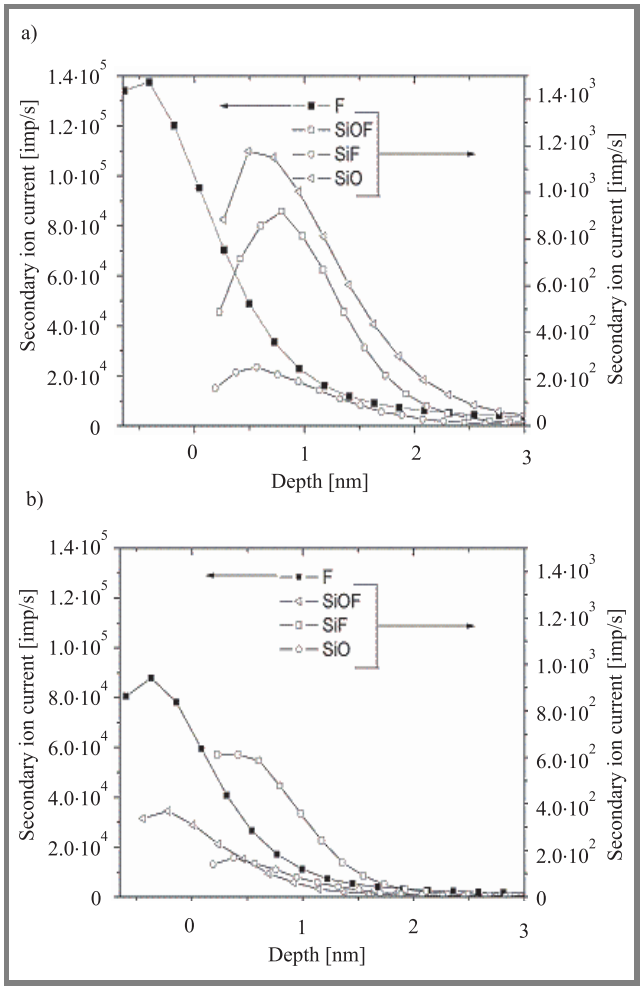

Fig. 1. Profiles of chemical components of the polymer layer (determined by ULE-SIMS) for two samples: (a) CF_4 = 50 sccm, $p = 200$ mTr, $P = 80$ W, $t = 2$ min; (b) CF_4 = 50 sccm, $p = 200$ mTr, $P = 80$ W, $t = 7$ min.

The results of ULE-SIMS obtained for two samples are presented in Fig. 1. It is clear that the surface of the silicon substrate is covered by a layer containing SiO_2, SiOF and SiF species with the thickness of a few nanometers. The chemical composition of this polymer layer has been measured by ULE-SIMS, which yields relative concentrations of chemical components only.

The SiOF concentration in ultra-thin polymer layer is constant with increasing etching time (compare Fig. 1 or see Fig. 2c) and is increased very strongly with increasing rf power and gas pressure (Fig. 2a and 2b).

The fluorine concentration in polymer layer is varying with RIE process parameters too, but in a different way. Fluorine concentration increases only with increasing etching time (compare Fig. 1 or see Fig. 2c).

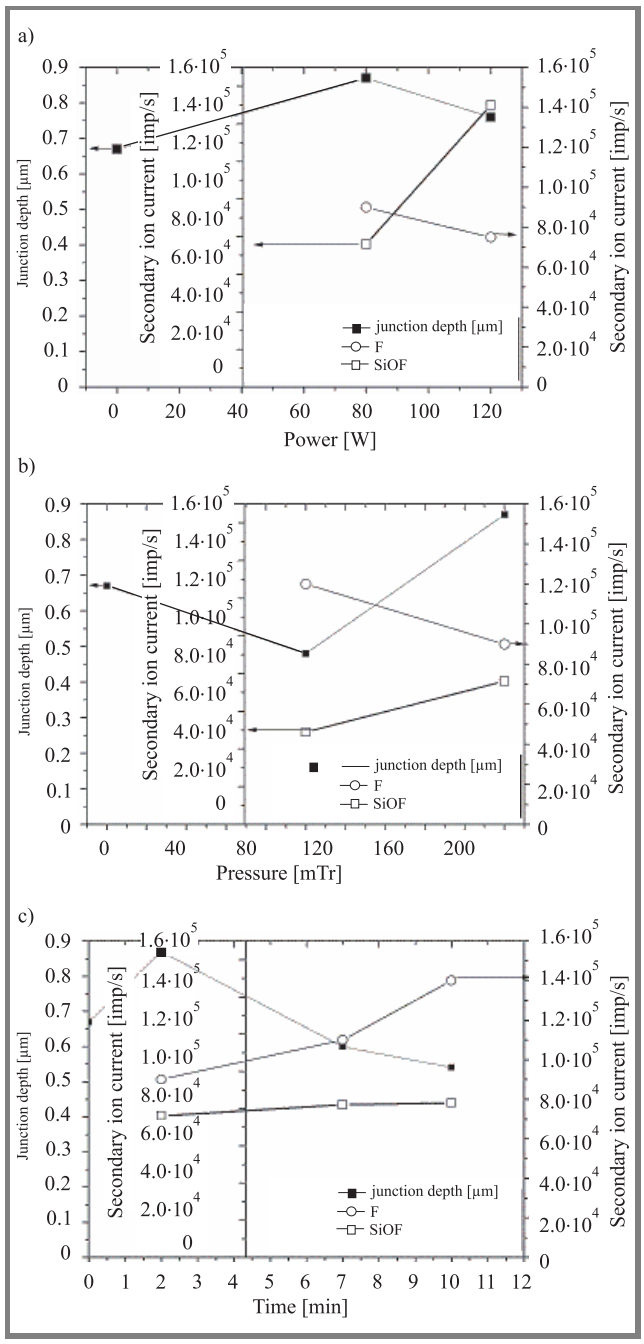

Fig. 2. Concentration of SiOF and F in the polymer layer formed on etched surface during RIE of silicon dioxide: (a) at constant etching time of 2 min, gas pressure of 200 mTr and rf power varying between 80 W and 120 W; (b) at constant rf power of 80 W, etching time of 2 min and gas pressure varying between 100 mTr and 200 mTr; (c) at constant rf power of 80 W, gas pressure of 200 mTr and etching time varying between 2 min and 10 min.

Figure 1 indicates that SiF concentration changes similarly to fluorine concentration. The amount of SiF in the layer increases with increasing etching time. For a short etching time (1 min or 2 min) and low rf power (80 W), SiOF concentration in the polymer layer is higher than that of SiF (see Fig. 1a). This may be due to the fact that many

more broken Si-O bonds exist at the etched surface than Si bonds.

This situation changes with increased etching time (7 min or 10 min). In this case, the concentration of SiF in the polymer layer increases, and is higher than the concentration of SiOF (see Fig. 1b). This is probably caused by reduced density of broken Si-O bonds and increased density of dangling and unsaturated Si and SiF bonds. Reduction of broken Si-O bond density is obtained at a certain moment, when the whole SiO_2 layer is already etched off and silicon etching begins. Free fluorine ions react then with broken Si bonds of the silicon substrate and form SiF species.

On the other hand, variation of rf power (from 80 W to 120 W – for longer etching time – 10 min) makes SiOF concentration increase (see Fig. 2a). This is probably due to high concentration of Si-F bounds existing at the etched surface for higher rf power. As it has already been established in [3] SiF species does not have preferable energetic structure. Therefore, exposing the sample to the air causes spontaneous reaction of this species with free oxygen, both from air and SiOF species, the energetic structure of which is much more stable [3]. Consequently, an increase of SiOF concentration is observed in the polymer layer.

As it can be seen in Table 2, the thickness of polymer layer depends on RIE process parameters. As expected, the thickness decreases with increasing etching time, while

Table 2
The relationship between SiOF layer thickness and RIE process parameters

Experiments	RIE parameters			Polymer layer thickness [Å]
	Time [min]	Power [W]	Gas pressure [mTr]	
1	1	80	200	98
2	2	80	200	50
3	7	80	200	24
4	10	80	200	4
5	10	120	200	8
6	10	180	200	12

increasing rf power makes it increase. The effects described by Da Zhang in [3] are probably responsible for these results. Da Zhang observed that the deposited polymer is simultaneously etched off by oxygen released from broken Si-O bonds during silicon dioxide etching. Free oxygen diffusses through silicon dioxide to the interface and etches the deposited polymeric layer from underside. This is why the layer formed on the etched surface is very thin (about 4 Å) [3]. Deposition and etching of the polymer layer take place in parallel.

As we can see in Table 2, with increasing rf power (from 80 W to 120 W) the thickness of the polymer layer increases from 4 Å to 10 Å – 12 Å. This is probably due to spontaneous oxidation of unsaturated bonds that replaced etching of the deposited polymer by oxygen (as described by Da Zhang in [3]).

F/SiOF concentration ratio decreases with increasing values of rf power or process pressure and increases with increasing time of etching (see Fig. 2).

In Fig. 3 boron profiles (obtained from SIMS measurements) resulting from thermal diffusion at 1000°C and

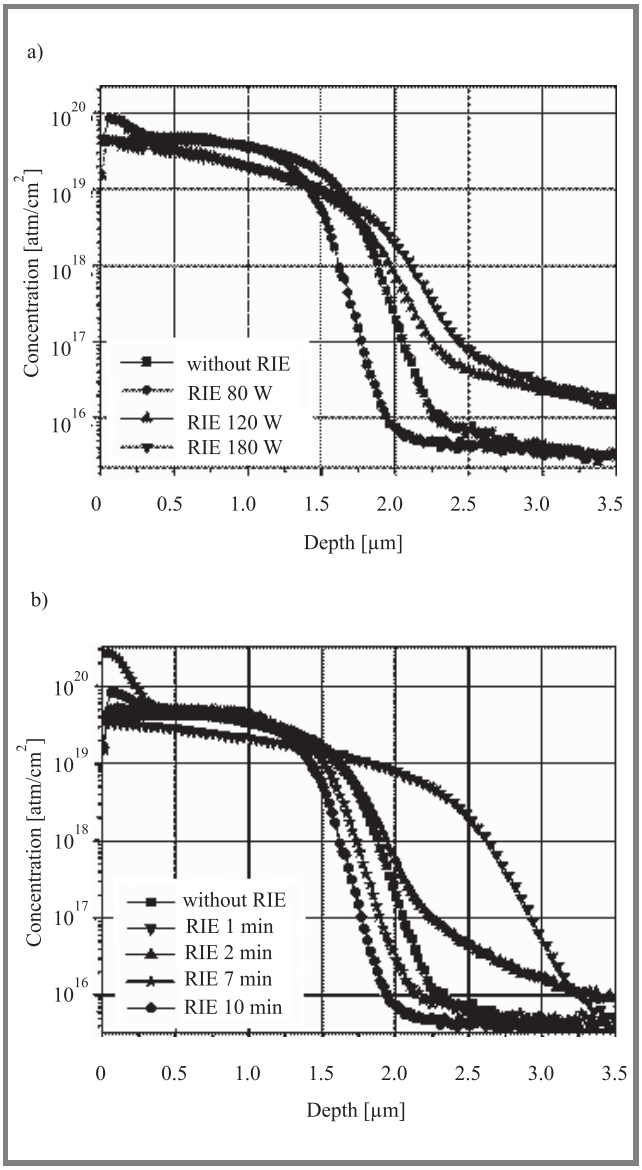

Fig. 3. Boron profiles for different: (a) rf power; (b) etching time.

1100°C are presented. For the sake of clarity, the reference profile of a sample not exposed to any RIE process is also shown. It is visible that both, the junction depth and the whole dopant profile, depend on the parameters of RIE.

If we compare all the obtained results, i.e., polymer layer composition, polymer layer thickness and the depth of boron thermal diffusion with RIE parameters, the depen-

dence of boron junction depth on the rf plasma power used during RIE is simple. The higher the rf power, the deeper the junction (Fig. 3a). It is, however, surprising to see the reference profile between these obtained at 80 W and 120 W of rf power. Surface modification during RIE process could possibly explain this result.

There is a significant difference between the reference samples and those that underwent RIE of thermal oxide. The silicon surface of the former ones is clean, while the latter ones the polymer layer on top of silicon. This layer obviously creates an additional barrier for boron thermal diffusion. Its thickness depends on RIE parameters, as has already been discussed above.

Intuitively one would expect that boron junction to deepen with thinner polymer layers. The results obtained at different rf power demonstrate that this simple relation does not hold true (see Fig. 3).

Our results show that boron thermal diffusion depends on the chemical composition of the polymer layer. Thinner layers, formed at low rf power, happen to have low SiOF concentration and high concentration of F species (Fig. 1b). As we know from [4] high concentration of F may reduce boron diffusion into silicon. This is probably why we get shallower junctions for thinner layers with high concentration of fluorine (compare Figs. 1b and 3a). In thicker layers the situation is opposite. High concentration of SiOF, obtained in polymer layers formed at high rf power, accelerates boron diffusion into silicon [5], therefore we get deeper junctions.

As we can see in Fig. 3b, with increasing time of etching, the depth of boron diffusion is decreased. Also in this case the reference profile is placed between these for short (1 min and 2 min) and long (7 min and 10 min) etching times. The hypothesis relating the boron profile depth to the composition of the layer may also be used in this case. For longer times of etchnig the concentration of SiOF in the polymer layer was lower and the concentration of SiF and F was higher (Fig. 1). Therefore, for short times of etching (1 min and 2 min), the depth of boron junction is higher than for clean silicon, and for long times of etching (7 min and 10 min), the depth of boron junction is lower than for clean silicon (see Fig. 3b).

A comparison of the obtained results indicates that boron profile depth depends on the relative concentration of SiOF and F in the polymer layer.

High F/SiOF concentration ratios slow down boron thermal diffusion into silicon and shallower junction is formed (Fig. 2). It seems reasonable to conclude that SiOF increases the diffusion rate, while F reduces it.

4. Conclusion

In this study, the influence of RIE parameters on the chemical components of polymer layer and depth of boron thermal diffusion was investigated. The obtained results show that the chemical composition of the polymer layer depends on RIE parameters and this, in turn, affects the depth of boron diffusion.

It is visible that RIE parameters determine the thickness and chemical composition of the polymer layer and the depth of boron diffusion into silicon. From the obtained results it becomes clear that the depth of boron thermal diffusion does not depend on the thickness of the polymeric layer formed on the silicon surface during RIE process in fluorocarbon plasma, but on its chemical composition. Each of polymer layer chemical components plays a different role during thermal diffusion of boron into silicon. SiOF accelerates boron diffusion into silicon, while SiF and F slow it down. The final conclusion is that RIE parameters determine the depth of boron thermal diffusion.

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Romuald B. Beck – for biography, see this issue, p. 7.

Michał Ćwil – for biography, see this issue, p. 8.

Paper

Oxidation kinetics of silicon strained by silicon germanium

Jarosław Grabowski and Romuald B. Beck

Abstract—This paper reports on the studies of oxidation kinetics of silicon strained by silicon germanium layers. Experimental results of natural, chemical and thermal oxide formation are presented. The oxidation rates of silicon strained by SiGe layers have been compared with the rates of pure Si oxidation. The oxidation kinetics was studied using the parallel model proposed by Beck and Majkusiak. This model was fitted with good result to the obtained experimental data and the parameter that is most probably responsible for the strain effect was identified, as well as its dependence on Ge content in the SiGe layer.

Keywords—oxidation, kinetics, modeling, silicon, silicon germanium.

1. Introduction

Constant increase of speed in every IC generation is an obvious trend in the development of microelectronics. So far it has been achieved mostly by continuous down-scaling of devices over the years. Using silicon germanium is another way to reach this goal (e.g., [1, 2]). A thin, relaxed layer of SiGe alloy can induce enough strain in a silicon cap to improve carrier mobility (e.g., [3]). However, introduction of any new material into IC production requires that both, processing and its successful integration, have to be ensured.

This paper covers selected types of strained Si oxidation, namely natural, chemical and thermal oxidation.

2. Experimental and results

In our experiments, samples containing silicon substrate covered with relaxed SiGe buffer (with varied Ge content) and topped with Si cap were used. The samples were fabricated at the University of Warwick by means of either molecular beam epitaxy (MBE) or low pressure chemical vapor deposition (LPCVD). We used J. A. Woolam spectroscopic ellipsometer to investigate the thickness of every oxide.

In the first part of the study the thickness of natural oxide grown spontaneously on the silicon cap strained by the underlying SiGe buffer was measured using spectroscopic ellipsometry. In chemical-oxidation experiments (second stage) we used SC1 mixture (H_2O-NH_4OH-H_2O_2 5:1:1). Samples were kept in this mixture for 10 min at 90°C. The obtained results (natural oxide and chemical experiment) are presented in Table 1.

Table 1
Results of natural and chemical oxide thickness measurements

Fabrication method	SiGe thickness [nm]	Ge fraction [%]	Native oxide thickness [nm]	Chemical oxide thickness [nm]
Si ref.	–	–	1.7	2.0
LPCVD	7	5	1.5	2.0
LPCVD	7	10	1.5	1.9
LPCVD	7	20	1.5	1.9
LPCVD	7	30	1.6	1.9
MBE	18	14	2.0	8.4
MBE	19	13	4.2	–

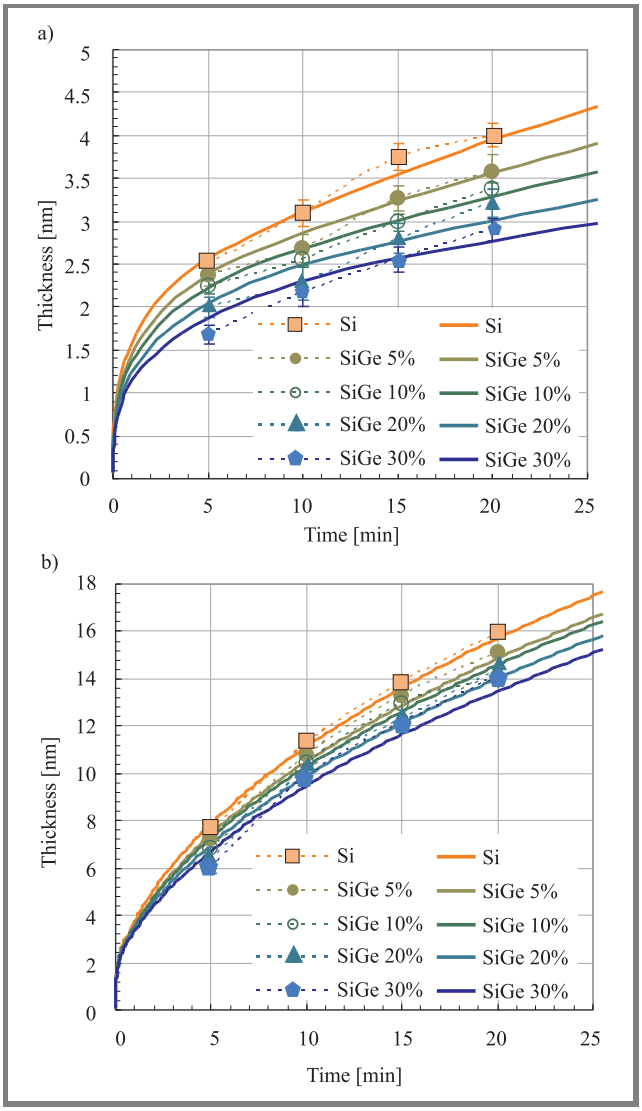

Fig. 1. Dependence of the kinetics of thermal oxidation at: (a) 800°C and (b) 900°C on Ge fraction in the SiGe layer (dots – experiment, lines – model).

In the third stage of this study, thermal oxidation experiments were performed at two different temperatures (800°C and 900°C) in dry oxygen with 0.25 l/min oxygen flow. Figure 1 shows the thickness (measured by means of ellipsometry) of thermal oxides grown at 800°C and 900°C, respectively.

The parallel model proposed by Beck and Majkusiak (B-M) and presented schematically in Fig. 2 has already been used

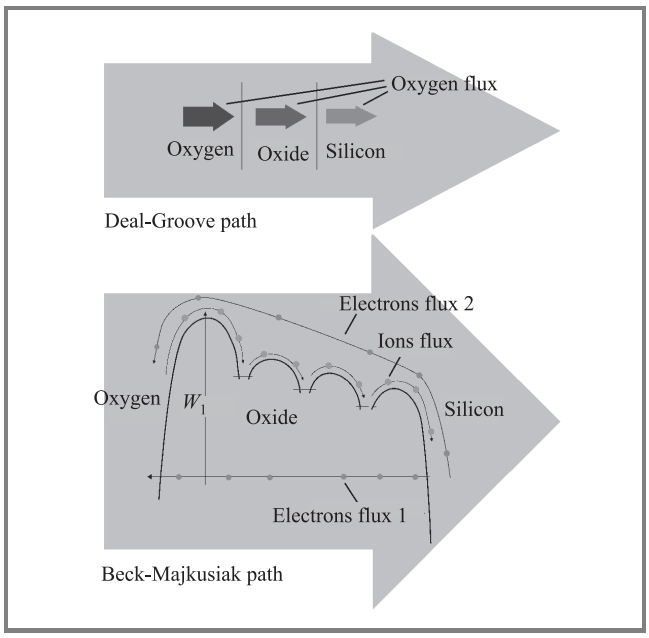

Fig. 2. Oxidation kinetics model proposed by Beck and Majkusiak.

to model thermal oxidation kinetics (e.g., [4–7]). According to this model oxidation species are supplied to the reaction site by two parallel paths. The first one is described by the traditional 3-parameter Deal-Groove model [8]. The other, parallel path is the flow of oxygen ions. This flux is controlled by electrochemical effects (balance of oxygen ions flow to the reaction sites and electrons supply to the surface) and is described by seven additional parameters. The B-M model was fitted to all the experimental data obtained in this study (Fig. 1) and all of its parameters were determined. It appears that only one of these model parameters is critical for good fitting of the B-M model to the data obtained from samples with different Ge concentration in SiGe buffer. This parameter is the initial potential barrier height (W_1) for the flux of ions entering the oxide (see Fig. 2).

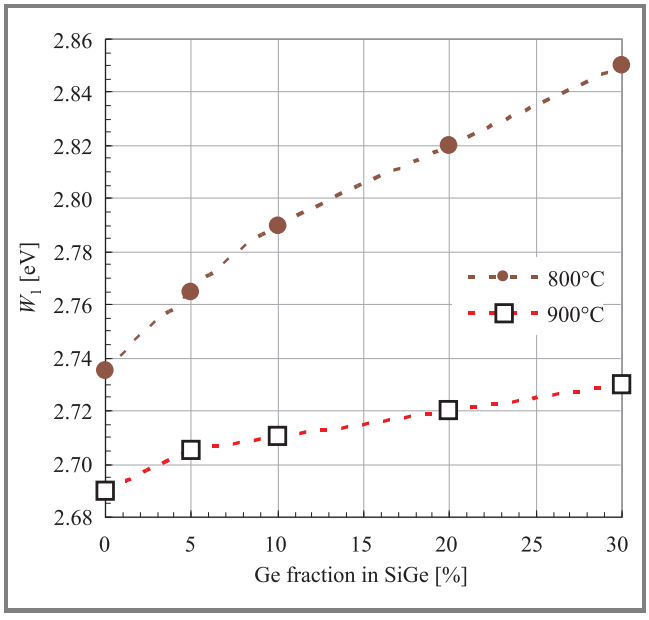

Fig. 3. Values of W_1 providing good fitting of the B-M model to the experimental data obtained from samples with different Ge fraction in the SiGe layer.

Figure 3 shows the values of the initial potential barrier height (W_1) that provide a good fit of the B-M model to the experimental data as a function of Ge concentration in the SiGe buffer for both studied temperatures. When Ge concentration and strain level in the silicon cap increase, the height of the initial potential barrier W_1 increases consistently for both temperatures.

3. Discussion

Significant differences in the natural and chemical oxide thickness are visible between MBE and LPCVD samples. This indicates that the method used for SiGe formation might have critical influence on its chemical and physical properties. Natural and chemical oxide thickness of LPCVD samples is almost independent of Ge concentration in the SIGe buffer. Very weak decrease of oxide thickness is observed with increasing Ge concentration. Relatively high oxide thickness of MBE samples might result from the strain induced in the silicon caps leading to higher oxidation rates.

In the case of LPCVD samples the results obtained in the course of thermal oxidation were similar to natural and chemical experiments. They show that strained silicon layers oxidize even more slowly than the reference Si wafers. It can be seen that when the strain increases (through the increase in Ge concentration in the SiGe layer), oxidation rate becomes lower.

In the B-M model, the initial potential barrier height (W_1) is the parameter responsible for the description of oxygen ions entering into the growing oxide. Therefore, a change of its value may mean a change of the growing oxide surface conditions (e.g., surface contamination). While the reasons for this effect are not clear, at least two hypotheses may be proposed.

First, germanium atoms may migrate from silicon germanium into the strained silicon cap and contaminate it. After oxidation these atoms may contaminate the newly formed oxide layer. The contamination of silicon to be oxidized also changes the conditions of the oxidation process (chemical reaction rate). The resulting changes in the oxidation rate may compete with the results of strain in the cap. Moreover, germanium outdiffusion from the SiGe layer

(due to high temperature during oxidation) tends to relax the strain in the cap. In such conditions the expected dependence of the oxidation rate on germanium concentration in SiGe should become weaker with increasing oxidation time. In fact this hypothesis seems to be confirmed by recent studies carried at the University of Warwick.
Second, it is possible that the B-M model is not suitable for strained samples. This would mean that good fitting of the B-M model to the oxidation kinetics affected by changes in Ge concentration in SiGe layer is merely a coincidence and that a parameter (or parameters) other than W_1 is really responsible for this effect. It should be mentioned, however, that the values of W_1 are in all cases physically meaningful and reasonable for the energy diagram assumed in the model, which would suggest that this hypothesis is less probable than the previous one.

4. Conclusions and summary

The presented results demonstrate that MBE samples exhibit higher oxidation rate than LPCVD ones in the case of natural and chemical oxidation experiments.
Oxidation rate of LPCVD samples is lower than that of reference Si wafers. It seems also that natural and chemical oxide thickness of LPCVD samples does not depend on Ge concentration in SiGe.
Thermal oxidation experiments (in the initial oxidation phase) show that increasing Ge concentration in the SiGe layer leads to lower oxidation rates for LPCVD samples.

The B-M model was used to study thermal oxidation kinetics. In this model only one parameter responsible for the observed changes in the oxidation kinetics was found. Although two different hypotheses explaining the correlation between this parameter and the observed strain effects were proposed, the recent study carried out at the University of Warwick seem to support only the first one.

Acknowledgments

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Paper

Influence of the deposition process parameters on electronic properties of BN films obtained by means of RF PACVD

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Abstract—This work presents results of investigations of electronic properties of undoped boron nitride (BN) films produced on Si substrates in the course of radio frequency (rf) PACVD process with boron triethyl $(C_2H_5)_3B$ as the boron source. The influence of the deposition process parameters on thickness and electronic properties (resistivity ρ, dielectric strength E_{BR}) of BN films based on ellipsometry and *I-V* curve measurements at room temperature is studied. The obtained results show that proper selection of deposition process parameters allows BN layers with the required thickness and advantageous values of ρ and E_{BR} to be fabricated. BN becomes therefore an interesting material for microelectronics applications.

Keywords*— *III-nitrides, thin BN films, electronic properties, RF PACVD.

1. Introduction

Dynamic development of microelectronics creates an increased demand for new materials. New areas of application emerge, where typical semiconductor devices run a risk of high-temperature and/or high power emission. Unfortunately, classic silicon-based devices are not capable of working in such operation regimes. One of the potential ways to overcome this problem is to develop fabrication technologies and applications involving the use of wide band-gap materials like diamond or III-group nitrides (GaN, AlN and in particular BN).

Cubic boron nitride (c-BN) with its unique properties, such as wide band gap (6.4 eV), chemical inertness, good thermal stability and thermal conductivity (~1300 W/mK), is considered a prospective material for electronic applications in high-temperature and high-power electronics, particularly in combination with other wide band-gap materials [1, 2]. It is worth to emphasize that the expected working temperature of BN-based devices can reach even up to 900°C! [2].

2. Experimental details

Boron nitride films were produced on p-type Si ($\langle 100 \rangle$, $\rho = 6 - 8$ Ωcm) substrates using radio frequency plasma assisted chemical vapor deposition (RF PACVD) method [3–5]. Layers were synthesized from boron triethyl $(C_2H_5)_3B$ vapors carried by nitrogen N_2. Then circular, aluminum (Al) electrodes (diameter = 1 mm, gate area = $7.85 \cdot 10^{-3}$ cm^2) were evaporated on the top of the deposited layers. As a result metal-insulator-semiconductor (MIS) structures with BN thin films acting as the insulator were fabricated.

Table 1
Process parameters of RF PACVD deposition

Parameters	Voltage [V]	Time [s]	N_2 flow [cm^3/min]	$(C_2H_5)_3B$ flow [a.u.]
Value 1	70	30	10	200
Value 2	105	60	20	250
Value 3	140	90	30	300

Table 2
Thickness of the deposited BN layers

Process	Voltage [V]	Time [s]	N_2 flow [cm^3/min]	$(C_2H_5)_3B$ flow [a.u.]	Thickness $x/(x+i\cdot\text{period})$; $i = 1, 2, 3\ldots$ [Å]
1	70	30	10	200	391 / 2579
2	70	60	20	250	1770 / 2540
3	70	90	30	300	111 / 1567
4	105	30	20	300	2220 / 2568
5	105	60	30	200	513 / 2514
6	105	90	10	250	985 / 2538
7	140	30	30	250	1039 / 2455
8	140	60	10	300	1515 / 2506
9	140	90	20	200	474 / 2524
1^{bis}	70	30	10	200	633 / 2532

Deposition parameters subsequently used in the Taguchi-based process analysis method [6] are presented in Table 1, whereas the results of BN film thickness measurements are collected in Table 2.

3. Results

Applying Taguchi's method allowed the influence of input process parameters (self-bias potential, deposition time, flow rates of reactant vapors N_2 and $(C_2H_5)_3B$) on its output parameters – in this case thickness x, resistivity ρ and critical electric breakdown field E_{BR} (being the measure of dielectric strength) of deposited BN layers to be analyzed. The dependence of the film thickness on process parameters is illustrated in Fig. 1.

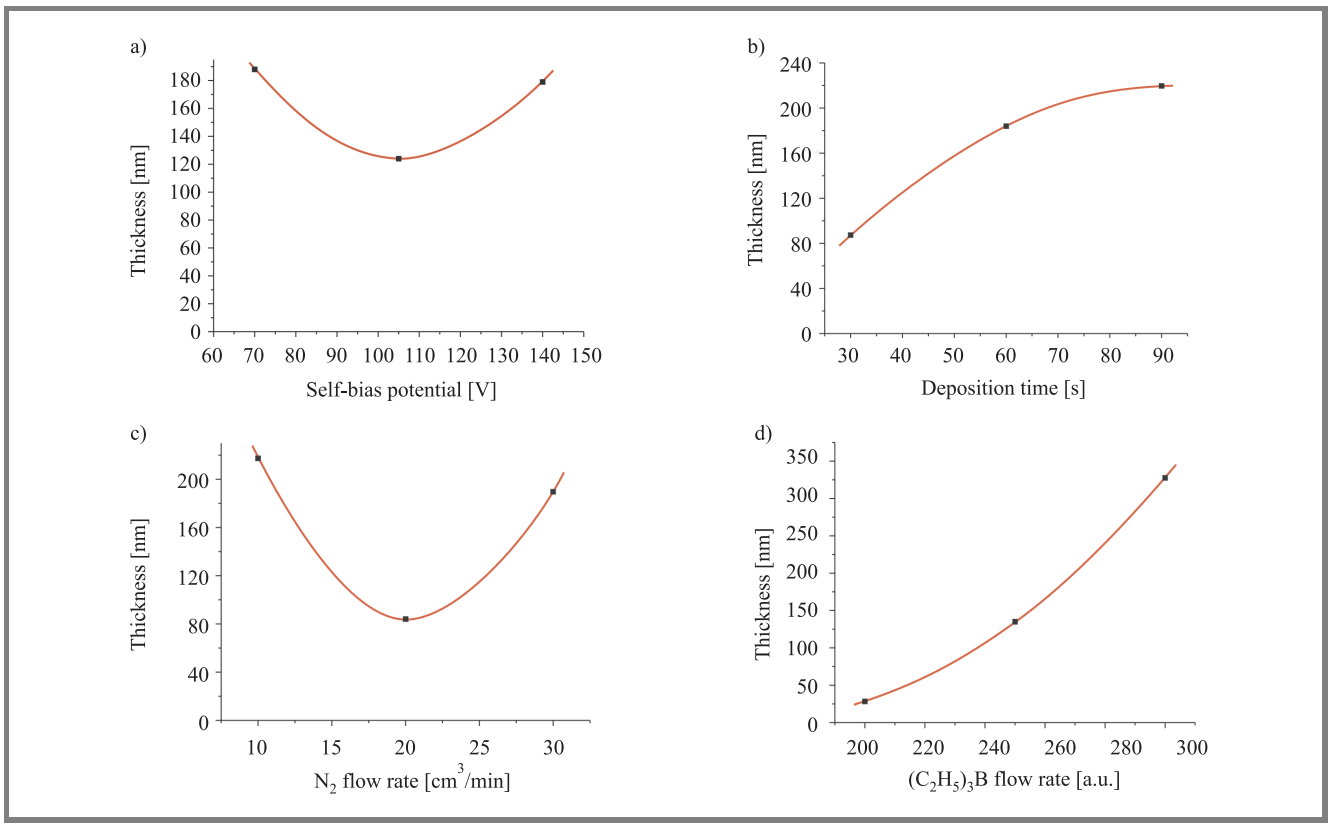

Fig. 1. Influence of the: (a) self-bias potential; (b) deposition time; c) N_2 flow rate; (d) $(C_2H_5)_3B$ flow rate on thickness of BN layers.

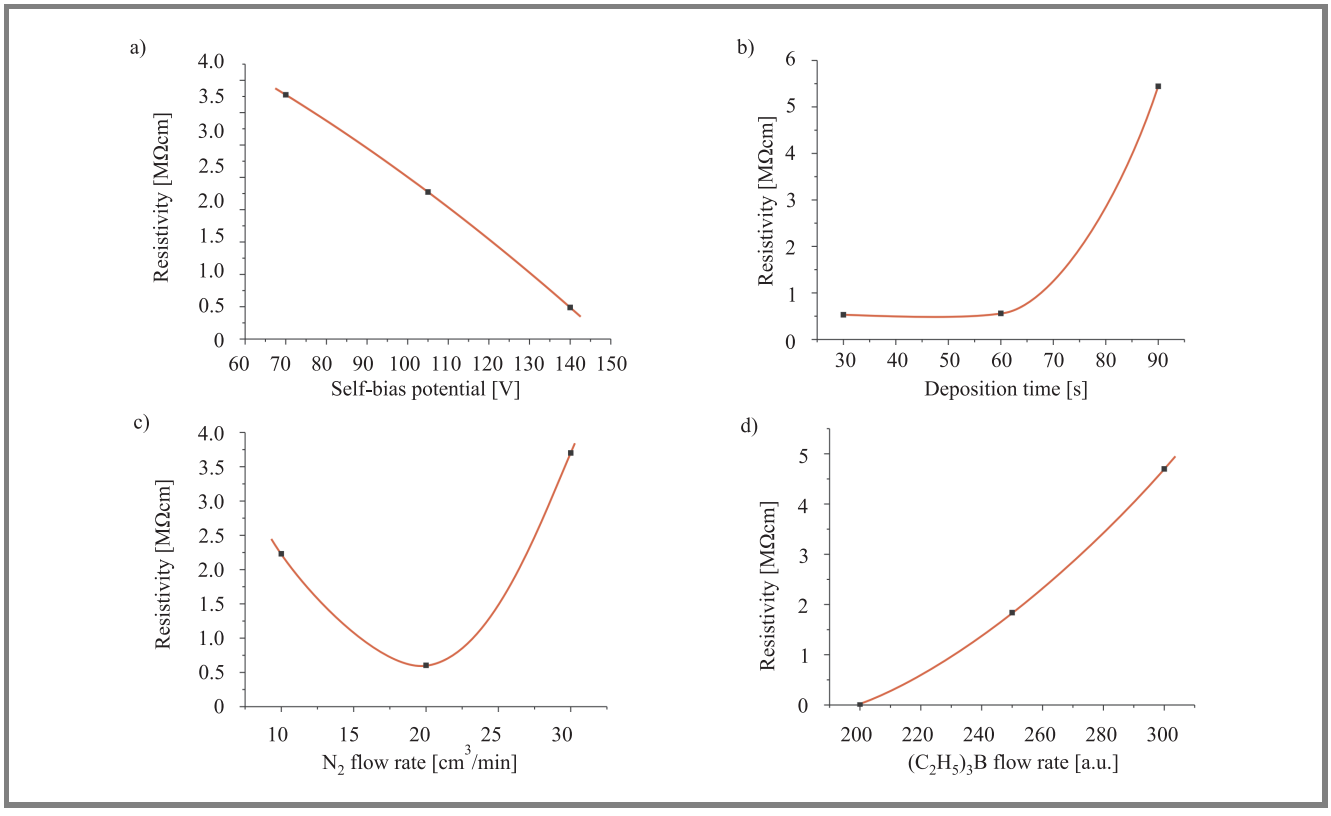

Fig. 2. Influence of the: (a) self-bias potential; (b) deposition time; c) N_2 flow rate; (d) $(C_2H_5)_3B$ flow rate on resistivity of BN layers.

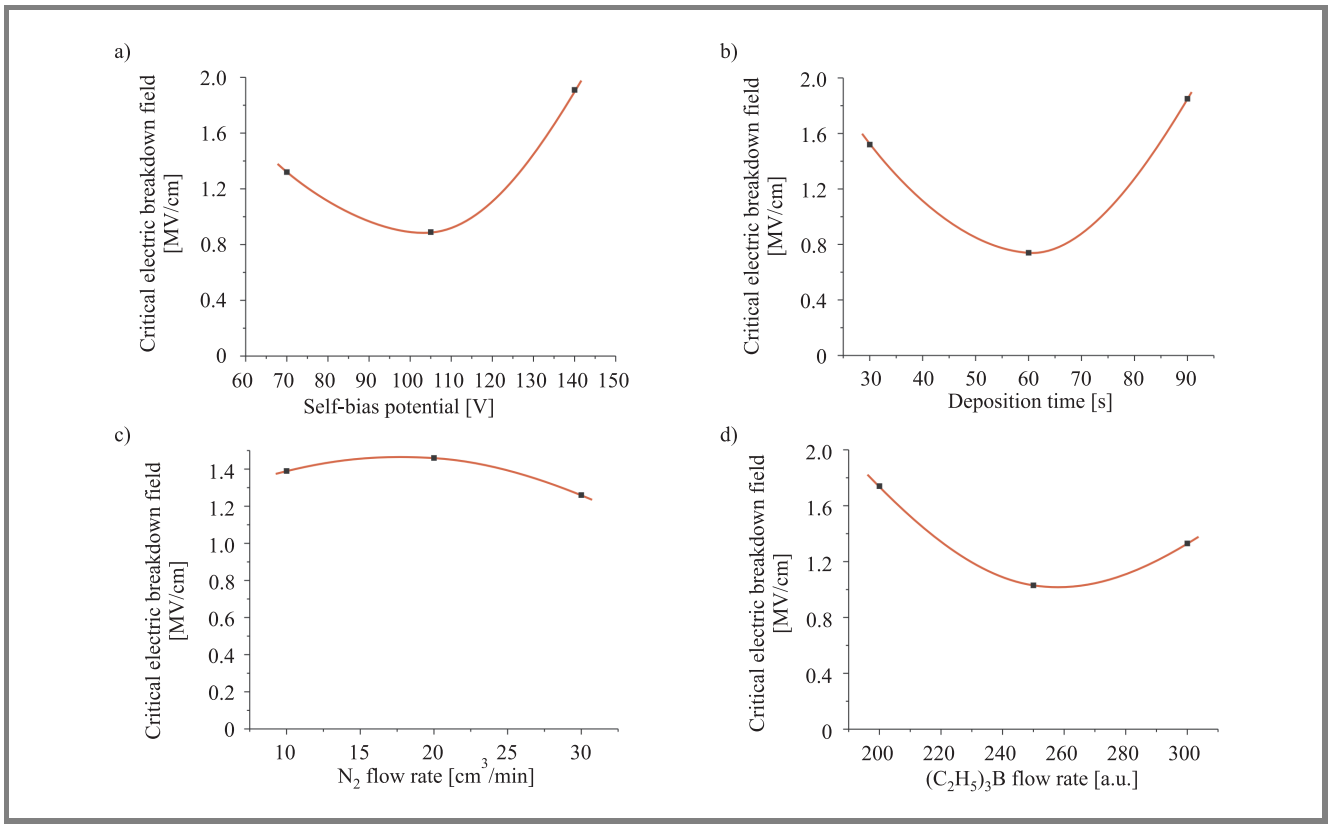

Fig. 3. Influence of the: (a) self-bias potential; (b) deposition time; c) N_2 flow rate; (d) $(C_2H_5)_3B$ flow rate on critical electric breakdown field of BN layers.

The obtained results show clearly that increasing deposition time results in thicker layers. The same is also observed when boron triethyl flow rate increases. On the other hand, the correlation between film thickness and self-bias potential, as well as nitrogen flow rate is more complicated. It suggests the presence of opposing phenomena during BN layer formation and needs further investigation.

Electrical characterization (current-voltage (*I-V*) measurements) of the fabricated MIS structures was performed to extract the resistivity ρ and critical electric breakdown field E_{BR} of BN layers. In order to determine the influence of the deposition process parameters on ρ and E_{BR} Taguchi's method was used again. The results are shown in Figs. 2 and 3.

As seen in Fig. 2, increasing self-bias potential (i.e., supplied power) leads to a decrease of the resistivity of BN layers. The opposite trend is observed in the case of boron triethyl flow rate growth.

As far as the dependence of deposition time on resistivity is concerned, the initial low value of this parameter might be attributed to the fact that for short growth times (therefore for thinner films) one has weaker control over the synthesis process, which usually results in inferior values of resistivity.

Obviously the nitrogen flow rate affects chemical composition of the layer and thus its parameters. At the same time nitrogen flow rate exerts influence on the pressure under which the coating is formed. The obtained results suggest however that higher resistivity is obtained when N_2 flow rate is increased to 30 cm^3/min.

In the case of the dielectric strength of BN films (Fig. 3) the character of its dependence on the deposition process parameters is more complicated as the obtained curves are not monotonic, showing minima or maxima instead. Nevertheless it can be seen that a certain set of process parameters (self-bias potential – 140 V, N_2 flow rate – 20 cm^3/min, boron triethyl flow rate – 300 arbitrary units) results in the highest value of critical electric breakdown field. On the other hand, Fig. 2 shows that ρ will not reach the required highest level with this combination of parameters. This indicates that it is necessary to find a trade-off between these parameters. Taking into account both resistivity and dielectric strength it appears that the best results are obtained with the following process parameters: self-bias potential – 70 V (substantial gain of with relatively small EBR loss), N_2 flow 30 cm^3/min (in spite of a slight drop of the dielectric strength, the resistivity increases almost twice). For the same reason using the maximum (300 arbitrary units) boron triethyl flow rate is the most advantageous.

4. Conclusions

The obtained results show that it is possible to achieve good electrophysical parameters of BN layers grown by means of RF PACVD. The method is relatively inexpensive and does not require substrate heating. Proper selection

of process parameters allows the quality of the fabricated films to be controlled, although further efforts (in particular involving the use of more advanced Taguchi procedures) towards process optimization are required.

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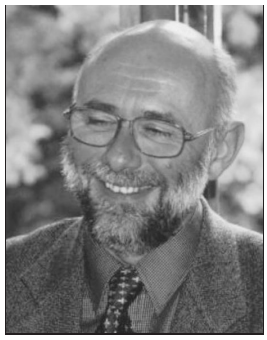

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Paper

Correlation between electric parameters of carbon layers and their capacity for field emission

Ryszard Gronau, Jan Szmidt, and Elżbieta Czerwosz

Abstract— The aim of this work is to study a possibility of field electron emission from carbon layers produced by radio frequency plasma chemical vapor deposition (RF PCVD) method. A correlation between electric parameters of the layers and the ability to produce electron emission is also studied through material (AFM) and electrical (*C-V*, *I-V*) characterization of the obtained layers. It is demonstrated that the layers deposited with the highest self-bias exhibit the highest capacity for electron emission.

Keywords— carbon layers, diamond-like carbon (DLC), field emission, RF PCVD, AFM, capacitance-voltage (C-V), current-voltage (I-V).

1. Introduction

The phenomenon of the electron cold emission has been extensively investigated recently. A number of applications based on this effect may be found in microelectronics, biology, chemistry and medicine. While technologies of emitter fabrication have been developed for production purposes, they are expensive and complicated. Therefore many laboratories are interested in new and competitive methods and materials suitable for field electron emitters. Carbon layers produced with radio frequency chemical vapor deposition (RF CVD) method seem to be very promising as a field emitting material.

2. Experimental details and results

The deposition processes were carried out on p-type silicon $< 100 >$ substrates ($5 - 7\ \Omega$cm resistivity). Carbon layers deposition process parameters are shown in Table 1.

Table 1
Parameters of carbon film deposition

Sample	Self-bias voltage [V]	Pressure [Pa]	Time [min]	Flow of gases CH_4/Ar [ml/min]
Z1	350	41.1	10	20/5
Z2	280	41.1	10	20/5
Z3	250	41.1	10	20/5

The electronic properties of carbon layers were calculated from the results of metal-insulator-semiconductor (MIS) capacitor high-frequency capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements. The carbon layers played the role of gate insulator in the investigated MIS structures.

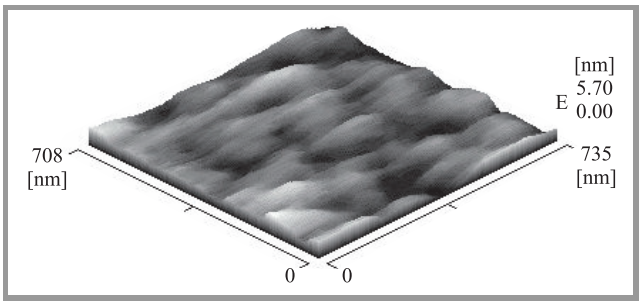

Fig. 1. AFM image of carbon layer surface after deposition, sample Z3.

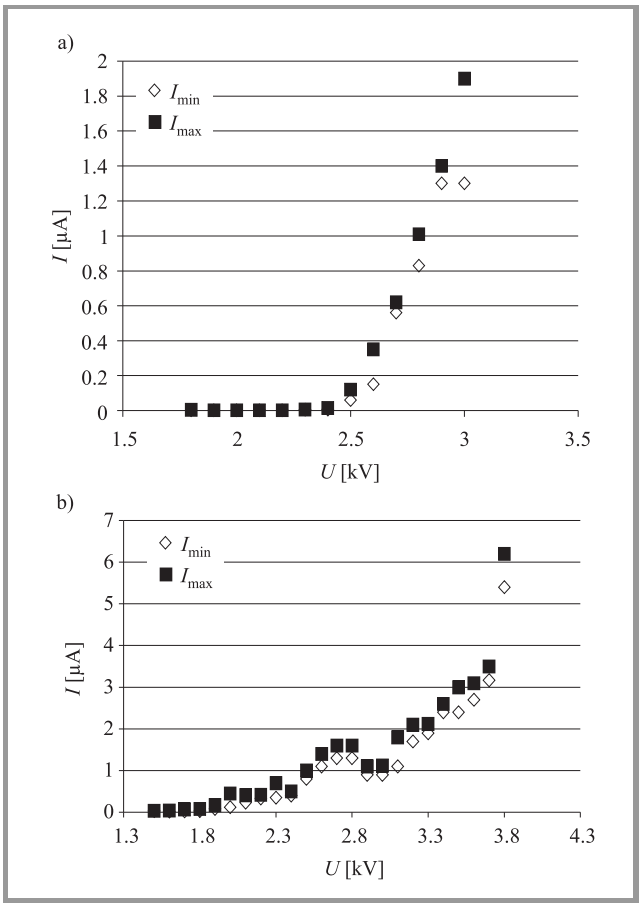

Fig. 2. Field emission current versus voltage: (a) Z2 sample; (b) Z3 sample.

The surfaces of carbon layers was investigated with atomic force microscope (AFM) (Fig. 1). The field emission was measured under the following conditions: voltage ranging from 0 to 4 kV, distance between electrodes in the range of $0-1$ mm and chamber pressure of 1 mPa. The results of emission current measurements are shown in Fig. 2.

3. Discussion and conclusions

Sample Z3 exhibits the highest capacity for field emission. Sample Z2 on the other hand has better electrical parameters and higher breakdown voltage than other samples. The results indicate that carbon layer of sample Z3 has higher content of graphite phase and less ordered carbon structure. The sample has higher capacity for field emission of electrons, but its breakdown voltage is low (Table 2).

Table 2

Electrical parameters of MIS Al/C/Si/Al capacitors

Parameters	Sample Z1	Sample Z2	Sample Z3
Thickness of carbon layer [Å]	2610	2380	2300
U_{FB} [V]	0.26	0.48	6.9
U_{MB} [V]	−4.6	−1.55	−2.13
Q_{eff} $[\mathrm{C}\cdot\mathrm{cm}^{-2}]$	$-4.600\cdot10^{-8}$	$-4.572\cdot10^{-8}$	$-1.312\cdot10^{-7}$
D_{it}	$6.71\cdot10^{12}$	$7.42\cdot10^{11}$	$1.63\cdot10^{12}$

The literature reveals the two major factors supporting field emission from carbon layers: irregularity of the surface and profusion of sp^2 phase in layer [1, 2]. The surface of deposited carbon layers is smooth (Fig. 1), therefore we believe that a better field emissivity from sample Z3 is caused by amorphous structure and profusion of sp^2 phase in the layer, rather than by irregularity of the surface or nanocrystalline diamond (NCD) forms. While the electrical quality of the layers is poor, our experiment has shown that they could be applicable in micro and nanoelectronics structures and devices.

Acknowledgements

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Jan Szmidt – for biography, see this issue, p. 36.

Paper

Investigations of electron emission from DLC thin films deposited by means of RF PCVD at various self-bias voltages

Dagmara Jarzyńska, Zbigniew Znamirowski, Marian Cłapa, and Elżbieta Staryga

Abstract— The aim of this paper is to report the results of field emission experiments on undoped, flat diamond-like carbon (DLC) thin films deposited at various self-bias voltages using radio frequency plasma chemical vapor deposition (RF PCVD) technique. It has been observed that the emission properties improve when the absolute value of self-bias voltage becomes higher, e.g., the turn-on field value decreases. The correlation between electron field emission and sp^2 content in these films showed improvement of electron emission properties of DLC films for higher amount of sp^2 phase.

Keywords— DLC, RF PCVD, Raman spectroscopy, turn-on field, electron emission, effective work function.

1. Introduction

Carbon-based materials grown by chemical vapor deposition (CVD) technique, which contain both diamond and non-diamond components, have been shown to have excellent field emission properties. It is supposed that the significant electron emission from diamond-like carbon (DLC) films may be caused by low positive or even negative electron affinity (NEA) [1–4]. Diamond-like carbon films are also known to have a high ratio of tetrahedral C-C sp^3 bonds to trigonal C-C sp^2 bonds. As a result, they have extreme physical hardness, high resistance and good adhesion to various substrates. The DLC coatings are also chemically inert. These properties make DLC a useful material for a wide variety of applications, especially as the material for field emitters.

In this paper, we present the results of investigation of electron emission properties of flat diamond-like carbon films synthesized by radio frequency plasma chemical vapor deposition (RF PCVD) method at various self-bias voltages. We estimated the influence of the structure of carbon films on the field emission. We also considered the role of the sp^2 bonds in electron emission effect.

In order to understand the role of the graphite content in diamond-like carbon films, the Raman spectroscopy (RS) was used. The scanning electron microscopy (SEM) was used to examine the surface microstructure of investigated carbon layers.

2. Experimental

Diamond-like carbon films were manufactured by RF PCVD, 13.56 MHz, process using methane as a carbon precursor. The coating deposition took place with the applied negative self-bias voltage of cathode from -60 V to -300 V. The gas pressure in the reactor chamber was about 26 Pa. As the substrate for DLC coatings, n-type flat silicon wafers ($< 0.002\,\Omega$cm) were used. The thickness of DLC films was less than 100 nm.

Figure 1 shows the image of typical surface morphology of examined carbon films. The amorphous DLC films had smooth, uniform surfaces which did not show any microcrystalline features. Both the SEM micrographs and Raman spectra proved that the investigated films were typical diamond-like layers of good quality having no detectable mechanical imperfections.

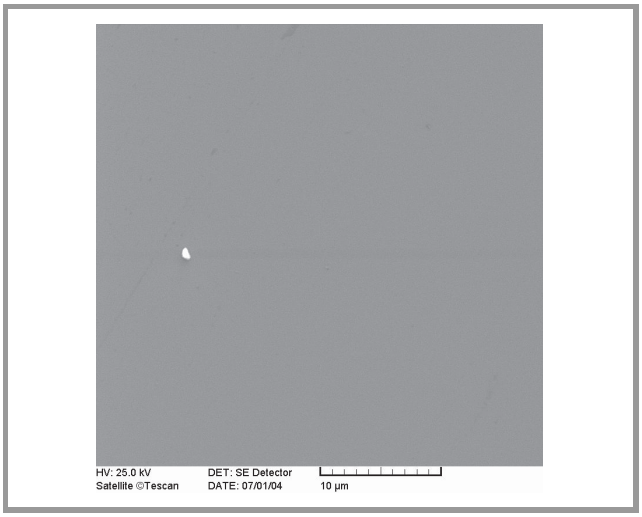

Fig. 1. The SEM micrograph of the smooth surface of a DLC film deposited on a flat silicon substrate by means of RF PCVD.

The structure of DLC films was evaluated using Raman spectroscopy. The Raman spectra were recorded at room temperature in back scattering geometry using Jobin-Yvon T64000 Raman micro-spectrometer. The instrument was equipped with a microscope whose focal spot diameter was $\sim 1.5\,\mu$m and 514.5 nm line from Argon laser

was used for excitation. The spectral resolution was set below 2 cm^{-1}.
Scanning electron microscopy (SEM, Hitachi S 3000 N) examination was carried out before and after emission current measurements to bring out the state of surface morphology.
The emissive characteristics of the samples were measured in oil-free vacuum of the order of 10^{-5} Pa using diode configuration. The stainless-steel ball anode with the diameter of 5 mm was placed at a distance of $\sim 15\,\mu$m from the cathode surface. The voltage in the range from 50 V to 2500 V was applied between the electrodes during the emission measurements. The electron field emission properties were analyzed using the Fowler-Nordheim (F-N) theory [5].

3. Results and discussion

The electron emission characteristics were taken for DLC films deposited on flat n-type Si substrates. The dependence of the emission current (I) on the applied electrical field (E) for the DLC films deposited at voltages -60 V, -120 V and -300 V is shown in Fig. 2.

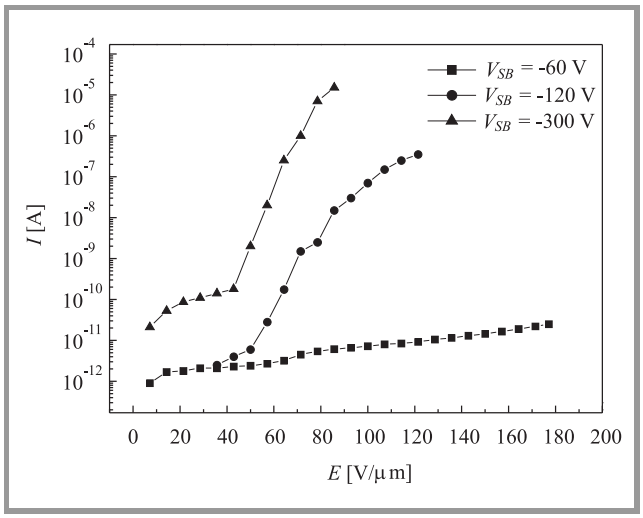

Fig. 2. Emission current I versus electric field E for DLC films deposited onto flat n-type Si substrates at various negative self-bias voltages (V_{SB}).

It can be seen that $DLC_{-60\,V}$ characteristics differ significantly from those of DLC films deposited at higher self-bias voltages. In the range about $50\,V/\mu m - 180\,V/\mu m$ the emission current for $DLC_{-60\,V}$ was very low in comparison with $DLC_{-120\,V}$ and $DLC_{-300\,V}$, for which the values of emission currents were several orders of magnitude higher. These results indicate that DLC films deposited at high self-bias voltages should have better field emission properties. The recorded *I-E* data of DLC specimens were used to generate F-N plots shown in Fig. 3.
The results of electron emission were analyzed using the F-N model. If the electron emission is controlled by the tunneling mechanism, the F-N plot: $\ln(I/E^2)$ versus $1/E$ presents almost straight line with negative slope giving reliable test of emission mechanism. Field emission properties were characterized by the parameters such as turn-on field and effective work function. The turn-on field indicates the beginning of the cold electron emission current, i.e., the state when the emission, with increasing electric field, begins to overwhelm the thermionic emission current and leakage currents. The turn-on field was defined by the intersection of two straight lines extrapolated from the low-voltage (thermionic and leakage currents) segment, and high-voltage (cold emission current) segment of the F-N plots (Fig. 3) [6].

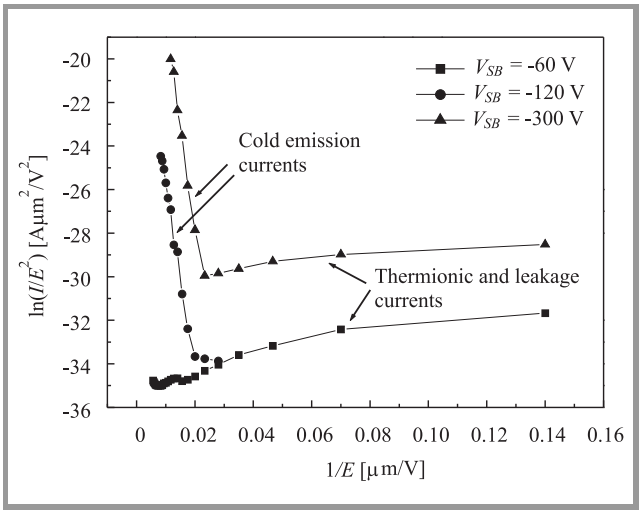

Fig. 3. The *I-E* data in the F-N system.

The effective work function φ_{ef} can be deduced from the F-N plots in cold emission region (Fig. 4) where its slope is in proportion to the ratio of the work function φ and field enhancement factor $\beta^{2/3}(\varphi_{ef} = \varphi/\beta^{2/3})$.

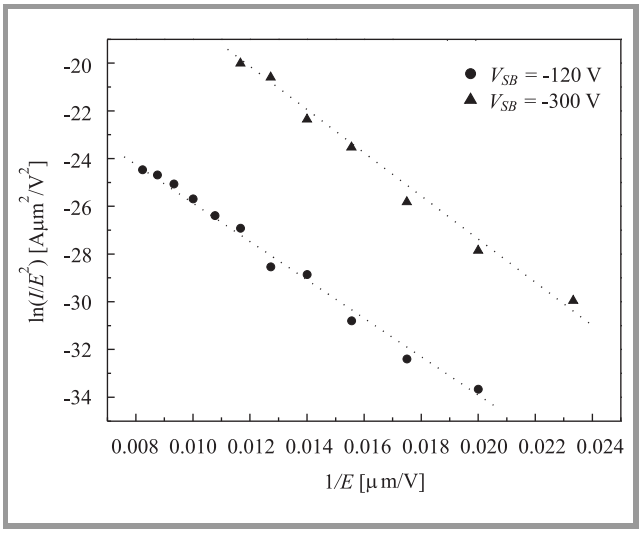

Fig. 4. The F-N plot of cold electron emission current for DLC films deposited with $V_{SB} = -120$ V and $V_{SB} = -300$ V.

We assume that for such flat and smooth surfaces as investigated DLC films the field enhancement factor β is equal

to one. As it is seen in Fig. 3, the $DLC_{-60\,V}$ film does not show any field emission of electrons in the testing range of electric field. Table 1 collects the emissive parameters for the investigated samples. As we can see in Table 1 the values of emissive parameters for $DLC_{-120\,V}$ and $DLC_{-300\,V}$ coatings do not vary significantly.

Table 1

The turn-on field and the effective work function for the investigated films

Sample	Type of silicon substrate	Negative self-bias voltage V_{SB} [V]	Turn-on field E_{t-on} [V/μm]	Effective work function [eV]
$DLC_{-60\,V}$	n-type, flat substrate	−60	–	–
$DLC_{-120\,V}$		−120	50	0.246
$DLC_{-300\,V}$		−300	42	0.257

The values of the effective work function seem to be too low if we take into account the gap width of DLC films (between 1 eV and 3 eV usually). This may be due to the assumption $\beta = 1$, which may be unjustified for DLC films with non-homogeneous conduction. The emission turn-on field for the sample $DLC_{-300\,V}$ is slightly lowers than the value E_{t-on} for the sample $DLC_{-120\,V}$. Although the turn-on field values for those samples were close, the electron emission from $DLC_{-300\,V}$ sample was more efficient process, as it is shown in Fig. 2. The emission current ($6 \cdot 10^{-12}$ A) for $DLC_{-120\,V}$ film was three orders of magnitude smaller in comparison with $DLC_{-300\,V}$ sample one ($2 \cdot 10^{-9}$ A) for the same electric field 50 V/μm.

The mechanism of electron emission from DLC films is still not clear, but the obtained results may indicate that at higher self-bias voltages the increasing amount of sp^2 phase improves the electron emission properties.

As Cui *et al.* [7] reported the graphite phase is a necessary requirement for electron emission, because it provides the emission sites. One should remember that results of many previous investigations showed that the electrical conductivity of DLC films is much higher than the conductivity of polycrystalline diamond films [8, 9]. It may be suggested that cold field emission from various carbon structures can be enhanced by a system of better conducting micro-channels related to sp^2 phase [10]. The structural investigations of DLC samples prove that the amount of sp^2 phase increases with increasing value of the self-bias voltage [8], which confirms the influence of sp^2 phase on field emission properties of DLC films.

In order to identify diamond and graphite phases in the investigated carbon layers, Raman spectroscopy was used. The Raman spectra of diamond-like carbon films deposited at various bias voltages are shown in Fig. 5. An asymmetric Raman spectrum composed of the graphitic band (*G*) at about 1550 cm^{-1} and the disorder band (*D*) between 1200 cm^{-1} and 1360 cm^{-1} was obtained for each investigated DLC film. Those spectra are typical for this kind of material and confirm the amorphous structure of these layers.

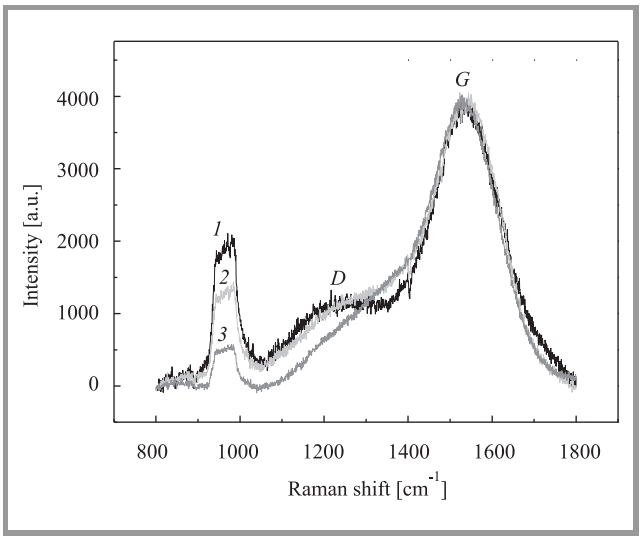

Fig. 5. Typical Raman spectra of DLC films obtained at $V_{SB} = -60$ V (curve *1*), $V_{SB} = -120$ V (curve *2*) and at $V_{SB} = -300$ V (curve *3*).

The Raman results indicated that the structure of DLC film deposited in high self-bias voltage (e.g., −300 V) differ slightly from the structure of the layer obtained at lower negative bias voltage (e.g., −60 V). The Raman spectra for those layers allowed us to assume that the disordered state (band *D*) was reduced with an increase of the absolute value of negative self-bias voltage during DLC films deposition. The decrease of the band *D* might indicate that the density of the sp^2 bonded carbon phase increases in the films.

The investigated carbon films are amorphous with the coexistence of graphite-like and diamond-like phase, the amount of which depends on the conditions of the RF PCVD process.

4. Conclusion

This work reports the results of a series of field emission experiments on amorphous DLC films deposited using RF PCVD. The investigations indicate that diamond-like carbon coatings on the silicon substrates show the ability to emit electrons from their surface. The deposition conditions of RF PCVD are of significant importance for the electron emission. The emission current-voltage characteristics show a good fit to the Fowler-Nordheim theory. The values of emission turn-on fields are between 40 V/μm and 50 V/μm for DLC films deposited at high negative self-bias voltages. There was no possibility to determine the turn-on field and the effective work function for the $DLC_{-60\,V}$ sample due to the domination of thermionic and leakage currents in the investigated range of the electric field. Samples $DLC_{-120\,V}$ and $DLC_{-300\,V}$ showed relatively low

values of effective work function and were characterized by good emissive properties. The effect of sp^2 content on the *I-E* and F-N plots of DLC films was discussed. The electron emission was probably associated with the coexistence of graphite-like and diamond-like phases in DLC amorphous films. The results indicate that carbon-based films with good emissive properties can be obtained by suitable choice of the parameters of the RF PCVD process.

Acknowledgments

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Paper

Ellipsometric spectroscopy studies of compaction and decompaction of Si-SiO_2 systems

Witold Rzodkiewicz and Andrzej Panas

Abstract— The influence of the strain on the optical properties of Si-SiO_2 system has been investigated by spectroscopic ellipsometry (SE), interferometry and weighing methods. Subtle changes of densification (compaction degree) in silicon dioxide layers on silicon substrates have been determined by weight technique (relying on measurements of the silicon dioxide layer mass and calculations of the volume). Elastic stress in the oxide layers has been measured by Fizeau fringes image analysis method. A comparison is made between the density of the silicon dioxide (ρ) and the results of calculations made using $\rho = f(n)$ relations (where n is the refractive index) given in the literature.

Keywords— Si-SiO_2 system, density, refractive index, spectroscopic ellipsometry.

1. Introduction

Oxidation of silicon has attracted much attention in the last decades. Due to the continuous miniaturization of integrated circuits and increased functionality in the modern microelectronics technology, better understanding of the mechanisms of elastic (instantaneous and reversible compaction) and non-elastic (irreversible and permanent densification) strain generation in the Si-SiO_2 system is necessary. Furthermore, when the structure size is reduced, their mechanical and optical properties may differ from the corresponding values of the bulk medium. Therefore, studies of both mechanical and optical properties of Si-SiO_2 system are of great importance.
Several methods, such as spectroscopic ellipsometry (SE), interferometry and weight technique (WT) have been used to determine these properties. In connection with this, the main goal of our work was to study the influence of strain on the optical properties of Si-SiO_2 system using the techniques mentioned above.

2. Experimental characteristics

Czochralski-grown, n-type (100) silicon substrates have been used in this study. We started with 4-inch wafers polished on both sides. Subsequently, the wafers were subjected to thermal oxidation process at 1000°C in either dry oxygen (in order to grow silicon dioxide layers with the thickness of approximately 45, 95, and 170 nm) or water vapor (in order to grow oxide layers with the thickness of approximately 50, 90, and 165 nm).

The thickness of SiO_2 layers formed in the way described above and their refractive indexes were determined using a variable angle spectroscopic ellipsometer (VASE) of J. A. Woollam Inc. Co.
Ellipsometric measurements were carried out at 5 points for each wafer in a wide spectral range (250–1000 nm) at three angles of incidence (65°; 70°; 75°). Interferometry was used to determine the radius of curvature of the investigated wafers.

2.1. Experiment methodology

The sequence of processing and measurement steps performed during our investigations was as follows:

1. Oxidation of 4-inch, n-type Si (100) wafers polished on both sides.
2. Interferometric measurements of oxidized wafers.
3. Ellipsometric measurements of oxidized wafers (to determine the thickness and refractive index of oxide).
4. Measurements of the mass of oxidized wafers.
5. The removal of both front-side SiO_2 layer and back-side SiO_2 layer of each wafer by etching in HF solution.
6. Measurements of the mass of as-etched wafers.
7. Interferometric measurements of as-etched wafers.
8. Calculations of the oxide mass as the difference between the wafer mass obtained before and after removal of both front-side and back-side oxide.
9. Calculations of oxide density as the ratio of the determined oxide mass to its calculated volume (product of oxide thickness and the surface area).

2.2. Optical model for ellipsometric data analysis

The optical model which used for spectro-ellipsometric data analysis consisted of a silicon dioxide layer and a silicon substrate. The Cauchy dispersive model enabled the silicon dioxide refractive index and its thickness to be determined. Determination of the SiO_2 index of refraction

is based on the he relationship represented by the Cauchy dispersion formula:

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} + \ldots, \tag{1}$$

where A, B, C are fitting coefficients, and λ stands for wavelength, expressed in μm. In the applied model, the three parameters of Eq. (1) and SiO_2 layer thickness were fitted.

3. Results and discussion

Dependence of silicon dioxide density, ρ_{ox} on the oxide refractive index n is illustrated in Fig. 1. This figure clearly shows that the refractive index is a measure of the densification degree of SiO_2 layers on silicon substrates. The measurement and calculation results for wafers with silicon dioxide thickness $t_{ox} \approx 50$ nm, 90 nm, 170 nm are presented in Tables 1–4.

Once the mass M_{SiO_2} of an SiO_2 layer is measured and its volume V_{SiO_2} is known (calculated as the product of the oxide thickness and surface area of the layer), one may determine directly the density of the layer:

$$\rho_{SiO_2} = \frac{M_{SiO_2}}{V_{SiO_2}}. \tag{2}$$

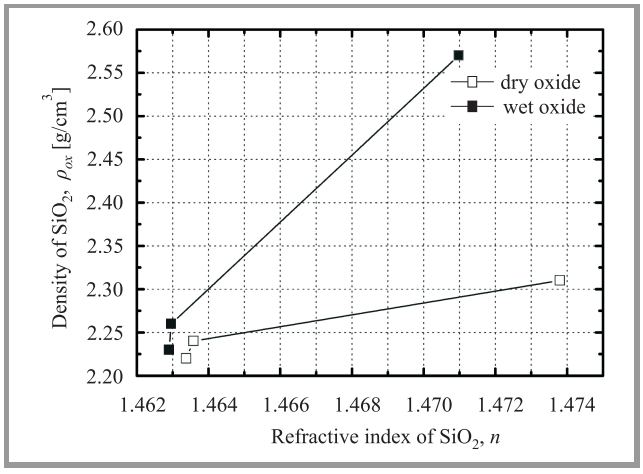

Fig. 1. Dependence of silicon dioxide density, ρ_{SiO_2} (experimentally determined by weight technique) on the oxide refractive index, n (determined by spectroscopic ellipsometry).

Table 1
The mass, density and averaged thickness values determined for silicon wafers oxidized in water vapor atmosphere

No. of wafer	t_{ox} [nm]	M_{ox} [mg]	ρ_{ox} [g/cm^3]
1	50.07	1.00	2.57
2	90.17	1.58	2.26
3	165.12	2.86	2.23

Table 2
The mass, density and averaged thickness values determined for silicon wafers oxidized in dry atmosphere

No. of wafer	t_{ox} [nm]	M_{ox} [mg]	ρ_{ox} [g/cm^3]
4	45.16	0.81	2.31
5	93.96	1.64	2.24
6	172.02	2.97	2.22

Table 3
Comparative collection of theoretical and experimental density values determined for the corresponding averaged refractive indexes (determined by SE at $\lambda = 630$ nm) of the wet oxides (oxides grown in water vapor)

No. of wafer	n_{630}	$\rho_{L\text{-}L}$	$\rho_{G\text{-}D}$	ρ_{Ta}	ρ_{Eyk}	ρ_{Drude}	ρ_{wt}
		[g/cm^3]					
1	1.4710	2.25	2.25	2.29	2.25	2.26	2.57
2	1.4630	2.21	2.22	2.23	2.21	2.22	2.26
3	1.4629	2.21	2.22	2.23	2.21	2.22	2.23

Table 4
Comparative collection of theoretical and experimental density values determined for the corresponding averaged refractive indexes (determined by SE at $\lambda = 630$ nm) of the dry oxides (oxides grown in dry oxygen)

No. of wafer	n_{630}	$\rho_{L\text{-}L}$	$\rho_{G\text{-}D}$	ρ_{Ta}	ρ_{Eyk}	ρ_{Drude}	ρ_{wt}
		[g/cm^3]					
4	1.4738	2.26	2.27	2.31	2.26	2.28	2.31
5	1.4636	2.21	2.22	2.23	2.22	2.22	2.24
6	1.4634	2.21	2.22	2.23	2.22	2.22	2.22

Next, the density of SiO_2 layers obtained in this way were compared with that determined from the value of the refractive index (established in the course of ellipsometric measurements). The Lorentz-Lorenz equation [1, 2] (L-L) is one of the most widely used formulae relating oxide density to its refractive index:

$$\Pi = \frac{1}{3} N_A \alpha = \frac{(n^2-1)}{(n^2+2)} \frac{M}{\rho}, \tag{3}$$

where: Π – molar polarization, N_A – Avogadro's number, α – mean polarizibility, M – molecular mass, ρ – density.

Substituting the following values: $M = 60.08$ g/mol (molecular mass of SiO_2), $\rho = 2.2$ g/cm^3 and $n = 1.46$ (density and refractive index of the relaxed SiO_2, respectively), we obtain molar polarization for SiO_2 layer $\Pi = 7.4797$ cm^3/mol and Eq. (1) becomes:

$$\rho = 8.0324 \frac{n^2-1}{n^2+2}. \tag{4}$$

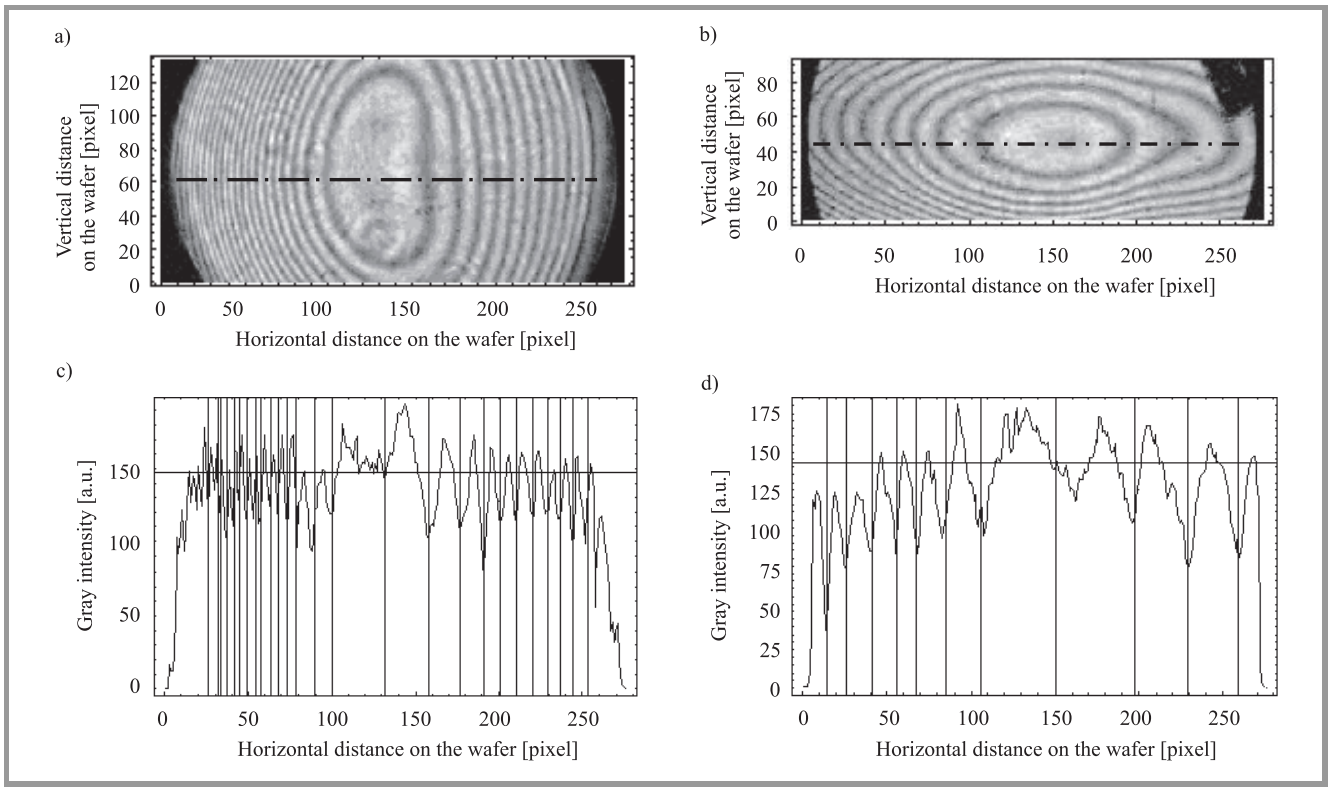

Fig. 2. Interferograms and theirs sections along horizontal axis and the center of Fizeau fringes for front-side (a), (c) and back-side (b), (d), of wafer no. 5 after dry oxidation.

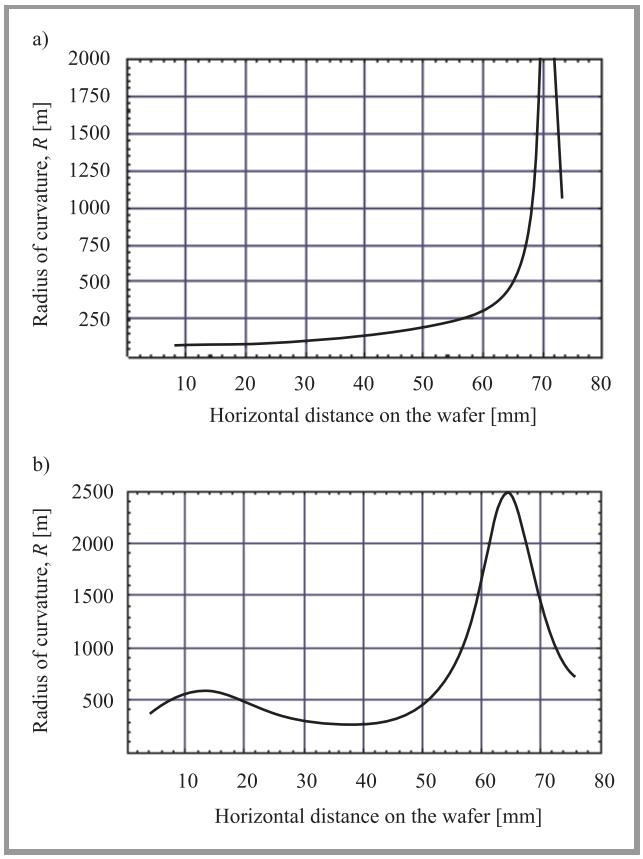

Fig. 3. Radius of curvature versus distance for front-side (a) and back-side (b) of wafer no. 5 after dry oxidation.

Other models of the relationship between oxide density and its refractive index include: Gladstone-Dale formula [2, 3] (G-D):

$$\rho = 4.785\,n - 4.784\,, \tag{5}$$

the empirical $\rho(n)$ relationship for SiO_2 layer derived by Taniguchi [4] (Ta):

$$\rho = 7.81\,(n-1)^{1.63}, \tag{6}$$

Eykman equation [5] (Eyk):

$$\rho = C\,\frac{n^2-1}{n^2+0.4}\,, \tag{7}$$

where $C = 3.6161$ (at room temperature) – empirical constant dependent on temperature; and Drude equation [2]:

$$\rho = 1.944\,(n^2-1)\,. \tag{8}$$

The last two equations have usually been used to study the optical properties of various liquids (such as chlorobenzene, methanol, water, etc.).

A comparison between values of SiO_2 density obtained both experimentally and theoretically is shown in Tables 3 and 4. It should be noticed that the results obtained for dry oxides by means of WT and calculated using Eq. (5) are in a good agreement (see Table 4).

The results of interferometric measurements are illustrated in Figs. 2–5. Interferograms and theirs sections along horizontal axis and the center of Fizeau fringes for front-side

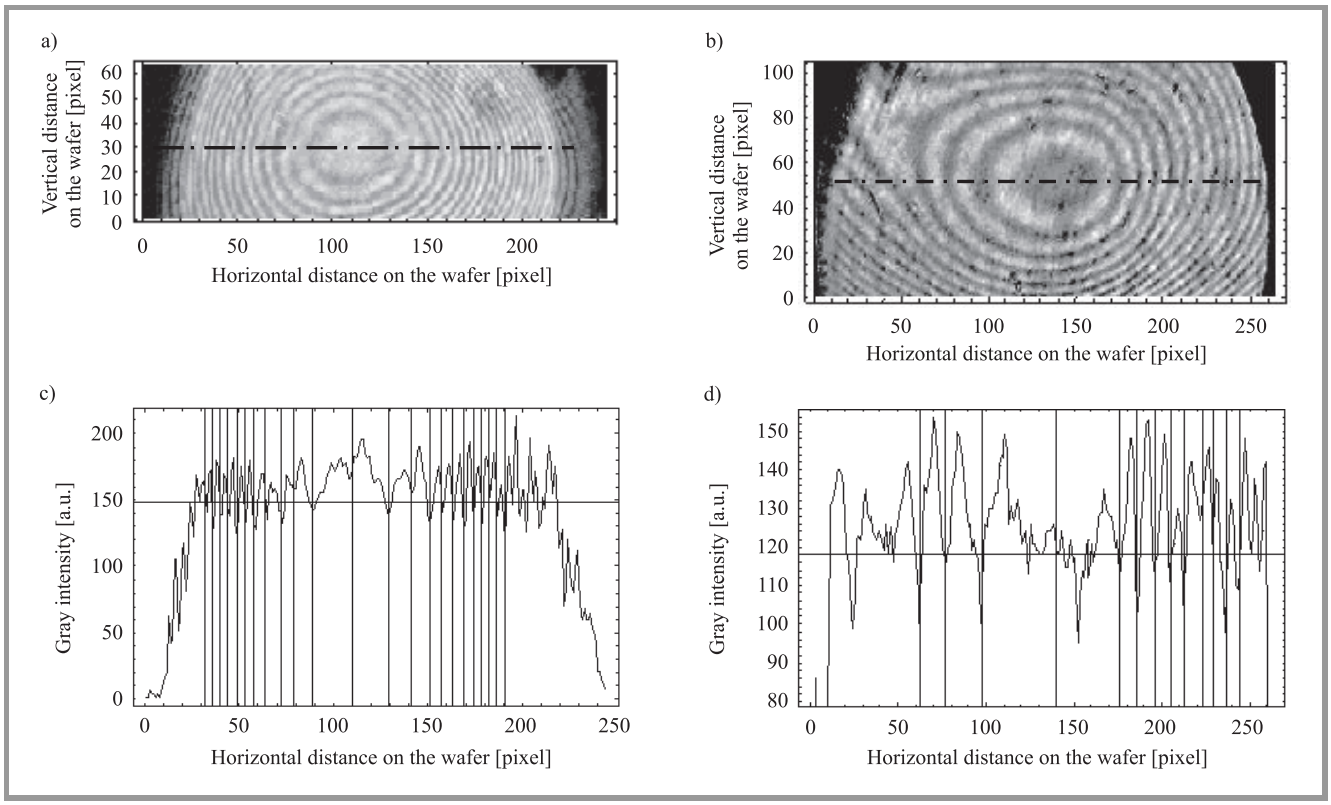

Fig. 4. Interferograms and theirs sections along horizontal axis and the center of Fizeau fringes for front-side (a), (c) and back-side (b), (d), of wafer no. 5 after removal of dry oxide.

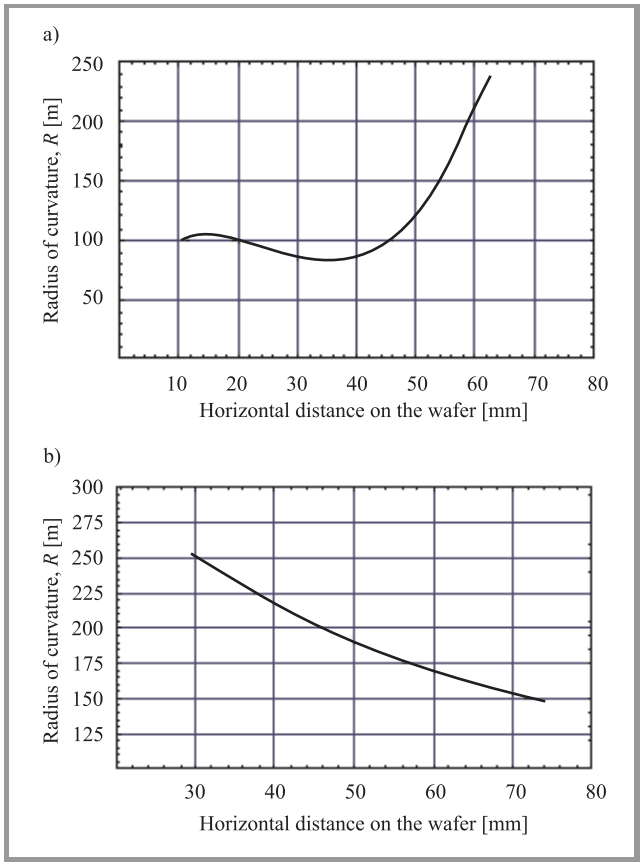

Fig. 5. Radius of curvature versus distance for front-side (a) and back-side (b) of wafer no. 5 after removal of dry oxide.

and back-side of wafer no. 5 after dry oxidation (thickness of ~ 90 nm) are shown in Fig. 2. Similar data obtained after removal of thick dry oxide is presented in Fig. 4.

Using the results shown in Figs. 2 and 4, the approximation function of curve of the sections, as well as the corresponding formula for reciprocal curvature Eq. (9), we have determined the radius of curvature R versus distance for front-side and back-side of the oxidized wafer (dry SiO_2 thickness of ~ 90 nm) (see Fig. 3):

$$R = \frac{1}{\kappa} = \frac{\left[1 + \left(\frac{dy}{dx}\right)^2\right]^{\frac{3}{2}}}{\frac{d^2y}{dx^2}}, \tag{9}$$

where κ is the curvature.

Similar results are shown in Fig. 5 for front-side and back-side of the wafer after dry oxide removal.

Comparison of the results obtained from wafer no. 5 after oxidation and after etching indicates that the curvature of an oxidized wafer is considerably smaller than that of an etched wafer (Figs. 3 and 5).

4. Conclusions

In this work, we have investigated the influence of strain on the optical properties of Si-SiO_2 system by spectroscopic ellipsometry and interferometry.

On the basis of the obtained results, we have drawn the following conclusions:

– refractive index of wet oxide is lower than that of dry oxide (Tables 3 and 4);

– for refractive index higher than 1.47, the divergence between the density calculated from the Taniguchi formula and that calculated from Lorentz-Lorenz, Gladstone-Dale, Eykman, and Drude equations becomes significant (Tables 3 and 4);

– measurement of oxide mass and calculated volume of the oxide layer enabled the densification degree of the oxide layers on silicon substrates to be properly determined for about 83% of the investigated wafers (with numbers: 2–6);

– the local radii of curvature of oxidized wafer no. 5 are considerably higher than those of the etched wafers (Figs. 3 and 5);

– interferometry and spectroscopic ellipsometry have turned out to be helpful and suitable methods in our studies.

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Paper

Investigation of barrier height distributions over the gate area of Al-SiO_2-Si structures

Krzysztof Piskorski and Henryk M. Przewłocki

Abstract—Distributions of the gate-dielectric $E_{BG}(x, y)$ and semiconductor-dielectric $E_{BS}(x, y)$ barrier height values have been determined using the photoelectric measurement method. Modified Powell-Berglund method was used to measure barrier height values. Modification of this method consisted in using a focused UV light beam of a small diameter $d = 0.3$ mm. It was found that the $E_{BG}(x, y)$ distribution has a characteristic dome-like shape which corresponds with the independently determined shape of the effective contact potential difference $\phi_{MS}(x, y)$ distribution. On the other hand, the $E_{BS}(x, y)$ distribution is of a random character. It is shown that the $E_{BG}(x, y)$ distribution determines the shape of the $\phi_{MS}(x, y)$ distribution. The model of the E_{BG} and E_{BS} barrier height distributions over the gate area has been proposed.

Keywords— barrier height, effective contact potential difference, MOS system.

1. Introduction

The present work is a logical continuation of our previous research (see, e.g., [1–4]) concerning the distribution of electrical parameters over the gate area of Al-SiO_2-Si structures. It has been experimentally proved that the effective contact potential difference (ECPD or ϕ_{MS}) and zero photocurrent gate voltage V_G^0 have a characteristic dome-like shape distribution over the gate area. An example of such a distribution is shown in Fig. 1. The distribution of V_G^0 obtained experimentally (see, e.g., [3, 4]) in two different directions (along the diagonal and through the center of the square gate) shows the highest values at the center of the gate and lowest values at the gate corners.

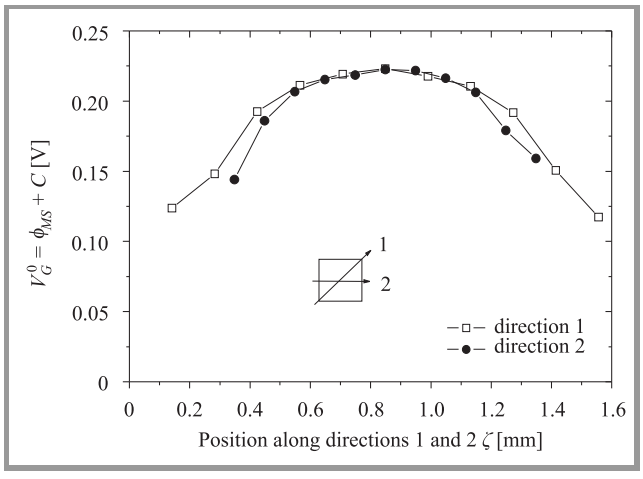

Fig. 1. Typical dependence of the V_G^0 voltage measured at the wavelength $\lambda = 244$ nm on the position in Al-SiO_2-Si(n^+) structures with aluminum gate thickness $t_{Al} = 35$ nm and SiO_2 layer thickness $t_{ox} = 60$ nm. The direction is either Eq. (1) along the diagonal of the square gate, or Eq. (2) through the center of the square gate and parallel to its edges.

We ascribe the characteristic shape of this distribution to the distribution of mechanical stress which is present in the oxide layer under the gate in the MOS system [5–8]. This non-uniform distribution of the mechanical stress is shown in Fig. 2.

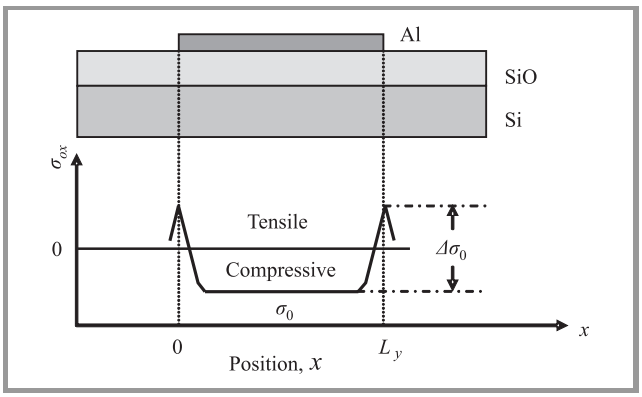

Fig. 2. A qualitative one-dimensional distribution of stress $\sigma_{ox}(x)$ in the oxide layer under the Al gate.

Assuming that changes in V_G^0 and ϕ_{MS} values are proportional to changes in mechanical stress σ under the gate, a model of $\phi_{MS}(x, y)$ distribution was developed and confirmed experimentally [3]. A typical distribution of ϕ_{MS} local values over the square gate area, calculated using this model is shown in Fig. 3. It is clearly seen in Fig. 3 that the $\phi_{MS}(x, y)$ distribution has a dome-like shape, with the highest values at the center of the gate, lower at the gate edges and still lower at gate corners.

The ECPD depends directly on the difference $E_{BG} - E_{BS}$ of barrier heights at both sides of the dielectric, as discussed in the next section. Hence, one or both of these barriers must have distributions which result in the characteristic $\phi_{MS}(x, y)$ distribution. Since it is the gate that causes the non-uniform distribution of mechanical stress in the oxide, it is more likely that the gate-dielectric E_{BG} barrier height has the decisive influence on the shape of $\phi_{MS}(x, y)$ distribution.

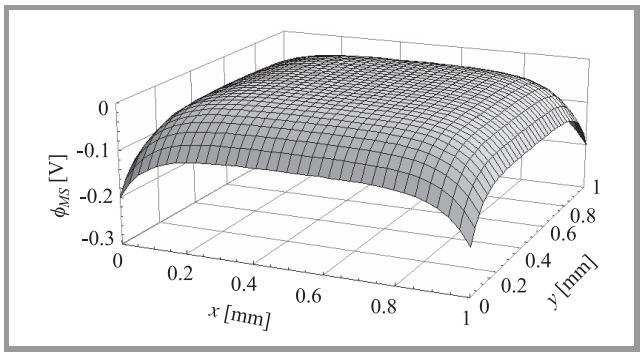

Fig. 3. Example of two-dimensional distribution of $\phi_{MS}(x, y)$ calculated using model [3, 4] for MOS structures with square gates of side length $L = 1$ mm.

The aim of this investigation was to determine the distributions of both E_{BG} and E_{BS} barrier height local values over the gate area and to find out how the individual barrier heights influence the ϕ_{MS} distribution. Moreover, barrier height measurement results have been compared in this work with independently determined ϕ_{MS} local values, to estimate the accuracy of barrier height determination. A model (similar to the above mentioned ϕ_{MS} distribution model) has also been applied in this work to the $E_{BG}(x, y)$ and $E_{BS}(x, y)$ distributions over the gate area.

2. Theory

The barrier height measurements were performed using internal photoemission phenomena, which can be observed in a MOS structure with a semitransparent gate under illumination by UV light. The UV radiation absorbed in both electrodes (gate or substrate) may cause excitation of some electrons. When the energy of the excited electrons is sufficient to surmount the potential barrier at the gate-dielectric or semiconductor-dielectric interface the photocurrent flow takes place. This photocurrent is a function of the barrier height E_B, the wavelength λ of UV light illuminating the structure and the gate potential V_G and can be measured

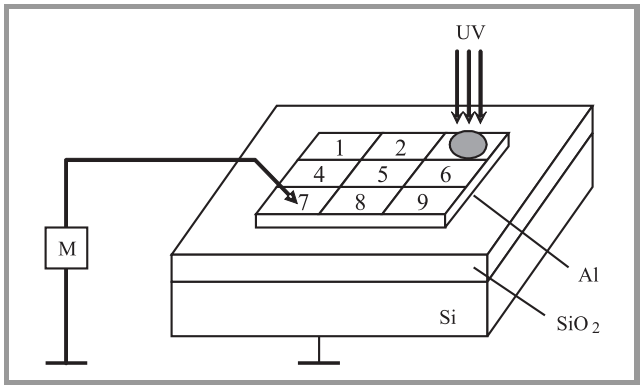

Fig. 4. The measurement system: the MOS structure with semitransparent Al gate is illuminated at 9 different locations over the gate area by a focused light beam. The photocurrent is measured in the external circuit M.

in the external circuit, as shown in Fig. 4. In this figure the measurement system with MOS structure illuminated by UV light beam is schematically illustrated. The beam may be focused in nine different positions over the gate area. In Fig. 5 the band diagram of the MOS system is shown.

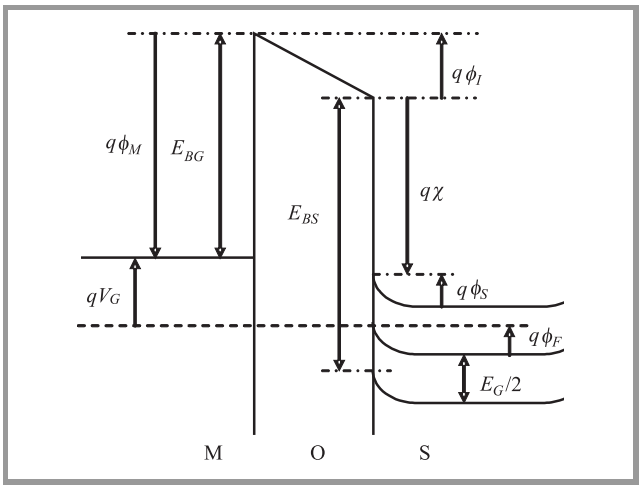

Fig. 5. Band diagram of the MOS system. E_{BG}, E_{BS} are potential barrier heights at gate-dielectric and semiconductor-dielectric interfaces, respectively.

Adding up all potentials on both sides of the dielectric layer leads to a formula (1):

$$\phi_M - V_G = \chi - \phi_I - \phi_S + \frac{E_G}{2q} + \phi_F \,, \tag{1}$$

where: ϕ_M – the barrier height at the gate-dielectric interface, V_G – gate potential, χ – the electron affinity of the silicon substrate at the interface, ϕ_I, ϕ_S – the potential drop across the dielectric and at the semiconductor surface, $E_G/2q$ – the voltage equivalent of half energy band gap in the semiconductor, q – the electron charge, ϕ_F – the Fermi potential.
The effective contact potential difference (ECPD or ϕ_{MS}) is defined as [9]:

$$\phi_{MS} \stackrel{def}{=} \phi_M - \left(\chi + \frac{E_G}{2q} + \phi_F\right). \tag{2}$$

Sometimes it is more convenient to use the value of the reduced effective contact potential difference (RECPD or ϕ^*_{MS}), defined as:

$$\phi^*_{MS} = \phi_M - \chi \tag{3}$$

or

$$\phi^*_{MS} = \phi_{MS} + \frac{E_G}{2q} + \phi_F \,. \tag{4}$$

It is clearly seen from Eq. (3) that the ϕ^*_{MS} value depends only on the barrier heights on both sides of the dielectric and does not depend on the doping concentration in the substrate (while the ϕ_{MS} value depends on it through the ϕ_F value).

The definition of ECPD, given by Eq. (2), allows a comparison to be made between the measured ϕ_{MS} values (by the photoelectric method [2]) and the independently measured values of both barrier heights (E_{BG} and E_{BS}). This can be done by comparing two ϕ^*_{MS} values, namely:

– the $\phi^*_{MS}(1)$ value calculated using Eq. (4) and the ϕ_{MS} value determined directly by the photoelectric method, and

– the $\phi^*_{MS}(2)$ value calculated using [13, 14]:

$$\phi^*_{MS}(2) = \frac{1}{q}\left(E_{BG} - E_{BS} + E_G\right) \tag{5}$$

with the values of E_{BG} and E_{BS} barrier heights measured using the modified Powell-Berglund method [10–14].

The R value defined as:

$$R = \phi^*_{MS}(1) - \phi^*_{MS}(2) \tag{6}$$

is an indicator of the accuracy of barrier height measurement. This is so because both the ϕ_{MS} (measured by the photoelectric method [2]) and the ϕ_F value (determined using capacitance voltage, $C(V_G)$ characteristics) needed to calculate $\phi^*_{MS}(1)$, are determined with high accuracy – better than ± 10 mV in both cases, while the barrier height measurements are known to be less accurate [15]. Obviously, the value of R decreases with improved accuracy of the measurements.

3. Experimental

Measurements were made on Al-SiO_2-Si MOS structures with semitransparent ($t_{Al} = 35$ nm) square gates (1×1 mm^2). To simplify interpretation of the photoelectric measurements [2], in this work the phosphorus doped n^+ substrates ($\rho = 0.015\ \Omega$cm) of $<100>$ orientation were used. After an initial hydrogen-peroxide-based cleaning sequence, the wafers were thermally oxidized at 1000°C in oxygen to grow silicon-dioxide layers of with the thickness of approximately 60 nm, and subsequently annealed in nitrogen for 10 min at 1050°C. It is obviously known, that current technological interest consists in measurements of oxide layers thinner than 3 nm, but in this case thicker oxides were used to optimize the sensitivity and accuracy of the applied photoelectric methods [2]. The frontside metalization was carried out in a thermal evaporator to the Al thickness of 35 nm. Postmetalization annealing was carried out at 450°C for 20 min in the forming gas atmosphere.

Photoelectric measurements of the barrier heights were made using the modified Powell-Berglund method. The modification of this method consisted in using a diameter of UV light beam ($d = 0.3$ mm) that was small in comparison with the dimension of the side length of the Al gate (1 mm). Hence, it was possible to scan the whole gate area and to measure local values of barrier heights (E_{BG} and E_{BS}), on both interfaces of the dielectric.

The 26 MOS capacitors were used in this investigation. On each of these capacitors local barrier heights were determined in 9 different locations, as illustrated in Fig. 4. The local values of barrier heights determined in this way were connected by 3rd order polynomial lines to obtain approximate distributions of barrier height over the entire gate area.

The results of barrier height measurements were compared with ϕ_{MS} measurements, as described in Section 2.

Based on measurements results, models have been developed of distributions of both barrier heights (E_{BG}, E_{BS}) over the gate area, as well as that of RECPD (ϕ^*_{MS}) values. The parameters of these models were fitted to obtain good agreement between measured and calculated distributions.

4. Results and discussion

Averaged distributions of E_{BG} and E_{BS} are shown in Fig. 6, while an averaged distribution of V^0_G is shown in Fig. 7.

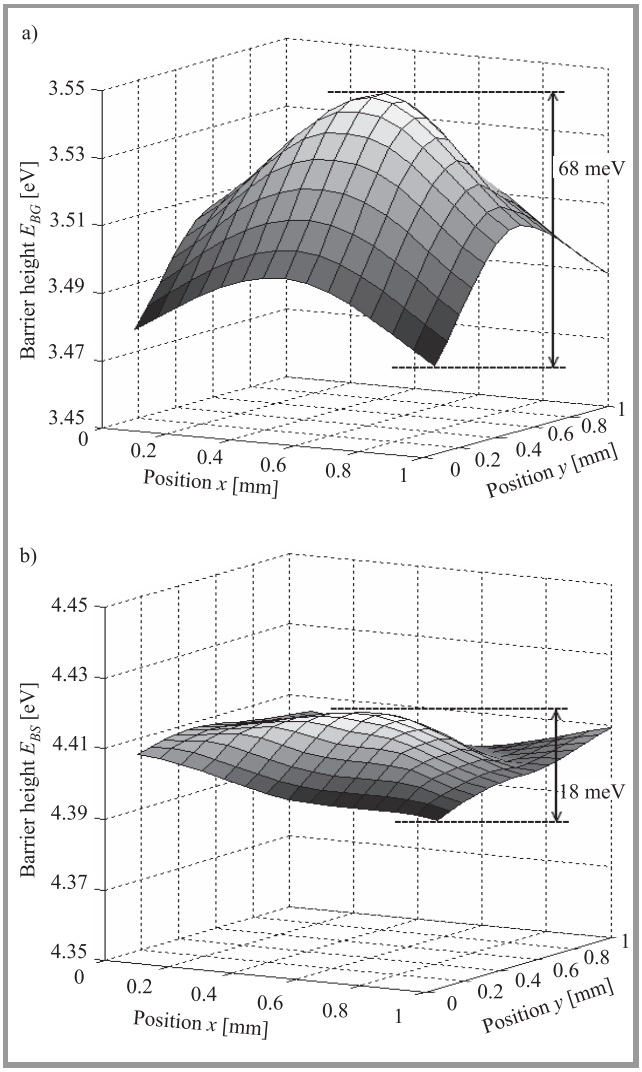

Fig. 6. Averaged two-dimensional distribution of: (a) E_{BG} and (b) E_{BS} barrier heights measured using modified Powell-Berglund method for 26 MOS structures. Average E_{BG} and E_{BS} values were found for each of the 9 locations over the gate area (shown in Fig. 4) and used to determine distributions shown in the figure.

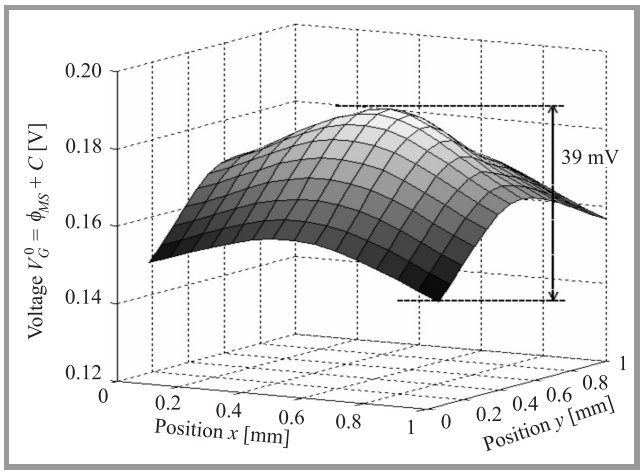

Fig. 7. Averaged two-dimensional distribution of V_G^0 voltage values measured for 26 MOS structures. Average V_G^0 values for the same wavelength $\lambda = 242$ nm were found for each of the 9 locations over the gate area (shown in Fig. 4) and used to determine the distribution shown in the figure.

In Figs. 6a and 7 it is seen that averaged E_{BG} and V_G^0 distributions have a characteristic dome-like shape with the highest values at the center of the square gate and lowest values at gate corners. On the other hand an averaged E_{BS} distribution is practically uniform, with random departures from uniformity. The averaged departures from the uniform distribution of E_{BS} decrease with the number of structures taken into account in the averaging process. Defining the amplitude A as the difference between the maximum and minimum local values of the same parameter over the gate area (e.g., $A(E_{BG}) = E_{BG\max} - E_{BG\min}$), one finds that the amplitude of E_{BG} distribution $A(E_{BG})$ is about four times

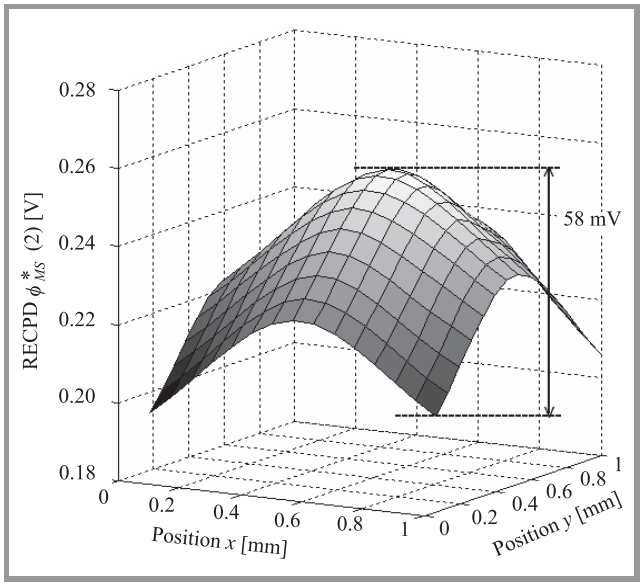

Fig. 8. Averaged two-dimensional distribution of $\phi^*_{MS}(2)$ calculated using E_{BG} and E_{BS} values for 26 MOS structures. Average $\phi^*_{MS}(2)$ values were found for each of the 9 locations over the gate area (shown in Fig. 4) and used to determine distributions shown in the figure.

larger than the amplitude $A(E_{BS})$ of the E_{BS} distribution ($A(E_{BG}) \approx 4A(E_{BS})$). This means that the distribution of the gate-dielectric barrier height $E_{BG}(x, y)$ has the decisive influence on the $\phi_{MS}(x, y)$ distribution.

Using Eq. (5) the average distribution of $\phi^*_{MS}(2)$ over the gate area was calculated and plotted in Fig. 8. This distribution has a similar shape to the distributions of the E_{BG} (Fig. 6) and the V_G^0 (Fig. 7) with the highest values at the gate center and lowest values at gate corners. It is well known [2] that the shape of $\phi^*_{MS}(1)$ distribution is the same as the shape of V_G^0 distribution, shifted by a constant value C.

Using Eq. (6) R values were obtained at each of nine positions over the gate area and are given in Table 1.

Table 1
Values of measurement errors R at the 9 positions over the gate area

Position (as indicated in Fig. 4)	1	2	3	4	5	6	7	8	9
R [mV]	20	1	9	13	–2	1	15	1	18

The values given in Table 1 are relatively small (we consider them as indicators of barrier height measurement accuracy). The accuracy of the both barrier height measurements is very good in the middle of the square gate (-2 mV, negative sign means that E_{BS} value is too low in comparison with E_{BG} value or that E_{BG} value is too high in comparison with E_{BS} value). There are larger differences between $\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$ at gate corners (the average value of R for four equivalent positions is 15 mV) and gate edges (4 mV is the average R value for four equivalent positions).

The model which has been applied to the ϕ_{MS} distribution [3, 4] can be also used to describe distributions of E_{BG}, $\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$. This model for the one-dimensional distribution $K(x)$ of the parameter K is given by the formula:

$$K(x) = K_0 + \Delta K \cdot \left[e^{\frac{x}{L}} + e^{\frac{a-x}{L}} \right], \qquad (7)$$

where: K_0 – value of K parameter far away from gate edges, ΔK – deviation of $K(x)$ from K_0, L – characteristic length of $K(x)$ distribution, a – side length of the square gate.

The predictions of the model are in good agreement with experimental results obtained on MOS structures with square gates used in this investigation. The model values at the gate center – K_0 were fitted to those obtained from the measurements. Values of all the parameters at gate corners were fairly close to the measured values.

Using the model based on Eq. (7), two-dimensional $E_{BG}(x, y)$ distribution was calculated and is shown in Fig. 9. The parameters used in model calculations are listed below the plot. The flat $E_{BS}(x, y)$ distribution can also be expressed in terms of the model Eq. (7), with the parameters: $E_{BS0} = 4.405$ eV, $\Delta E_{BS} = 0$ eV, $L = 0$ mm.

The RECPD distributions of $\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$ calculated using the model based on Eq. (7) are shown in Fig. 10.

In both cases the K_0 parameter of the model was so chosen as to obtain the same ϕ^*_{MS} value at the center of the gate as that obtained from measurements. Parameters used in model calculations are indicated below the diagrams. Clearly, $\phi^*_{MS}(2)$ values are lower than $\phi^*_{MS}(1)$ at the gate corners, as reflected in the $\Delta\phi^*_{MS}$ values ($|\Delta\phi^*_{MS}(2)| > |\Delta\phi^*_{MS}(1)|$. This is demonstrated more clearly in the one-dimensional distributions of $\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$ shown in Fig. 11.

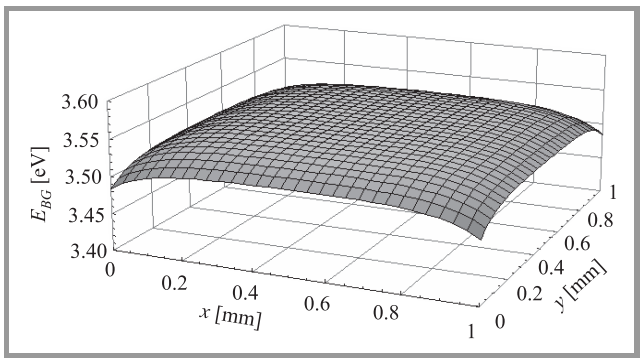

Fig. 9. Two-dimensional distribution of E_{BG} barrier height values calculated using the model based on formula (7). Model parameters: $E_{BG0} = 3.545$ eV, $\Delta E_{BG} = -0.061$ eV, $L = 0.1$ mm, $a = 1$ mm.

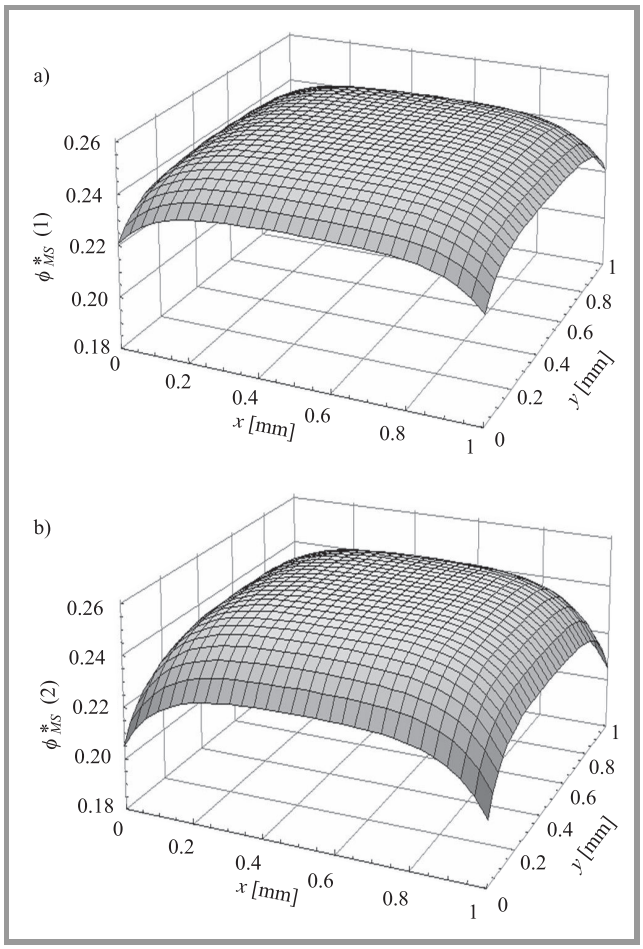

Fig. 10. Two-dimensional distributions of: (a) $\phi^*_{MS}(1)$ and (b) $\phi^*_{MS}(2)$ reduced effective contact potential difference values calculated using the formula (7). Model parameters: (a) $\phi^*_{MS0}(1) = 0.253$ V, $\Delta\phi^*_{MS}(1) = -0.032$ V, $L = 0.1$ mm, $a = 1$ mm; (b) $\phi^*_{MS0}(2) = 0.255$ V, $\Delta\phi^*_{MS}(2) = -0.05$ V, $L = 0.1$ mm, $a = 1$ mm.

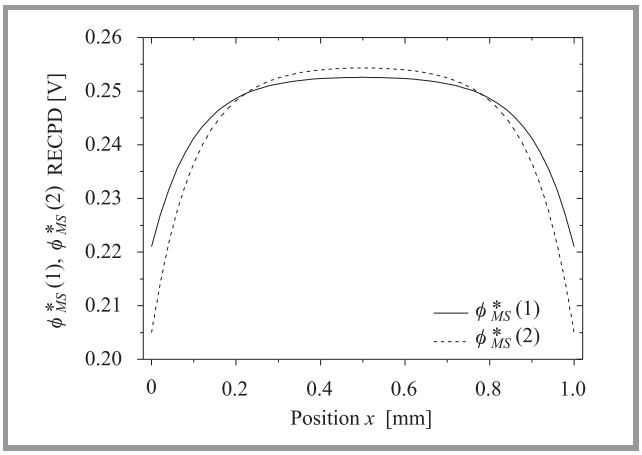

Fig. 11. Comparison of the $\phi^*_{MS}(1)$ (solid line) and $\phi^*_{MS}(2)$ (dashed line) distributions calculated using the model.

5. Conclusions

Distributions of E_{BG} and E_{BS} barrier heights, V^0_G voltage as well as RECPD ($\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$) over the gate area were studied. Measurements were made on a series of 26 Al-SiO_2-Si(n^+) MOS capacitors on one silicon wafer. Barrier heights were measured by modified Powell-Berglund method using a UV light beam of small diameter. This allowed the gate area to be scanned with the light beam and to measure local barrier height values at nine different positions over the gate area. It was found that E_{BG}, V^0_G, $\phi^*_{MS}(1)$ and $\phi^*_{MS}(2)$ values have a characteristic dome-like shape, with the highest values at the gate center, lower at gate edges and still lower at gate corners. On the other hand, E_{BS} barrier height distribution is essentially uniform, with random departures from uniformity.

The accuracy of both barrier height measurements was checked by comparing the $\phi^*_{MS}(1)$ value (determined using the ϕ_{MS} measured by the photoelectric method) with the value of $\phi^*_{MS}(2)$ (obtained from E_{BG} and E_{BS} measurements). It has been shown that the difference R between these values is very small (2 mV) at the center of the gate and becomes larger (~ 15 mV) at the corners of the square gate. These results (as well as the results of other experiments not reported in this paper), allow the accuracy of the measurement of local barrier height values by the modified Powell-Berglund method to be estimated. Our (rather conservative) estimation is that the possible measurement error ΔE_B does not exceed ± 50 meV in this case.

It was found that models of 2D distributions, similar to the model previously developed for $\phi_{MS}(x, y)$ distribution, can be successfully applied to other parameters – in particular to $E_{BG}(x, y)$ and $\phi^*_{MS}(2)(x, y)$ distributions.

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Paper

Electrical characterization of ISFETs

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Abstract— Methodology of electrical characterization of ISFETs has been described. It is based on a three-stage approach. First, electrical measurements of ISFET-like MOSFETs and extraction of basic parameters of the MOSFET compact model are performed. Next, mapping of the ISFET channel conductances and a number of other characteristic parameters is carried out using a semi-automatic testing setup. Finally, ISFET sensitivity to solution pH is evaluated. The methodology is applied to characterize ISFETs fabricated in the Institute of Electron Technology (IET).

Keywords—ISFET, CMOS, electrical measurements, I-V characteristics, characterization, parameters extraction.

1. Introduction

Ion-sensitive MOS transistors (ISFETs) operate as depletion-mode devices. Their electrical characterization must combine techniques typical for CMOS evaluation and those necessary for description of mechanisms specific to depletion-mode MOS transistors. In the electrical characterization of these devices it must be taken into account, that there are no gates in the functional devices. Thus the characterization must be done using first of all the ISFET-like MOS transistors with gates. The functional ISFETs are also tested and evaluated. The paper reports methods and selected results of electrical characterization of these devices.

2. Devices

Fabrication of ISFETs is partially based on the standard CMOS process. Device parameters are given in Table 1, whereas their structure is shown in Fig. 1. Also the topology of an ISFET-like MOSFET is shown in Fig. 2. The specific features of ISFET structure are as follows:

Table 1
Ion-sensitive MOS transistor parameters

Parameters	Values
Total area	4.9×4.9 mm^2
Channel width (W)	600 μm
Channel length (L)	16 μm
Gate oxide thickness (T_{SiO_2})	65 nm
Silicon nitride thickness ($T_{Si_3N_4}$)	65 nm
p-well junction depth ($X_{J\text{-}well}$)	6 μm
Source/drain junction depth ($X_{J\text{-}S/D}$)	1.5 μm

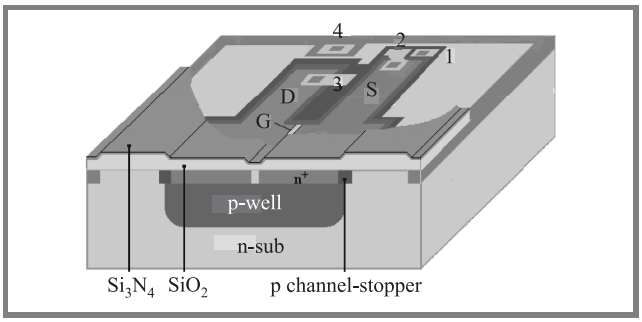

Fig. 1. Cross-section of a p-well ISFET; numbers denote the electrodes: p-well (1), source (2), drain (3), substrate (4).

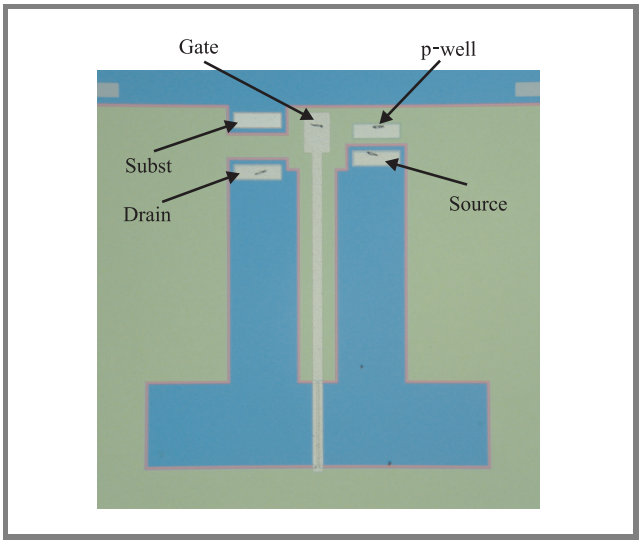

Fig. 2. A photo of an ISFET-like MOSFET. An Al-gate covers the active area of the device. The electrodes are seen clearly.

– p-well insulation of active areas (relevant mainly in the case of ISFET arrays); such insulation is necessary for ISFETs to operate in a typical application, that is as a source and drain follower [1, 2];

– long source/drain leads designed for the purpose of sufficient separation between the pads and the active area exposed to the solution-under-test; the separation is particularly necessary in the case of front-side contacted ISFETs; this obviously results in increased S/D series resistance.

3. Measurements

A Keithley System 93 IV controlled by METRICS software is used for electrical characterization of ISFETs and ISFET-like MOSFETs. In the case of wafer-scale measurements this system works concurrently with a semi-automatic probe station. The system is used for the following tests:

– measurements of *I-V* characteristics of ISFET-like MOSFETs;

– evaluation of ISFETs on a semi-automatic probe station;

– investigation of the insulation between ISFETs arranged as arrays of devices fabricated in the same substrate;

– measurements of *I-V* characteristics of ISFETs exposed to pH-solutions.

Selected measurement (subthreshold *I-V* characteristics of the ISFET-like devices and measurements of dark currents of the p-n junctions) are performed using a shielding box.

3.1. Measurement and characterization of ISFET-like MOSFETs

A measurement setup typical for MOSFET characterization is used (Fig. 3). Below, characterization procedures are described in more detail.

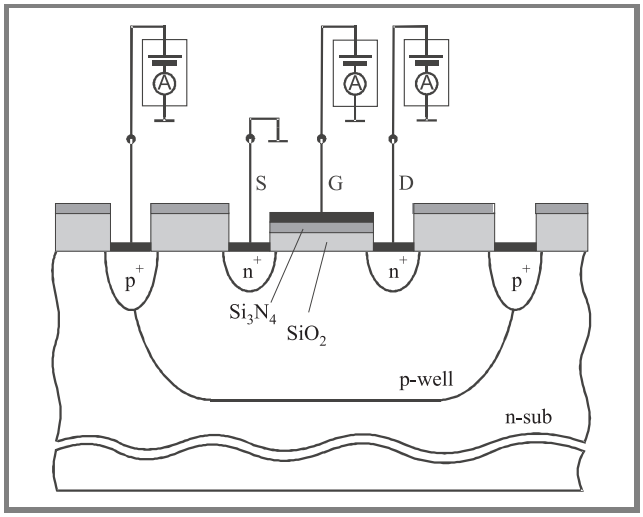

Fig. 3. Measurement setup used for characterization of ISFET-like MOSFETs.

3.1.1. Overall evaluation of electrical characteristics of the MOSFETs based on the *I-V* data

This procedure is based on the simple model of MOSFETs *I-V* characteristics, given by Eq. (1), where the symbols have their standard meanings:

$$I_D = \frac{W}{L_{eff}} \mu_{eff} C_I \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} . \qquad (1)$$

It should be mentioned that oxide capacitance C_{OX}, used commonly in models of MOSFET *I-V* characteristics, has been replaced by insulator capacitance C_I. This is due to the fact that the dielectric layer in ISFETs consists of oxide and nitride layers (see Fig. 1).

3.1.2. Extraction of basic parameters of MOSFETs

Transconductance coefficient $KP = \mu_{eff} C_I$, threshold voltage at $V_{BS} = 0$ V VTO, body factor $GAMMA$ and Fermi voltage PHI are evaluated through analysis of $I_D(V_{GS})$ data measured at constant V_{DS} voltage and a set of V_{BS} values. First, $I_D(V_{GS})$ data is differentiated to obtain $G_m(V_{GS})$ curves. Next, $I_D(V_{GS})$ and $G_m(V_{GS})$ data is used to extract KP and threshold voltage V_T. Threshold voltage corresponds to an abscissa of intersection point between a tangent line of the $I_D(V_{GS})$ curve and the V_{GS} axis. A position of the tangent line is determined by the coordinate of this $G_m(V_{GS})$ curve maximum. This method is illustrated in Fig. 4. It should be mentioned, that in the case

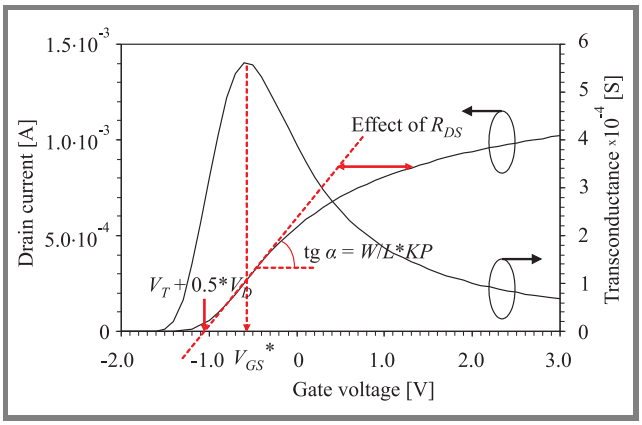

Fig. 4. Extraction of threshold voltage and transconductance coefficient ($V_D = 0.5$ V, $V_B = 0$ V).

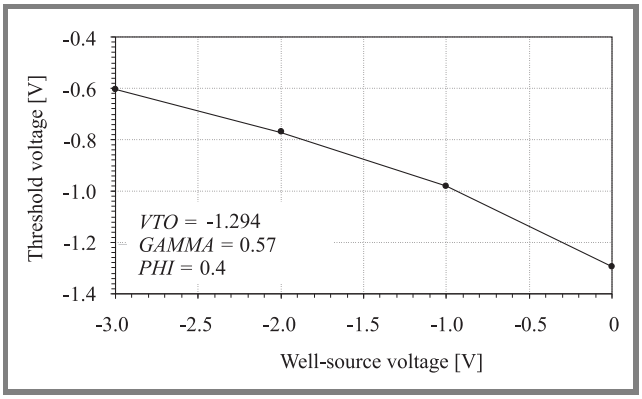

Fig. 5. Extraction of threshold voltage parameters ($V_{DS} = 0.5$ V).

of ISFETs a significant $I_D(V_{GS})$ degradation range can be observed in strong inversion. This is due to series resistance (from the devices topology), rather than mobility degradation. Both effects have a similar influence on the $I_D(V_{GS})$ data. Next, the calculated $V_T = f(V_{BS})$ characteristics are used to evaluate VTO, $GAMMA$ and PHI.

For this purpose a well-known square-root formula given by Eq. (2) is used:

$$V_T = VTO + GAMMA\left(\sqrt{PHI - V_{BS}} - \sqrt{PHI}\right). \qquad (2)$$

Figure 5 illustrates the methods used for extraction of these parameters.

3.1.3. Extraction of the weak inversion parameters of MOSFETs: *S*, *NFS*

This method is based on the MOSFET model of *I-V* characteristics in the subthreshold range presented in [3]:

$$I_D = I_{D,ON}\exp\left(\frac{V_{GS} - V_{ON}}{n\dfrac{kT}{q}}\right) = I_{D,ON}\exp\left(\frac{V_{GS} - V_{ON}}{S/\ln 10}\right), \qquad (3)$$

where:

$$S = n\frac{kT}{q}\cdot\ln 10,$$

$$n = 1 + \frac{q\cdot NFS + C_D}{C_I},$$

$$C_D = \frac{\varepsilon_{Si}}{W_D} = \frac{GAMMA\cdot C_I}{2\cdot\sqrt{PHI - V_{BS}}}.$$

The capacitance C_D is understood here as the capacitance per unit area of the gate-induced depletion region at the onset of strong inversion. The *NFS* parameter denotes the density of fast surface states at the insulator-silicon interface. The capacitance of the interface traps degrades the slope of the $I_D(V_{GS})$ curve *S*, which is reflected in the non-ideality factor *n* [3]. Other parameters have standard meanings. The estimation procedure is illustrated in Fig. 6.

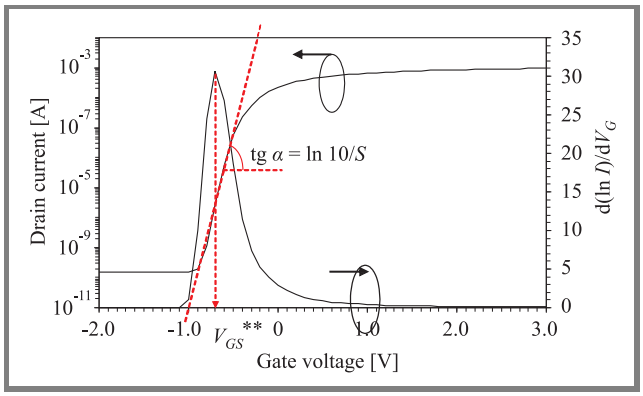

Fig. 6. Extraction of the subthreshold slope (V_D = 0.5 V, V_B = −3 V).

First, $\ln I_D(V_{GS})$ data is differentiated and a sharp peak is found. The coordinate of this peak determines a position of the subthreshold slope.

3.1.4. Estimation of ISFET current in the off-state, evaluation of the insulation between devices

As mentioned earlier, ISFETs operate as depletion-mode devices. However, for the purpose of characterization it is also necessary to evaluate the true dark current of S/D junctions. This test is performed by measurement of $I_D(V_{DS})$ characteristics for a set of negative gate voltages. The characteristics are measured both in the reverse and forward bias range. The junction dark current under reverse bias can be determined by measurement at the gate voltages below –1 V. Then the channel leakage current is switched off. Under these conditions *I-V* characteristics of the forward biased drain junction may be observed, too. The measurement results are shown in Fig. 7.

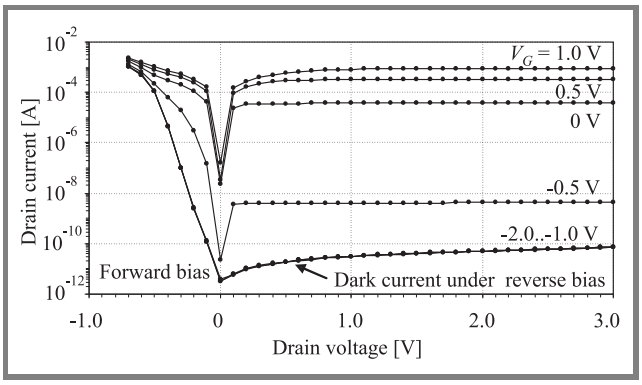

Fig. 7. Extraction of the dark current of the drain-well junction.

Perfect insulation between ISFETs is a very important requirement for their application in ISFET matrices. The devices operate independently, therefore any interaction, resulting, e.g., from a high well-substrate leakage and/or poor encapsulation, leads to degradation of the matrix functionality. The dark currents of adjacent devices have been measured in two configurations: separately and simultaneously. The results indicate that there is no interaction between the devices. The p-well insulation used in the presented technology is satisfactory.

3.2. Evaluation of ISFETs on a semi-automatic probe station

A semi-automatic measurement system is used in order to evaluate the fabricated ISFETs and to determine whether the measured parameter values are uniform over the wafer area. The measurements require multiplexing, therefore a Keithley 707A/7072 switching matrix is also used. The following parameters are measured:

- current of the forward-biased drain-well n^+-p junction;
- current of the reverse-biased drain-well n^+-p junction;
- source-drain current/source-drain resistance.

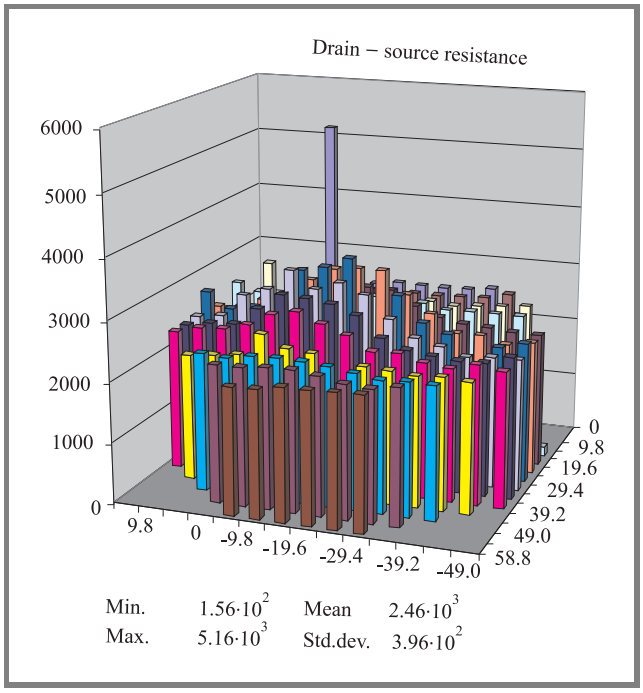

Fig. 8. On-wafer distribution of channel resistance of ISFETs in the on-state.

Post-processing of the measured data is done automatically including filtering, statistical processing (calculation of mean value, standard deviation, frequency) and smoothing. The output data is presented as discrete contour maps and bar charts. Figure 8 illustrates this set of measurements. The result show a satisfactory process uniformity.

3.3. Characterization of ISFETs exposed to pH-solutions

These measurements complete ISFET characterization. Operation of ISFETs with different p-well doping densities has been tested. Three calibrated buffer solutions with pH = 4.0, 6.694, and 8.358 have been used. The measurement setup configuration is shown in Fig. 9.

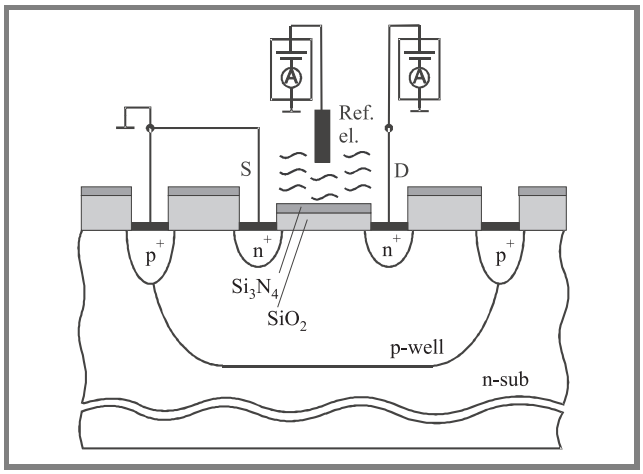

Fig. 9. Measurement setup for testing ISFETs exposed to pH-solution.

Characteristics $I_D(V_{GS})$ have been measured and threshold voltages have been calculated using the transconductance data. In accordance with the theory the experimental results show linear V_T(pH) dependence with sensitivities of the order of 50 mV/pH (Fig. 10). The increase of sensitivity

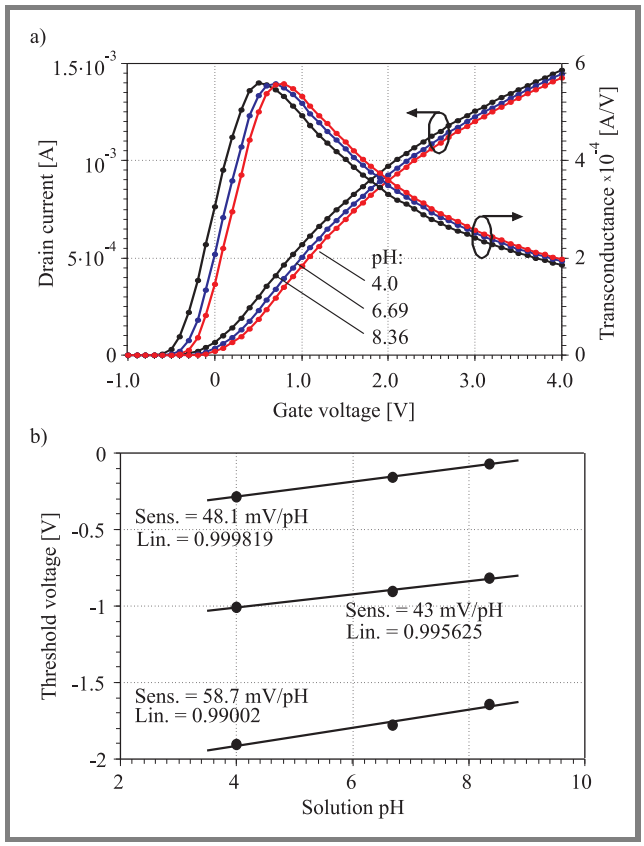

Fig. 10. Influence of pH on ISFETs characteristics: (a) a shift of the $I_D(V_{GS})$ and $G_m(V_{GS})$ characteristics; (b) a resulting ISFET-like MOSFETs threshold voltage variation due to the pH change.

of sample with DHF (diluted HF) dip up to 58.7 mV/pH results from a native oxide removal. Moreover, it has been determined, that the subthreshold slope of ISFETs increases for increasing pH values. In the case of these devices it has changed between 115 and 130 mV/dec.

4. Summary

A methodology of electrical characterization of ISFETs has been presented. It is based on a concept of CMOS characterization system. The presented measurement and parameters extraction methods have been used for evaluation of the devices manufactured in the Institute of Electron Technology.

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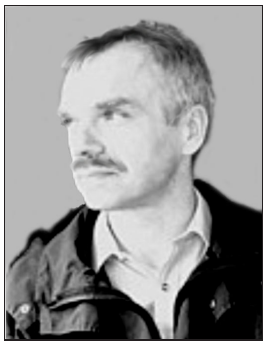

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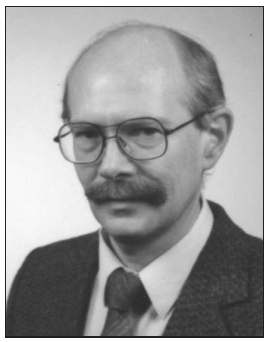

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Paper

Charge-pumping characterization of SOI devices fabricated by means of wafer bonding over pre-patterned cavities

Grzegorz Głuszko, Lidia Łukasiak, Valeriya Kilchytska, Tsung Ming Chung, Benoit Olbrechts, Denis Flandre, and Jean-Pierre Raskin

Abstract—The quality of the silicon-buried oxide bonded interface of SOI devices created by thin Si film transfer and bonding over pre-patterned cavities, aiming at fabrication of DG and SON MOSFETs, is studied by means of charge-pumping (CP) measurements. It is demonstrated that thanks to the chemical activation step, the quality of the bonded interface is remarkably good. Good agreement between values of front-interface threshold voltage determined from CP and *I-V* measurements is obtained.

Keywords— charge-pumping, electrical characterization, interface traps, SOI, wafer bonding, Si layer transfer.

1. Introduction

Silicon-on-insulator (SOI) technology, and especially double-gate (DG) transistors, offers well-known advantages for device operation, such as reduction of short-channel effects (SCE). While in single-gate SOI, improved SCE (in comparison to bulk devices) is reduced due to film thickness, in the case of double-gate devices, short-channel effects may be further lowered thanks to increased vertical electrical control [1].

The aim of this paper is to investigate the quality of SiO_2-Si interface in devices fabricated by a novel process developed in the Université Catholique de Louvain (UCL). This new fabrication process aims at obtaining planar DG and silicon-on-nothing (SON) MOSFETs by the transfer and bonding of a thin Si film on a substrate patterned with cavities and by the subsequent alignment of the device active area and gate definitions over the cavities [2]. Here the quality of the bonded interface is assessed using charge-pumping (CP) measurements on single-gate PIN diodes fabricated simultaneously with the DG SON MOSFETs.

2. Device processing

The devices investigated in this paper were obtained using a novel fabrication method [2] schematically shown in Fig. 1. More details about bonding process can be found in [2]. One of the process critical step, particularly important for the present study, is surface activation prior to bonding, since it plays a major role in the bonded interface quality. Activation using oxygen plasma (which is usual in wafer bonding process) has shown to be detrimental for

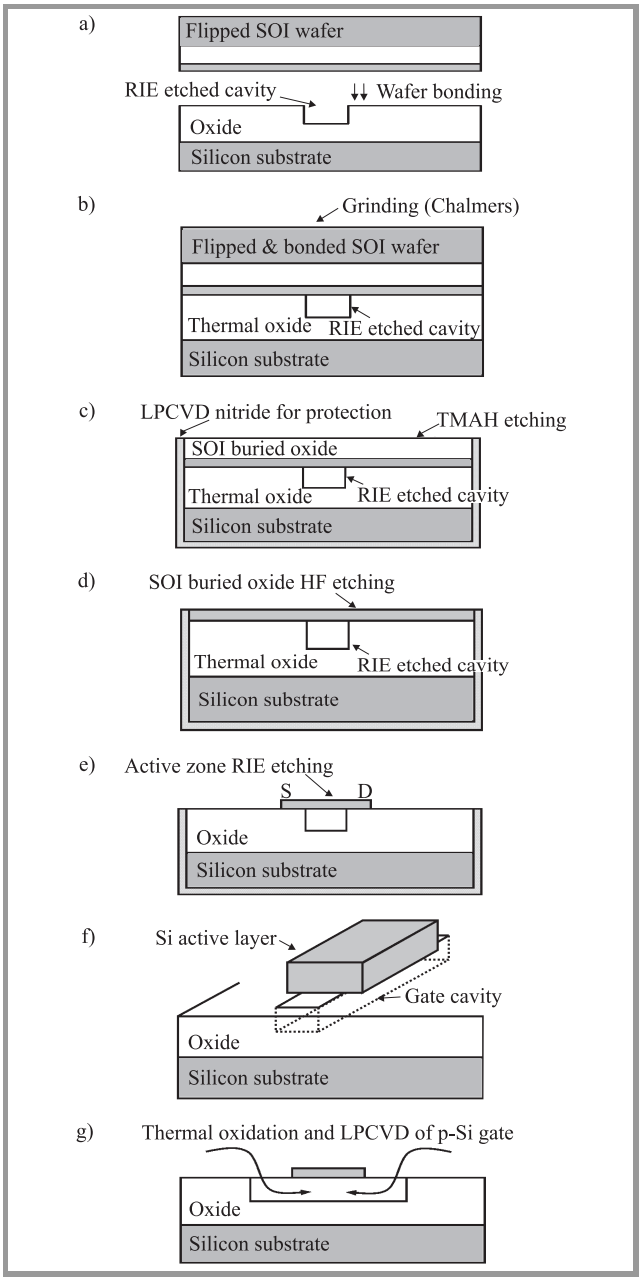

Fig. 1. Novel fabrication method: (a) oxidation of handle wafer, reactive ion etching (RIE) and wafer bonding; (b) SOI substrate thinning via grinding; (c) LPCVD nitride deposition and TMAH etching; (d) BHF etching of SOI BOX; (e) patterning of silicon islands by RIE etching; (f) 3D view of Si island; (g) MOS oxidation and CVD of polysilicon gate.

the electrical properties: high density of interface states and reduced mobility. To assure the good electrical quality of the bonded interface, which is especially important in DG devices, since conduction will take place at this interface,

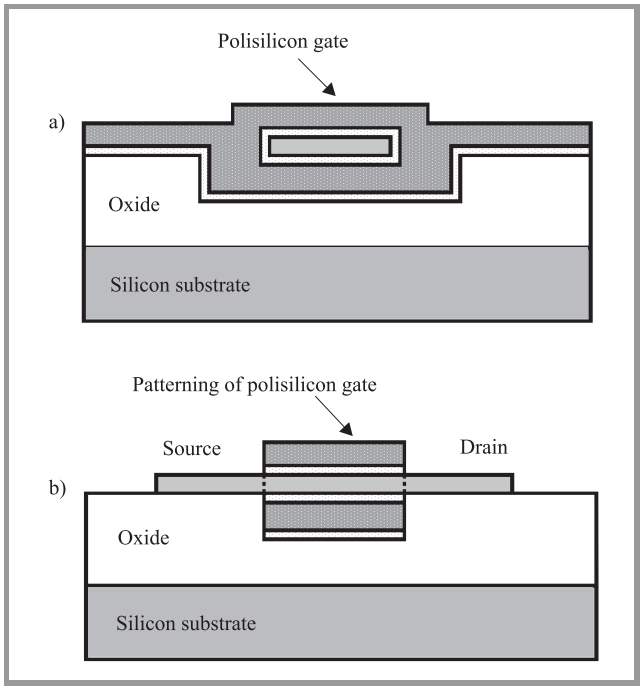

Fig. 2. Cross-section of a DG MOSFET: (a) transversal; (b) longitudinal.

chemical activation has been used. Warm nitric acid has been proven to be a good activation agent [3] and hence in this process we performed activation in nitric acid 70% at 70°C during 10 minutes [2]. Transversal and longitudinal cross-sections of a DG transistor are presented in Fig. 2. A photo of a final device is shown in Fig. 3.

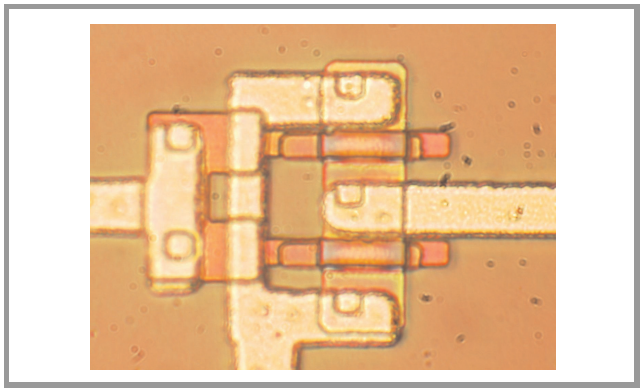

Fig. 3. Photo of a final working double-gate transistor.

Characterization results were compared to those obtained from reference devices. These devices were fabricated using the standard UCL process described in [4] on commercially available UNIBOND® SOI substrates. Otherwise, processing conditions were the same for both device types.

3. Charge-pumping measurements

Since single and double gate fully-depleted transistors had no contact to the body, PIN gated diodes were chosen for charge-pumping measurements using the approach first presented in [5]. Thus the two investigated SiO_2-Si interfaces were the front-gate interface and the back interface between the buried oxide (BOX) and body (Fig. 4). The latter interface is a measure of wafer-bonding quality.

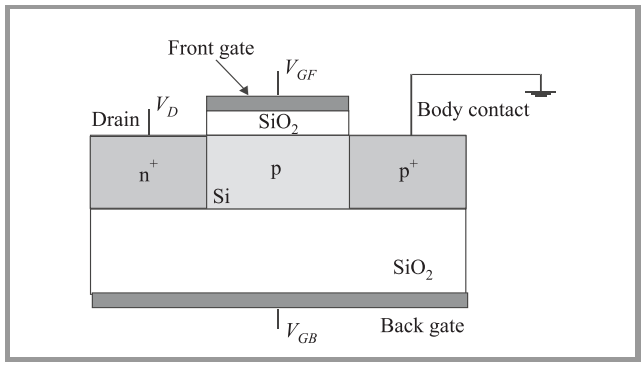

Fig. 4. Schematic cross-section of a SOI PIN diode.

The investigated devices were SG PIN diodes with gate oxide thickness $t_{ox} = 30$ nm, body thickness $t_{Si} = 80$ nm and BOX ≈ 600 nm (400 nm in the reference devices). The effective body doping is approximately $N_A = 10^{15}$ cm^{-3}. Gate dimensions ($W \times L$) of PIN diodes are 570 μm $\times$ 10 μm, 758 μm $\times$ 5 μm and 852 μm $\times$ 3 μm.

Charge-pumping current measured at front-gate interface of a PIN diode fabricated using the novel process flow is plotted as a function of gate base voltage in Fig. 5 for back-gate bias of 0 V and –20 V, respectively. The amplitude of the gate signal (parameter of the family of curves in the diagram) was changed from 2 V to 5 V (solid lines) and then the whole measurement sequence was repeated (squares). The fact that the results of both experiments are very close indicates that no visible generation of interface traps was caused during measurements. Similar results obtained from the back interface are presented in Fig. 6 for front-gate bias of 0 V and –2 V, respectively. In this case, the back gate-signal amplitude was changed between 10 and 30 V and again, no visible degradation due to the applied voltages was observed. The CP curves presented in Fig. 6b do not saturate, it is visible, however, that with increasing amplitudes the increase of maximum charge-pumping current becomes weaker. We believe, therefore, that the maximum charge-pumping current obtained at gate voltage amplitude of 30 V can serve as a good indication of the total density of interface traps at the back interface. Unfortunately, higher amplitudes would damage the structures permanently.

Analysis of CP curves presented above yields a total density of interface traps N_{it}, as well as threshold V_T and flat-band V_{FB} voltage. The obtained results are listed in Table 1.

Table 1
Results of CP characterization performed on PIN diodes fabricated using the novel process flow

Interfaces		$W \times L$ = 570 μm × 10 μm			$W \times L$ = 758 μm × 5 μm			$W \times L$ = 852 μm × 3 μm		
		V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]
Front	$V_{GB} = 0$ V	–0.8	–0.2	$3.1 \cdot 10^{10}$	–0.7	–0.2	$2.6 \cdot 10^{10}$	–0.7	–0.2	$2.9 \cdot 10^{10}$
	$V_{GB} = -20$ V	–0.7	0.3	$2.2 \cdot 10^{10}$	–0.5	0.5	$1 \cdot 10^{10}$	–0.5	0.5	$0.7 \cdot 10^{10}$
Back	$V_{GF} = 0$ V	–5	–2.5	$2.6 \cdot 10^{10}$	–8	–3	$2.2 \cdot 10^{10}$	–8	–3	$2.5 \cdot 10^{10}$
	$V_{GF} = -2$ V	3	12	$1.3 \cdot 10^{10}$	7	12	$0.7 \cdot 10^{10}$	6	12	$0.4 \cdot 10^{10}$

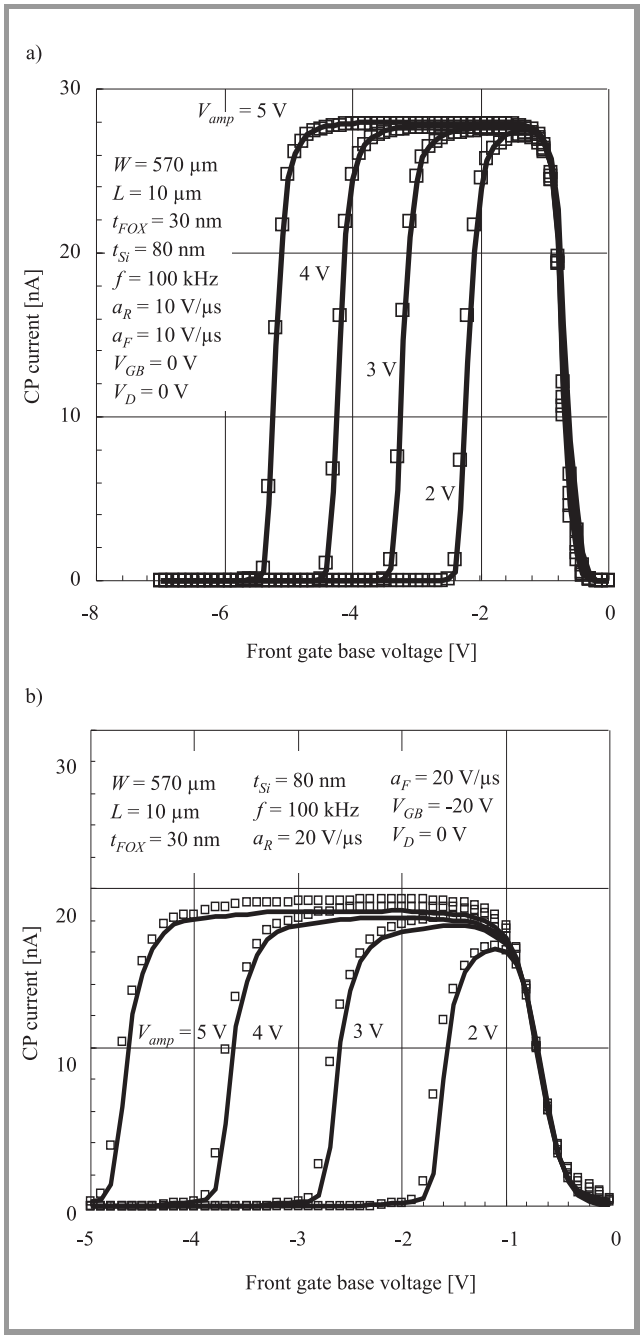

Fig. 5. Charge-pumping current as a function of top-gate base voltage for different amplitudes of the top-gate signal: (a) $V_{GB} = 0$ V; (b) $V_{GB} = -20$ V.

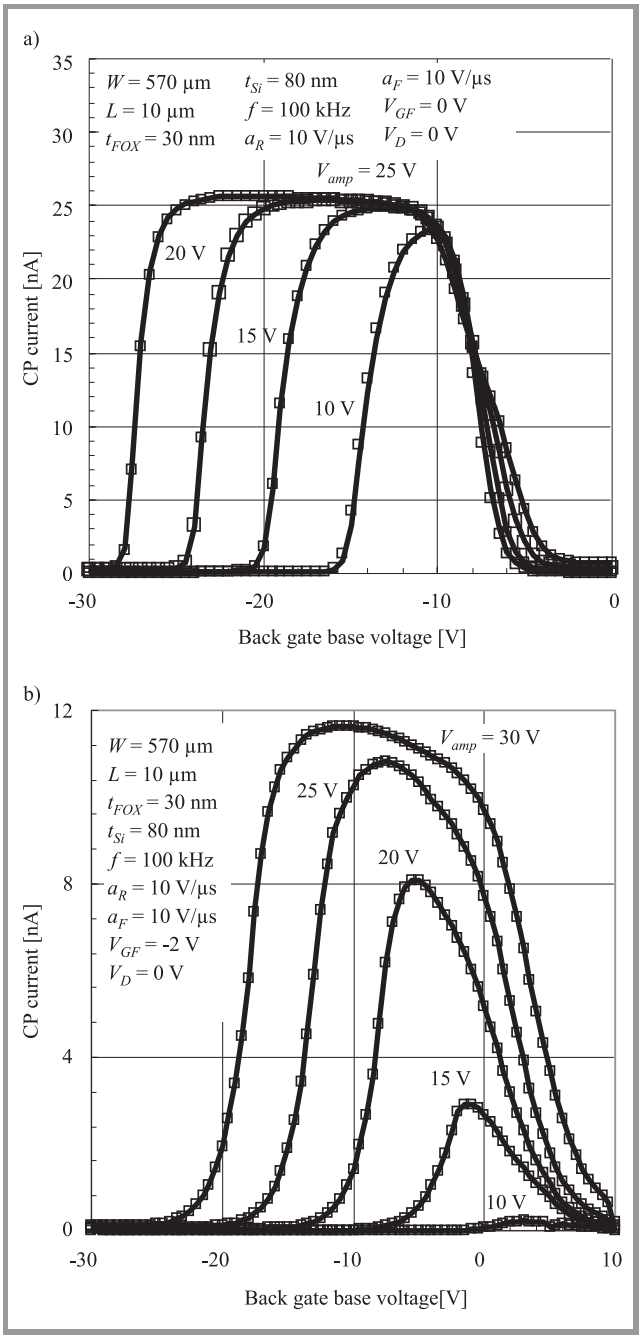

Fig. 6. Charge-pumping current as a function of back-gate base voltage for different amplitudes of back-gate signal: (a) $V_{GF} = 0$ V; (b) $V_{GF} = -2$ V.

It may be seen that interface-trap density is unexpectedly low at both interfaces indicating very good quality of both front-gate oxidation process and additional wafer bonding. The threshold voltage of the front interface obtained at back-gate bias of 0 V is in excellent agreement with that extracted from *I-V* characteristics of single-gate transistors. Threshold voltage was extracted from the intersection of straight lines approximating the log-lin $I_D = f(V_{GS})$ characteristics in the subthreshold and strong inversion regions (Fig. 7) (e.g., [6]).

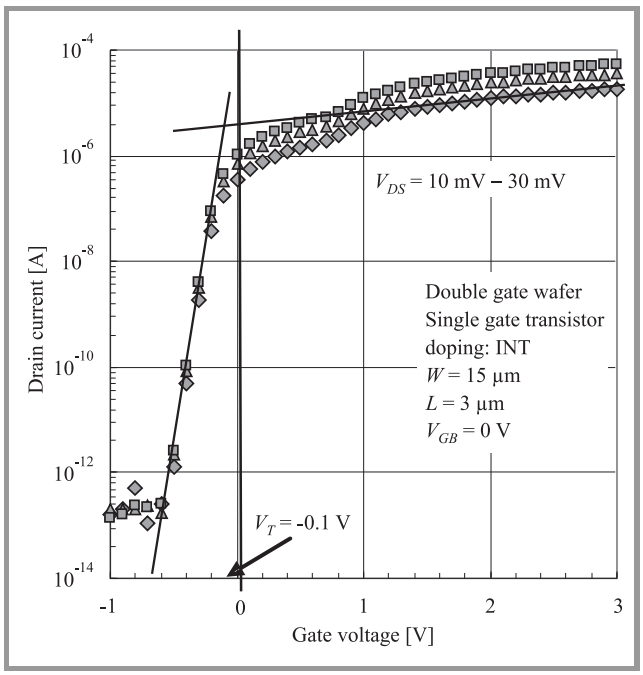

Fig. 7. Transfer characteristics of a single-gate transistor ($V_{GB} = 0$ V).

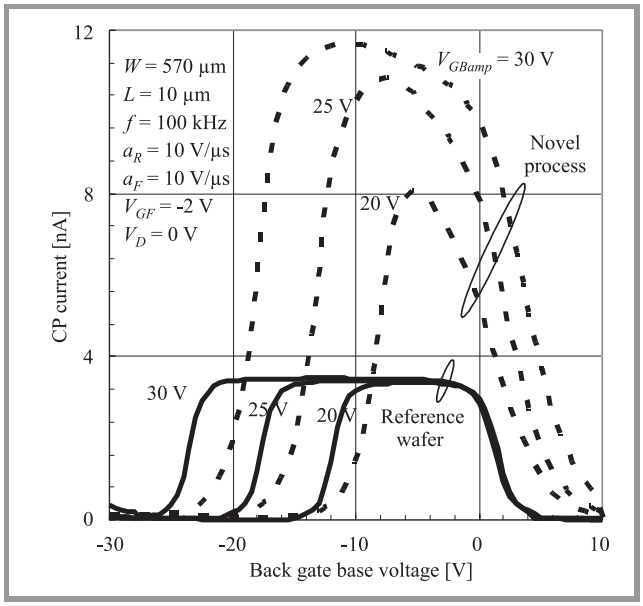

Fig. 8. Comparison of CP measurements performed on novel (dashed line) and reference (solid line) structures.

A comparison with CP measurements performed on back-interface of reference PIN diodes fabricated on a standard UNIBOND® wafer is presented in Fig. 8. The interface trap density at the back interface is slightly lower ($N_{it} = 0.4 \cdot 10^{10}$ cm^{-2}) for reference devices than for those fabricated using the novel process flow ($N_{it} = 1.3 \cdot 10^{10}$ cm^{-2}), which indicates that additional bonding used in our experimental DG SON process only slightly worsens the BOX-Si film interface quality when compared to a commercial well-established UNIBOND® process, in which bonded interface is placed at BOX-substrate interface [7].

4. Conclusions

Thanks to chemical activation of the bonded interface, the density of interface traps is remarkably low at both interfaces of structures fabricated using the novel technique described in [2]. The reliability of CP measurements is confirmed by a very good agreement between the values of front-interface threshold voltage determined by means of CP and *I-V* techniques. Further studies are needed to eliminate potential inaccuracies of the obtained results.

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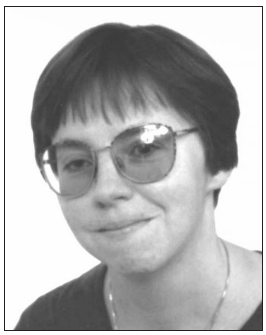

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Grzegorz Głuszko – for biography, see this issue, p. 8.

Paper

Characterization of SOI MOSFETs by means of charge-pumping

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Abstract—This paper presents the results of charge-pumping measurements of SOI MOSFETs. The aim of these measurements is to provide information on the density of interface traps at the front and back Si-SiO_2 interface. Three-level charge-pumping is used to obtain energy distribution of interface traps at front-interface.

Keywords—charge-pumping, electrical characterization, interface traps, SOI MOSFET.

1. Introduction

Silicon-on-insulator (SOI) technology has several well-known advantages over classical bulk technology, e.g., enhanced current, ideal subthreshold slope, reduced short channel effects and lower junction capacitance [1], as well as superior mobility and decreased power consumption [2]. Moreover, it is immune to latch-up effects, while complete isolation of devices and feasibility of high-resistivity substrate result in reduced substrate-loss for RF applications [3]. The performance of SOI MOSFETs is, however, determined to a large extent by the quality of the top and bottom SiO_2-Si interface. Therefore in this paper the quality of these interfaces is studied by means of charge-pumping (CP) [4].

2. Investigated structures

SOI MOSFETs with body contacts (BC) have been fabricated on SOITEC substrates with an initial top-silicon thickness of $t_{SOI} = 100$ nm and a buried oxide (BOX) thickness of $t_{BOX} = 200$ nm (see schematic Fig. 1a). Top-silicon layers have been doped by boron ion implantation and subsequent annealing to achieve one sample with a nominal channel doping of $N_{ch} = 10^{17}/\text{cm}^3$ and two samples with $N_{ch} = 10^{18}/\text{cm}^3$. Channel regions including source, drain and body contacts have been defined by mesa isolation using inductive coupled plasma reactive ion etching (ICP-RIE) with a two step HBr/O_2 process [5]. After a modified RCA clean, a thermal gate oxide with a thickness of $t_{ox} = 8.5$ nm has been grown at 900°C. Subsequently, polysilicon with a thickness of $t_{poly} = 150$ nm has been deposited by low pressure chemical vapor deposition (LPCVD). Polysilicon has been removed completely except from the gate and BC regions by ICP-RIE, again with a two step HBr/O_2 process [5]. Source and drain have been completed by self aligned arsenic (n^+) ion implantation and rapid thermal annealing (RTA). BCs have been uncovered by ICP-RIE with a two step HBr/O_2 process [5]. The etch mask has then been used in a self aligned manner to dope the BC leads by boron (p^+) ion implantation and RTA.

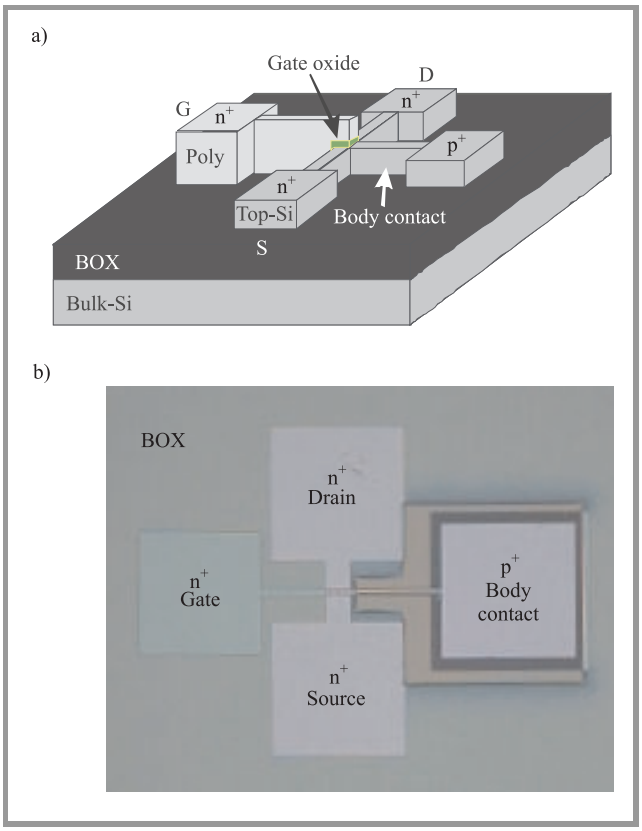

Fig. 1. SOI MOSFET with body contact: (a) schematic; (b) microscope image.

Forming gas annealing in N_2/H_2 for 30 min at 400°C to cure oxide and interface charges has been applied to one sample with $N_{ch} = 10^{18}/\text{cm}^3$. A microscope image of a fabricated device is shown in Fig. 1b. Gate length and gate width are $L_g = 10\,\mu$m and $W = 20\,\mu$m, respectively.

3. Charge-pumping measurements

This section is divided into three parts. The first two are devoted to characterization of front- and back-interface by means of two-level charge-pumping, while the third presents preliminary results of front-interface studies using three-level charge-pumping.

3.1. Two-level charge-pumping – front-interface

Front-interface charge-pumping curves were measured for different values of back-gate bias V_{GB}. Comparison of these curves indicates that no or very weak interface coupling takes place at $V_{GB} = -30$ V, therefore all subsequent measurements of front-interface CP current were carried out at this back-gate bias. The influence of source-body and drain-body junction reverse bias on front-interface CP current is illustrated in Fig. 2. In the case of non-annealed structures significant geometric component is observed for $V_D = V_S < 0.5$ V. This is most probably due to considerable resistance of the body contact. As a result, all subsequent measurements on these structures were made at $V_S = V_D = 0.5$ V.

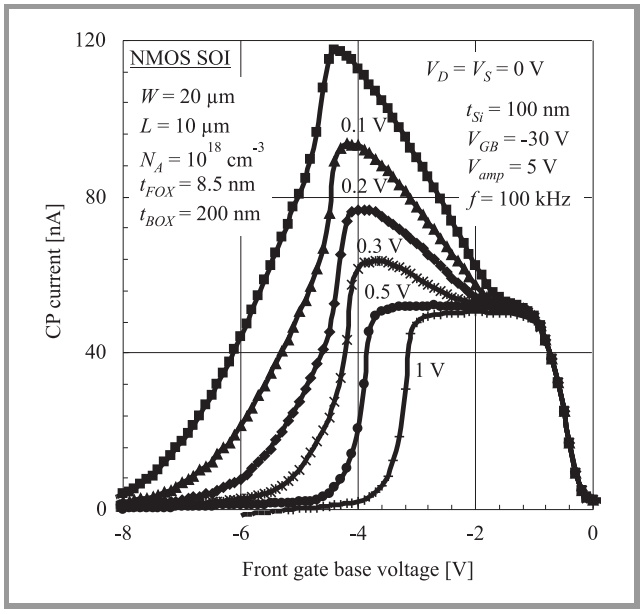

Fig. 2. Front-interface CP current as a function of front-gate base voltage with source-body and drain-body junction bias as a parameter.

An example of CP current measured on structures with body doping of 10^{17} cm^{-3} is shown in Fig. 3a as a function of front-gate base voltage with gate voltage amplitude as a parameter.

The fact that the middle part of each curve is not perfectly flat is probably due to the fact that the resistance of the body contact is considerable due to a relatively low body thickness.

Table 1
Parameters determined from 2-level charge-pumping measurements

Structure type	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]
$N_{body} = 10^{17}$ cm^{-3}	$1.7 \cdot 10^{12}$	−0.5	1.1
$N_{body} = 10^{18}$ cm^{-3} (non-annealed)	$2.0 \cdot 10^{12}$	−0.4	1.5
$N_{body} = 10^{18}$ cm^{-3} (annealed)	$8.4 \cdot 10^{10}$	−1.0	0.0

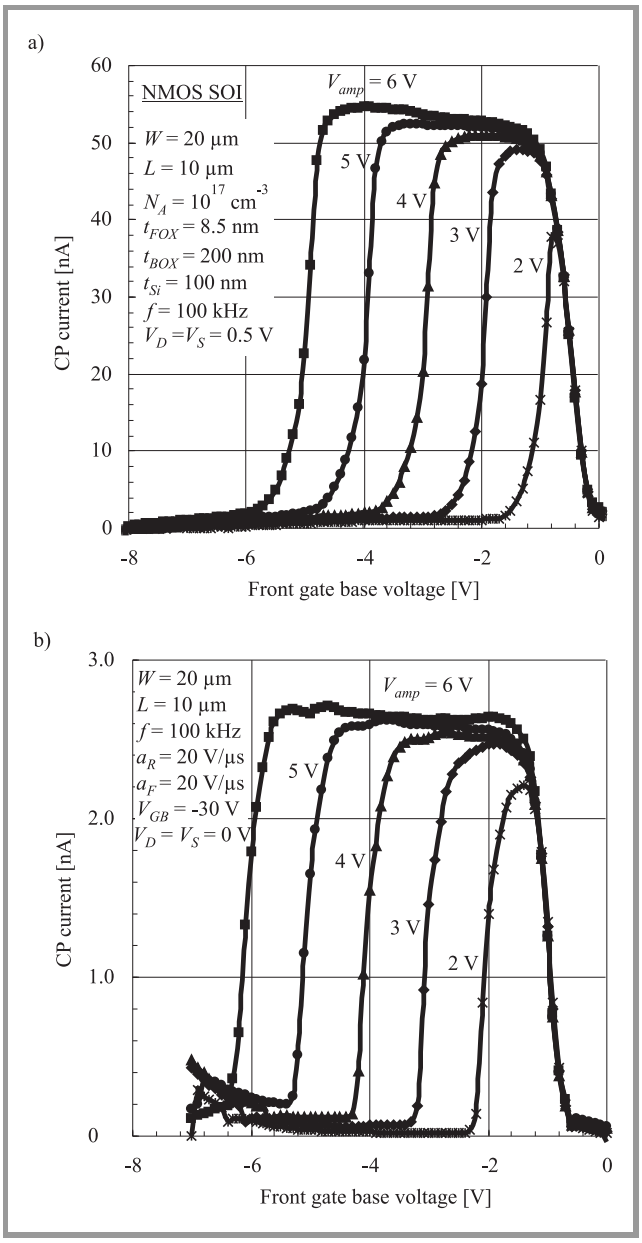

Fig. 3. Front-interface CP current as a function of front-gate base voltage with gate voltage amplitude as a parameter: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

In the case of annealed structures with body doping of 10^{18} cm^{-3} the CP current is more than an order of magnitude lower, which can be seen in Fig. 3b. Moreover, reverse bias of source and drain junctions is not necessary in this case.

Analysis of the obtained CP curves yields the total density of interface traps N_{it}, flatband voltage V_{FB} and threshold voltage V_T. Similar measurements were performed on both annealed and non-annealed structures with body doping of 10^{18} cm^{-3}. The results are listed in Table 1.

As expected, the lowest density of interface traps is obtained in the case of annealed structures with $N_{body} = 10^{18}$ cm^{-3}. Values of flatband and threshold voltages indicate that CP curves of this structure are shifted to the left

when compared to those of the other two structures. This difference is most probably due to the annealing process. The highest concentration of interface traps was found in non-annealed structures with $N_{body} = 10^{18}$ cm^{-3}. Since this structure type had the worst quality of front-gate interface, it was excluded from further investigations.

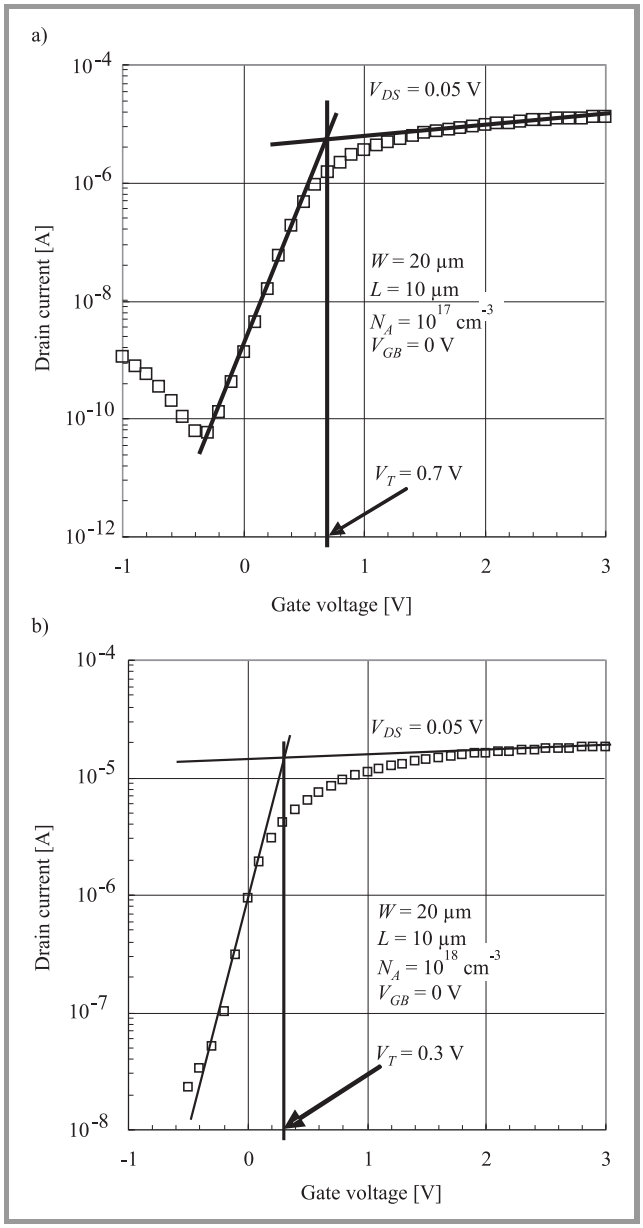

Fig. 4. Drain current as a function of gate voltage: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

Extraction of flat-band and threshold voltages from CP curves yields only approximate values. For comparison threshold voltage was also determined from transfer characteristics of the drain current shown in Fig. 4 for devices with body doping of 10^{17} cm^{-3} and 10^{18} cm^{-3}, respectively.

It may be seen that values extracted from *I-V* curves are lower by approximately $0.3 - 0.4$ V, which is partly due to the fact that current was measured at $V_{GB} = 0$ V (much more natural operation conditions) instead of -30 V used in CP measurements to eliminate the contribution of the back-interface to CP current. On the other hand, both methods are in qualitative agreement indicating that threshold voltage of transistors with body doping of 10^{17} cm^{-3} is considerably higher than that of annealed devices with $N_{body} = 10^{18}$ cm^{-3}.

3.2. Two-level charge-pumping – back-interface

Similar analysis was performed for back-interface. To avoid interface coupling the front-interface was biased in accumulation ($V_{GF} = -2$ V). Typical CP curves obtained in the case of structures with $N_{body} = 10^{17}$ cm^{-3} and annealed

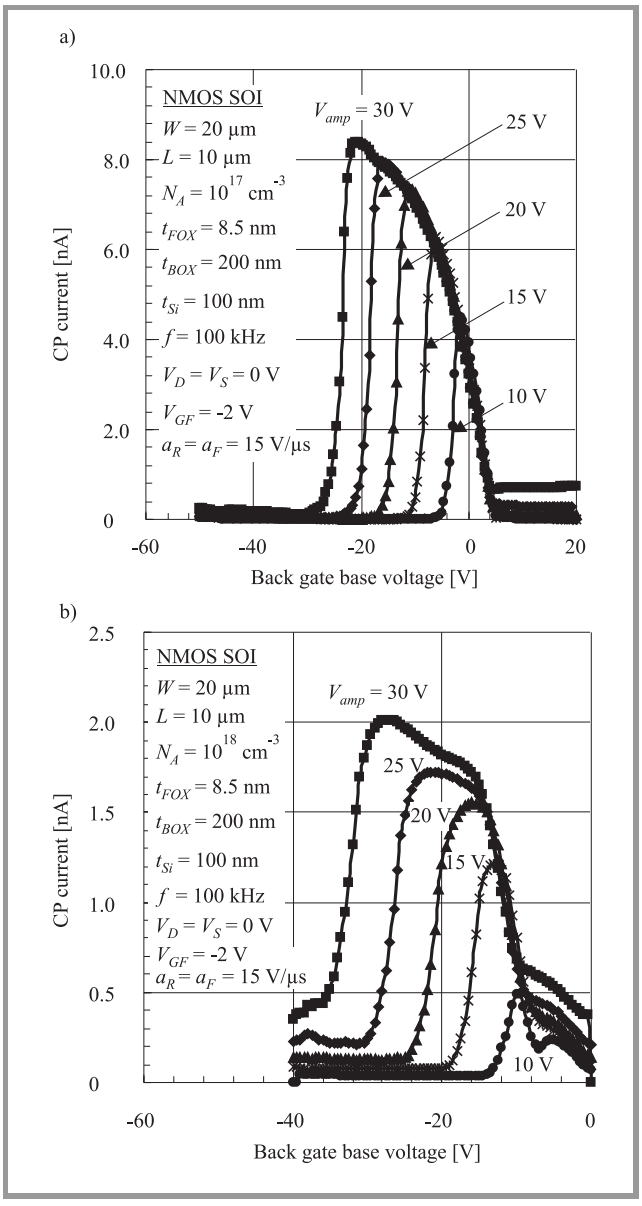

Fig. 5. Back-interface charge-pumping current versus back-gate base voltage with back-gate voltage as a parameter: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

structures with $N_{body} = 10^{18}$ cm^{-3} are shown in Fig. 5, respectively. It may be seen that the maximum charge-pumping current does not saturate in either case. Using higher back-gate voltage amplitudes leads to a permanent damage to the structure. If N_{it} is determined from the highest CP current obtained, the results are approximately $2.8 \cdot 10^{11}$ cm^{-2} for $N_{body} = 10^{17}$ cm^{-3} and $1.2 \cdot 10^{10}$ cm^{-2} for $N_{body} = 10^{18}$ cm^{-3}. This is either much lower or comparable to the result obtained for front-interface (approximately $1.7 \cdot 10^{12}$ cm^{-2} or $8.4 \cdot 10^{10}$ cm^{-2}, respectively). Normally, back interface has considerably lower quality than the front-interface.

The obtained results could be due to the fact that the structures are damaged before the true maximum back-interface CP current is reached. It is interesting to note that the CP current is again much lower in the case of annealed structures with $N_{body} = 10^{18}$ cm^{-3}. This indicates that the annealing process could have influenced positively the quality of the back-interface, too.

3.3. Three-level charge-pumping – front-interface

Determination of the energy distribution of interface traps from 3-level CP measurements requires the knowledge of front-surface potential as a function of gate voltage. Appropriate simulations were performed using SILVACO/ATLAS software yielding both front and back surface potentials.

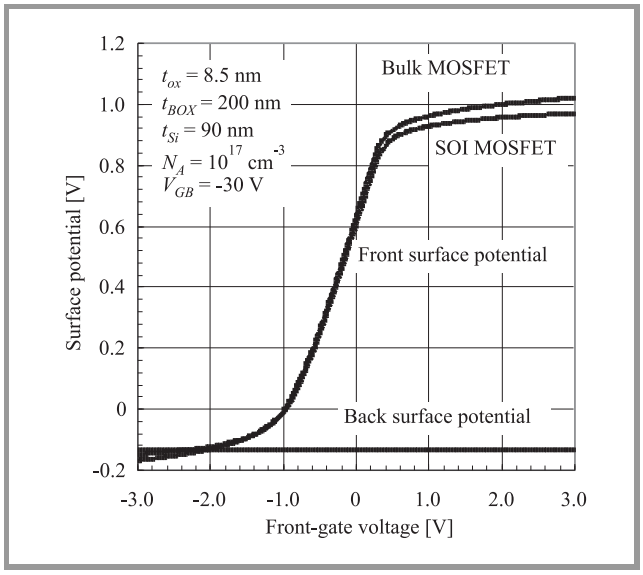

Fig. 6. Front and back surface potential of a SOI structure simulated as a function of front-gate voltage using SILVACO/ATLAS software (simple, numerical simulation of surface potential in a bulk MOSFET added for comparison).

The results are shown in Fig. 6 for body doping of 10^{17} cm^{-3}. For comparison, front-gate surface potential was also calculated in a classical way, that is assuming a bulk MOSFET (with the same gate-oxide thickness and substrate doping) instead of SOI one:

$$V_{GF} - V_{FB} = \frac{\mathrm{k}T}{q} \cdot G \cdot F(\varphi_s) + \varphi_s \,, \tag{1}$$

where: $\mathrm{k}T/q$ – thermal voltage, G – ratio of intrinsic semiconductor capacitance at flatband to gate-oxide capacitance, φ_s – surface potential and $F(\varphi_s)$ – the Kingston function.

It may be seen that the surface potential calculated according to Eq. (1) is in good agreement with that obtained from SILVACO/ATLAS, meaning that there is little coupling between the front and back-interface at $V_{GB} = -30$ V. Moreover, the back surface potential is almost constant in the investigated range of front-gate voltage, therefore

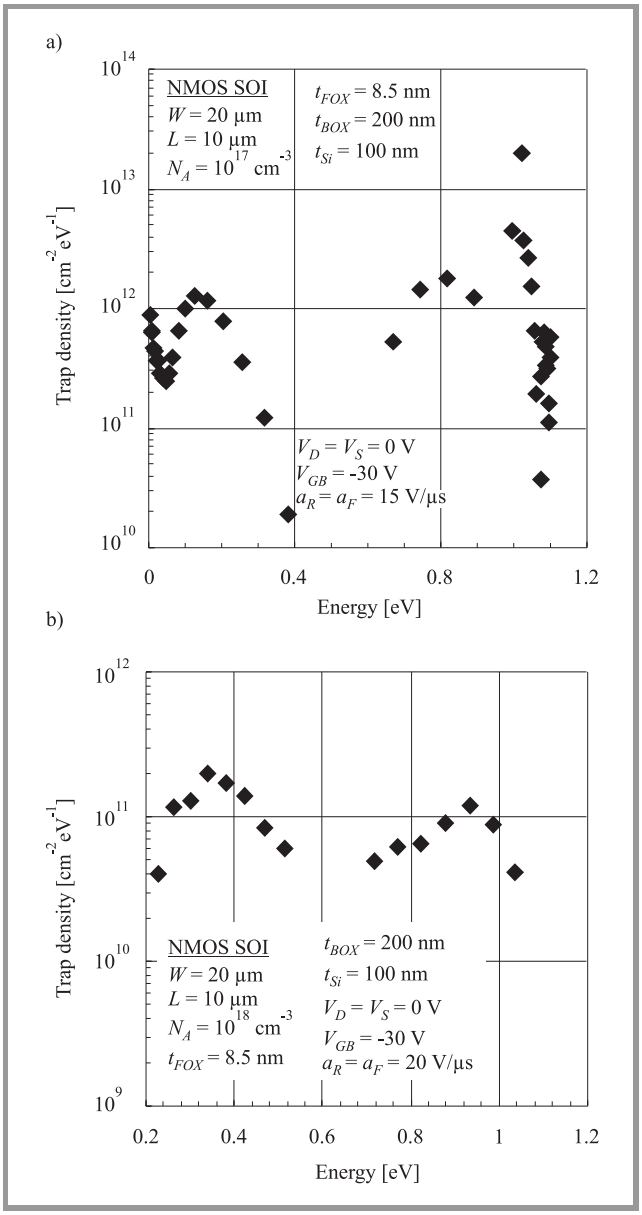

Fig. 7. Energy distribution of interface traps obtained from 3-level CP measurements: (a) $N_{body} = 10^{17}$ cm^{-3}; (b) $N_{body} = 10^{18}$ cm^{-3}, annealed.

back-interface does not contribute to charge-pumping current.

Formula (1) indicates that flatband voltage value is needed to obtain the relation between gate voltage and surface potential. The standard way to determine flat-band voltage from 2-level charge-pumping measurements is to find the front-gate base voltage at which the falling edge of the CP curve reaches half maximum (approximately, -0.5 V in this case). However, if this value is assumed for 3-level charge-pumping, the obtained results have no physical meaning. This is no surprise as the method of establishing V_{FB} value considered here is only a rough guess. Since the Authors of this paper had no other means to find the true value of V_{FB}, the process of determining trap energy levels was carried out for different values of flatband voltage until the region where no meaningful measurement results could be obtained coincided with the vicinity of midgap (trap time constants near midgap are very long, therefore CP current is too small to be measured accurately). This situation occurred at $V_{FB} = -0.98$ V. It may be seen in Fig. 3 that the transition between the flat part and the falling edge of the CP curve takes place at approximately this voltage.

The obtained energy distribution of interface traps is illustrated in Fig. 7. The region between 0.4 and 0.6 eV is too close to midgap to be measured using 3-level CP.

A similar energy distribution of interface traps is shown in Fig. 7a for annealed structures with body doping of 10^{18} cm^{-3}. In this case obtaining meaningful results requires assuming that flat-band voltage is -0.7 V (instead of -1.0 V extracted from 2-level CP measurements). It may be seen in Fig. 3b that -0.7 V is a voltage at which CP current practically falls to zero.

In view of the above energy distribution of interface traps presented in Fig. 7 may only be treated in qualitative terms. Further studies are required to develop an efficient method of V_{FB} extraction suitable for 3-level charge-pumping.

4. Summary

Charge-pumping measurements were performed on SOI MOS transistors with different body doping and subjected to different thermal processing. It was found that in all investigated structures the total density of interface traps at the back-interface was lower than that at the front-interface. This is probably due to the fact that the investigated devices were damaged before saturation of back-interface CP current could be obtained. It was found that annealing in N_2/H_2 at 400°C had a very positive effect on the quality of both front- and back-interface. Values of threshold voltage extracted from CP curves are in qualitative agreement with those obtained from transfer characteristics of drain current. Preliminary results of 3-level charge-pumping were presented, however further studies are needed to develop an appropriate method of flat-band voltage extraction suitable for this characterization technique.

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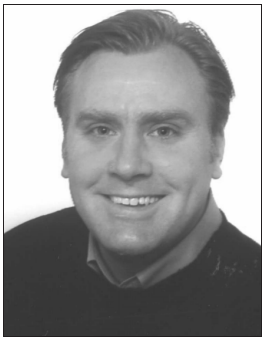

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Grzegorz Głuszko – for biography see this issue, p. 8.

Lidia Łukasiak – for biography see this issue, p. 65.

Paper

Charge-pumping characterization of FILOX vertical MOSFETs

Grzegorz Głuszko, Lidia Łukasiak, Enrico Gili, and Peter Ashburn

Abstract—This paper presents for the first time the results of charge-pumping (CP) measurements of FILOX vertical transistors. The aim of these measurements is to provide information on the density of interface traps at the Si-SiO_2 interface fabricated in a non-standard process. Flat-band and threshold voltage, as well as density of interface traps are determined. Good agreement between threshold-voltage values obtained from CP and *I-V* measurements is observed.

Keywords—charge-pumping, FILOX, interface traps, MOSFET, vertical MOSFET.

1. Introduction

Vertical transistors (VMOSFETs) offer increased packing density when compared to standard CMOS transistors at a defined technology node (e.g., [1]). So far several papers have appeared discussing the structure of a vertical transistor, fabrication method and performance (e.g., [2–4]). In terms of electrical characterization the analysis of standard *I-V* and *C-V* characteristics has been presented only.

Therefore, the aim of this paper is to address for the first time the issue of interface traps in vertical transistors through charge-pumping studies. While charge pumping measurements of power double-diffused vertical transistors (VDMOSFET) have been reported in, e.g., [5], the devices investigated in that work are totally different from those studied in this paper.

2. Experimental

The devices were fabricated by the University of Southampton using the self-aligned fillet (or spacer) local oxidation (FILOX) that enables a thin second field oxide to be grown in the active area without oxidizing the sidewalls of the pillars. For details of the fabrication process (see [6]).

Process flow and a schematic cross-section of the device with surround gate are shown in Fig. 1a. A photo of the device is presented in Fig. 1b. Vertical transistors with two different values of gate oxide thickness (7 nm and 4 nm) were investigated.

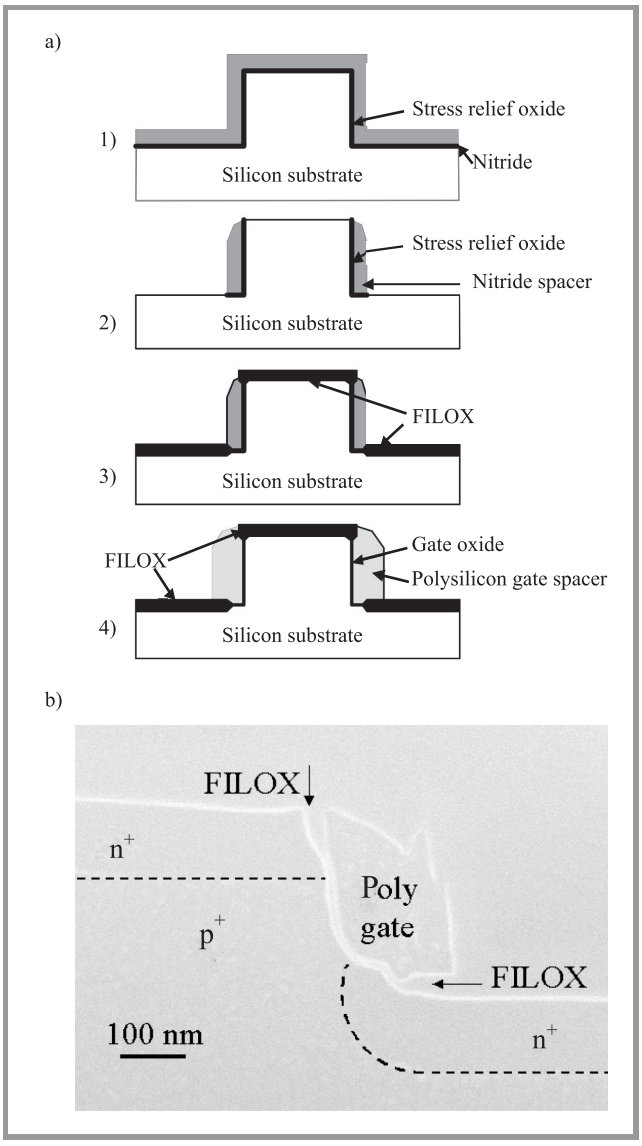

Fig. 1. Vertical MOSFET: (a) process flow and schematic cross-section of a FILOX; (b) photo of the device.

3. Results of electrical characterization

3.1. Analysis of I-V characteristics

A family of output characteristics measured on MOSFETs with the same channel dimensions but gate oxide thickness

of 7 nm and 4 nm is shown in Fig. 2. It may be seen that the saturation drain current of 4-nm VMOSFETs is more than an order of magnitude higher than that of devices with 7-nm oxide at the same gate voltage. While significant

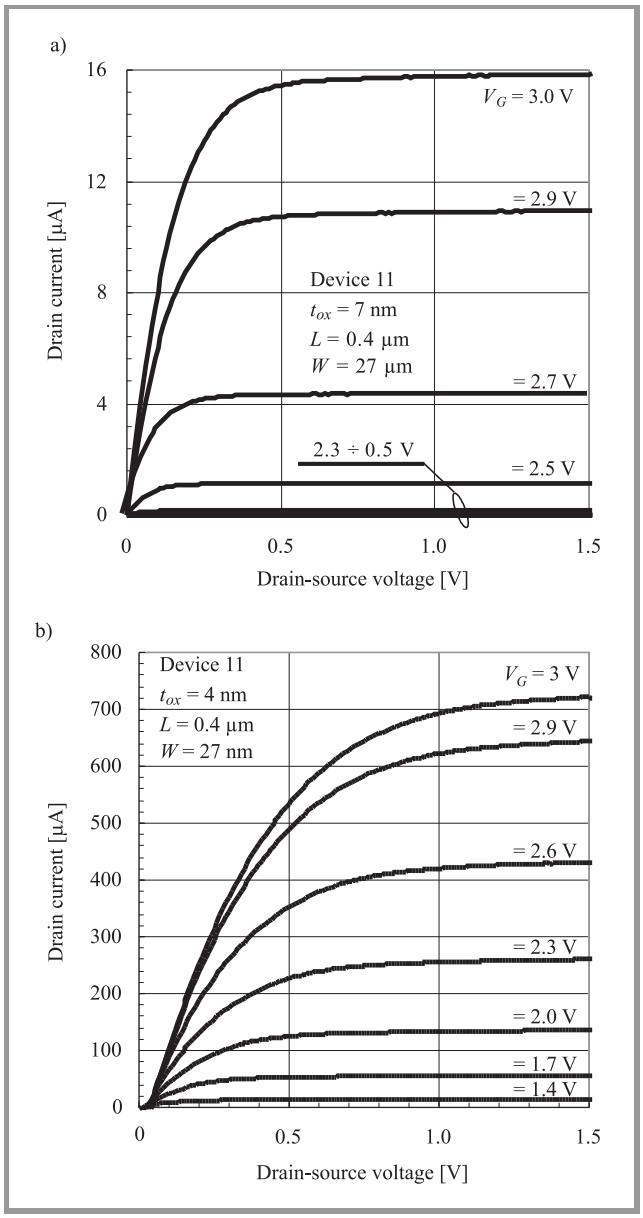

Fig. 2. Output characteristics of a FILOX vertical MOSFET: (a) $t_{ox} = 7$ nm; (b) $t_{ox} = 4$ nm.

enhancement of drain current is a positive consequence of the reduction of gate-oxide thickness, considerable increase of gate current is not. In Fig. 3 transfer characteristics of 7-nm and 4-nm VMOSFETs are shown, respectively, with gate current added for comparison. As seen, gate current is practically negligible in the case of 7-nm VMOSFETs, whereas for 4-nm devices it is comparable to the drain current in the above-threshold region and much higher in the subthreshold region (Fig. 3b). Thus, in terms of leakage current the quality of 4-nm gate oxide is much worse than that of the 7-nm oxide. Threshold voltage determined from

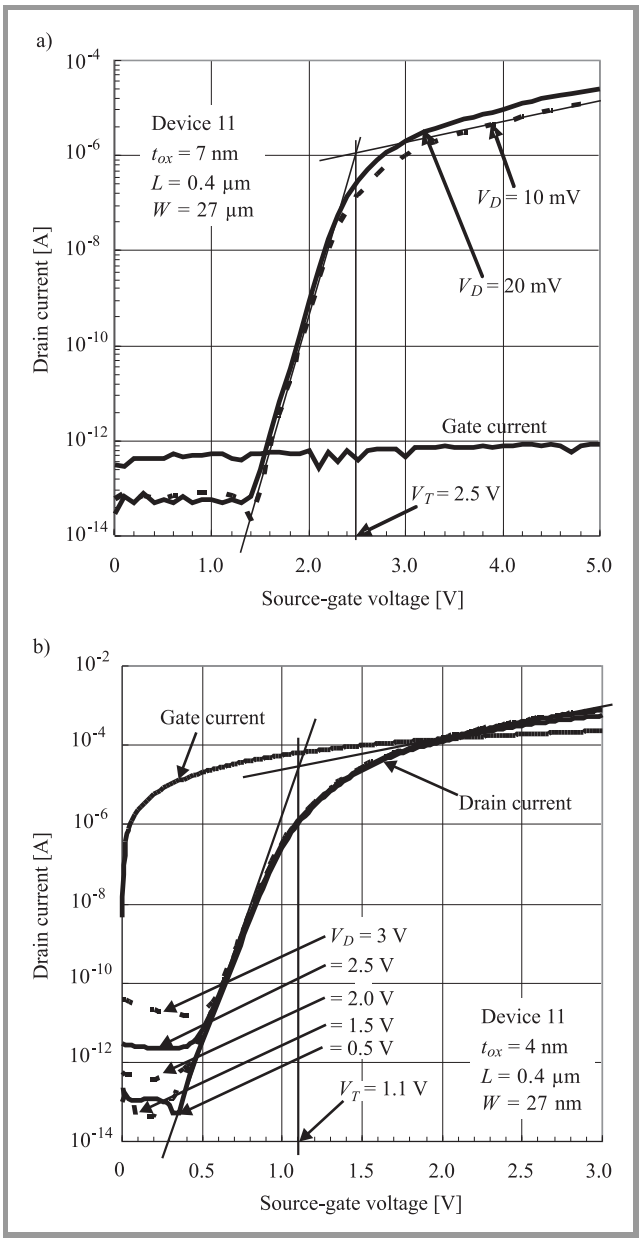

Fig. 3. Transfer characteristics: (a) of a 7-nm FILOX vertical MOSFET; (b) of a 4-nm FILOX vertical MOSFET.

the linear region and from transfer characteristics plotted in logarithmic-linear scale is approximately 2.4 V and 2.5 V for devices with 7-nm oxide and around 1.1 V for 4-nm VMOSFETs.

3.2. Charge-pumping measurements

Charge-pumping (CP), in its numerous forms, yields information on the density, energy levels and other properties of interface traps. Its main advantage is the fact that the device under test is a MOSFET, therefore no special test structures have to be fabricated. The method consists in switching the transistor between accumulation and strong inversion and measuring the DC substrate current that is caused by carrier recombination in interface traps.

The maximum charge-pumping current $I_{cp\max}$ is a measure of interface-trap density according to [7]:

$$I_{cp\max} = A_G q f N_{it}\,, \tag{1}$$

where: A_G – gate area, q – elementary charge, f – gate-signal frequency, N_{it} – total density of interface traps per unit area.

Equation (1) indicates that the maximum charge-pumping current is proportional to gate-signal frequency. Therefore the straight line obtained in Fig. 4 for devices with gate-oxide thickness of 7 nm indicates that the measured current is, indeed, related to charge-pumping. Similar results have been obtained in the case of 4-nm VMOSFETs.

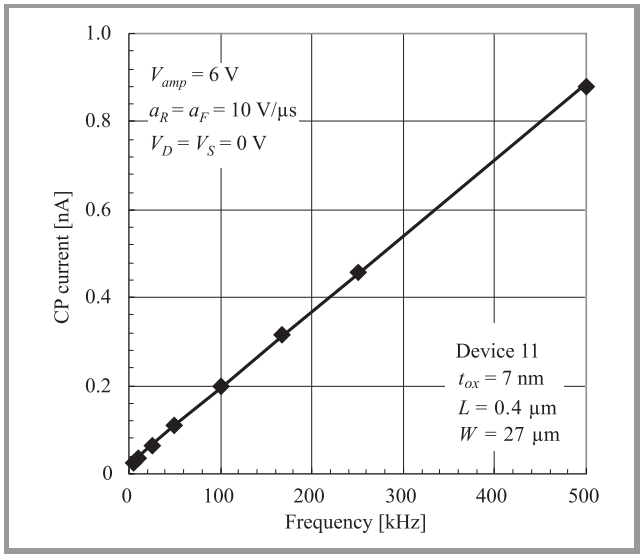

Fig. 4. Maximum charge-pumping current as a function of frequency ($t_{ox} = 7$ nm).

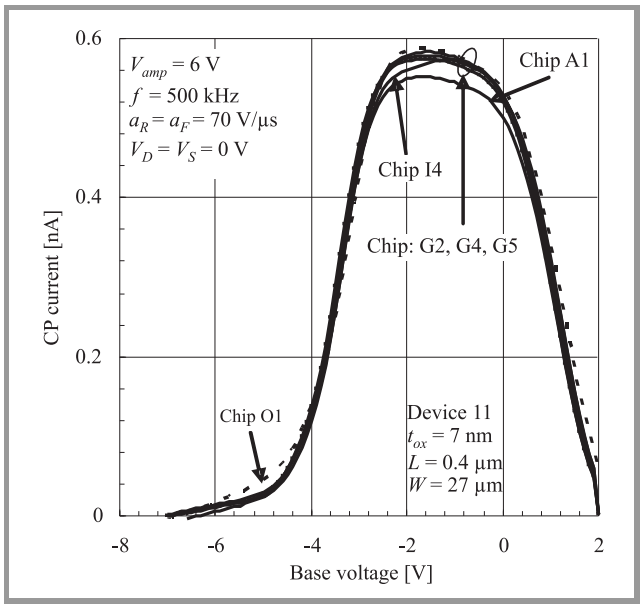

Fig. 5. Charge-pumping current as a function of base voltage for transistors located in several different chips ($t_{ox} = 7$ nm).

Charge-pumping current measured as a function of base voltage on transistors located in different chips (but all with the same gate dimensions) is shown in Fig. 5 for gate-oxide thickness of 7 nm. The results are comparable for all measured devices, which indicates good spatial uniformity of the fabrication process. In the case of 4-nm VMOSFETs the discrepancies between CP curves obtained from devices located at different chips are higher.

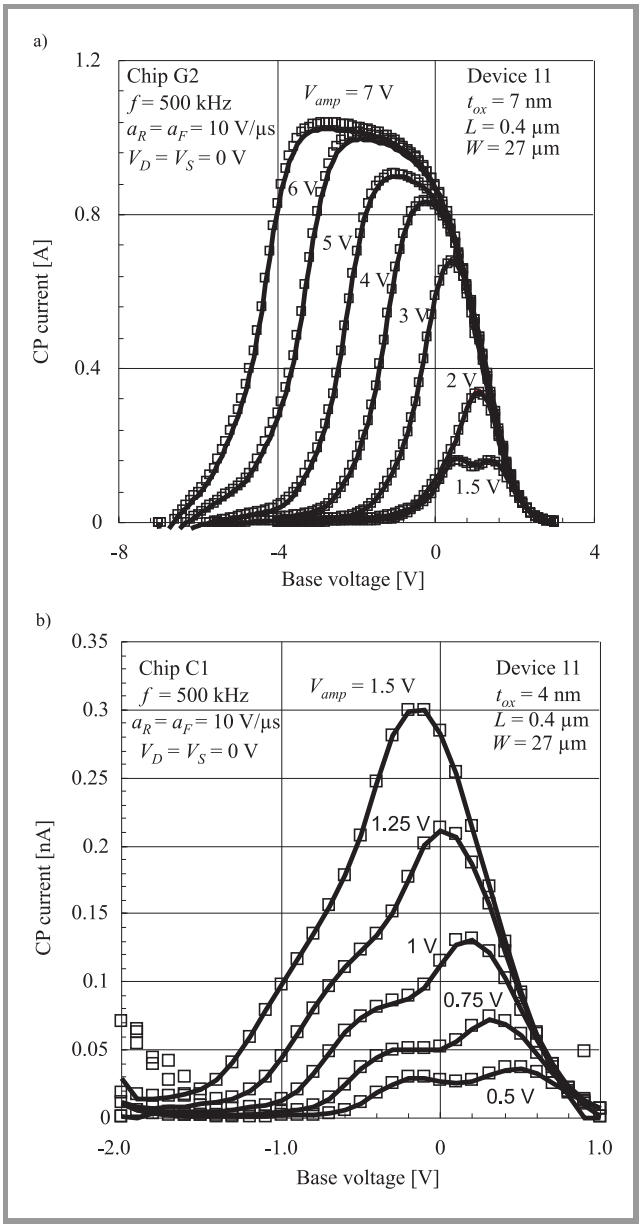

Fig. 6. Charge-pumping current as a function of base voltage with gate-signal amplitude as a parameter (a) $t_{ox} = 7$ nm; (b) $t_{ox} = 4$ nm. The results of repeated measurement are marked as squares.

The results of CP current measurements as a function of base voltage with gate-signal amplitude as a parameter are presented in Fig. 6 for gate-oxide thickness of 7 nm and 4 nm. In the first case the amplitude of the gate signal was successively increased from 1.5 V to 7 V and then

the whole measurement sequence was repeated once. The only difference in the case of $t_{ox} = 4$ nm was that the amplitude varied between 0.5 V and 1.5 V. The results of the first measurement sequence are represented by solid lines, while those of the second sequence by empty squares. Since the difference between the results obtained in either sequence is little, it may be concluded that measurements did not cause visible generation of interface traps. It should be noted that transistors with $t_{ox} = 7$ nm did not break down even at high electric fields in the gate oxide (> 10 MV/cm), while those with $t_{ox} = 4$ nm were damaged at lower electric fields. This indicates again that the quality of the 4-nm oxide is worse than that of the 7-nm one. This is probably the reason for our failure to obtain saturation of the maximum CP current with increasing amplitude for $t_{ox} = 4$ nm.

Comparison of the curves obtained at gate-voltage amplitude of 1.5 V and shown in Fig. 6 for devices with gate-oxide thickness of 7 nm and 4 nm, respectively, indicates that the maximum CP current is lower in the case of $t_{ox} = 7$ nm. The possible reasons for this effect are:

- lower density of interface traps for $t_{ox} = 7$ nm (better quality of the SiO_2-Si interface);
- smaller part of the energy gap is investigated in devices with 7-nm oxide (surface potential is a weaker function of gate voltage than in the case of 4-nm oxide);
- switching the devices with 7-nm oxides between accumulation and strong inversion is more difficult at such low amplitudes because their threshold voltage is higher than that of transistors with 4-nm oxide.

Comparison at higher amplitudes of gate voltage could not be made due to breakdown of the latter devices.

In the case of n-channel devices the location of the rising edge of the CP curve brings information on the value of the threshold voltage V_T (shifted in the direction of lower values by gate-voltage amplitude), whereas the location of the falling edge is a straight indication of the flat-band voltage V_{FB} [8]. The obtained values of the flatband and threshold voltage of a device with gate-oxide thickness of 7 nm are shown in Fig. 7 as a function of gate-signal amplitude. The value of flat-band voltage is approximately 1 V, and a weak dependence on gate-voltage amplitude is observed. If the amplitude is sufficiently high, the values of threshold voltage saturate at the level of 2.6 V, which is in very good agreement with values obtained from *I-V* curves. It should be noted, however, that saturation of the CP curve would be expected in this case at gate-voltage amplitudes of $2-3$ V, while in reality amplitudes of at least $5-6$ V are required. The explanation of this phenomenon is not known at this stage.

In the case of device with $t_{ox} = 4$ nm both flat-band and threshold voltage are strong functions of gate-voltage amplitude. This again is most probably due to the fact that no saturation of the maximum CP current could be obtained for those devices.

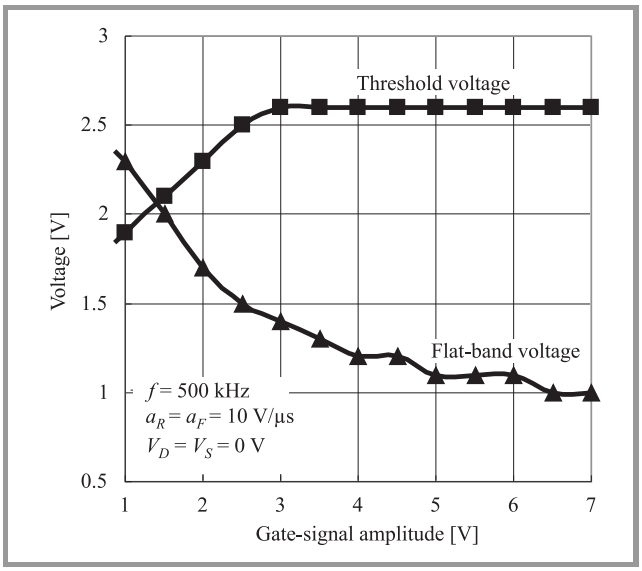

Fig. 7. Flat-band and threshold voltage as a function of gate-signal amplitude ($t_{ox} = 7$ nm).

As it had been mentioned before, the maximum charge-pumping current is used to determine the total density of interface traps N_{it}. Since it was not possible to obtain well-behaved CP curves in the case of $t_{ox} = 4$ nm, only devices with gate-oxide thickness of 7 nm are considered here. Interface trap density N_{it} measured for devices with different channel width varies between $1.3 \cdot 10^{11}$ cm^{-2} to 10^{12} cm^{-2} in a random manner. The reasons for these variations are not known at this stage.

4. Conclusions

Charge-pumping measurements were performed for the first time on FILOX vertical transistors. Well-behaved CP curves were obtained in the case devices with gate oxide thickness of 7 nm, whereas no saturation of CP current was obtained for VMOSFETs with $t_{ox} = 4$ nm, most probably due to high gate leakage current. For devices with $t_{ox} = 7$ nm values of flatband and threshold voltage, as well as total density of interface traps, were determined. Threshold-voltage values were in good agreement with those obtained from *I-V* curves. Further studies are required to explain why considerably higher gate-voltage amplitudes than indicated by V_T and V_{FB} values are needed for the CP current to saturate, and why interface trap density varies for devices with different channel length.

Acknowledgements

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Grzegorz Głuszko – for biography see this issue, p. 8.

Lidia Łukasiak – for biography see this issue, p. 65.

Paper

Arbitrary waveform generator for charge-pumping

Marcin Iwanowicz, Zbigniew Pióro, Lidia Łukasiak, and Andrzej Jakubowski

Abstract—The paper presents a new signal generator for charge-pumping. Modular structure of the generator is discussed with special emphasis on signal-generation module consisting of five independent signal channels. Digital signal synthesis is chosen to minimize inaccuracies. Noise analysis is performed to demonstrate the validity of the design of signal channel. Calibration procedure is also discussed.

Keywords— arbitrary waveform generator, calibration, charge-pumping, digital synthesis, noise.

1. Introduction

A new signal generator for charge-pumping (CP) is presented. Charge-pumping is one of the most versatile methods to estimate the quality of the Si-SiO_2 interface of MOS structures. It enables determination of such parameters as: average density of interface traps, energy distribution of interface traps and capture cross-sections, distribution of interface traps along the channel, rough estimation of flat-band and threshold voltages. New generations of MOS structures impose new requirements on CP measurements. For example, due to reduced gate-oxide thickness, gate-voltage amplitude has to be lower, thus voltage resolution becomes of importance.

2. Charge-pumping

Charge-pumping is widely used to characterize interface traps in MOS devices. It consists in measuring substrate DC current induced by repeated switching of a MOS transistor between strong inversion and accumulation as shown in Fig. 1. The main component of the measurement set-up is signal generator. The main task of this generator is to provide gate pulses that switch the investigated structure between accumulation and strong inversion, but also to generate appropriate bias voltages for the source and drain, and possibly for the back gate of silicon-on-insulator (SOI) devices. The density of interface traps is described as [1]:

$$D_{it} = \frac{I_{cp}}{qAf\Delta E}, \qquad (1)$$

where: I_{cp} – measured charge-pumping current, q – elementary charge, A – gate area, f – gate signal frequency, ΔE – energy range of traps participating in charge-pumping.

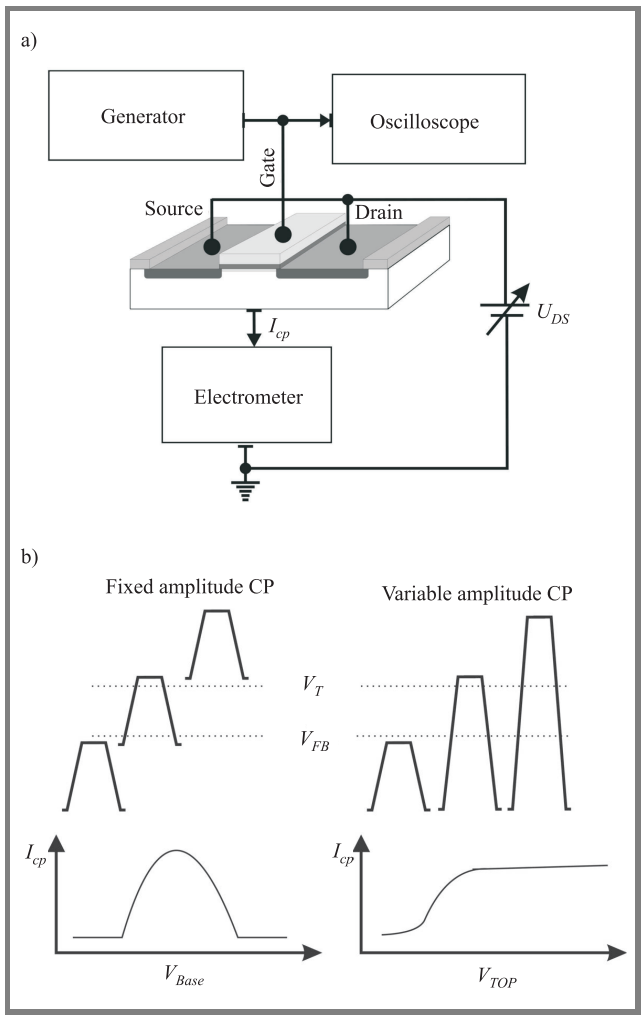

Fig. 1. The principle of charge-pumping: (a) measurement setup, (b) charge-pumping current versus base voltage [11].

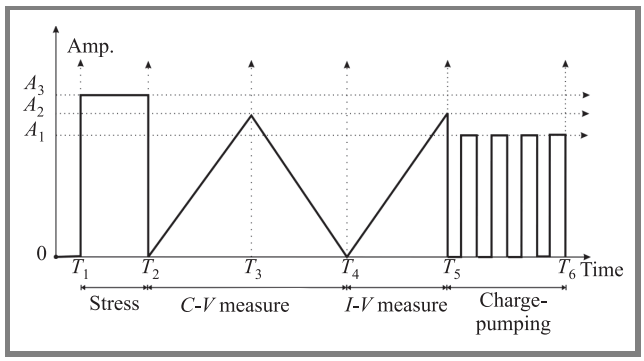

Fig. 2. Waveform of the applied voltage versus time for a "stress and sense" measurement [11].

Many different versions of charge-pumping method have been developed, such as [1, 2]:

- two-level method (square pulses) with constant amplitude, gate-voltage base level or top level;
- two-level method (trapezoidal pulses) with variable rising/falling time;
- two-level method (symmetrical or non-symmetrical triangular pulses) with variable frequency;
- three-level method (square pulses with additional middle level) with variable pulse duration;
- and "stress and sense", composition (see Fig. 2) charge-pumping and other methods (*C-V*, *I-V*) with pulse stress [11].

3. Generator parameters

The available generators have usually high output noise (up to 70 mV_{pp}) [3]. The obtained measurement results are therefore averaged over several kT/q, which may shade the details of the shape of the measured quantity. This undesirable effect may be further intensified by low resolution and very low precision.
The generator must provide several synchronous multiphase voltage signals. In the case of a typical SOI structure at least four channels are necessary: two for independent biasing of source and drain and two for front and back gate. A fifth channel is added for future applications. The electrical parameters of the generator should be suitable for measurement of modern semiconductor devices with small geometry and thin gate dielectric. It should be remembered, though, that the final values of these parameters are, to a large extent, determined by electronic components used to build the generator (DAC, FPGA, etc.). The parameters of the presented generator are shown in Table 1.

Table 1
Basic parameters of the generator

Parameters	Values
Number of channels	5
Maximum rising/falling rate of the output voltage	10^8 V/s (100 V/1 μs)
Output voltage range	$\pm$5 V_{pp} (into 50 Ω) $\pm$10 V_{pp} (into open circuit)
Phase duration	min –50 ns max –20 s
Triggering	internal and external
Trigger pulses for other equipment	2 per channel
Voltage resolution	0.15 mV (into 50 Ω) 0.30 mV (into open circuit)
Resolution of phase duration	5 ns
Noise (with 50 Ω load)	$\pm$1 mV_{RMS}

4. Arbitrary waveform generator (AWG)

In the vast majority of cases charge-pumping does not require truly arbitrary signals but vector ones [4]. Limiting the generator to this class of signals results in considerable simplification of the design and enables digital synthesis to be used to shape the output signal.
The generator consists of three modules: main module, power module and signal-generation module (5 channels), see Fig. 3 [4]. They have been defined to ensure the highest possible autonomy of each module. In this way the amount of data exchanged between modules is minimized.

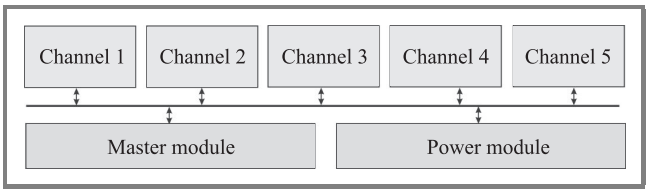

Fig. 3. Diagram of signal generator.

The task of the main module is to ensure communication between the channels of the signal-generation module and the outside world (usually a PC). Moreover, the module checks and updates the status of each channel of the signal-generation module. The role of the power module is obvious. It provides the supply bias necessary for the operation of the whole device. The signal-generation module (5 channels) is the most important module of the generator as it produces the desired signals necessary for characterization of semiconductor devices. Each channel is in the form of EURO CARD 3U.

4.1. Main module

The main module programs/controls all signal channels as well as provides communication between the generator and external computer. The module reads the status of each signal channel and sends this information to the computer. It also reads the information on signal parameters from the computer and sends it to the appropriate signal channel. The generator is seen by the computer as a USB mass-storage device.

4.2. Power module

The power module provides supply bias necessary for correct operation of the whole generator. It protects the generator from overvoltage and monitors the supply bias. In the case of inappropriate supply bias the module may turn the generator off to avoid damage.

4.3. Signal-generation module

As it was mentioned before, the signal-generation module consists of 5 independent signal channels. A channel consists of (Fig. 4.):

- synthesis block (FPGA structure);
- analog block;
- control block with SiLabs C8051F064 microcontroller;
- calibration circuit with two analog-to-digital converters (ADC) integrated in the microcontroller.

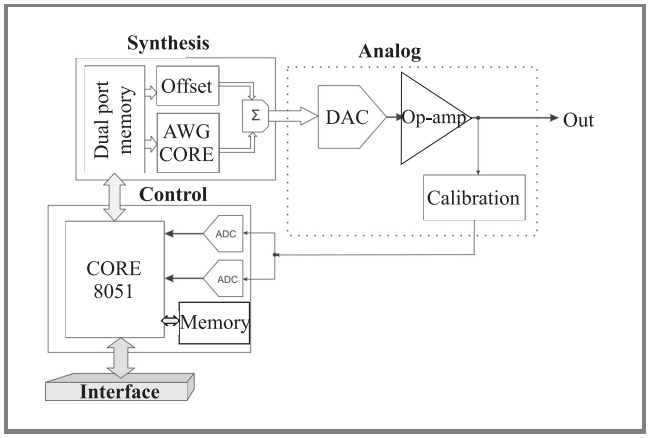

Fig. 4. Block diagram of the signal channel.

4.3.1. Synthesis block

As it was mentioned before, the class of the generated signals was narrowed to vector signals. Therefore each phase of the generated signal may be described with three parameters, i.e., offset, duration and slope (in the case of constant voltage the slope is zero).

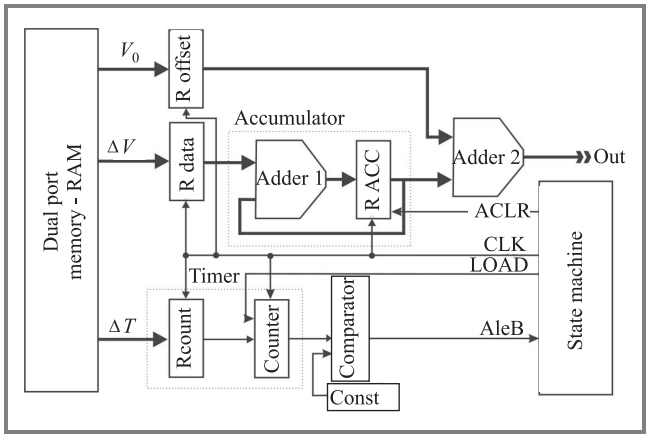

Fig. 5. Diagram of the synthesis block.

Signal synthesis is performed using two components: an accumulator and a timer (Fig. 5). Synthesis of a ramp phase of the pulse consists in adding an appropriate voltage increment ΔV to the accumulator every elementary time increment ΔT (period of CLK clock) until the timer signals the end of the phase. In the case of a constant voltage the value contained in the accumulator does not change [4]. The signal may be additionally modified by an offset voltage V_0. To ensure smooth transition between signal phases, the control block starts preparation of the next phase a certain period of time (9 clock periods) before the current phase is completed. This is achieved by means of comparing the time measured by the timer with the phase duration as shown in Fig. 5. The accumulator data is 32-bit long with the upper 16 bits representing the integer part of the voltage to be obtained and the lower 16 bits representing the fractional part. Only the upper 16 bits are connected to the digital-to-analog converter (DAC) input, therefore the errors associated with addition do not exceed 1LSB.
The input data for the offset, accumulator and timer (V_0, ΔV and ΔT in Fig. 5) are held in a dual-port RAM (Fig. 6). The memory receives data describing the signal

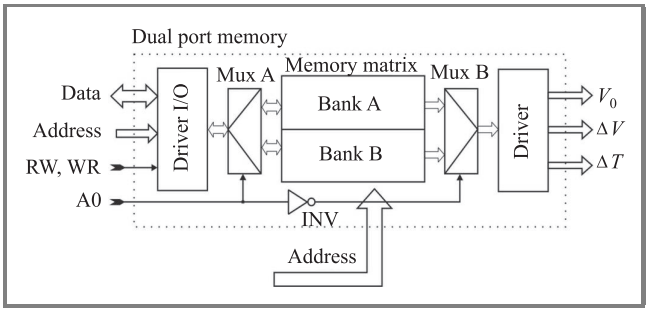

Fig. 6. Diagram of dual-port static RAM.

to be generated from external circuits and provides this data to the signal-synthesis block. Due to the fact that the memory is equipped with two ports, the accumulator and timer may read the data while the parameters of the new signal shape are written to the memory. The synthesis block was designed and implemented in a CYCLONE FPGA from Altera.

4.3.2. Analog block

The analog block consists of a DAC (with all components necessary to ensure its proper operation) and two operational amplifiers Op1 and Op2 (Fig. 7). The first is operating as a differential amplifier (with gain $G_1 = 2$). The second op-amp is an amplifier output buffer ($G_2 = 5$).
The noise at the output of the DAC results from arithmetic errors (mentioned in the description of the synthesis block), non-linearity, temperature drift and quantization errors. To calculate the total noise at the output of the analog block the noise of both operational amplifiers has to be taken into account. For this purpose we assume that the clock frequency is 200 MHz and bandwidth is 30 MHz.
The RMS noise V_{NA} of the DAC (MAX 5888) resulting form arithmetic errors is 35 μV_{RMS} (1 LSB). Its non-

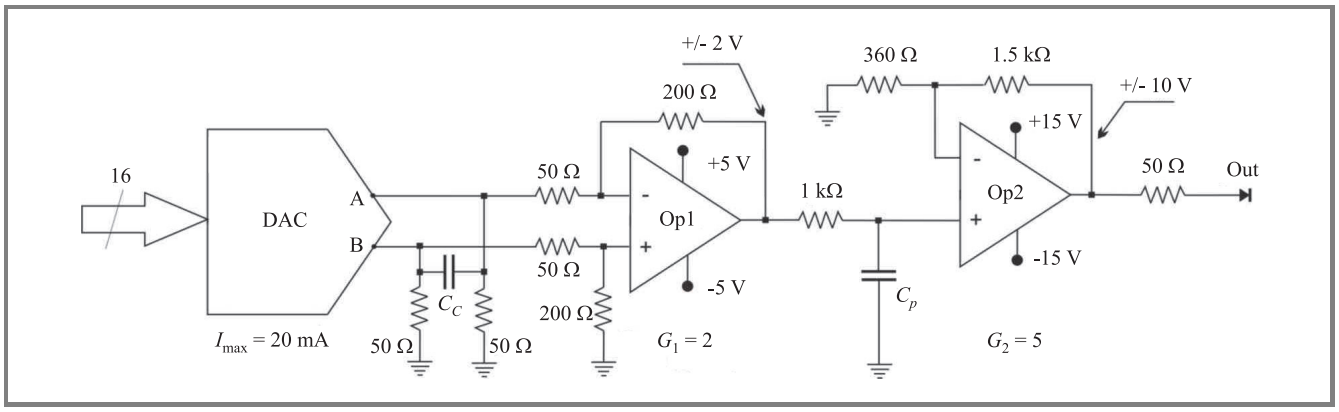

Fig. 7. Circuit diagram of analog block.

linearity V_{NNL} is ±0.003% FS (i.e., ±2 LSB) [5], thus the quantization noise may be estimated as 50 μV_{RMS} (2 LSB). The total RMS noise at the DAC output is therefore:

$$V_{NDAC} = \sqrt{V_{NA}^2 + V_{NNL}^2} = 61\ \mu V_{RMS}\,. \tag{2}$$

To continue noise analysis the circuit illustrated in Fig. 7 should be transformed as shown in Fig. 8. The input components of noise density calculated based on Fig. 8 are listed in Table 2.

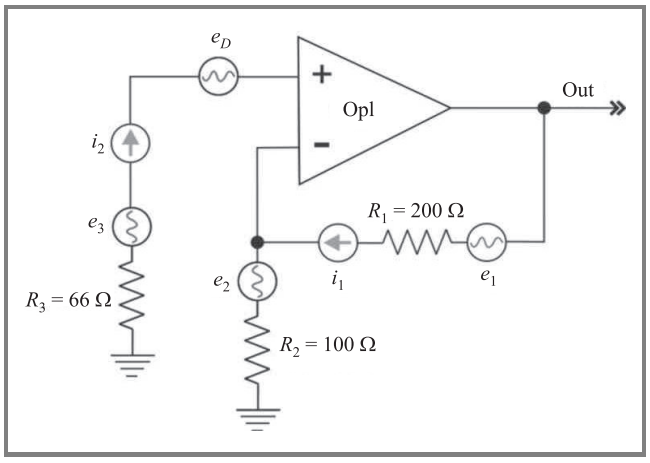

Fig. 8. Analysis of the noise generated by the operational amplifier Op1.

To calculate voltage components of noise density associated with e_1, e_2 and e_3 the widely-known formula was used [6]:

$$V_{Ni} = \sqrt{4kTR_iB}, \tag{3}$$

where: k – the Boltzmann constant, T – absolute temperature [K], R_i – resistance, B – bandwidth [Hz].

It is assumed that current components of noise density associated with i_1 and i_2 are 1 pa/$\sqrt{\text{Hz}}$ [7] and the voltage component of noise density associated with e_D is 5.2 nV/$\sqrt{\text{Hz}}$ [8]. The noise density components identified in Fig. 8 are listed in Table 2.

Table 2
Noise density components
($T = 20°C$, $B = 30$ MHz, $G_{Op1} = 2$)

Input component of noise voltage/current	Noise density before amplification	Gain factor of input components of noise density	Noise density at output [nV/$\sqrt{\text{Hz}}$]
$e_D = \text{Op1}_{NOISE}$	5.2 nV/$\sqrt{\text{Hz}}$	$G = 2$	10.4
e_3	1.2 nV/$\sqrt{\text{Hz}}$	$G = 2$	2.4
e_2	1.4 nV/$\sqrt{\text{Hz}}$	$G-1 = 1$	1.4
e_1	2 nV/$\sqrt{\text{Hz}}$	1	2
i_1	1 pA/$\sqrt{\text{Hz}}$	R_1	0.20
i_2	1 pA/$\sqrt{\text{Hz}}$	$R_3 \cdot G$	~0
Σ			16.4

The total noise density SND_{Op1} at the output of Op1 is 16.4 nV/$\sqrt{\text{Hz}}$ and the total RMS noise is

$$V_{NOp1} = SND_{Op1}\sqrt{B} = 90.18\ \mu V_{RMS}\,. \tag{4}$$

At the output of amplifier Op2 ($G_{Op2} = 5$) one obtains:

$$V_{NOp2} = V_{NOp1}\,G_{Op2} = 450\ \mu V_{RMS}\,. \tag{5}$$

The total noise of the analog block is therefore:

$$V_{Ntotal} = \sqrt{V_{NOp2}^2 + V_{NDAC}^2} = \sqrt{(450)^2 + (61)^2} \approx 455\ \mu V_{RMS}\,. \tag{6}$$

As a result of a 16-bit DAC and appropriate arithmetic the "digital" noise is totally negligible in comparison with the noise generated by the analog part of the block. Since RMS noise at the output of signal generator is ~455 μV_{RMS} we may assume that the accuracy of the generated signal is ±1 mV.

4.3.3. Control block

The control block is based on SiLabs C8051F064 microcontroller equipped with two 16-bit analog-to-digital converters that are used for calibration and on-line correction of the signal. The main task of this block is to provide communication with the main module in the SCPI standard (over internal RS-232 interface).
Moreover, the control block is responsible for preparation of the necessary data for the signal-synthesis block. The parameters of the generated signal are calculated based on the data received from the main module and calibration table and then written to the dual-port RAM implemented in FPGA.

4.3.4. Calibration block

Temperature drifts of the MAX5888 16-bit DAC used in the analog block are quite substantial (offset drift: ±50 ppm/°C, gain drift: ±50 ppm/°C). This means that the accuracy of the generated signal will be less than 14 bits if the temperature changes even by 1°C. If we assume that

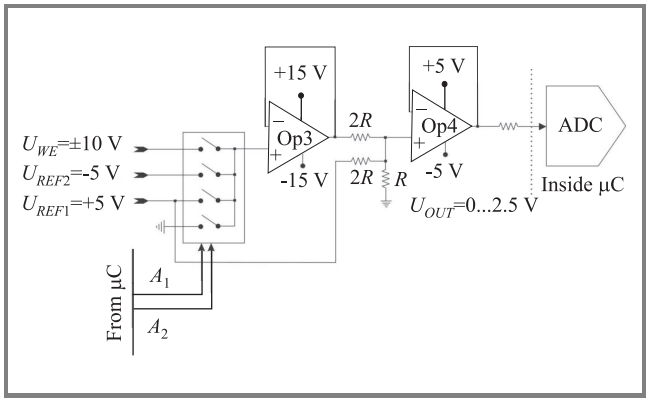

Fig. 9. Circuit diagram of the calibration block.

the output voltage range is 10 V (±5 V) and the accuracy of the generated output voltage is to be ±1 mV, 15-bit resolution is required (total error at the level of 30 ppm). Such parameters may be obtained if at least 16-bit ADC is used for calibration.
The calibration block consists of:

- two 16-bit unipolar analog-to-digital converters integrated in the C8051F064 microcontroller of SiLabs [9];
- precision voltage reference ±5 V VRE405 of THALER CORPORATION with the total thermal drift < 3 ppm/°C [10];
- multiplexer (controlled by the microcontroller) with inputs connected to +5 V reference voltage, −5 V reference voltage, ground and signal taken directly from the generator output (see Fig. 9.);
- voltage-level converter from ±5 V to 0/2.5 V, according to Fig. 9.

Calibration consists of three processes:

Autocalibration – the self-calibration of the calibration block – the inputs of the ADC are successively connected to the minimum and maximum voltage (from reference) and calibration coefficients A_1 and B_1 (see Fig. 10) are calculated based on the obtained results:

$$A_i = \frac{Y_1 - Y_2}{X_1 - X_2}, \tag{7}$$

$$B_i = Y_2 - \frac{(Y_1 - Y_2)X_2}{X_1 - X_2}, \tag{8}$$

where: X_1, X_2 – digital representation of the minimum and maximum voltage (0000h i FFFFh), Y_1, Y_2 – results of conversion. This procedure is performed every time the generator is switched on.

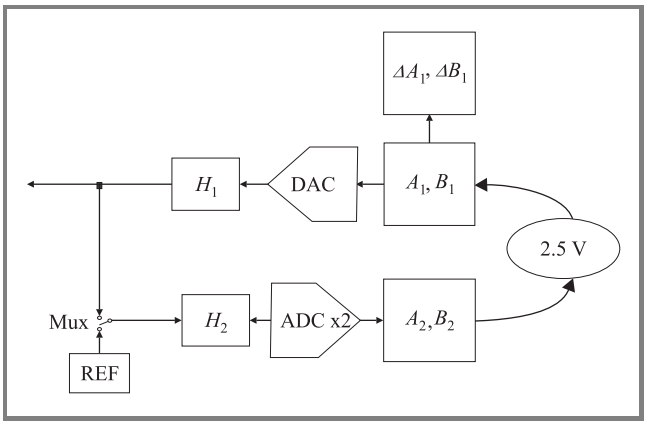

Fig. 10. Diagram of calibration.

Calibration of the analog block – two digital representations corresponding to the extreme values of the voltage range are written to the DAC inputs. The obtained voltages are then measured by the ADC. Calibration coefficients A_2, B_2 (see Fig. 10) are determined as in the previous case with X_1 and X_2 being the values written to the DAC and Y_1 and Y_2 being the values read from the ADC. This routine is performed every time correction indicates the error exceeding a selected threshold (ΔA_1, ΔB_1, see Fig. 10). The generator must be warm and the measurement set-up fixed.

Correction – in-flight calculation of corrections to calibration coefficients. This stage is necessary due to ambient changes (temperature, humidity, etc.). Calibration coefficients are calculated again, the difference being that the digital representations fed to the inputs of the DAC are now the levels of the currently generated signal, not extreme values. One ADC cannot measure two levels of the output voltage because its sampling and conversion time is too long. Therefore, correction is performed by two ADC's. The routine is triggered at user's request at selected levels of the generated signal. If the difference between the previous and current calibration coefficient exceeds an admissible threshold, calibration procedure should be performed.

5. Summary

Progress in the area of semiconductor devices requires measurements with ever smaller voltage amplitudes, therefore digital synthesis is the best way to design a signal generator. Even though a digital generator yields a starcase signal, it is not necessarily worse than a fully analog generator. This is because the quantization noise is almost an order of magnitude lower that the thermal Johnson noise introduced by the components used to build the analog block. Digital synthesis allows the analog block (the biggest source of noise) to be minimized, therefore generators with digital synthesis are pushing analog generators out of the market.

Acknowledgements

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Lidia Łukasiak – for biography, see this issue, p. 65.

Andrzej Jakubowski – for biography, see this issue, p. 7.

Paper

Electron mobility and drain current in strained-Si MOSFET

Jakub Walczak and Bogdan Majkusiak

Abstract— Electron mobility and drain current in a strained-Si MOSFET have been calculated and compared with the mobility and drain current obtained for the relaxed material. In the first step, our mobility model has been calibrated to the "universal mobility" according to the available experimental data for unstrained Si MOSFETS. Then, employing the mobility parameters derived in the calibration process, electron mobility and the drain current have been calculated for strained-Si MOSFETs.

Keywords— electron mobility, strained-Si MOSFET.

1. Introduction

Employing strained Si in MOSFET channel may significantly improve the performance of the device by an increase of electron mobility due to strain-induced alteration of the energy band structure. Therefore, the strained-Si technology is a promising solution for ultra-scaled devices and undergoes an intensive research work along with successful introduction to the market [1].

In this work, electron mobility and drain current for both: a relaxed-Si and a strained-Si MOSFETs have been modeled. In the first step, our mobility model has been calibrated to the "universal mobility" according to available experimental data for unstrained Si MOSFETs [2]. Then, employing the calibrated mobility model with parameters derived in the calibration process, electron mobility for a strained-Si MOSFET has been calculated, and finally, the drain current has been calculated for a strained-Si MOSFET designed as a template device for the SINANO Project Deliverable D4.14 on strained silicon [3].

2. Mobility calculation

According to the idea of this work, our electron mobility model should be calibrated to the "universal mobility" of experimental data for unstrained Si MOSFETs, and then it should be employed to a strained-Si MOSFET, with literally the same mobility parameters as those used to calculate the mobility for the unstrained device. The modeled strained devices should be bulk NMOSFETs with strained-Si channel layer resting on the $Si_{0.8}Ge_{0.2}$ virtual substrate.

Our electron mobility model is based on the relaxation time approximation, including the mobility components limited by the phonon scattering, the Coulomb scattering, and the surface roughness scattering. The effective mobility is calculated by combining these components according to Matthiessen's rule.

First, the potential and carrier concentration distributions have been obtained by self-consistent solution of 1-dimensional Poisson and Schrödinger equations, giving also quantized energy levels and envelope wave functions in the direction z perpendicular to the surface. Figure 1 shows an example of band diagram for a strained-Si bulk MOSFET, illustrating also the distribution of electron concentration, and energy levels along with the eigenfunctions (only the non-primed series of eigenstates is shown). In the calculations open boundaries have been assumed, i.e., the wave functions are allowed to penetrate into the oxide. Band offsets for strained-Si/SiGe interface are calculated according to [4, 5].

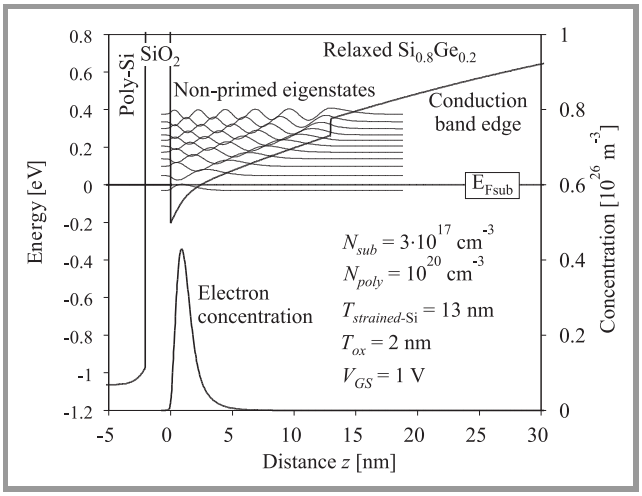

Fig. 1. Energy band diagram for a strained-Si bulk MOSFET.

A silicon layer, when grown on a $Si_{1-x}Ge_x$ substrate, is subjected to biaxial tensile strain, due to a mismatch between lattice constants of the materials under consideration. This strain rearranges the energy band structure within the strained layer. It separates the non-primed series of eigenstates from the primed series, shifting the latter up, thus promoting electron occupation in the non-primed energy subbands, which, in turn, is beneficial for electron mobility, since the transport effective mass for electrons in the non-primed subbands is smaller than for those in the primed subbands. Moreover, due to the separation of the non-primed and primed subbands, the intervalley scattering is significantly suppressed in the strained silicon. Additionally, the strain produces a discontinuity of the conduction band edge at the interface between the SiGe layer and the strained-Si layer, which can be observed in Fig. 1 as a potential step, thus confining the electrons still more within the strained channel layer. The above effects contribute to a significant mobility enhancement and make the strained silicon so attractive as a material for MOSFET channel.

Phonon scattering rates have been calculated within the approximation of isotropic effective acoustic deformation potential, which was assumed to be $D_{ac} = 12$ eV. Moreover, intervalley phonon scattering was included, and a set of phonon parameters was employed which involves a stronger coupling for intervalley phonons [6, 7] than typically used for unstrained silicon [8], and therefore reflects the mobility enhancement observed in strained-Si channels. So, the following intervalley phonons have been included: a single phonon of type-f: $E_k = 59$ meV, $D_k = 8.0 \cdot 10^8$ eV/cm, and a single phonon of type-g: $E_k = 63$ meV, $D_k = 8.0 \cdot 10^8$ eV/cm. No surface optical phonons were considered.

The matrix element for surface roughness scattering includes:

– the component due to the geometrical shift of the potential energy:

$$M_{ij} = \int \xi_i(z)\Delta_{sr} \cdot \mathrm{d}V/\mathrm{d}z(z)\xi_j(z)\mathrm{d}z, \qquad (1)$$

– the components due to the influence of the deviated plane and image potential modification [9].

The screening effect has been applied according to the Thomas-Fermi approximation with the finite extension of the wave function. Exponential spectrum was assumed with $\Delta_{rms} = 0.22$ nm, $\lambda_{sr} = 1.5$ nm.

Screened Coulomb scattering potentials induced by impurities located in the substrate were found by numerical solution of Poisson's equation [10–12] across the semiconductor and the oxide (infinite oxide thickness assumed), see Eqs. (2) and (3). No interface states and remote charges have been included:

$$\phi_{Si}(q,z,z_0) = \int_0^\infty \mathrm{d}z_1 \phi_{Si}(q,z_1,z_0)$$

$$\times\left\{-\sum_i |\xi_i(z_1)|^2 S_i \int_0^\infty \mathrm{d}z_2 |\xi_i(z_2)|^2 \frac{1}{q}\exp\left(-q|z-z_2|\right)\right\}$$

$$+\frac{2}{2\varepsilon_{Si}q}\exp\left(-q|z-z_0|\right) + A_1\exp\left(-qz\right), \qquad (2)$$

$$\phi_{ox}(q,z,z_0) = \frac{2}{2\varepsilon_{ox}q}\exp\left(-q|z-z_0|\right) + A_2\exp\left(-qz\right). \qquad (3)$$

Figure 2 shows the calculated electron effective mobility as a function of the effective field for unstrained MOSFETs, compared with the experimental universal mobility curve by Takagi *et al.* [2]. Simulations for all substrate doping levels were carried out employing the same scattering parameters mentioned above, calibrated to obtain the best possible fit to the experimental data.

Figure 3 shows a comparison of the dependence of the effective mobility on the effective field for strained MOSFETs and unstrained MOSFETs for doping levels of $3 \cdot 10^{17}$ cm^{-3} and $3 \cdot 10^{18}$ cm^{-3}, while Fig. 4 presents the enhancement of electron mobility obtained in the strained devices relative to the unstrained ones, as a function of the effective field. As can be seen, strain induces a mobility enhancement of the order of several dozen per cent.

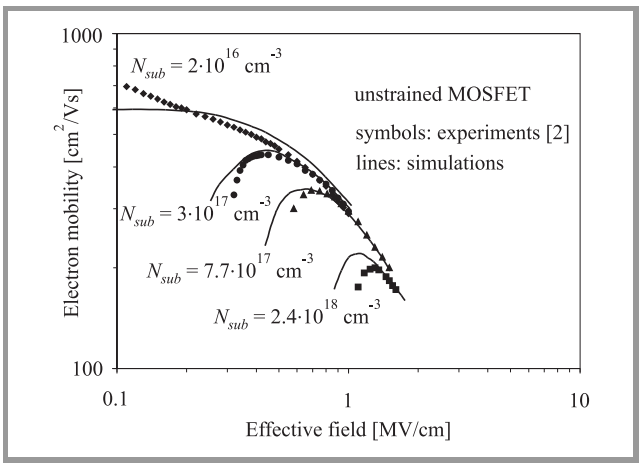

Fig. 2. Effective mobility versus effective field for unstrained MOSFETs.

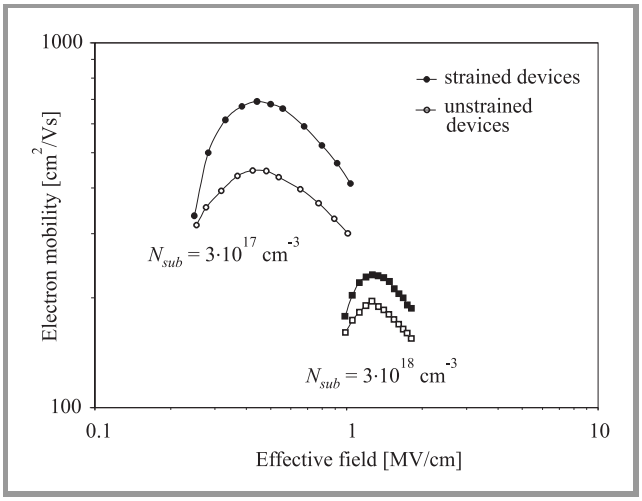

Fig. 3. Effective electron mobility versus effective field for strained and unstrained MOSFETs.

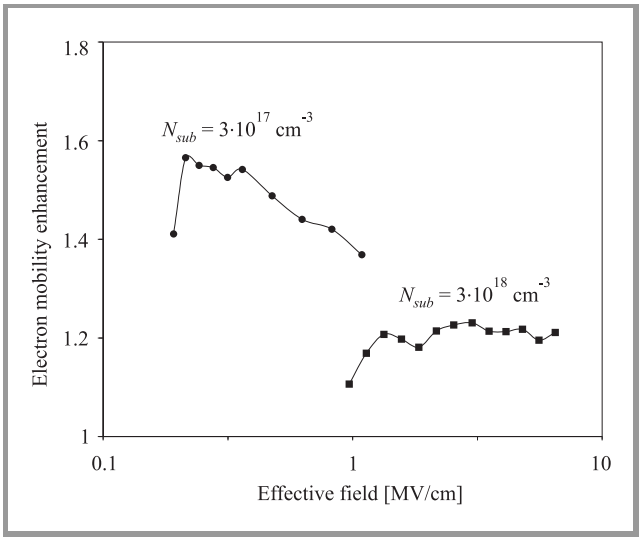

Fig. 4. Electron mobility enhancement versus effective field for two substrate doping levels.

3. Drain current calculation

Having calibrated mobility model, the next step was the calculation of the drain current for an n-channel strained-Si bulk MOSFET, which was designed as a template device for the SINANO Project Deliverable D4.14 on strained silicon. The parameters of the transistors were as follows: channel length $L = 25$ nm, oxide thickness $T_{ox} = 1.6$ nm, oxide dielectric constant $K_{ox} = 7$, acceptor doping level in the channel: $N_{sub} = 3 \cdot 10^{18}$ cm^{-3}. In spite of ultrashort channel to be modeled, we calculated the drain current within the long channel approximation, according to the Pao-Sah model [13], by integration of the product of the electron charge Q_{inv} and the electron mobility μ_{eff} over the quasi-Fermi level split u_n along the channel:

$$I_D = -\frac{W}{L}\frac{\mathrm{k}T}{q}\int_{V_{SB}}^{V_{SB}+V_{DS}} \mathrm{d}u_n\, \mu_{eff}\, Q_{inv}\,. \tag{4}$$

The current was calculated in two independent routines. First, the potential and charge distributions along with the energy levels and envelope functions were obtained and stored for all desired gate voltages and quasi-Fermi level splits related to the considered source-drain voltages. Next, the stored data were post-processed in order to calculate electron mobilities and carry out the integration according to the drain current model.

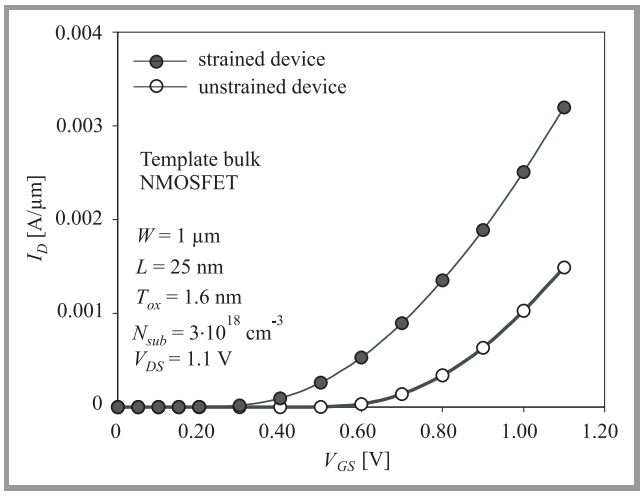

Fig. 5. Transfer characteristics for the unstrained (open symbols) and strained NMOSFETs (closed symbols).

Figure 5 shows an example of the calculated drain current transfer characteristics obtained for the drain-source voltage of 1.1 V. As a consequence of the mobility enhancement, an enhancement of the drain current is obtained for the strained-Si MOSFET.

4. Conclusions

In this work electron effective mobility and drain current for both strained-Si MOSFETs and unstrained MOSFETs have been calculated. Significant enhancements of the mobility and the current have been obtained, resulting from the biaxial tensile strain in the channel layer.

Acknowledgements

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Paper

Modeling of the inverse base width modulation effect in HBT transistor with graded SiGe base

Agnieszka Zaręba, Lidia Łukasiak, and Andrzej Jakubowski

Abstract—A model of the position of the edge of emitter-base junction in the base and collector current pre-exponential ideality factor in HBT transistor with a SiGe base is presented. The model is valid for transistors with nonuniform profiles of doping and Ge content. The importance of taking into account the dependence of the effective density of states in SiGe on local Ge content and that of electron diffusion coefficient in SiGe on drift field for modeling accuracy is studied.

Keywords— heterojunction bipolar transistor, SiGe, base width modulation.

1. Introduction

SiGe heterojunction bipolar transistors (HBT) are widely used in wireless and high-speed digital communications due to their many advantages over Si bipolar junction transistors (BJTs): higher current gain (β), cut-off frequency (f_T) and early voltage (V_A). SiGe HBTs are a low-cost alternative to GaAs technology. Moreover, they offer great flexibility in design of germanium content profile in the base.

In SiGe HBTs band gap grading gives rise to a drift field, which aids the minority carrier transport through the base. However, in transistors with steep Ge grading in the base, collector current (J_C) is more affected (in comparison with BJT) by the so-called "inverse base width modulation effect", e.g. [1]. This effect is connected with the collector current dependence on the position of the edge of emitter-base junction space-charge region (SCR) in the base (x_0), which varies with emitter-base voltage (V_{BE}) changes. In the HBT case, this position determines not only the width of electrically neutral base but also the germanium content at x_0. Shrinking of SCR in a forward-biased emitter-base junction increases the effective base width, which in turn lowers J_C. In addition, Ge content at x_0 decreases and so does the difference between emitter and base band gaps. This results in lower injection of minority carriers and lower values of J_C (i.e., β). A collector current pre-exponential ideality factor m is defined as [1]:

$$m = \frac{\mathrm{k}T}{q}\,\frac{1}{J_C}\,\frac{\mathrm{d}J_C}{\mathrm{d}V_{BE}} = 1 - \delta m < 1\,. \tag{1}$$

The inverse base width modulation effect in SiGe-base HBTs has been calculated numerically (e.g., [2]). For transistors with exponential doping profile in the base, an analytical model of m has been presented in [1]. In this model two important effects have been neglected: the dependence of the diffusion coefficient ($D_{n\mathrm{SiGe}}$) on the drift field (F) and the dependence of the effective density of states in SiGe ($N_{V\mathrm{SiGe}}$, $N_{C\mathrm{SiGe}}$) on local Ge content in the base (y_{Ge}). Moreover, this model needs a complicated procedure for determining the position of x_0 involving numerical simulations.

A model of x_0 for AlGaAs HBT with graded base has been derived in [3], but it is only valid for constant base doping. This model is not quite appropriate for SiGe-based HBT case, because of the differences in the energy band diagrams of those two transistor types. Moreover, it assumes constant effective density of states throughout the whole transistor, which is not true for Si/Si$_{1-x}$Ge$_x$/Si structure.

The aim of this paper is to present a new extensive model of x_0 and m. To determine x_0 the Poisson equation is examined with mobile charges in SCR taken into account. Moreover, nonuniform doping and Ge profiles in the base are considered for the first time.

Our model of m incorporates not only high-doping effects and the dependence of band gap and $D_{n\mathrm{SiGe}}$ on local y_{Ge} in the base (similarly to [1]), but also the dependence of the effective density of states in SiGe on $y_{\mathrm{Ge}}(x)$ and the dependence of $D_{n\mathrm{SiGe}}$ on the drift field in the base. Moreover, it is valid for any doping and germanium profiles in the base of HBT.

2. Model

In this paper we focus on n-p-n SiGe-based HBT properties, but the treatment in this section holds for all heterojunctions with nonuniform composition. The only assumption is constant electron affinity ($\chi(x) = \mathrm{const}$) along the whole structure, which is a good approximation for a Si/Si$_{1-x}$Ge$_x$ structure. Moreover, the presented models easily extended to include the dependence of χ on material composition (see, e.g., [3]).

In further considerations material parameters are defined as follows. Intrinsic carrier concentration in the SiGe base is given as [4]:

$$\begin{aligned} n^2_{i\mathrm{SiGe}}(x) &= \gamma(x) n^2_{i0\mathrm{Si}} \exp\left(\frac{\Delta E_{GEFF}(x)}{\mathrm{k}T}\right) \\ &= \gamma(x) n^2_{i0\mathrm{Si}} \exp\left(\frac{\Delta E_{G\mathrm{Ge}}(x) + \Delta E_{GAPP}(x)}{\mathrm{k}T}\right), \end{aligned} \tag{2}$$

where: $n_{i0\mathrm{Si}}$ – intrinsic carrier concentration in pure silicon, ΔE_{GEFF} – the effective band gap narrowing in the base due to the presence of Ge ($\Delta E_{G\mathrm{Ge}}$) and due to heavy doping effects (ΔE_{GAPP}). It is assumed that band gap depends

linearly on y_{Ge} (7.5 meV per 1% of Ge, e.g., [4]). The model of Klaassen-Slotboom-de Graaff [5] was chosen to describe ΔE_{GAPP}. The ratio of the effective density of states in a SiGe base to that in a silicon one is defined in the following way as a function of Ge content (for $y_{Ge} \geq 0.01$) [4]:

$$\gamma(x) = \frac{N_{C\mathrm{SiGe}}(x) N_{V\mathrm{SiGe}}(x)}{N_{C\mathrm{Si}} N_{V\mathrm{Si}}} = \exp\left(-\sqrt{5 y_{\mathrm{Ge}}(x)}\right). \quad (3)$$

We also assume that $N_{C\mathrm{SiGe}} = 2/3 N_{C\mathrm{Si}}$ [6].

The model of intrinsic carrier concentration in Si ($n_{i\mathrm{Si}}$) adopted here takes into account the apparent band gap narrowing due to high doping concentration (ΔE_{GAPP}).

2.1. Position of the edge of emitter-base junction space-charge region in the base (x_0)

The energy band diagram of emitter and base regions of a HBT with exponential doping profile ($N_A(x)$) and linearly graded Ge content ($y_{\mathrm{Ge}}(x)$) in the base and constant doping in the emitter region (N_D) is presented in Fig. 1.

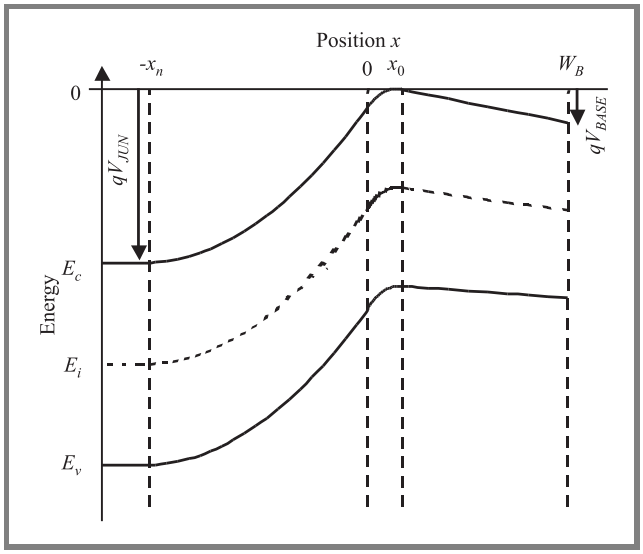

Fig. 1. Energy band diagram of emitter and base of a HBT with exponential doping profile and linearly graded Ge content in the base and constant doping in the emitter region.

As usual, $E_C(x) = -qV(x)$, $E_V(x) = -qV(x) - E_G(x)$. Moreover, we assume that $qV(x_0) = 0$. The built-in potential of the junction is

$$V_{JUN}(x_0) = V(-x_n) - V(x_0) = V_{BJ} - V_{BASE}(x_0), \quad (4)$$

were V_{JB} is the potential drop across the emitter-base junction and the base:

$$V_{JB} = V(-x_n) - V(W_B) = \frac{\mathrm{k}T}{q} \ln\left(\frac{N_A(W_B) N_E}{n_{i\mathrm{Si}}^2}\right) + \frac{E_G(W_B) - E_G(-x_n)}{q} + \frac{\mathrm{k}T}{q} \ln\left(\frac{N_V(-x_n)}{N_V(W_B)}\right) - V_{BE} \quad (5)$$

and V_{BASE} is the potential drop across the base:

$$V_{BASE}(x_0) = V(W_B) - V(x_0) = V(W_B) - 0 = \frac{\mathrm{k}T}{q} \ln\left(\frac{N_A(x_0)}{N_A(W_B)}\right) + \frac{E_G(x_0) - E_G(W_B)}{q} + \frac{\mathrm{k}T}{q} \ln\left(\frac{N_V(W_B)}{N_V(x_0)}\right). \quad (6)$$

For low injection level, it may be assumed that the concentration of majority carrier at SCR boundaries is $p(x_0) \approx N_A(x_0)$ and $n(x_n) \approx N_D(x_n)$. Therefore, the carrier concentration in the base part of SCR $(0 \leq x \leq x_0)$ may be approximated as:

$$p_p(x) = N_A(x_0) \frac{N_V(x)}{N_V(x_p)} \exp\left(\frac{E_G(x_0) - E_G(x) - qV(x)}{\mathrm{k}T}\right), \quad (7)$$

$$n_p(x) = \frac{n_{i\mathrm{SiGe}}^2(x_0)}{N_A(x_0)} \exp\left(\frac{qV(x)}{\mathrm{k}T}\right) \quad (8)$$

and in the emitter part of SCR $(-x_n \leq x \leq 0)$:

$$n_n(x) = N_D \exp\left(\frac{q\big(V(x) - V_{JUN}(x_0)\big)}{\mathrm{k}T}\right), \quad (9)$$

$$p_n(x) = \frac{n_{i\mathrm{Si}}^2}{N_D} \exp\left(\frac{q\big(V_{JUN}(x_0) - V(x)\big)}{\mathrm{k}T}\right). \quad (10)$$

Considering mobile charges in the junction SCR, the standard procedure (e.g., [3]) is applied to solve the Poisson equation for the base and the emitter SCR. As a result the following set of equations is obtained:

$$F(0^+)^2 - F(x_0)^2 = \frac{2\mathrm{k}T}{\varepsilon_{\mathrm{SiGe}}} \left\{ N_A(0) \frac{qV(0)}{\mathrm{k}T} + \big(p_p(0) - N_A(x_0)\big) + \big(n_p(0) - n_p(x_0)\big) \right\}, \quad (11)$$

$$F(0^-)^2 = \frac{2\mathrm{k}T}{\varepsilon_{\mathrm{Si}}} \left\{ -N_D \frac{q\big(V(0) - V_{JUN}(x_0)\big)}{\mathrm{k}T} + \big(p_n(0) - p_n(-x_n)\big) + \big(n_n(0) - N_D\big) \right\}. \quad (12)$$

To relate the electric field to SCR boundaries, we employ the depletion approximation and integrate the Poisson equation once to obtain equations $F(0^-) = f(N_D - x_n)$ and $F(0^+) - F(x_0) = f(N_A(x),\ x_0)$.

Combining the sets of equations described above with the condition that the electric flux density must be continuous, the value of x_0 may be calculated numerically using the Newton method (for more details see, e.g., [3]).

In our model the dependence of the dielectric constant in the base ($\varepsilon_{\mathrm{SiGe}}$) on $y_{\mathrm{Ge}}(x)$ is taken from [7]. Assuming, however, that x_0 is small and $\varepsilon_{\mathrm{SiGe}}$ changes only slightly between $x = 0$ and $x = x_0$, in our calculations we assume that in this region $\varepsilon_{\mathrm{SiGe}} = \mathrm{const} = 0.5\big[\varepsilon_{\mathrm{SiGe}}(0) + \varepsilon_{\mathrm{SiGe}}(x_0)\big]$.

2.2. Collector current pre-exponential ideality factor (m)

The collector current density of a SiGe HBT with arbitrary Ge and doping profiles may be expressed as [8]:

$$J_C = \frac{q\exp\left(\frac{qV_{BE}}{kT}\right)}{\int\limits_{x_0}^{W_B}\frac{N_A(x)}{n_{i\mathrm{SiGe}}^2(x)D_{n\mathrm{SiGe}}(x)}\mathrm{d}x+\frac{N_A(W_B)}{n_{i\mathrm{SiGe}}^2(W_B)v_{SAT}}} = J_{C0}\exp\left(\frac{qV_{BE}}{kT}\right), \tag{13}$$

where: v_{SAT} – saturation velocity of electrons.

The model of $D_{n\mathrm{SiGe}}$ in the SiGe base used in our analysis is described as $D_{n\mathrm{SiGe0}} = D_{nrel}D_{n\mathrm{Si0}}$, where $D_{n\mathrm{SiGe0}}$ is electron diffusion coefficient in SiGe for low drift fields and D_{nrel} is parameter dependent on Ge content [7]. The impurity-concentration-dependent diffusion coefficient $D_{n\mathrm{Si0}}$ in silicon is taken from [9]. The $D_{n\mathrm{SiGe}}$ dependence on the drift field F in SiGe is also defined similarly to the case of silicon [9].

Substituting Eq. (13) into Eq. (1) one obtains:

$$m = \frac{kT}{q}\frac{1}{J_C}\frac{\mathrm{d}J_C}{\mathrm{d}V_{BE}} = 1-\frac{kT}{q}\frac{N_A(x_0)}{n_{i\mathrm{SiGe}}^2(x_0)D_{n\mathrm{SiGe}}(x_0)}\frac{J_{C0}}{q}\frac{\partial x_0}{\partial V_{BE}}. \tag{14}$$

3. Results and discussion

As it was mentioned above, SiGe-based HBTs have many advantages over Si BJTs. In general, Ge gradients in the base are necessary to improve transistor speed, while HBTs with $y_{\mathrm{Ge}}(0) > 0$ have higher current gains. Optimization of $y_{\mathrm{Ge}}(x)$ is beyond the scope of this paper, but we examine some cases of interest from the point of view of emitter-base junction properties.

In the present study, we consider transistors with emitter doping concentration $N_D = 10^{18}$ cm^{-3} and with exponential doping profile in the base: $N_A(0) = 10^{19}$ cm^{-3}, $N_A(W_B) = 5\cdot 10^{17}$ cm^{-3}, $W_B = 30$ nm. Linearly graded Ge profiles with different $y_{\mathrm{Ge}}(0)$ and $y_{\mathrm{Ge}}(W_B)$ (meaning also different gradients) are considered.

First of all, we examine the model of x_0. This parameter was calculated for $V_{BE} = 0.3$ V in three ways:

- assuming depletion approximation in SCR;
- considering mobile charges in SCR and assuming that the effective densities of states in SiGe are the same as those in Si ($\gamma(x) = 1$);
- considering mobile charges in SCR and taking into account the dependence of the effective density of states in SiGe on local Ge content $\gamma(x) = f\left(y_{\mathrm{Ge}}(x)\right)$.

The results are shown in Fig. 2. The position of x_0 moves deeper into the base with the increase of the built-in electric field in the base (i.e., increase of Ge gradient), while W_B is moving towards the collector. Of course, the depletion approximation results in overestimation of x_0 and this overestimation increases with increasing V_{BE}.

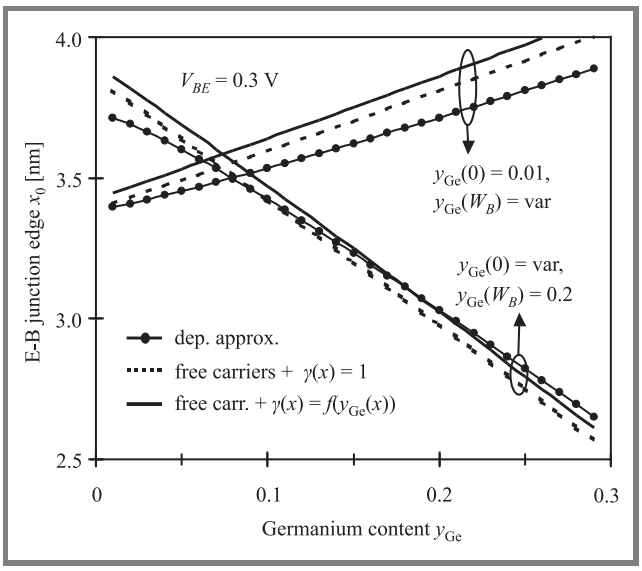

Fig. 2. The position of emitter-base junction space-charge region in the base calculated for different Ge content profiles.

In the case where $\gamma(x) = f\left(y_{\mathrm{Ge}}(x)\right)$, the calculated built-in electric field in the base is lower than that calculated assuming $\gamma(x) = 1$. Therefore x_0 moves towards the emitter (see "$y(W_B) = $ var" in Fig. 2).

When the value of x_0 is known it is possible to obtain the collector current pre-exponential ideality factor m. Using our full model we calculate m for 7 transistors with different $y_{\mathrm{Ge}}(x)$ linear profiles in the base (Fig. 3). As expected,

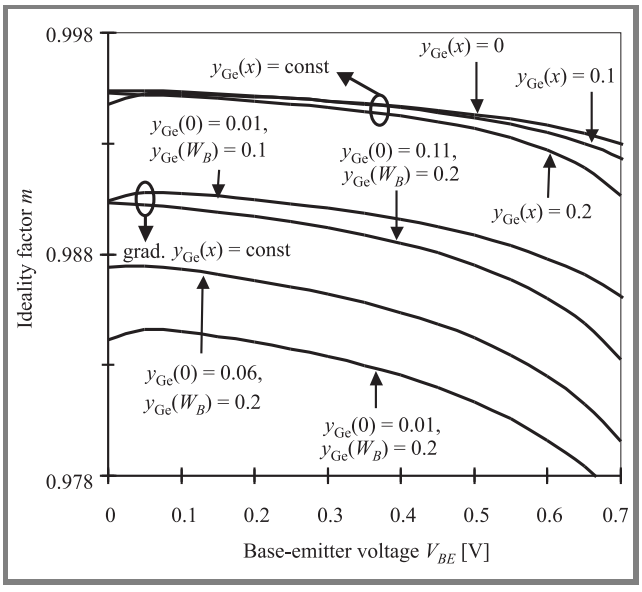

Fig. 3. The collector current pre-exponential ideality factor calculated as a function of emitter-base voltage for different Ge content profiles.

the increase of Ge gradient lowers m, i.e., collector current becomes much more dependent on V_{BE}.

The importance of including the dependence of $D_{n\mathrm{SiGe}}$ on F and that of $\gamma(x)$ on $y_{\mathrm{Ge}}(x)$ in J_C model of SiGe-based HBT has been demonstrated in [4]. The influence of these two effects on the collector current pre-exponential ideality factor m is discussed below.

To illustrate the influence of $D_{n\mathrm{SiGe}}$ reduction due to the drift field, the parameter m was calculated in two ways: with $D_{n\mathrm{SiGe}}$ either dependent or independent of the field. This yields two sets of δm values calculated from Eq. (1) – δm_{DF} and δm_D, respectively. To make further analysis more transparent we define the accuracy of δm calculations as:

$$\Delta\delta m_D = \frac{\delta m_{DF} - \delta m_D}{\delta m_{DF}}\,[\%]\,. \tag{15}$$

This value is plotted in Fig. 4 as a function of V_{BE} for 5 transistors. As seen, it is important to incorporate the investigated effects for transistors with high Ge gradients in the base. Surprisingly, for two transistors with the same Ge gradient but different $y_{\mathrm{Ge}}(x)$ content ("$y_{\mathrm{Ge}}(0) = 0.01$, $y_{\mathrm{Ge}}(W_B) = 0.1$" and "$y_{\mathrm{Ge}}(0) = 0.11$, $y_{\mathrm{Ge}}(W_B) = 0.2$") the calculated $\Delta\delta m_D$ values differ strongly. This is associated with the dependence of $D_{n\mathrm{SiGe}}$ on $y_{\mathrm{Ge}}(x)$ (for more information see [7]).

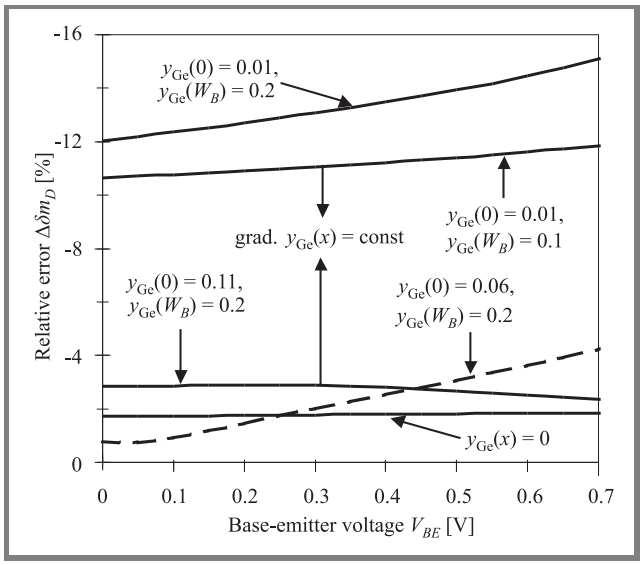

Fig. 4. Accuracy of modeling of the collector current pre-exponential ideality factor assuming that $D_{n\mathrm{SiGe}}$ is independent of the drift field for different Ge content.

The importance of including the dependence $\gamma(x) = f\big(y_{\mathrm{Ge}}(x)\big)$ in the model of m was studied in a similar way. Again, the calculation yields two sets of δm: first $\delta m_\gamma\big(\gamma(x) = f(y_{\mathrm{Ge}}(x)\big)$ and second $\delta m_1\big(\gamma(x) = 1\big)$. The results are plotted as a function of V_{BE} in Fig. 5. The highest error is obtained for transistors with high total germanium

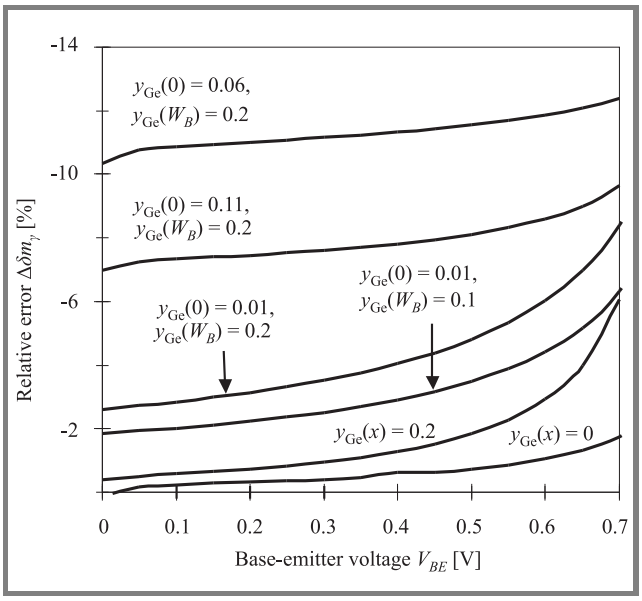

Fig. 5. Accuracy of modeling of the collector current pre-exponential ideality factor assuming $\gamma(x) = 1$ for different Ge content profiles.

content in the base ("$y_{\mathrm{Ge}}(0) = 0.06$, $y_{\mathrm{Ge}}(W_B) = 0.2$" and "$y_{\mathrm{Ge}}(0) = 0.11$, $y_{\mathrm{Ge}}(W_B) = 0.2$").

4. Conclusions

In this paper a new model of the position of the edge of emitter-base junction space-charge region in the base and the collector current pre-exponential ideality factor in SiGe-base HBTs was presented. This model is valid for any doping and germanium content profiles. It includes, for the first time, the dependence of the effective density of states in SiGe base on local Ge content and the dependence of the diffusion coefficient on the drift field in the base.

Both investigated parameters turned out to be sensitive to appropriate modeling of the dependence of the effective density of states in SiGe base on local Ge content.

It was found that in the case of modern HBTs with high built-in fields in the SiGe base collector current ideality factor should be modeled taking into account the dependence of diffusion coefficient on the drift field and on the local Ge content in the base.

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Paper

Comparison of 4H-SiC and 6H-SiC MOSFET *I-V* characteristics simulated with Silvaco Atlas and Crosslight Apsys

Jędrzej Stęszewski, Andrzej Jakubowski, and Michael L. Korwin-Pawlowski

Abstract—A set of physical models describing silicon carbide with fitting parameters is proposed. The theoretical *I-V* output and transfer characteristics and parameters of MOS transistors were calculated using Silvaco Atlas and Crosslight Apsys semiconductor device simulation environments.

Keywords*— *silicon carbide, SiC MOSFET, 4H-SiC, 6H-SiC, Crosslight Apsys, Silvaco Atlas.

1. Introduction

Wide band gap, high breakdown field, high thermal conductivity and low thermal expansion make silicon carbide a very interesting material for high-temperature and high-frequency electronics (e.g., [1, 2]). Selected material parameters of silicon and two hexagonal polytypes of silicon carbide are shown in Table 1.

Table 1
Comparison of basic parameters of silicon, 4H-SiC and 6H-SiC [1, 2]

Parameters	4H-SiC	6H-SiC	Si
$E_{g(300\,\mathrm{K})}$ [eV]	3.23	2.90	1.12
$n_{i(300\,\mathrm{K})}$ [cm^{-3}]	$1.5 \cdot 10^{-8}$	$2.1 \cdot 10^{-5}$	10^{10}
$E_{crit(300\,\mathrm{K})}$ [V/cm]	$2.2 \cdot 10^{6}$	$2.5 \cdot 10^{6}$	$0.25 \cdot 10^{6}$
ε_S	9.66	9.66	11.7
$\mu_{n\max} \perp$ [cm^2/Vs]	947	415	1400
$\mu_{p\max} \perp$ [cm^2/Vs]	124	99	450
V_{SAT} [cm/s]	$2.1 \cdot 10^{7}$	$2 \cdot 10^{7}$	10^{7}

Figure 1 shows the influence of temperature on intrinsic concentration of 4H-SiC and 6H-SiC materials, associated with the temperature-induced band gap narrowing. In the case of 4H-SiC the intrinsic concentration is only one order of magnitude higher at the temperature of 900 K than the intrinsic concentration of silicon at room temperature. That proves very significant, theoretical suitability of silicon carbide as a material for high temperature applications. Moreover SiC is the only wide band-gap semiconductor with native insulator – SiO_2. Figure 2 presents band offsets of 4H-SiC and 6H-SiC compared to silicon [3]. That makes silicon carbide a promising choice for MOSFET devices.

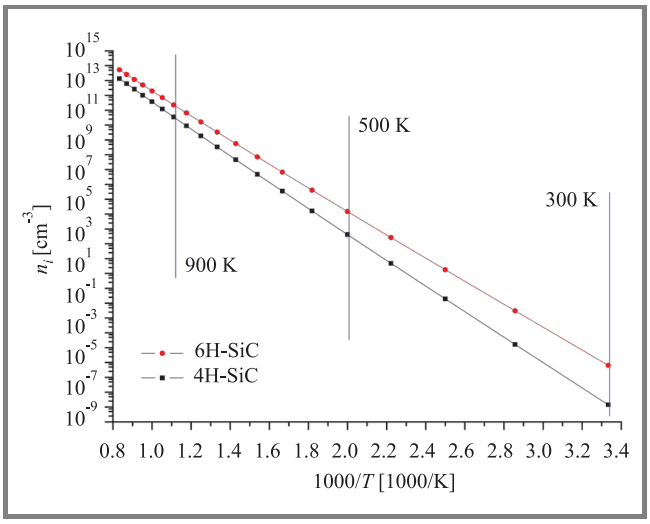

Fig. 1. Simulated influence of the temperature on intrinsic concentration of 4H-SiC and 6H-SiC – temperature-induced band gap narrowing phenomenon taken into account.

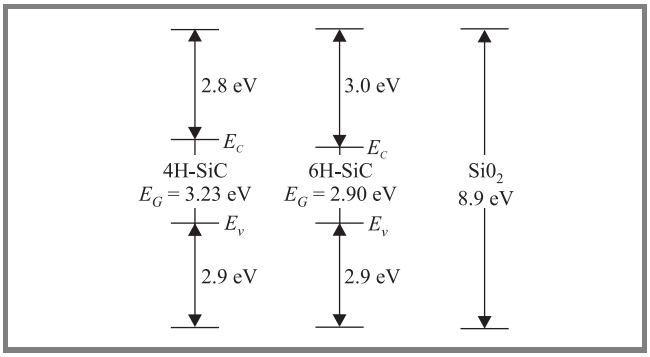

Fig. 2. Band offset of 4H- and 6H-SiC in comparison to silicon dioxide [3].

2. Calculations

In order to obtain accurate calculation results, a variety of physical models with fitting material parameters were implemented in the semiconductor device simulation envi-

ronments: Silvaco Atlas [4] and Crosslight Apsys [5]. The theoretical *I-V* output and transfer characteristics of 4H-SiC and 6H-SiC NMOSFETs were calculated. Moreover, the influence of the temperature on output characteristics was simulated.

3. Physical model summary

The following models were amongst the most important used:

1) carrier mobility:
   - low electric field – Caughey-Thomas formula,
   - high electric field – FLDMOB model [6];
2) carriers ionization effects:
   - incomplete ionization [7],
   - impact ionization – Selberherr model [8];
3) generation-recombination phenomenon:
   - Auger recombination [9],
   - SRH recombination [10];
4) band gap narrowing:
   - temperature dependence – analytical formula,
   - doping influence – Slotboom model [11].

In all simulations anisotropy of silicon carbide electrical parameters was neglected. It was assumed that the dominant direction of carrier flow is oriented along the transistor channel.

4. Results

Figures 3 and 4 show output and transfer characteristics of 4H-SiC and 6H-SiC NMOS transistor ($N_B = 2 \cdot 10^{17}$ cm^{-3}, $t_{ox} = 10$ nm, $L_{ch} = 1$ μm, $D_{it} = 10^{11}$ cm^{-2}), respectively.

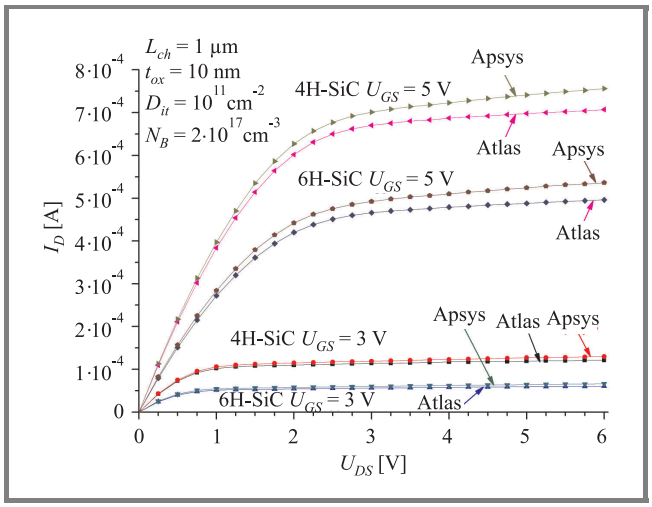

Fig. 3. Simulated output characteristics of 4H-SiC and 6H-SiC NMOSFETs.

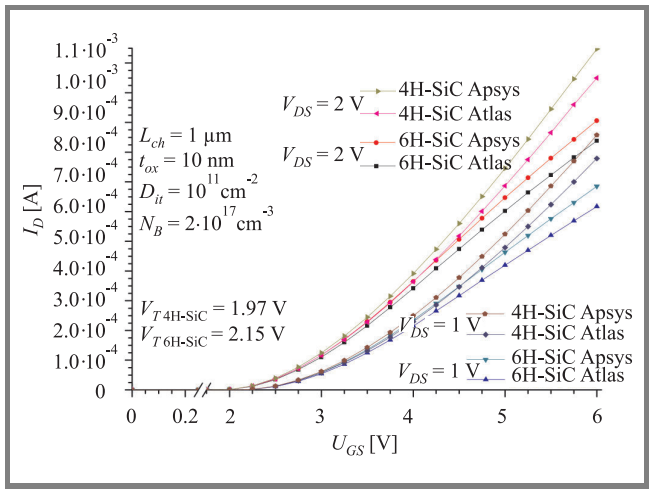

Fig. 4. Simulated transfer characteristics of 4H-SiC and 6H-SiC NMOSFETs.

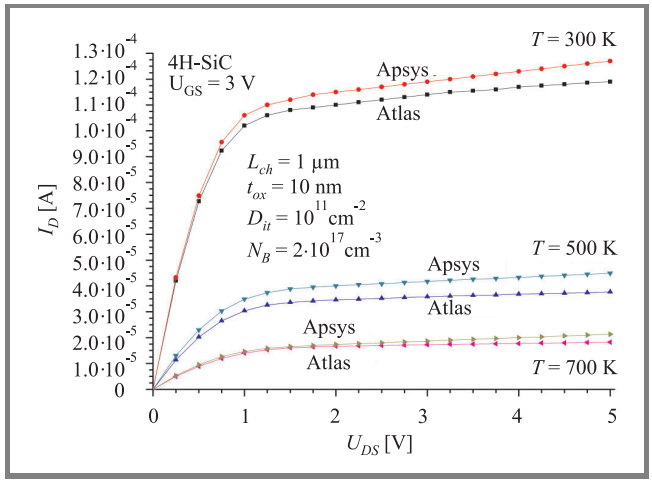

Fig. 5. Simulated influence of temperature on 4H-SiC NMOSFET output characteristics.

The characteristics were calculated using both simulators. The influence of temperature on output characteristics of 4H-SiC NMOSFET is presented in Fig. 5.

5. Discussion and conclusions

Presented results obtained with Silvaco Atlas and Crosslight Apsys show noticeable difference in drain current values. In the case of *I-V* output characteristics, drain current calculated with Apsys is, on the average, 7 to 9% higher, while transfer characteristics exhibit 8 to 11% drain current difference in favor of Apsys. Moreover, simulated drain current at elevated temperatures displays 8 to 18% difference.

Both device simulators – Silvaco Atlas and Crosslight Apsys use the same computational approach: Poisson's equation and electron/hole continuity equations are solved in a coupled manner.

The differences in drain currents obtained with both environments might be caused by the mesh discretization tactics

and distinct numerical methods, as well. Possible overestimation of MOSFETs drain current might also be a consequence of the omission of anisotropy in the calculations carried out.

The paper introduces band gap narrowing models (which are generally neglected) to the simulation of silicon carbide devices. The proposed modification is based on Slotboom (doping influence) and analytical (temperature influence) models with appropriate parameters, well known for silicon. Significant influence of temperature-induced band gap narrowing on carrier concentration at elevated temperatures is commonly overlooked. Eventually, it leads to overestimation of SiC device applicability in extremely high temperatures.

Obtaining of reliable simulation results is difficult by significant differences in the values of silicon carbide material parameters reported in various papers. Further studies are needed.

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Paper

Monte Carlo method used for a prognosis of selected technological parameters

Małgorzata Langer

Abstract—In this paper a smart modeling approach for realistic simulation of selected technological parameters is presented. The technology of making contacts with plasma vapor deposition (PVD) method has been chosen for this purpose. The analysis is based on the Monte Carlo (MC) method and uses the Excel worksheet – the simplest tool, easily accessible to anyone. The statistic parameters are calculated and discussed as we introduce this experiment to demonstrate the advantages of design for six sigma (DFSS).

Keywords—DFSS, MC method, PVD, contacts, Excel randomizing.

1. Design for six sigma

Design for six sigma (DFSS) [1] and its metric – the probability of non-compliance [2] make it possible to consider different sources of variation when applied in manufacturing. The philosophy of this approach is that variation exists in all systems, components, and procedures. The probabilistic analysis is to be run when analysing and optimising all the successive phases of the design and its implementation (Fig. 1a). DFSS approach may also be applied in research, such as experiments, simulations, result analysis, etc. (Fig. 1b). In this paper a methodology presented in Fig. 1b is proposed.

Using DFSS one analyses the whole statistical distribution of input values or parameters over their possible range, instead of estimating the influence of extreme (therefore rare) values on the operation or the condition of the object. Thus instead of calculating the limits of the result range, one calculates the probability of the distribution of possible results. And the distribution of probability is the basic metric for DFSS.

When an output response represents the total influence of independent input values and parameters, the output distribution tends to be normal as a result of the central limit theorem [3]. The significance of this is that there is no precondition for probability distributions of the input design parameters (they do not have to be normal) to obtain a normal output response. The majority of physical phenomena and variables are represented by the normal distribution.

The Tchebychev inequality known in statistics [3], states that at least $1-(1/k^2)$ per cent of any distribution is within the product: ($\pm k \times$ deviation $\times$ mean).

Table 1

The per cent of normal distribution covered by the range calculated with Tchebychev inequality

k [--]	1	1.415	2	3	4	5	6
[%]	68.3	84.3	95.5	99.7	99.99	99.99994	99.9999998

In the case of normal distribution the percentage in this range is known exactly (Table 1).

2. Monte Carlo method

Monte Carlo (MC) methods were used already in 1947 to simulate the neutron transport in the research on the hydrogen bomb [4]. Since their first presentation (at a conference in Los Alamos in 1949), they have been used to predict "almost everything", from a simple bingo game, through weather forecasts to atomic fusion.

The goal of the MC method is to simulate an existing object (an equation, a model, a process, etc.) by randomly sampling the input ranges (input distributions) and then calculating the output response. The flow chart is shown in Fig. 2.

The fundamental problem of using MC to perform a probabilistic analysis is that it requires a large number of trials to obtain a sufficient confidence in the results. With the development of PCs many techniques have been developed to generate random numbers; with many of them still requiring huge time and memory resources. MC methods can be applied to extremely complex finite element models, fluid dynamics, etc., but every trial may last long hours and the computer grids (parallel processing) are the only solution to meet these demands. They are beyond the scope of this paper, as we propose to use Excel RAND() function, that is adequate for application in a great number of cases.

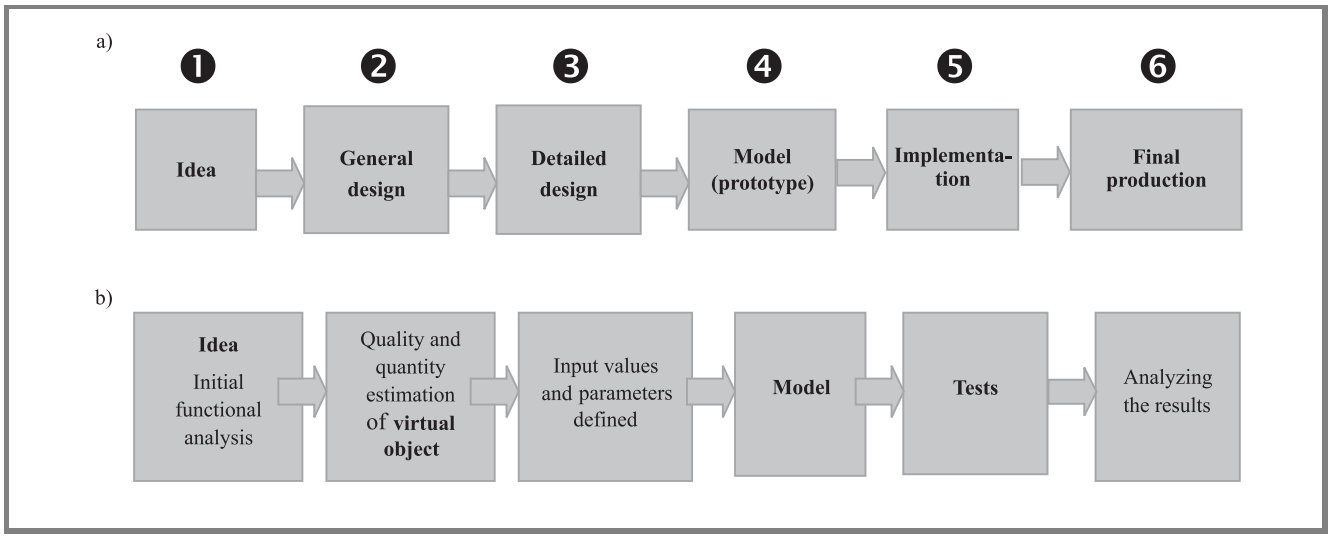


Fig. 1. Phases of considering the variations (a) in the production; (b) in testing the model.

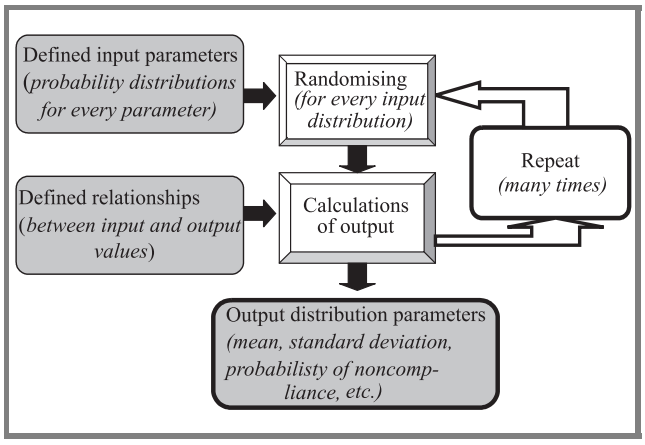


Fig. 2. Monte Carlo method. Flow chart.

3. Distributions prepared in Excel

A standard uniform random number (any number between 0 and 1; denoted as *RU*) is required to generate a random value from any probability density function. In Microsoft Excel the RAND() function returns *RU*. Some experts claim that the algorithm applied in Excel does not meet the rigorous standard required for cryptography, but it is absolutely sufficient for simulations in engineering. Random numbers for a standard normal distribution (denoted as *RN*; both mean and standard deviation are equal to zero) can be computed with Box-Muller method, known since 1958 [4]:

$$RN = \sqrt{-2\ln(RU1)} \cdot \cos\left(2\pi \cdot (RU2)\right), \qquad (1)$$

where $RU1$ and $RU2$ are uniform random numbers.

The Excel function is:

$$\mathrm{RN} = \mathrm{SQRT}(-2{*}\mathrm{LN}(\mathrm{RAND}()){*}\mathrm{COS}(2{*}\mathrm{PI}(){*}\mathrm{RAND}()).$$

Having *RU* and *RN* numbers one may generate a common distribution (e.g., uniform, normal, log-normal, exponential, etc.) using the appropriate formulae with the desired values of mean and standard deviation. For a uniform distribution between the minimum (min) and maximum (max) values the random value (denoted as *RV*) is calculated as:

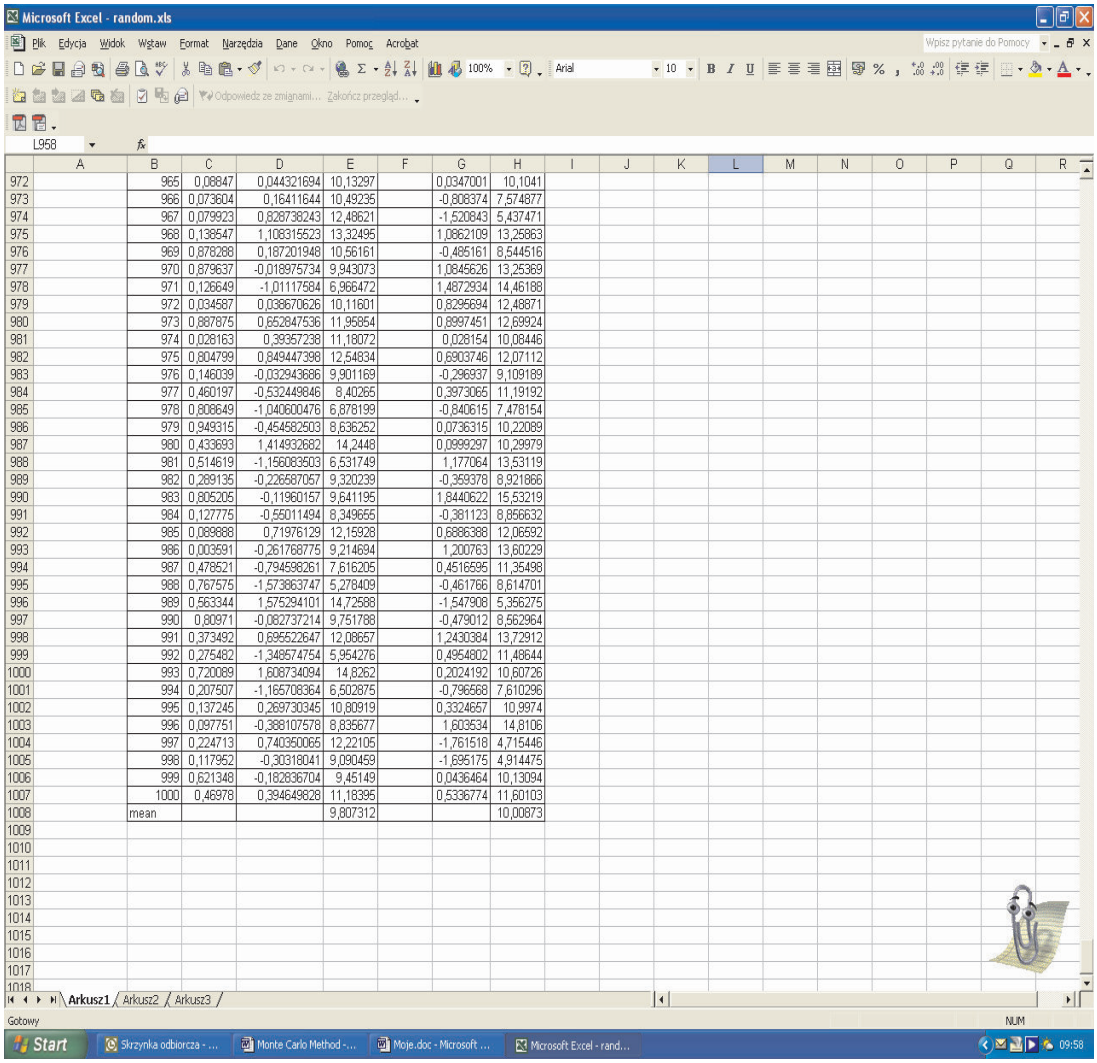
$$RV = (\max - \min)RU + \min \qquad (2)$$

and for a normal distribution:

$$RV = mean + deviation \cdot RN. \qquad (3)$$

The more random numbers we generate, the closer the mean and the standard deviation are to specified values. If one generated an infinite number of *RN*s – the calculated mean and deviation would be equal exactly to the specified ones.

As it was mentioned before, Microsoft Excel may be used to generate random numbers. The maximum number of MC trials is limited by the maximum number of rows in the worksheet (65,536 trials in Excel 2002). It is assumed that one thousand trials already meet the requirements, with a limited confidence. The author checked tens randomised normal distributions (ND) with one thousand runs, assuming the mean of 10 and the calculated means equalled to 9.8 – 10.2 so the error was not greater than 2 per cent. A screen capture with typical results is shown in Fig. 3. In the simulated experiment described later 5000 trials were used.



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
972		965	0,08847	0,044321694	10,13297		0,0347001	10,1041										
973		966	0,073604	0,16411644	10,49235		-0,808374	7,574877										
974		967	0,079923	0,828738243	12,48621		-1,520843	5,437471										
975		968	0,138547	1,108315523	13,32495		1,0862109	13,25863										
976		969	0,878288	0,187201948	10,56161		-0,485161	8,544516										
977		970	0,879637	-0,018975734	9,943073		1,0845626	13,25369										
978		971	0,126649	-1,01117584	6,966472		1,4872934	14,46188										
979		972	0,034587	0,038670626	10,11601		0,8295694	12,48871										
980		973	0,887875	0,652847536	11,95854		0,8997451	12,69924										
981		974	0,028163	0,39357238	11,18072		0,028154	10,08446										
982		975	0,804799	0,849447398	12,54834		0,6903746	12,07112										
983		976	0,146039	-0,032943686	9,901169		-0,296937	9,109189										
984		977	0,460197	-0,532449846	8,40265		0,3973065	11,19192										
985		978	0,808649	-1,040600476	6,878199		-0,840615	7,478154										
986		979	0,949315	-0,454582603	8,636252		0,0736315	10,22089										
987		980	0,433693	1,414932682	14,2448		0,0999297	10,29979										
988		981	0,514619	-1,156083503	6,531749		1,177064	13,53119										
989		982	0,289135	-0,226587057	9,320239		-0,359378	8,921866										
990		983	0,805205	-0,11960157	9,641195		1,8440622	15,53219										
991		984	0,127775	-0,55011494	8,349655		-0,381123	8,856632										
992		985	0,089888	0,71976129	12,15928		0,6886388	12,06592										
993		986	0,003591	-0,261768775	9,214694		1,200763	13,60229										
994		987	0,478521	-0,794598261	7,616205		0,4516595	11,35498										
995		988	0,767575	-1,573863747	5,278409		-0,461766	8,614701										
996		989	0,563344	1,575294101	14,72588		-1,547908	5,356275										
997		990	0,80971	-0,082737214	9,751788		-0,479012	8,562964										
998		991	0,373492	0,695522647	12,08657		1,2430384	13,72912										
999		992	0,275482	-1,348574754	5,954276		0,4954802	11,48644										
1000		993	0,720089	1,608734094	14,8262		0,2024192	10,60726										
1001		994	0,207507	-1,165708364	6,502875		-0,796568	7,610296										
1002		995	0,137245	0,269730345	10,80919		0,3324657	10,9974										
1003		996	0,097751	-0,388107578	8,835677		1,603534	14,8106										
1004		997	0,224713	0,740350065	12,22105		-1,761518	4,715446										
1005		998	0,117952	-0,30318041	9,090459		-1,695175	4,914475										
1006		999	0,621348	-0,182836704	9,45149		0,0436464	10,13094										
1007		1000	0,46978	0,394649828	11,18395		0,5336774	11,60103										
1008		mean			9,807312			10,00873										

Fig. 3. The part of the spreadsheet to check the error at one thousand trials.

4. The experiment

The MC method was used to simulate plasma vapor deposition (PVD) metallization from a resistive source (Fig. 4) intended to form aluminium contacts. A detailed description of this process may be found, e.g., in [5, 6]. The technique is used in the Technical University of Łódź, Institute of Electronics (TUL IE) during studies to improve the quality of contacts to such materials as SiC. The process takes place in a vacuum chamber (Fig. 5). The goal of the virtual experiment is to anticipate the solution of the Langmuir formula [5] for the evaporation rate:

$$v = 77.8\sqrt{\frac{M}{T}} \cdot p_s \quad [\mathrm{g/cm^2 s}], \tag{4}$$

where: M – molecular weigh [g/mole], T – material temperature [K], p_s – vapor pressure at the temperature T [Pa].

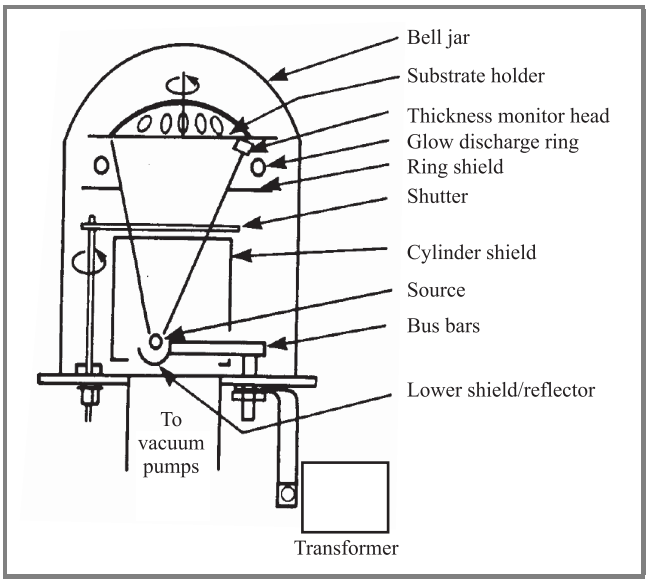


Fig. 4. The typical system for PVD from the resistive source [from student manual, TUL IE].

Table 2

Range and distribution of input parameters

Parameters	Experiment I		Experiment II	
	Range	Distribution	Range	Distribution
Purity of aluminium	±0.5%	uniform	±0.5%	uniform
Temperature	±1% (∼12 degrees)	Gaussian (deviation = 0.66)	±2%	Gaussian (deviation = 1.3)
Pressure	±10% (changes logarithmically)	Gaussian (deviation = 1)	±20%	Gaussian (deviation = 2)

The formula (4) is true when the pressure of residual gases is lower than 1.33^{-4} Pa. It takes 30–40 min to deposit a layer with the typical thickness of 1–1.2 μm at substrates heated to $\sim$475 K. Process duration increases to 40–60 min at temperatures of 572–625 K [7]. The pumping, heating and cooling rate strongly affects the quality of the layers.

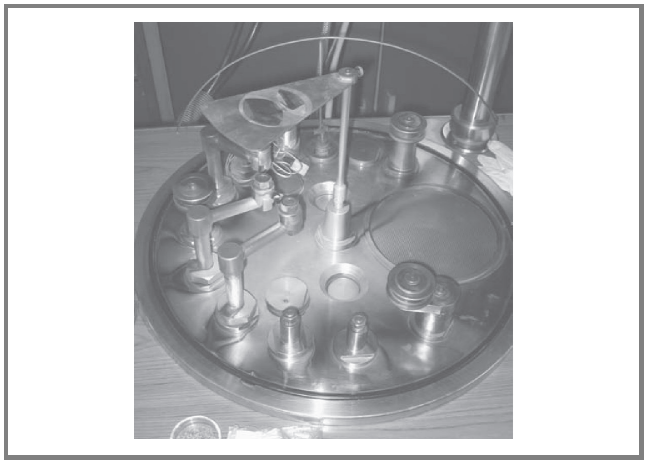


Fig. 5. The interior of the chamber in TUL IE.

The melting point of pure aluminium is 932 K and its evaporation takes place at 1421 K. The optimum evaporation rate is $0.85 \cdot 10^{-4}$ g/cm^{2}s [5]. Temperature stability is very important here since its increase by approximately 10–15 per cent may elevate the pressure as much as ten times, and the evaporation rate depends on the diffusion of the outer layers of the cloud of vaporised aluminium.

5. The MC simulation

The optimum values of input (purity of aluminium M, temperature T and vapor pressure p_s) and output (evaporation rate) parameters are assumed to be 100 per cent. The goal of the simulation is to study the variation of evaporation rate with the variation of input parameters (strongly depending on the conditions in the lab).

The range and distribution of input parameters are listed in Table 2. Every experiment covers 5000 trials.

The obtained distribution of evaporation rate is presented in Fig. 6 for experiments I (Fig. 6a) and II (Fig. 6b).

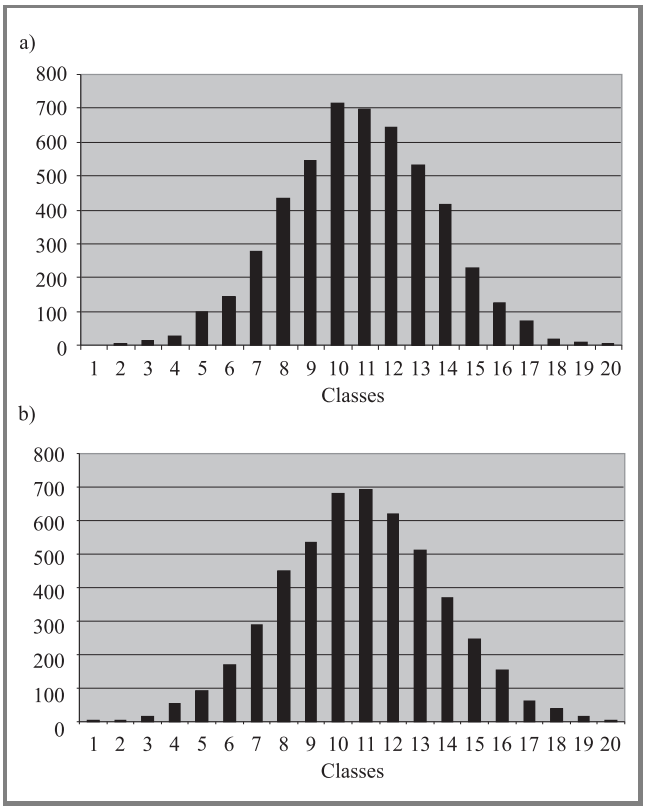


Fig. 6. The distribution of results – quantity of events in the classes: (a) experiment I; (b) experiment II.

The whole range of rates (maximum rate – minimum rate) was divided into 20 equal sub-ranges (we have established 20 classes). Quantities in classes are listed in Table 3, which contains also basic statistical parameters. The accepted limit value may be chosen arbitrarily. The last row in Table 3 means that the assumed maximum allowed change of the output (i.e., evaporation rate) is 5 per cent for our experiments. It may be seen that more

than 30 per cent of output values will not meet this requirement in experiment II and less than 5% in experiment I.

Table 3
Simulation results

Classes	Quantity in classes	
	Experiment I	Experiment II
1	1	2
2	5	3
3	12	16
4	29	52
5	98	94
6	144	168
7	275	289
8	433	450
9	547	533
10	717	681
11	698	694
12	644	619
13	532	511
14	417	369
15	226	245
16	125	154
17	71	63
18	16	37
19	7	15
20	3	5
Parameters	Values	
Mean [%]	100.022	99.99087
Deviation	1.066626	2.110416
Min value [%]	96.00374	92.44879
Max value [%]	103.7724	107.0591
Median [%]	100.0243	100.0857
Within the range of coarse values: 98–102	95.5% of events	68.3% of events

These are our probability of non-compliance (PNC) results for the assumed parameters.

6. Conclusions

The example given in this paper focused on math and statistics, but MC method may be used in numerous considerations. When the distribution type for a population is determined, one can simulate any object for which an appropriate model exists. One can calculate characteristic parameters for the investigated distributions; determine what the tolerance limits or the range should be (based on expected behavior); estimate how great is PNC for a given case and assumptions. The presented example shows how helpful Excel may be in this research. In the investigated case the time to make a population and to calculate the statistic parameters was very short (a few seconds). Thus it has been demonstrated that Excel is sufficient as a DFSS tool.

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Paper

The influence of yield model parameters on the probability of defect occurrence

Michał Rakowski and Witold A. Pleskacz

Abstract—This paper describes the analysis of the influence of yield loss model parameters on the calculation of the probability of arising shorts between conducting paths in IC's. The characterization of the standard cell in AMS 0.8 μm CMOS technology is presented as well as obtained probability results and estimations of yield loss by changing values of model parameters.

Keywords—yield model parameters, spot defect, probability of defect occurrence, critical area.

1. Introduction

Contemporary digital circuits become more complex making their testing and diagnostics more difficult. Having an accurate defect model is therefore essential. Since the model affects the efficiency of defect detection, it should be tuned as well as possible to reflect the reality. On the other hand, however, excessive complication of the model could result in many practical difficulties. The time of running the defect detection procedure should be acceptable, especially for large VLSI circuits.

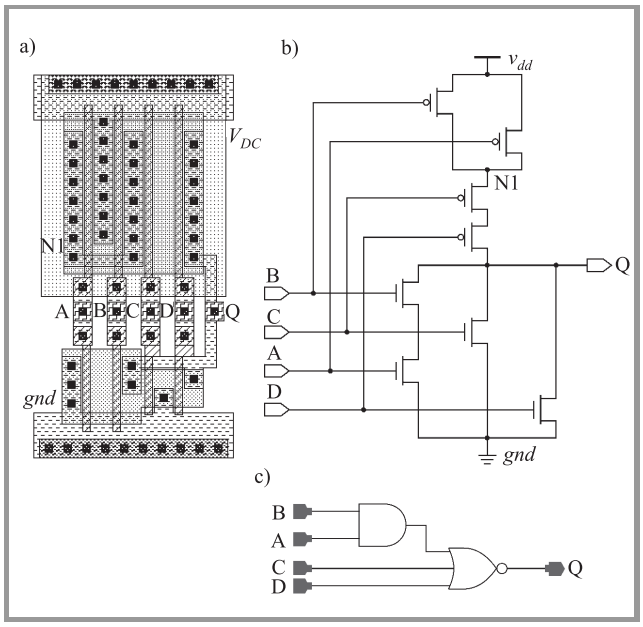

Fig. 1. The AN3 complex gate: (a) the layout; (b) schematic diagram; (c) logic diagram.

Spot defects in ICs still cause many functional and catastrophic faults [1–3]. The degree of the influence of spot defects, such as shorts or opens, on IC manufacturability is determined by the sensitivity of the layout to these defects. It is believed that only full layout analysis enables one to proceed with complex estimation of defect-occurrence probabilities and yield calculations [4].

In this work we use a quite efficient and easy-to-implement model of critical area that enables the probability of different catastrophic faults caused by spot defects to be estimated. The model is used to calculate the probability of shorts and opens between two conductive paths on a circuit layout, as well as to estimate yield.

The analysis of the model parameters is limited in this paper only to the defects cause by shorts. A standard AN3 complex gate from 0.8 μm CMOS industrial library (see Fig. 1) has been used as a testing circuit.

2. Probabilistic yield model

A short is a piece of extra conducting material that connects a pair of separate conducting regions in the integrated circuit. This affects the connectivity of the circuit: two separate electrical nets become connected. It is intuitively obvious that probabilities of shorts depend on the layout of the circuit. Conducting regions that are adjacent to one another are more susceptible to shorts than regions that are separated by a large distance. We assume that every defect that results in a short can be approximated by a circle. To estimate the probabilities of shorts between pairs of nodes we use the concept of critical area for shorts [3]. The critical area for shorts is such a region in the circuit that, if the center of a defect of a given radius R is located anywhere inside the critical area, a short between two adjacent conducting paths occurs (see Fig. 2).

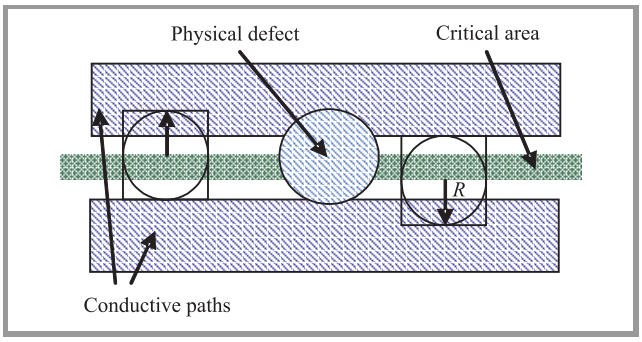

Fig. 2. The concept of critical area.

The probability that two electrical nodes will be shorted by a physical defect is given by the following formula derived from Poisson-based yield model:

$$Y = \prod_{i=1}^{N} Y_i;\ Y_i = \exp\Big[- \int_0^{+\infty} Acr_i(r) \cdot D_i(r)\, dr \Big], \qquad (1)$$

where: Y – defect-related yield for an IC, N – number of defect types, Y_i – defect-related yield for defect type "i", r – defect radius random variable, $Acr_i(r)$ – critical area function, $D_i(r)$ – defect size distribution.

The defect size distribution can be calculated from the formula [2, 3]:

$$D_i(r) = D_{oi}(r) \cdot f_{ri}(r), \qquad (2)$$

where: $D_{oi}(r)$ – density of spot defect of type "i", $f_{ri}(r)$ – size distribution function for defect of type "i" given by [2, 3]:

$$f_{ri}(r) = \begin{cases} \dfrac{2(p_i - 1)\, r}{(p_i + 1) X_{oi}^2} & \text{for} \quad 0 < r \le X_{oi}, \\ \dfrac{2(p_i - 1) X_{oi}^{p_i - 1}}{(p_i + 1) r^{p_i}} & \text{for} \quad X_{oi} < r \end{cases}. \qquad (3)$$

The size distribution function has two parameters: X_{oi} (which is modeled to be very small compared to the minimum feature size of a given manufacturing process) and parameter p_i. In our calculation of the probability of shorts the most important three conductive layers – polysilicon, metal1 and metal2 were taken into account.

Parameter D_{oi} is the density of physical defects and p_i and X_{oi} are model parameters. P_i is set to 3, X_{oi} to 20% of the minimum distance between the shapes of a given conducting layer, and D_o to 10 defects/cm^2 [3, 4].

3. Experimental results

The analysis of parameter influence on manufacturing yield as well as probability of shorts between conducting paths was perfomed by means of variation of each parameter within a predefined range. The analyzed range of the variation of the examined parameters is compared to the corresponding nominal values in Table 1.

Table 1
Analyzed range of variation of the yield model parameters

Description	Layers	Parameters			
		p	D_o [cm^{-2}]	X_o [%]	
Nominal value	Poly1	3	10	20	0.2
	Met1				0.2
	Met2				0.24
Range of changes	All	$<2-5>$	$<5-15>$	$<5-40>$	
Step	All	0.5	2.5	5	

The probability analysis was performed using the extracted layout of AN3 complex gate resulted in a list of faults for shorts with non-zero probability. To extract critical areas and calculate the probability of shorts we used our tool [5] *Critical Areas* written in the SKILL language. By running geometrical operations on the conducting layers of the layout the tool extracts the critical area function $Acr_i(r)$, which is further used to carry out the probability calculation and yield estimation.

We calculated the probability of shorts between all possible pairs of two electrical nodes for complex gate AN3 (see Table 2). The obtained calculations were taken as the basis for further analysis of model parameters.

Table 2
Distribution of probabilities of faults for AN3 gate

AN3		Y	$P_{sh} = 1 - Y$	$P_{sh}/P_{sh}(sum)$
Conductive layers		0.999998718	$1.28 \cdot 10^{-6}$	
For all pair of nets				
No.	Fault	Y	$P_{sh} = 1 - Y$	$P_{sh}/P_{sh}(sum)$
1	B/C	0.999999796	$2.04 \cdot 10^{-7}$	0.124693127
2	C/D	0.999999796	$2.04 \cdot 10^{-7}$	0.124693127
3	N1/v_{dd}!	0.999999853	$1.47 \cdot 10^{-7}$	0.089854335
4	D/Q	0.999999864	$1.36 \cdot 10^{-7}$	0.083128754
5	Q/*gnd*!	0.999999875	$1.25 \cdot 10^{-7}$	0.076285516
6	A/B	0.999999913	$8.74 \cdot 10^{-8}$	0.053516526
7	B/D	0.999999913	$8.74 \cdot 10^{-8}$	0.053516526
8	Q/v_{dd}!	0.999999940	$5.96 \cdot 10^{-8}$	0.036462936
9	C/Q	0.999999942	$5.83 \cdot 10^{-8}$	0.035677684
10	N1/B	0.999999945	$5.51 \cdot 10^{-8}$	0.033746016
11	A/C	0.999999949	$5.10 \cdot 10^{-8}$	0.031200232
12	N1/A	0.999999949	$5.08 \cdot 10^{-8}$	0.031091017
13	N1/Q	0.999999957	$4.26 \cdot 10^{-8}$	0.026086434
14	N1/C	0.999999959	$4.07 \cdot 10^{-8}$	0.024884915
15	A/*gnd*!	0.999999965	$3.46 \cdot 10^{-8}$	0.021187114
16	B/Q	0.999999966	$3.40 \cdot 10^{-8}$	0.020800155
17	A/D	0.999999969	$3.15 \cdot 10^{-8}$	0.019256726
18	B/*gnd*!	0.999999973	$2.74 \cdot 10^{-8}$	0.016744255
19	C/*gnd*!	0.999999974	$2.58 \cdot 10^{-8}$	0.015772579
20	N1/D	0.999999978	$2.20 \cdot 10^{-8}$	0.013441077
21	B/v_{dd}!	0.999999979	$2.14 \cdot 10^{-8}$	0.013084317
22	D/*gnd*!	0.999999979	$2.13 \cdot 10^{-8}$	0.013054676
23	A/v_{dd}!	0.999999981	$1.87 \cdot 10^{-8}$	0.011463841
24	C/v_{dd}!	0.999999985	$1.49 \cdot 10^{-8}$	0.009137585
25	A/Q	0.999999987	$1.31 \cdot 10^{-8}$	0.007990456
26	D/v_{dd}!	0.999999989	$1.06 \cdot 10^{-8}$	0.006487213
27	N1/*gnd*!	0.999999993	$7.27 \cdot 10^{-9}$	0.004451322
28	*gnd*!/v_{dd}!	0.999999996	$3.74 \cdot 10^{-9}$	0.002291538

The analysis of each parameter was conducted with nominal values of the remaining parameters. Every parameter has a significant influence on defect size distribution.

The increase of parameter p causes that maximum value of defect size distribution to increase (see Fig. 3). Moreover,

for higher values of defect radii the probability of shorts becomes smaller. The parameter X changes the defect size distribution slightly in different way.

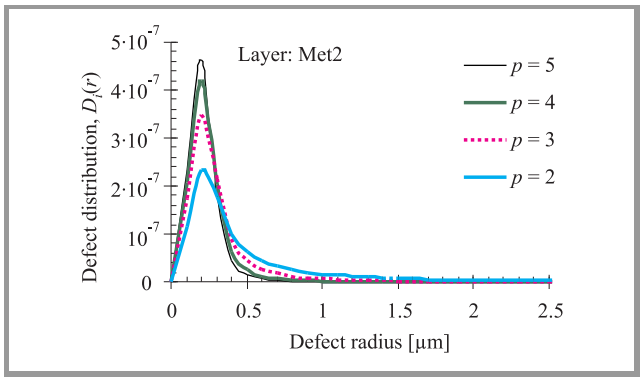

Fig. 3. Defect size distribution for different values of parameter p ($D = 10$ cm^{-2}, $X = 0.24$).

The density of the probability reamains constant, but the maximum shifts towards higher values of defect radii with increasing X (see Fig. 4).

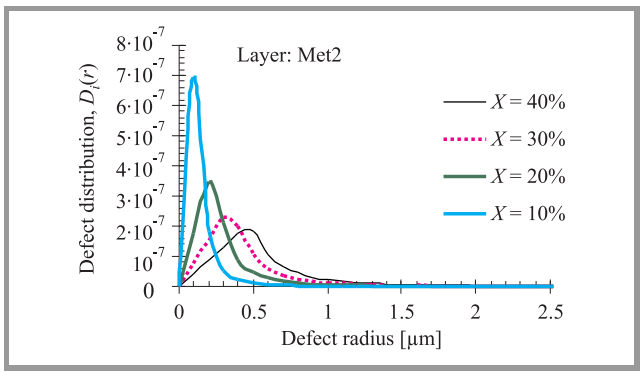

Fig. 4. Defect size distribution for different values of parameter X ($D = 10$ cm^{-2}, $p = 3$).

Parameter D can only change the density of probability of short occurrences (see Fig. 5).

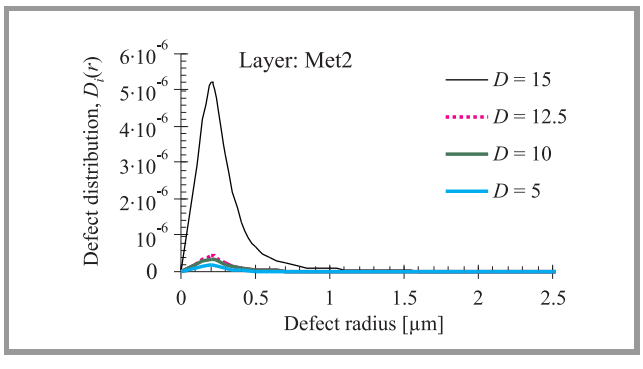

Fig. 5. Defect size distribution for different values of parameter D ($X = 0.24$, $p = 3$).

The parameter p seems to have the most significant influences on the obtained results. The probability does not change in the same way for all critical nets because with the increase of p the probability of fault decreases for radii higher than the one determined by the parameter X. In this way the biggest probability changes are observed for the least critical pair of nets and their significance increases with the growth of p.

In Table 2 pairs of critical paths have been listed in the order of decreasing probability of short occurrence. We have noticed, however, that this order depends on the value of p. This fact may be very important for the generation of test vectors. The efficiency of test vector components in detection of catastrophic faults for the circuit is changing with the parameter p.

The probability of manufacturing yield (lack of occurrence catastrophic fault) for three masks, as well as the total probability of manufacturing yield for all layers is shown in Fig. 6 as a function of the parameter p. Probability values are normalized to nominal ones obtained at $p = 3$.

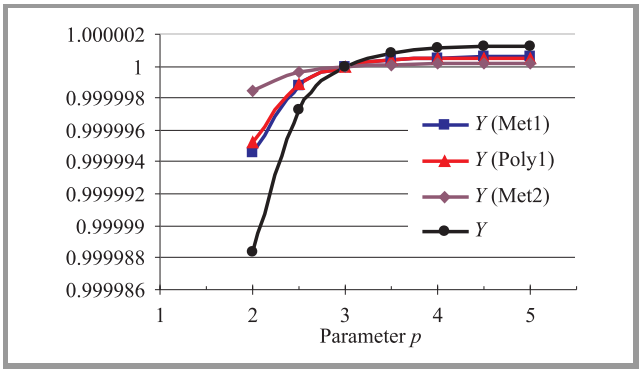

Fig. 6. Defect-related yield normalized to that obtained at nominal value of parameter p ($D = 10$ cm^{-2}, $X = 20\%$).

Parameters X and D seem to be less important, but each may strongly affect the probability of fault occurrences, especially parameter D. Its changes have an exponential influence on the yield estimation. In contrast to parameter p, probability values change in the same way with parameters X and D for all critical pairs. As a result the list of the most significant pairs of critical nets stays unchanged.

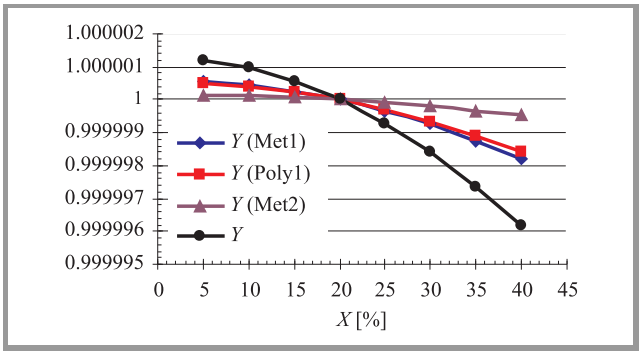

Fig. 7. Defect-related yield normalized to that obtained at nominal value of parameter X ($D = 10$ cm^{-2}, $p = 3$).

The probability of manufacturing yield for three conductive layers and total probability of manufacturing yield for all layers are shown as a function of parameter X and D

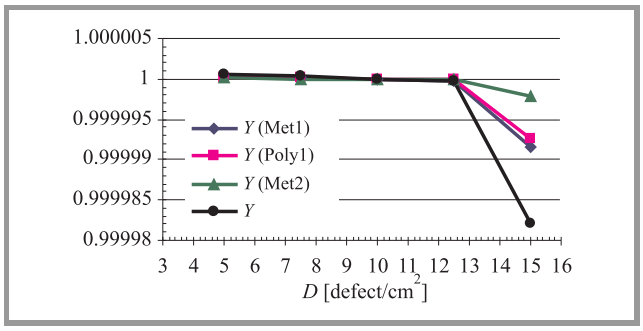

Fig. 8. Defect-related yield normalized to that obtained at nominal value of parameter D ($X = 20\%$, $p = 3$).

in Figs. 7 and 8, respectively. The probability values are normalized to those obtained at nominal value of each parameter.

4. Conclusions

We analyzed the sensitivity of the obtained probability on the yield model parameters. Our investigations indicate that:

- the changes of parameter p have the most influence on the calculated probabilities of fault;
- parameter p causes changes the order of the list of the most critical pair of nets;
- with the growth of parameter p the yield is decreasing exponentially;
- the changes of parameters X and D have the same influence on all critical pairs of nets in a circuit;
- with the growth of parameters X and D the probability of fault in a circuit is increasing (for parameter D the growth of this function is exponential).

Acknowledgement

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Paper

Optical interconnections in future VLSI systems

Grzegorz Tosik, Zbigniew Lisik, and Frederic Gaffiot

Abstract—This paper is focused on the latency and power dissipation in clock systems, which should be lower when the optical interconnects are applied. Simulation shows that the power consumed by an optical system is lower than that consumed by an electrical one, however the advantages of optics drastically decrease with the number of output nodes in H-tree. Additionally, simple replacement of an electrical system by an optical clock distribution network (CDN) results in high clock skew, which will be higher than 10% of the clock period for the 32 nm technology node.

Keywords—optical interconnects, clock skew, clock distribution network, OCDN, OVLSI.

1. Introduction

Progress of VLSI systems has been driven by the downsizing of their components and increasing operating speed. According to ITRS [1] prediction high performance integrated circuits will contain up to $2 \cdot 10^9$ transistors per chip and work with clock frequencies up to 10 GHz by 2010. One of the greatest challenges in designing such IC's is to design high-performance communication networks between their active elements. While transistor scaling provides improvements in both density and device performance, interconnect scaling improves interconnect density but generally at the cost of degraded propagation delay and power losses. In modern technologies, the interconnect delay dominates over the logic delay in spite of new metallization technologies such as copper or new low-*k* dielectrics. Signal integrity issues that occur with the global interconnect for data transfer can cause extreme problems for the clock distribution systems. Due to the bandwidth limitation of upper level interconnects the high speed clock signal cannot be distributed globally across the chip. Additionally, clock skew due to variation sources is becoming difficult to control with traditional balanced distribution networks. Since a single-chip processor available commercially consumes more than 100 W of power, thermal management is also a major concern. The main consumer (up to 30–50%) [2] of delivered power in modern IC's is the clock distribution network (CDN), that requires several hundreds of repeaters to drive the metallic tracks over the entire chip.

It becomes evident that the electrical interconnects are approaching their fundamental limits and represents the present performance bottleneck. The new materials proposed by ITRS can only extend the life of the conventional interconnect by a few years, so to meet the performance challenge, revolutionary approach will be needed. Due to such features as large bandwidth, low latency, low power requirements, reduced crosstalk, electromagnetic immunity and electrical isolation, the application of optical interconnects in VLSI systems is considered as an alternative solution.

This paper presents the estimation of the power budget and timing properties of optical clock distribution network (OCDN).

2. Optical clock distribution network

As a possible solution that can overcome problems of electrical interconnects we propose the integration of III-V active optoelectronic devices and passive silicon waveguides on the standard silicon chip as presented in Fig. 1. Silicon waveguides will be placed on the upper metallization layers and connected to the off-chip photonic source and on-chip optical receivers. To form the planar optical structure described above, the use of Si as the core and SiO_2 as the cladding materials is assumed. The Si/SiO_2 system has been chosen because it is compatible with conventional silicon technology, transparent for $1.3 - 1.55$ μm wavelength and has attenuation as low as 0.8 dB/cm [3]. Additionally, such waveguides with high relative refractive index difference $\Delta \approx (n_1^2 - n_2^2)/2n_1^2$ between the core ($n_1 \approx 3.5$ for Si) and claddings ($n_2 \approx 1.5$ for SiO_2) allow compact optical circuits to be designed and fabricated with bend radius of the order of a few micrometers. To avoid modal dispersion, improve coupling efficiency and reduce loss, single mode conditions are applied to the waveguide dimensions. The optical process is completely independent from the CMOS process and does not require a revolutionary mutation in the CMOS process.

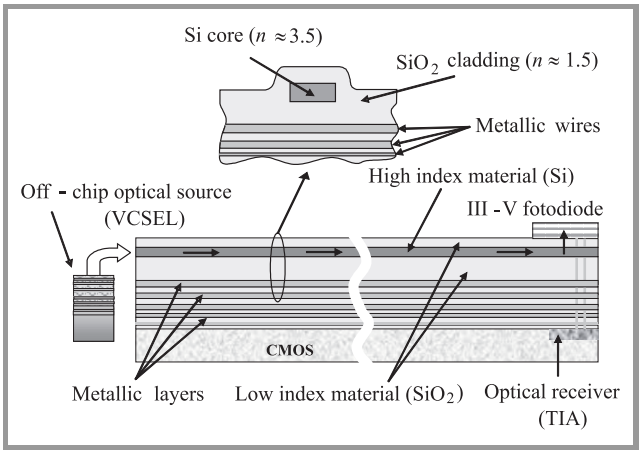

Fig. 1. Cross-section of optical interconnect structure.

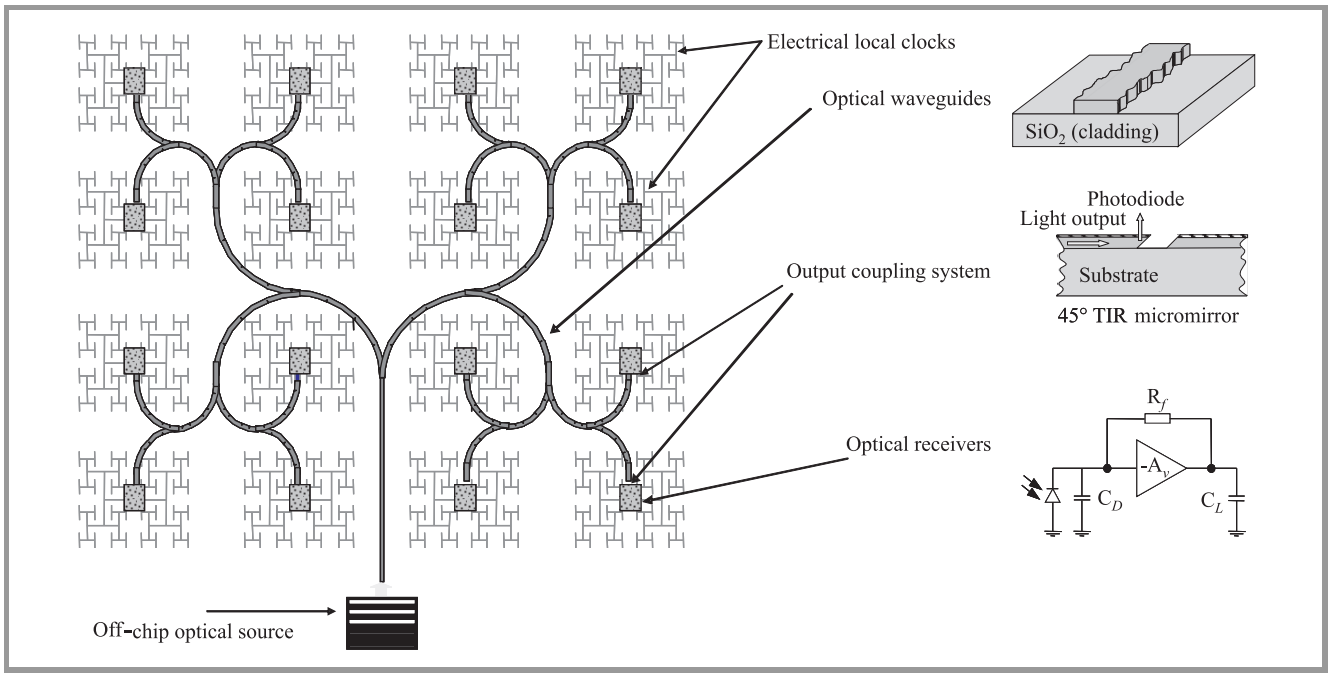

Fig. 2. General approach to optical global clock distribution network.

A tree-like structure is the most common strategy for the conventional clock system routing. This strategy is also adopted to design optical clock system. In the proposed system, shown in Fig. 2 a low-power vertical cavity surface emitting laser (VCSEL) is used as an off-chip photonic source. The VCSEL is coupled to the H-tree symmetrical passive waveguide structure and provides the clock signal to n optical receivers. The number and placement of the receivers in optical clock system is equivalent to the number and placement of the output nodes in the electrical H-tree.

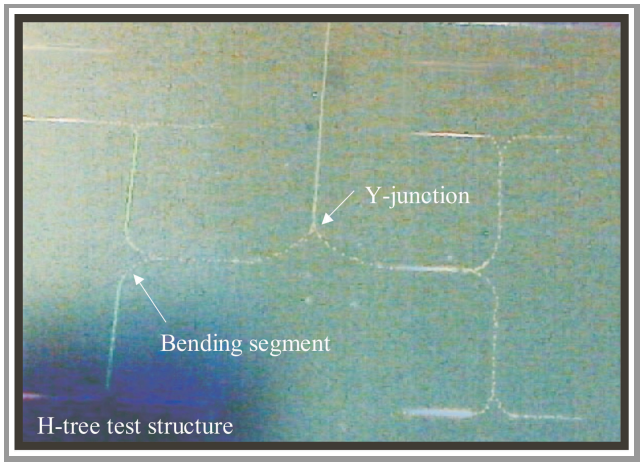

Fig. 3. Test structure of optical H-tree.

At the receivers, the high speed optical signal is converted to an electrical signal and subsequently distributed by the local electrical networks. The number of O/E converters is a particularly crucial parameter in the overall system since optoelectronic interface circuits at these points are of course necessary and consume power. The methodology and the assumptions used to properly design the optical H-tree are presented in detail in [4, 5]. Figure 3 shows a picture of the optical H-tree test structure fabricated by LETI.

3. Optical system properties

The optical alternative is, of course, acceptable only if it demonstrates significantly improved performance over the all-electrical solution. First, the power consumption of both systems is compared. The comparison is based on the ITRS technology roadmap in the case of electrical clock system and on the state-of-the-art device parameters in the case of optical clock. This assumption may result in a pessimistic estimation of the performance of the optical CDN, for future technology nodes. The results presented in Fig. 4 show the comparison between power consumption of electrical and optical clock systems both designed for the 70 nm technology node. For a small number of H-tree nodes the power

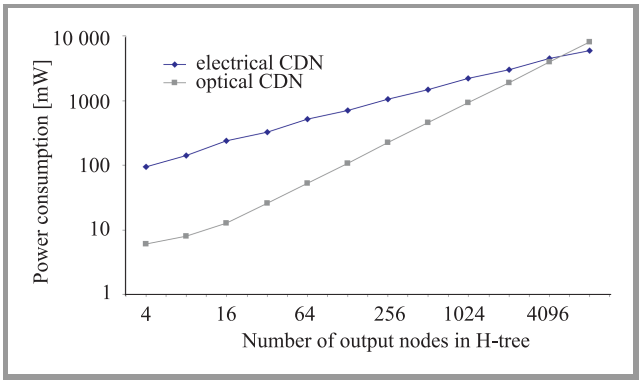

Fig. 4. Electrical power consumption of optical and electrical CDN's versus the number of H-tree nodes (20 mm chip width).

consumed by the optical H-tree is more than one order of magnitude lower than in the electrical one. However, along with the growth of circuit complexity, the advantage of the optical system tends to decrease. Finally, with 8172 output nodes in the considered case, the power consumed by the optical system becomes higher than that consumed by the electrical one. This fact can be easily explained taking into consideration the optical power budget [4, 5]. Along with doubling the number of H-tree output nodes, the optical power, which needs to be emitted by the VCSEL to meet the overall system quality increases at least by 3.2 dB (because of the Y-splitters), which in turn increases the electrical power consumed by VCSEL by more than 100%. Additionally, since the number of receivers is equal to the H-tree output nodes, the power consumed by receivers also doubles. In the case of an electrical system the power consumption increases much less rapidly. These results clearly show that the advantages of optics drastically decrease with the number of output nodes.

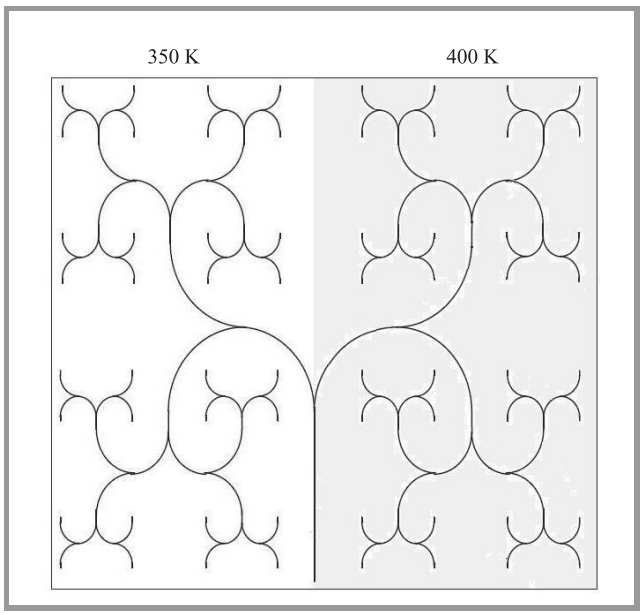

Fig. 5. Chip structure with temperature gradient.

In the next step the clock skew of the optical system is calculated. There are several sources of clock skew in optical system. Apart from process parameter variations, which are mainly the tolerance of device and waveguide physical parameters, system level fluctuations like temperature variations have to be considered. In our analysis only the impact of temperature variations on optical signal speed has been taken into account. Along with the growth of chip temperature, the refractive index of waveguide core increases thus reducing the speed of clock signal. Typical temperature gradients over the entire chip presented in literature are less then 50 K [6]. The calculation has been performed for the chip structure where the temperature of one part is lower (350 K), while that of the other part is higher (400 K) as presented in Fig. 5. This represents the worst-case scenario.

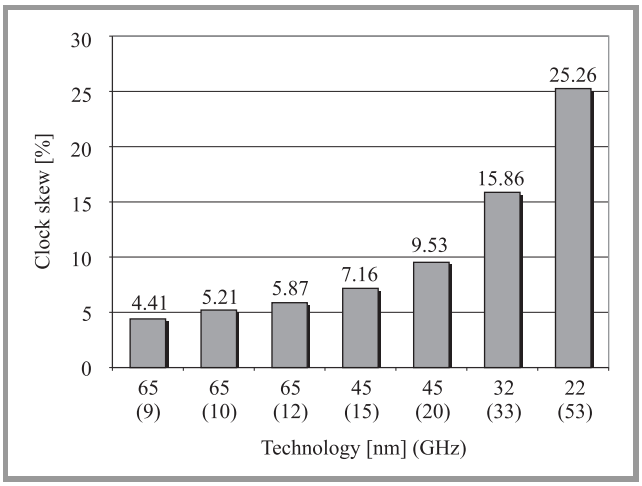

Fig. 6. Clock skew of a 64-output-node optical H-tree compared to the clock period as a function of technology.

Figure 6 shows the clock skew of a 64-output-node optical H-tree compared to the clock period as a function of technology. It is clear from this figure that just for the 32 nm technology node (33 GHz) the clock skew is higher than 10% of the clock period. This will result in a serious system failure.

4. Conclusion

Integrated optics are considered as a possible alternative to overcome metallic interconnect limitations that can be the barrier for further gigascale integration predicted by ITRS. These expectations are focused on the latency and power dissipation mainly, which should be lower when the optical interconnects are applied. In [4, 5] we demonstrate that the proposed optical solution allows the distribution of high local frequency signals across the chip with significantly lower power dissipation than the electrical one. Particularly, in the case of 45 nm technology node, the power consumed by a 256 node optical H-tree system is over 5 times less than the power dissipated in the equivalent electrical system. However, the absolute magnitude of the power dissipation in the global H-tree is a rather small part of the overall losses in the CDN system. Therefore it is necessary to increase the complexity of the optical H-tree, but the advantages of optics drastically decrease with the number of output nodes in H-tree. Additionally, a simple replacement of an electrical system by an optical CDN results in a high clock skew, which will be higher than 10% of the clock period for the 32 nm technology node. It is then clear that for the present optical technology direct replacement of classical electronic interconnections by optical ones does not exhibit a sufficient increase of the system performance (in terms of power consumption and latency). If optical interconnects are to replace metallic wires the main challenge is to develop a new generation of optoelectronics converters with low latency and low power consumption.

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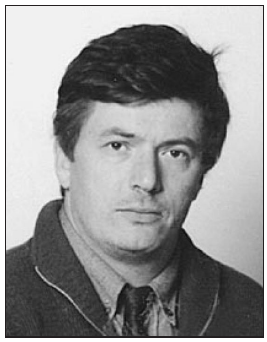

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Paper

Optimization of an integrated optical crossbar in SOI technology for optical networks on chip

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Abstract—In this paper a novel design for an optical network on chip (ONoC), enabling optical on-chip signal routing, is presented. Requirements for such a network are defined and the design of ONoC passive components is described and validated by experimental results.

Keywords—integrated optics, optical interconnections, optical filtration, add-drop filters, microdisk resonators, SOI waveguides.

1. Introduction

Electrical intra-chip or inter-chip interconnects will constitute a major bottleneck to the improvement of performance of very deep sub-micron technologies (half-pitch under 0.1 μm). Predicted limitations are formulated in terms of power consumption and latency for intra-chip interconnects and bandwidth for inter-chip interconnections. Optical solutions should enable the industry to address these problems. For example, an optical network on chip (ONoC) enables high bandwidth and low contention routing of data using wavelength multiplexing.

2. Principles of optical network on chip

The 4 × 4 ONoC is presented in this section. The basic element is an optical crossbar based on passive add-drop filters, described hereafter.

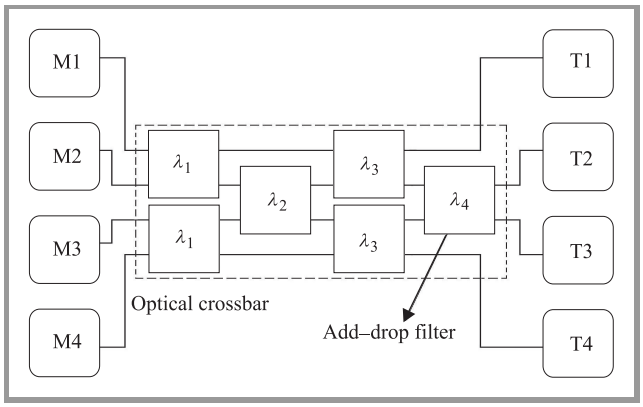

Fig. 1. A schematic overview of the 4 × 4 ONoC.

Figure 1 illustrates the 4 × 4 ONoC. The symbols *M* (masters) and *T* (targets) represent electronic subsystems (including the optoelectronic interface which is outside the scope of this paper) that need to communicate with each other. The core of the optical system, called a crossbar, is a fully passive network, based on wavelength routing. Each cell λ_i of this crossbar is a wavelength selective add-drop filter. The crossbar has to be completely reversible (each master can become a target and each target can become a master).

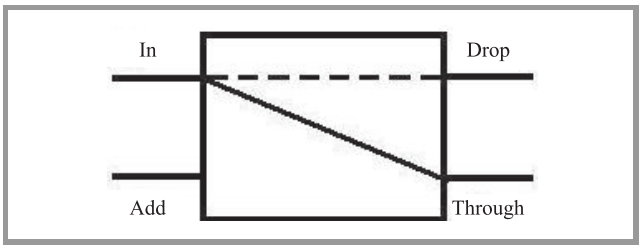

Fig. 2. Signal routing of the elementary add-drop filter (for 4 × 4 ONoC).

Figure 2 presents the design requirements for the add-drop filter in the 4 × 4 ONoC. In order to totally connect all the master ports with all the targets a specific design of the filter is necessary. For four ports placed on two parallel waveguides, it transmits non resonant wavelengths in the diagonal direction, and it drops resonant wavelengths in the straight direction. This phenomenological description allows us to establish the operation table of the crossbar given in Fig. 3.

	T1	T2	T3	T4
M1	λ_2	λ_3	λ_1	Non resonance
M2	λ_3	λ_4	Non resonance	λ_1
M3	λ_1	Non resonance	λ_4	λ_3
M4	Non resonance	λ_1	λ_3	λ_2

Fig. 3. Operation truth table of 4 × 4 ONoC.

3. Optical crossbar design

The key building blocks of the optical crossbar are the wavelength selective add-drop filters. In this section we take into consideration two types of add-drop filters: a single-disk device and a filter based on two coupled disks.
Figure 4 shows a rather complex waveguide routing scheme necessary to achieve the properties described in Fig. 2, when implementing a single-disk add-drop filter (referred to hereafter as filter A) into the optical crossbar. One can notice two intersections potentially incurring additional crosstalk and attenuation.

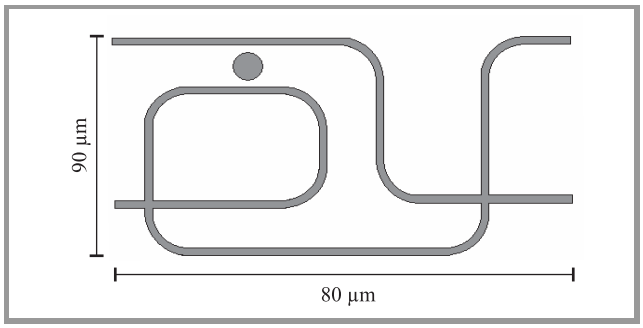

Fig. 4. Single microdisk add-drop filter waveguide routing scheme.

An alternative structure uses filters with forward dropping direction, which is the case of filters with two identical coupled microdisks, presented in Fig. 5 (referred to hereafter as filter B) [3]. This allows a simpler routing design with

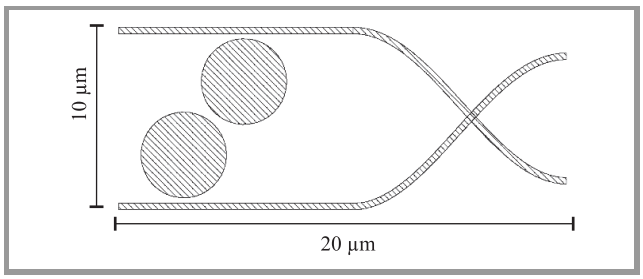

Fig. 5. Coupled two-microdisk add-drop filter waveguide routing scheme.

a smaller number of crossings. But such filters may be more sensitive to fabrication defects, such as slightly different disk radii or a difference of coupling between disks and guides.

4. Fabrication of the optical crossbar demonstrators

Both types of crossbars have been fabricated using SOI technology of CEA-LETI in Grenoble, which allows compact integration and is compatible with silicon microelectronics. Deep UV photolithography has been used to fabricate the samples. In the crossbar based on filter A (Fig. 6),

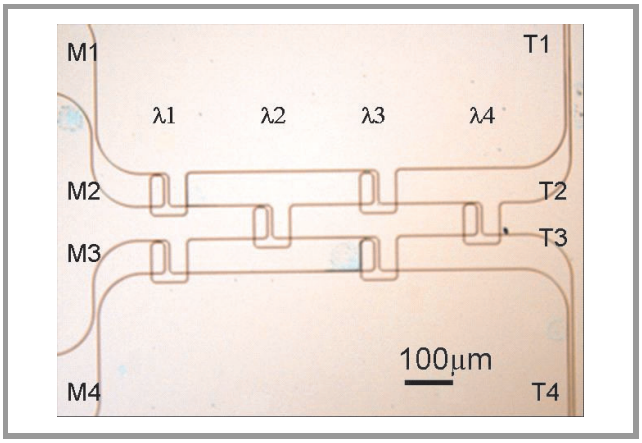

Fig. 6. Demonstrator of ONoC based on single-disk add-drop filters. Radii: 1.5 μm (λ_1), 2 μm (λ_2), 2.5 μm (λ_3), 1 μm (λ_4).

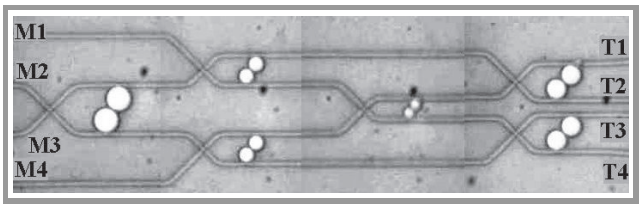

Fig. 7. Demonstrator of ONoC based on coupled two-disk add-drop filters. Radii: 2.5 μm (λ_1), 1.5 μm (λ_2), 1 μm (λ_3), 2 μm (λ_4).

the bend radius has to be large enough to avoid radiative losses; it is then far less compact than the crossbar based on filter B (Fig. 7).

5. Optical crossbar characterization results

The crossbars have been characterized using an edge coupling insertion losses optical bench. The source used in the characterization is a tuneable laser. An InGaAs CCD allows the observation of the top scattered light.

5.1. Characterization of the optical crossbar based on single-disk add-drop filter A

Figure 8 presents the light switching in the optical crossbar, depending on the injected wavelength. Light is injected to the input M1 and subsequently collected at the outputs T1…T4. At the wavelength of 1530 nm a non-resonant transfer to port T4 is observed (Fig. 8a); at 1515.3 nm, the signal is dropped to port T3 (Fig. 8b); at 1510.55 nm, to T2 (Fig. 8c), and at 1508 nm, to port T1 (Fig. 8d).
One can notice the directional transfer of most of the signal at the resonant dropping wavelengths of the filters λ_1, λ_2, λ_3. The bright points correspond to scattered losses at waveguide intersections.

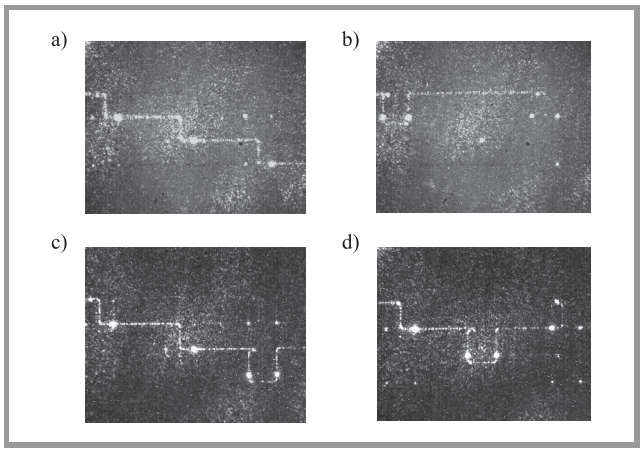

Fig. 8. Images of crossbar based on single-disk filter for wavelengths: (a) 1530 nm; (b) 1515.3 nm; (c) 1510.55 nm; (d) 1508 nm injected into port M1.

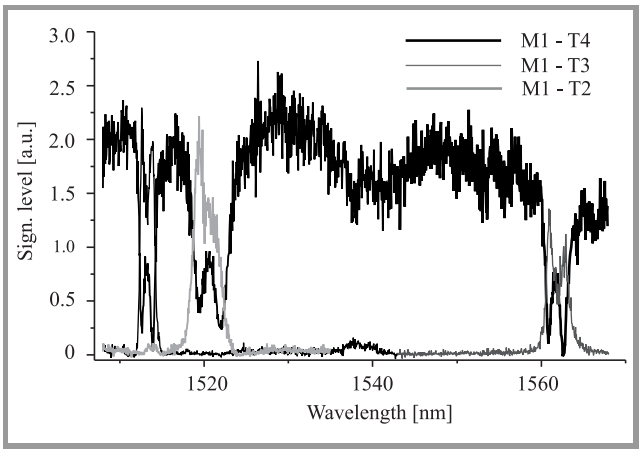

Fig. 9. Transmission spectra of the signal injected into port M1 and collected at the different outputs of the optical crossbar based on coupled two-disk add-drop filter.

Table 1 reports the transfer wavelengths of most of the different routing configurations. It should be noted that filter λ_4 does not exhibit any resonant wavelength: due to the fact that its radius is too small (1 μm), the resonant gallery modes suffer from high losses. This makes it impossible to route the signal from port M2 to T2 and from port M3 to T3.

Table 1
Transfer wavelengths [nm] of the crossbar based on single-disk filter

Port	T1	T2	T3	T4
M1	1508	1510	1515.5	Non resonance
M2	1510	Impossible	Non resonance	1515.5
M3	1515.5	Non resonance	Impossible	1510
M4	Non resonance	1515.5	1510	1508

5.2. Characterization of the crossbar based on coupled two-disk add-drop filter B

Figure 9 presents the experimental spectra of the optical crossbar based on add-drop filter B. In this figure non-resonant transmission from port M1 (see Fig. 7 for reference) to port T4 is presented. One can also observe resonance dropping of the signal to port T3 (with the wavelength of 1513 nm) and to port T2 (1520 nm). The wavelength of 1513 nm is the resonance wavelength of the filter with disk radii of 2 μm and the 1520 nm of the one with disk radii of 1.5 μm. The free spectral range of 50 nm is also shown in this figure. Dropping from port M1 to port T1 is impossible due to incorrect operation of the add-drop filter with disk radius of 1 μm.

A close-up of the optical crossbar transmission spectrum is presented in Fig. 10. One can observe a splitting in the resonance peak caused by the strong coupling between the microdisk resonators of add-drop filters. The low quality factor of these resonant peaks is caused by strong coupling between the disks and the waveguides. Due to the smaller radii of the resonators (1.5 μm versus 2 μm) the gallery mode confinement at 1520 nm is much weaker than at 1513 nm. This weaker confinement results in a wider peak and a lower quality factor at 1520 nm than at 1513 nm.

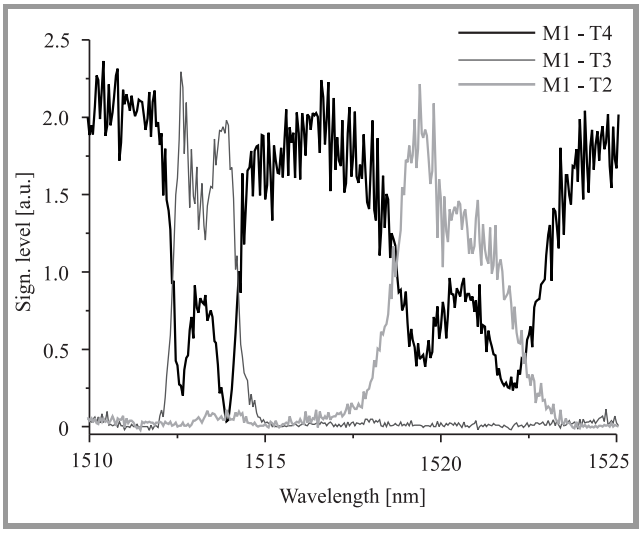

Fig. 10. Close-up of the transmission spectra of the optical crossbar in the range of 1510–1525 nm.

6. Optimization of the optical crossbar: the improved design of the filter

Both designed types of crossbar are operational and allow 4 × 4 optical communication. Although they suffer from

imperfections and cannot be directly applied without improvements, they show that the ONoC does operate as predicted. As an improvement to the basic structure we now present an improved type of channel-dropping filter based on two microdisk resonators which, when used in an optical crossbar, can potentially both amplify the strong points and reduce the weaknesses of both types of crossbar that were previously presented.

6.1. Operation principles of the cross based two-disk add-drop filter

In Fig. 11 a design for a cross based two-disk add-drop filter (referred to hereafter as filter C) is presented. It consists of two microdisk resonators coupled with the waveguide

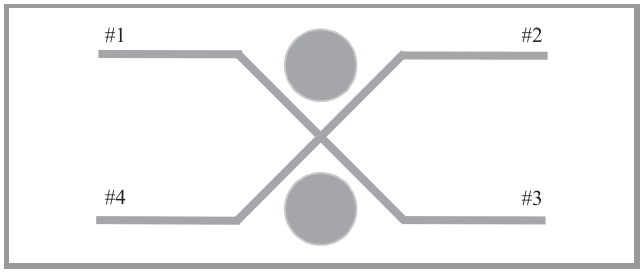

Fig. 11. Design of a novel type of add-drop filter based on two-microdisk resonators.

intersection. This type of design described in [4] has several advantages:

– it allows simpler waveguide routing compared to the 1st type of add-drop filter;

– thanks to the central symmetry the properties of the filter do not depend on the port into which the transmitted signal is injected;

– due to the fact that the two microresonators are coupled via waveguides it is not as sensitive to micro-

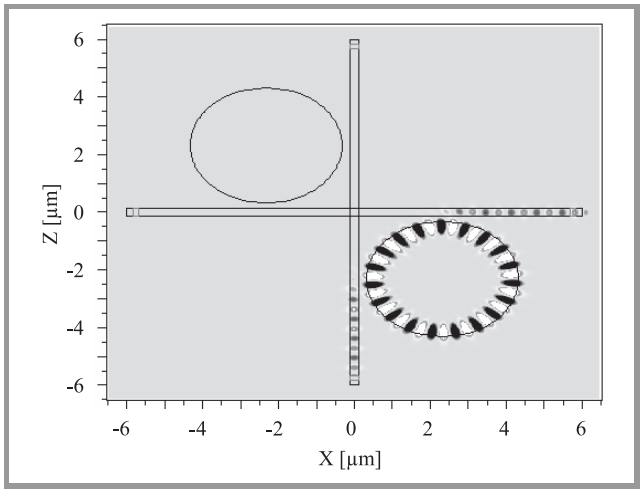

Fig. 12. The 2DFDTD simulation of electromagnetic field distribution for resonant wavelength of 1570 nm.

resonator imperfections as add-drop filter B (more particularly, a difference between the radii of the two-disk filter B drastically reduces the transmittance, whereas it introduces only a split in the transmittance spectrum of the filter C).

Figure 12 displays the 2DFDTD simulation of the add-drop filter C. At the resonant wavelength the light is fully removed from the injection waveguide and dropped to the output waveguide through the gallery mode of the first disk "met" by the light, as shown in Fig. 12. Thus at this wavelength losses of the waveguide intersection do not affect the level of the dropped signal.

6.2. Design of the optical crossbar based on add-drop filters C

The above mentioned advantages of the cross based add-drop filter allow the design of an optical crossbar that should be a good compromise between the properties of the two crossbar designs described earlier in this paper. It should also eliminate their weaknesses.

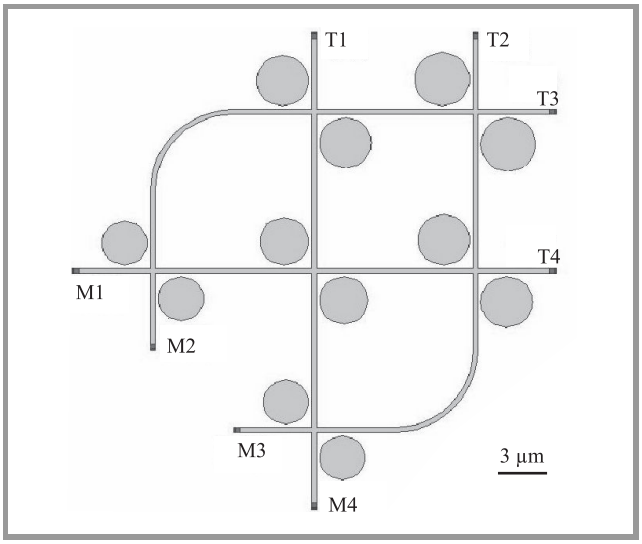

Fig. 13. Design of the optical crossbar with add-drop filters C.

Figure 13 presents the design of the optical crossbar with add-drop filters C. This design is very promising due to the minimized number of intersections and reduced area compared to the crossbar with add-drop filters A. With this design we can also avoid the problems with disk uniformity-very important in the crossbar with add-drop filters B. In this design we implemented microdisk resonators with the radii of 1.5 μm, 1.55 μm, 1.6 μm and 1.65 μm.

6.3. The 2DFDTD simulations of the 3rd type add-drop filter based crossbar

The operation of the optical crossbar has been validated with 2DFDTD simulation. Figure 14 presents the simulation spectra of the transmission from input port M1 to the four output ports. One can observe dropping to all

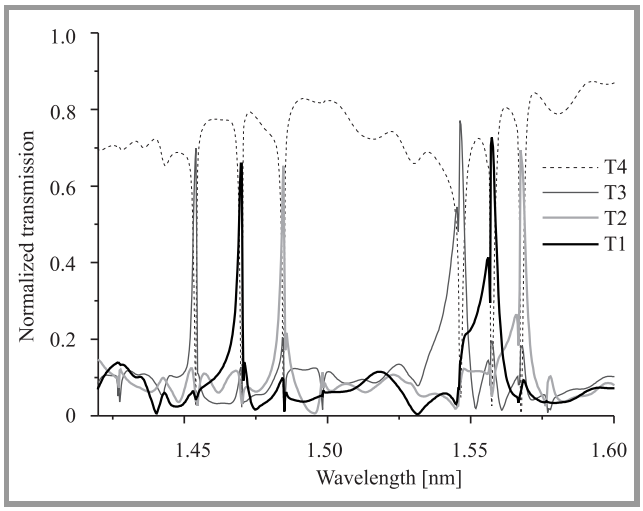

Fig. 14. The 2DFDTD simulation of the optical crossbar with add-drop filters C.

the output ports with a signal level better than 70% between 1500 nm and 1600 nm and the free spectral range of about 100 nm for the filters with radii of 1.5 μm, 1.55 μm and 1.6 μm.

7. Conclusions

Two types of 4 × 4 optical crossbars have been designed, fabricated and characterized. Both crossbars have been demonstrated to operate correctly despite losses. These losses occur mainly either at waveguide intersections in the case of the crossbar based on single-disk filter, or in the microdisks themselves in the case of the crossbar based on coupled two-disk filter. The introduction of a new type of filter, with two uncoupled disks separated by a single crossing may both enable a simple design and reduce the losses.

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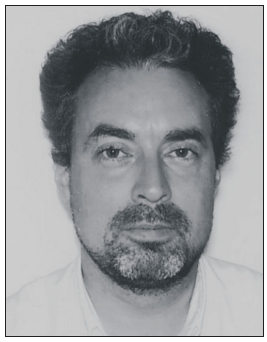

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Frederic Gaffiot and **Zbigniew Lisik** – for biographies, see this issue, p. 108.