

Invited paper

Charging Phenomena at the Interface Between High- k Dielectrics and SiO_x Interlayers

Olof Engström, Bahman Raeissi, Johan Piscator, Ivona Z. Mitrovic, Stephen Hall,
Heinrich D. B. Gottlob, Mathias Schmidt, Paul K. Hurley, and Karim Cherkaoui

Abstract—The transition regions of $\text{GdSiO}/\text{SiO}_x$ and $\text{HfO}_2/\text{SiO}_x$ interfaces have been studied with the high- k layers deposited on silicon substrates. The existence of transition regions was verified by medium energy ion scattering (MEIS) data and transmission electron microscopy (TEM). From measurements of thermally stimulated current (TSC), electron states were found in the transition region of the $\text{HfO}_2/\text{SiO}_x$ structures, exhibiting instability attributed to the flexible structural molecular network expected to surround the trap volumes. The investigations were focused especially on whether the trap states belong to an agglomeration consisting of a single charge polarity or of a dipole constellation. We found that flat-band voltage shifts of MOS structures, that reach constant values for increasing oxide thickness, cannot be taken as unique evidence for the existence of dipole layers.

Keywords—defects, dielectrics, high- k , metal oxide semiconductor.

1. Introduction

The gate function of future metal oxide semiconductor (MOS) transistors has attracted a large scientific community to an expedition into the periodic system for tracking the Dielectric Grail. Wanted is a material with acceptable energy offset values, ΔE , between the energy bands of the dielectric and the silicon crystal while, in addition, having a high enough dielectric constant, k . Yet, to fulfill the demands of low current leakage and high capacitive coupling between gate metal and transistor channel, the crucial property is the product $k \times \Delta E$ of these two quantities [1]. So far, for CMOS applications most of the efforts have been limited to metal oxides. The change from the extremely well mastered thermal SiO_2 material, to an oxide based on metals among the transition or rare earth series, has disclosed obstacles that were unnoticeable for traditional technology. Beside the problems of chemical stability between these new “high- k ” oxides and the silicon substrate, crystallization, sensitivity to humid environment, higher concentrations of oxide traps and interface states are properties, not uncommon among these materials. Driven by technology, this has given rise to needs for understanding their microscopic properties from chemical, physical and electrical point of view.

A common attribute of high- k oxide films deposited on silicon is the occurrence of an SiO_x interlayer between

the high- k material and the silicon crystal. This evokes interface electron state properties similar to those at thermal SiO_2/Si interfaces [2], [3]. Even if the interlayer lowers the effective k value of the film, it often gives better conditions for a transistor channel than those offered by a direct interface due to lower charge carrier scattering by the former. However, it must be paid for by an extra interface occurring between SiO_x and the high- k material [4]. As the total physical thickness of the film is in the range of 5 nm or smaller, on this length scale the transition from SiO_x to the high- k material can hardly be considered abrupt. It is found to include a transition region with undefined stoichiometry and thus with possible structural instabilities [5]–[11]. Recently, the occurrence of traps either singular or in dipole configurations have been noticed as the potential origin of charge sources decreasing the quality of presumptive gate insulators [11]–[16]. In the present paper, we will describe the physical and electrical properties of transition regions at $\text{GdSiO}/\text{SiO}_x$ and $\text{HfO}_2/\text{SiO}_x$ interfaces and demonstrate how charge carrier traffic at such positions can be interpreted in order to characterize the trap properties. Based on this reasoning, the possible existence of a dipole layer in the transition region will be addressed.

2. Properties of Transition Regions

The dominating defect causing charge carrier traps in the bulk of transition and rare-earth metal oxides is commonly considered to be the oxygen vacancy. It has similar properties as the E' center in SiO_2 and has been the object of a rich theoretical [15], [16] and experimental [10], [11] literature. In HfO_2 it has been predicted to be an amphoteric center with four [15] or five [16] charge states ranging from double donor to double acceptor behavior with the latter states positioned in the range 1–2 eV from the HfO_2 conduction band edge. Furthermore, the double acceptor level is argued to be connected with large lattice relaxation [16]. It has even been proposed that the double negatively charged energy level falls below the single negatively charged level, thus exhibiting negative-U property [17]. These trap properties will be further discussed below in relation to the results from electrical measurements.

As one example of the complex high- k oxide/ SiO_x interface, we will discuss data from GdSiO . This dielectric was

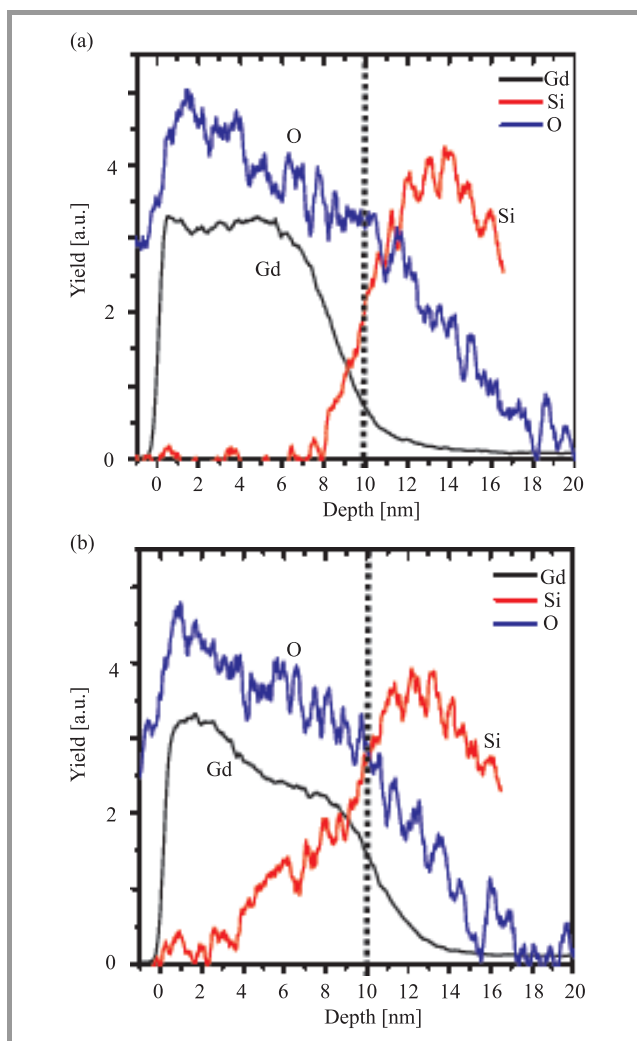


Fig. 1. MEIS data for samples with GdSiO evaporated on top of a 4 nm thermal oxide: (a) as deposited and (b) after RTA at 900°C for 1 s.

prepared by evaporating Gd_2O_3 on a 4 nm thick thermal SiO_2 layer on silicon [18]–[21]. The double layer was partly transformed into GdSiO by rapid thermal anneal (RTA) for 1 s at 900°C. The depth distribution of elements before and after the thermal anneal is shown by medium energy ion scattering (MEIS) data in Fig. 1. A steeply decreasing silicon concentration from the silicon side into the oxide directly after deposition (Fig. 1(a)), reflects a complicated diffusion process taking place already at this stage. At the 10 nm mark, the concentration of oxygen is a factor of 2 higher than the concentration of silicon. This indicates a reminiscence of SiO_2 which quickly becomes a suboxide at larger distances from this interface, where a nearly stoichiometric Gd_2O_3 takes over. The extremely high gradient of Si at the 10 nm point would be expected to stage structural instability. After the RTA at 900°C, silicon has penetrated the whole oxide layer (Fig. 1(b)) creating a GdSiO with varying concentration of Si. This structure has been demonstrated to fulfill the industrial target for low standby power, 22 nm double gate SOI transistors [18].

A second example is given by a transmission electron microscopy (TEM) picture showing the interface between HfO_2 and SiO_x in Fig. 2. This sample was prepared by reactive sputtering of Hf and O_2 followed by an anneal at 800°C for 10 min [12]. Between the white string showing the SiO_x layer and HfO_2 , appearing as a black area,

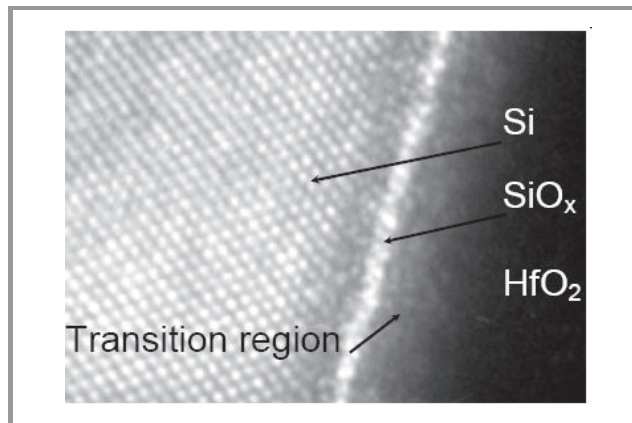


Fig. 2. TEM graph from a cross section of $\text{Si}/\text{SiO}_x/\text{HfO}_2$, where the HfO_2 layer was deposited by reactive sputtering.

a milky band is shown with a width of about 2 nm. Here, one may expect the same type of diffusion taking place as in the case of GdSiO above. As will be shown below, traps formed in this region consequently have an unusual electric behavior.

3. Charge Carrier Traffic at Transition Regions

3.1. Energy Relations and Charge Exchange

We consider an interface between a high- k oxide and an SiO_x interlayer on silicon as schematically shown in Fig. 3. The transition region is marked by a wide patterned band and includes a trap level at an energy distance ΔE below the silicon conduction band edge. A negative net charge is present in the interlayer, such that an electric field F is directed from the silicon crystal towards the high- k oxide. Assuming that the thickness of the interlayer is about 1 nm, tunneling through this layer is non-negligible and can be described as assisted by a decay of the effective density of states, N_C , from the silicon conduction band determined by $N_C \exp[-x_0/\lambda]$, where x_0 is the distance from the SiO_x/Si interface to the trap and λ is a damping factor. A captured electron can be transferred into the Si bulk by a two step process, starting with a thermally driven mechanism to the tunneling states at the energy level of the silicon conduction band edge. As long as the electric field is high enough, this process is followed by tunneling into the silicon conduction band as depicted in Fig. 3. Emitting electrons from the trap position will lower the electric field. The system

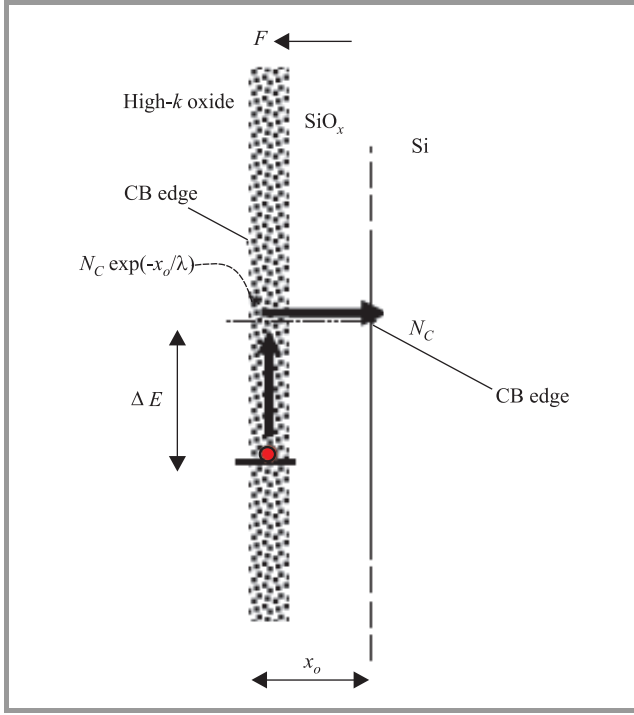


Fig. 3. Two step emission path of electrons captured in traps positioned in the transition region. The first step is thermal, to decaying states from the silicon conduction band followed by tunneling to the silicon.

may, therefore, reach a situation where the electric field becomes too low for the second transfer step to occur, which means that the emission process stops. As the tunneling probability is very sensitive to the magnitude of the electric field, this termination may be very abrupt as we will see in the experimental data following.

As long as the tunneling rate dominates, the bottleneck of this process is the thermal electron emission rate, e_n , from the trap to an effective density of states decreased by the tunneling probability

$$e_n = \sigma_n v_{th} N_C \exp\left(-\frac{x_0}{\lambda}\right) \exp\left(-\frac{\Delta E}{k_B T}\right), \quad (1)$$

where σ_n is the capture cross section representing a local transition from the tunneling state to the trap state, v_{th} is the average thermal velocity of electrons in the silicon conduction band, k_B is Boltzmann's constant and T is absolute temperature. As will be described in detail below, using thermally stimulated current (TSC) technique to determine the emission rate, the temperature is linearly increased with time during the measurement cycle. As the electric field, F , decreases due to the decrease of negative charge in the SiO_x layer, the energy distance ΔE will increase. In addition, the temperature increase will move the Fermi level in the silicon bulk to deeper energy in the band gap. For a given applied voltage across the structure, this will lower the position of the silicon conduction band edge at the SiO_x/Si interface which will increase the voltage drop across the interlayer and tend to decrease ΔE . Assuming, as a first

order approximation, that both these processes are linear with temperature, we write

$$\Delta E = \Delta E_0 - \alpha T, \quad (2)$$

where ΔE_0 is the energy distance between the silicon conduction band edge and the trap level extrapolated to $T = 0$ K and α is a constant determined by the two competing processes described above. Using Eq. (2) in (1), we get

$$e_n = \sigma_e v_{th} N_C \exp\left(-\frac{\Delta E_0}{k_B T}\right), \quad (3)$$

where

$$\sigma_e = \sigma_n \exp\left(\frac{\alpha}{k_B}\right) \exp\left(-\frac{x_0}{\lambda}\right) \quad (4)$$

can be considered as an effective capture cross section, influenced by the changing energy level position and the tunneling probability. We notice that, measuring the emission rate as a function of temperature and plotting this quantity in an Arrhenius graph would give an activation energy corresponding to an extrapolation of ΔE to $T = 0$ K under the assumption of linear conditions. However, this reasoning does not take into account the properties related to local molecular dynamics of the trap volume.

For a case like the oxygen vacancy, where the transition is argued to be connected with a strong lattice relaxation [16], the emission process would be influenced also by the vibronic properties of the trap [21] and characterized by “hysteretic tunneling”, adding a simultaneous trap relaxation and tunneling into the picture [22]. This would lead to two additional pre-exponential factors in the expressions for the thermal emission rate one originating from a possible thermally activated σ_n :

$$\sigma_n = \sigma_0 \exp\left(-\frac{\Delta U}{k_B T}\right), \quad (5)$$

where σ_0 depends on a combination of matrix elements including electronic and atomic wave functions involved in the process while ΔU is an activation energy originating from the vibrational properties of the trap system [21], [23]. The second effect comes from the entropy factor [21], [23], [24]:

$$X_n = \exp\left(\frac{\Delta S}{k_B}\right), \quad (6)$$

where ΔS is the change in entropy due to the change in vibrational frequency of the ionic part of the trap when the electron is released. Hence, combining the effects of the change in ΔE due to de-charging and those of a vibrating electron-ion trap system, we find from Eqs. (1)–(6):

$$e_n = \sigma_0 \exp\left(-\frac{\Delta U}{k_B T}\right) \exp\left(\frac{\Delta S}{k_B}\right) \exp\left(\frac{\alpha}{k_B}\right) \times \exp\left(-\frac{x_0}{\lambda}\right) v_{th} N_C \exp\left(-\frac{\Delta H_0}{k_B T}\right), \quad (7)$$

where the activation energy now is represented by an enthalpy, $\Delta H_0 = \Delta E_0 + \Delta S T$, including the heat, $\Delta S T$, stored by the local vibrational modes [21], [23], [24].

For this case the first factors in Eq. (7) make up an “effective” capture cross section, σ_e , which would be obtained from an Arrhenius plot of the thermal emission rate, e_n :

$$\sigma_e = \sigma_0 \exp\left(-\frac{\Delta U}{k_B T}\right) \exp\left(\frac{\Delta S}{k_B}\right) \exp\left(\frac{\alpha}{k_B}\right) \exp\left(-\frac{x_0}{\lambda}\right). \quad (8)$$

As will be shown below, TSC results demonstrate instabilities among the traps investigated in the HfO₂/SiO_x transition region. This is most probably originating from restructuring of the molecular arrangement around the trap volume, thus changing the matrix elements for charge carrier transition involved in σ_0 as well as quantities of the vibrational properties reflected by ΔU , ΔS , and ΔH_0 in Eqs. (7) and (8).

3.2. Thermally Stimulated Current

When measuring TSC from traps in a MOS system [12], the sample is first brought into accumulation at room temperature followed by a temperature decrease to about 50 K. During this procedure, traps at the interface and in the oxide are filled by charge carriers. At the low temperature point, the system is biased into deep depletion and a temperature increase, linear as a function of time, is applied. For an n-type semiconductor this gate bias is negative. As long as the temperature is lower than about 200 K and the total scanning time up to that temperature is shorter than

about 10 min, it should be noticed that, due to the low temperature, an extremely low concentration of holes is expected in the valence band of the silicon crystal. Therefore, all de-charging processes observed as a TSC can be expected to originate from electron exchange at the insulator/silicon interface. The current created by emitted electrons is expressed by [12]

$$i(T) = \frac{C_{ox}}{C_s + C_{ox}} q N_T e_n \exp\left[-\int_{T_0}^{T_1} \beta e_n(u) dU\right], \quad (9)$$

where C_{ox} and C_s are the capacitances of the oxide and the depleted semiconductor, respectively, N_T is the surface concentration of captured carriers and β is the scanning rate of the temperature, linear in time, t , such that $T = \beta t$. The function given by Eq. (9) is plotted in Fig. 4(a) for an activation energy of 0.13 eV and an effective capture cross section of 10^{-24} cm². Using the rather complicated expression in Eq. (8) for parameter extraction from experimental data is not practical. However, calculating the integral factor in this equation as a function of temperature, for the same input data as used above, one finds the graph shown in Fig. 4(b). It is noticed that the integral takes a value close to 1 for the initial part of the TSC curve in Fig. 4(a). Furthermore, as $C_{ox} \gg C_s$ for the deep depletion conditions used in the experiment, this part of the experimental data is proportional to the thermal emission rate e_n . Estimating the total concentration, N_T , of trap levels from the area under the TSC peak, therefore, gives a possibility to find effective capture cross sections from Arrhenius plots of e_n [12].

3.3. Experimental TSC Results on the HfO₂/SiO_x Interface

Figure 5 shows experimental TSC data from electron emission in the transition region of an MOS capacitor with an Al/HfO₂/SiO_x/Si structure like the one shown by TEM in Fig. 2. Two important features can be observed in Fig. 5:

- 1) repeated measurement gives a different TSC peak position on the temperature scale;
- 2) the TSC curves are terminated before they reach the maximum point of the theoretical curves (solid curves) fitted to the experimental data.

These results are typical and occur for a large majority of the present samples with HfO₂ prepared by reactive sputtering as well as for samples prepared by atomic layer deposition (ALD) [25]. The observation (1), reveals an instability of the traps as mentioned above in relation to Eq. (9). Such instability after voltage stress under similar conditions as in the present experiment, was observed also by Bersuker *et al.* in [10]. The observation (2), can be interpreted as a result of the tunneling process involved in the electron emission. During the emission process, the negative charge in the transition region, born by the captured

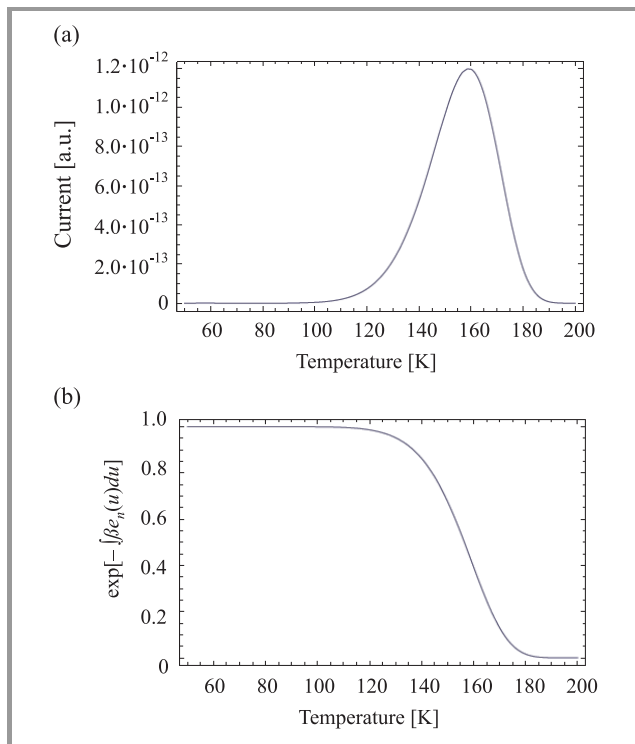


Fig. 4. (a) Theoretical plot of thermally stimulated current for an activation energy of 0.13 eV, an effective capture cross section of 10^{-24} cm² and a temperature scan rate of 20 K/minute. (b) The integral factor in Eq. (9) as a function of temperature. This function is close to 1 for the initial part of the curve in (a).

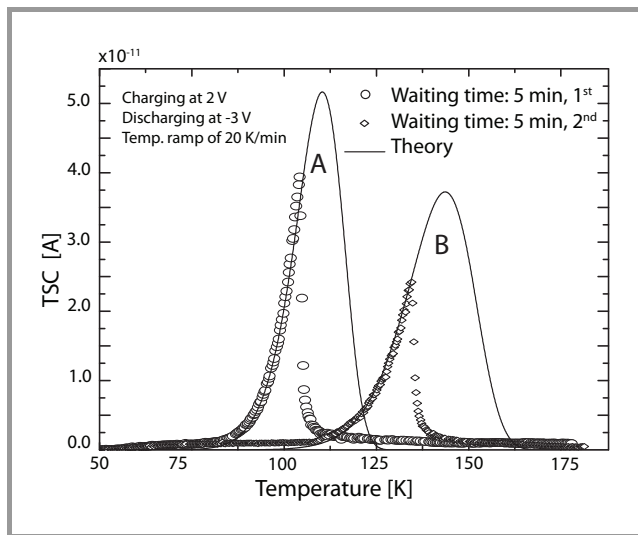


Fig. 5. Experimental TSC data (points) for MOS structures with HfO₂ prepared by reactive sputtering compared with theoretical calculations (solid curves) calculated from Eq. (9). Repeated measurement gave rise to a shift of the TSC peak along the temperature axis, reflecting structural changes of the emitting electron traps. The activation energy for the curves A and B is 0.13 eV and 0.16 eV, respectively, and the corresponding capture cross sections are $6 \cdot 10^{-22}$ cm² and $9 \cdot 10^{-21}$ cm², respectively.

electrons, will decrease. This will decrease the electric field driving the tunneling until the field strength is too weak for continued emission. As the tunneling probability is very sensitive to a change in electric field, the TSC will get an abrupt termination as shown for the two curves in Fig. 5.

4. Single Charge Versus Dipole Charge

The recent increasing interest in the properties of high-*k*/SiO_x transition layers includes novel ideas about a possible occurrence of closely separated charge planes with different polarities within this region [13]. It has been described as dipole planes occurring as a result of oxygen transfer across the interface between the high-*k* and the SiO_x material [14]. According to an idea proposed in [14], such transition would take place from the material with the highest surface density of oxygen atoms to that with lower density. For transition metal oxides, like HfO₂, this would imply that oxygen is transferred from this material into SiO_x, creating interstitials and leaving oxygen vacancies behind. As the relation between oxygen surface densities of rare-earth metal oxides, like Gd₂O₃ and SiO_x is the opposite, such transfer would instead go from the SiO_x to the high-*k* side.

The influence of a single negative charge and a dipole surface on the conduction band relations for the metal/HfO₂/SiO_x/n-type Si structure is depicted in Fig. 6. The geometries are shown in Fig. 6(a), while Fig. 6(b) and Fig. 6(c) show the charge relations and the conduction band relations for an open circuit case and a short circuit case, respectively. In order to demonstrate the specific influences of these charge planes, we assume that no other charges

are present in the structure. Considering first the single charge case in the left column of Fig. 6 for an open circuit case in Fig. 6(b), where the opposite positive charge is assumed to exist at a long distance, the electron energy of the whole structure is lifted in parallel in relation to an earth plane. Short circuiting, as shown in Fig. 6(c), will cause positive charge to appear at the metal gate and in the depletion region occurring in the n-type semiconductor. Compared with an ideal structure without charge, an increased positive voltage, V_{FB} , on the gate would be needed to obtain flat-band condition for this case. Furthermore, V_{FB} would increase linearly with increasing thickness of the HfO₂ layer.

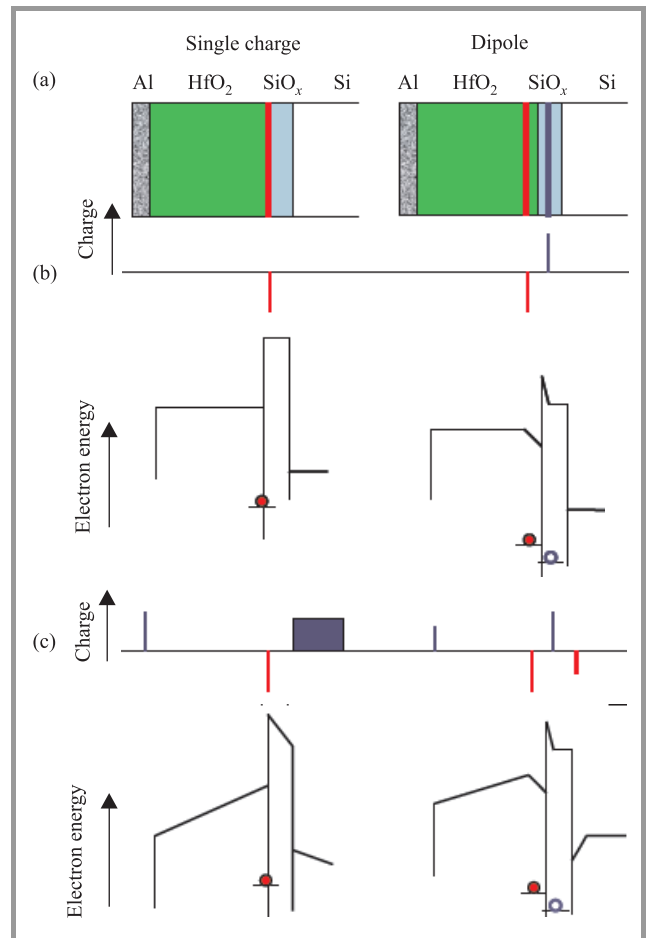


Fig. 6. Illustration of (a) charge configuration, and conduction band relations for (b) open circuit and (c) short circuit conditions of a metal/high-*k*/SiO_x/Si structure. The columns demonstrate the conditions for a single charge plane (left) and a dipole plane (right), respectively.

For a dipole layer at the HfO₂/SiO_x interface, as shown in the right column of Fig. 6, under open-circuit conditions, one would expect an electric field between the two charge planes only (Fig. 6(b)). This would create a potential drop in that domain, while constant potentials would occur outside the two planes separated by a voltage created inside the dipole. Short-circuiting this structure gives rise to a positive charge on the gate and a negative charge in

the semiconductor, forcing the latter into accumulation condition. These two charges are exactly equal and vary depending on the HfO₂ thickness in such a way that the sum of the energy drops in HfO₂ and in the semiconductor is constant and equal to qV_{FB} . In this case a negative V_{FB} , equal to the potential drop inside the dipole, is needed to obtain flat-band conditions. However, contrary to the situation with a single negative charge, the dipole combination would give a V_{FB} which is independent of the thickness of HfO₂. Such a behavior was indicated in [14] for HfO_x/Si_x interfaces.

The single charge case demonstrated by Fig. 6(a) offers a model for straightforward explanation of the anomalous TSC data as discussed in Section 3. The dipole case in Fig. 6(b) likewise gives rise to an energy relation of the conduction bands supporting electron injection into the silicon and thus a TSC with similar behavior as that from a single negative charge plane. Therefore, TSC does not give direct information on which of these two charge constellations is the source of current.

5. Discussion

In order to explain the saturating flat-band voltage and its positive sign as observed in [12] when increasing the thickness of HfO₂, the idea put forward in [13] requires injection of negatively charged traps from the high- k side into SiO_x. This would give rise to a dipole directed in the opposite way to that discussed in relation to Fig. 6. Such a model is not completely unproblematic. First, injecting an oxygen ion from the HfO₂ into the SiO_x layer might be expected to give rise to an interstitial, leaving behind a vacancy in the HfO₂. According to recent theoretical results [15], [16], vacancies are amphoteric and act as acceptors with energy levels at about 1.5 eV from the HfO₂ conduction band. They may therefore tend to be filled by electrons from the silicon conduction band and thus become negatively charged. On the other hand, the donor levels connected with oxygen vacancies are expected close to the middle of the bandgap of HfO₂ and are most probably occupied by electrons and neutral at voltages of the flat-band values at about 0.5 V in [13]. The origin of positive charge required on the HfO₂ side, therefore, is questionable.

A second problem with a dipole model may be the quantity of charge needed to obtain V_{FB} shifts in the range of 0.3 – 0.5 V as observed in [13]. As the thickness of the SiO_x layer normally is about 1 nm, the maximum value for the distance between the two charge sheets of an assumed dipole would be about that value. In order to achieve a shift of 0.3 V, this requires a charge density of more than $5 \cdot 10^{15} q \text{ As cm}^{-2}$. It can be compared with the charge contained in the TSC curves of Fig. 5, which is in the range of $10^{13} q \text{ As cm}^{-2}$. Finally, the strongest argument for a dipole model might be the saturating flat-band voltage. However, this result does not uniquely lead to a dipole configuration as shown in the following. Taking into account the continuous character of the transition region, a satu-

rating V_{FB} may result also from single charge condition. Contrary to the assumption made in [13], the transition from HfO₂ to SiO_x cannot be considered abrupt on length scales in the range of a few nm. As noticed in Fig. 1, the oxygen concentration increases with distance from the silicon side due to diffusion into the silicon crystal. Similar behavior of oxygen concentration has been observed by elastic recoil detection analysis (ERDA) studies on HfPrO samples [26]. Therefore, it is reasonable to assume that the concentration of oxygen vacancies decreases with distance from the silicon side. Furthermore, assuming that thinner HfO₂ layers, due to the out-diffusion of oxygen to the surface, also as observed in Fig. 1, have a lower decay of vacancies, it is probable that they have a smaller decay in concentration.

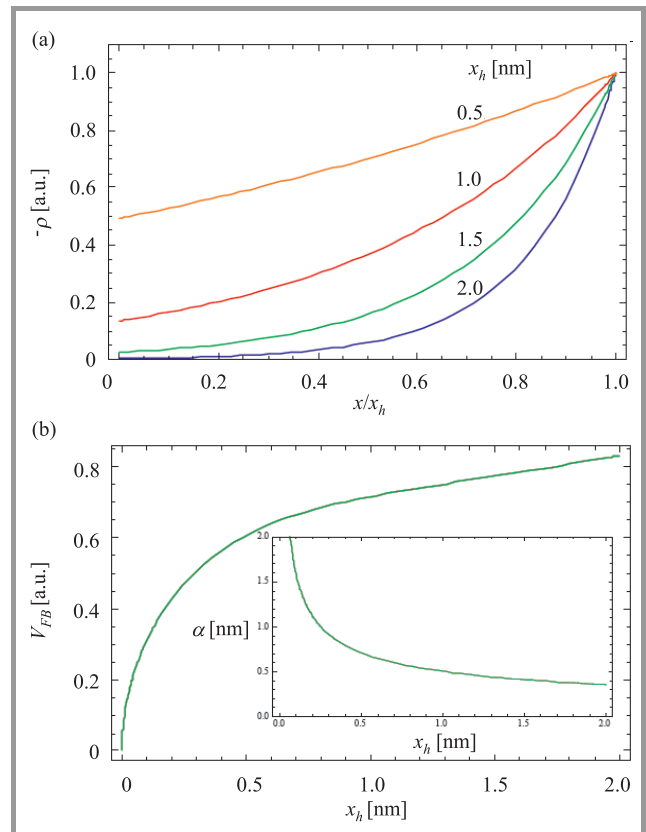


Fig. 7. (a) Assumed depth distribution of acceptor state volume concentrations in the transition region for HfO₂ with thicknesses of 0.5, 1.0, 1.5 and 2.0 nm. The point $x = 0$ is at the HfO₂ surface, while $x = x_h$ is at a reference point where SiO₂ transfers to suboxides. (b) The flat-band voltage as a function of HfO₂ thickness for acceptor concentrations as shown in (a) with the decay constant, α , varying as a function of x_h as shown in the inset of (b).

A theoretical example is shown in Fig. 7(a), where the concentration of traps is plotted for different thicknesses as a function of normalized distance from a defined reference point in the transition region. Such a point could be the one, where SiO₂ transfers to suboxides. For simplicity, the curves in Fig. 7(a) are exponential functions with decay factors, α , decreasing with the thickness x_h of HfO₂, as

shown in the inset of Fig. 7(b). Solving Poisson's equation for the functions in Fig. 7(a):

$$\frac{d^2V}{dx^2} = -\frac{\rho_0}{k\epsilon_0} \exp\left(-\frac{x_h - x}{\alpha}\right), \quad (10)$$

where V is electrical potential, ρ_0 is the volume charge density at the reference point, x_h , ϵ_0 is the dielectric permittivity of vacuum and x is distance from the HfO_2 surface, we find V_{FB} from the potential at $x = 0$ as

$$\frac{k\epsilon_0}{\rho_0} V_{FB} = -\alpha \left\{ x_h + \alpha \left[1 - \exp\left(-\frac{x_h}{\alpha}\right) \right] \right\}. \quad (11)$$

The V_{FB} normalized by the pre-factor in Eq. (11) is plotted in Fig. 7(b) as a function of HfO_2 thickness, x_h . The shape of this curve, with a tendency to saturate for increasing, x_h , was interpreted in [12] as a result of a dipole layer. Figure 7(b) demonstrates that under assumptions based on MEIS data, it is possible to obtain similar behavior from a singly charged layer.

6. Conclusions

The theoretical TSC curves shown in Fig. 5 were calculated assuming an ensemble of electron states with one common discrete energy level. The agreement between the initial curvature of these graphs and the experimental data indicates that the majority of traps observed by TSC have similar properties of their charge carrier statistics and are positioned with limited spread in distance from the silicon/ SiO_x interface. This excludes bulk traps in the HfO_2 as candidates and suggests a trap distribution concentrated at the $\text{HfO}_2/\text{SiO}_x$ interface as depicted in Fig. 7(a) for delivering electrons to the TSC. Also, TSC peaks from states at the Si/SiO_x interface are ruled out by earlier experiments as they have been demonstrated to occur at temperatures above 200 K, outside the scale of Fig. 5 [12]. The extremely low values of capture cross sections in the range $10^{-26} - 10^{-19} \text{ cm}^{-2}$, normally found by TSC for this kind of experiments [11], [27], are explained by the tunneling process needed for carrier injection into the silicon substrate and the thermally activated process expected for carrier capture into oxygen vacancies [16]. Also, taking into account the flexible structural network anticipated in the transition region, the shift of the TSC peaks as shown in Fig. 5 may be assigned to the restructuring of oxygen vacancy defects as discussed in Section 2.

The argument in [13], for the existence of a dipole plane at the interface between HfO_2 and SiO_2 layers, was based on the observation of flat-band voltage as a function of the thickness of HfO_2 . It was shown that V_{FB} saturated to a near constant value when this thickness increases as expected for a dipole charge and discussed above in connection with Fig. 6. However, such a result is not unique for a dipole. By assuming an oxygen vacancy distribution in the high- k layer as estimated from MEIS data, we have demonstrated in the present work that similar V_{FB} dependence may be the result of a single charge distribution. We conclude, therefore, that more evidence is necessary before

the existence of a dipole layer occurring in high- k/SiO_x transition regions is confirmed.

Acknowledgment

The authors collaborate under the banner of the "High- k -Gang" (<http://www.high-k-gang.eu/>). The work has benefited from funding provided by the European Network of Excellence NANOSIL within FP7 (ICT-216171).

References

- [1] O. Engström, B. Raeissi, S. Hall, O. Buiu, M. C. Lemme, H. D. B. Gottlob, P. K. Hurley, and K. Cherkaoui, "Navigation aids in the search for future high- k dielectrics: physical and electrical trends", *Solid-State Electron.*, vol. 51, iss. 4, pp. 622–626, 2007.
- [2] B. Raeissi, J. Piscator, O. Engström, S. Hall, O. Buiu, M. C. Lemme, H. D. B. Gottlob, P. K. Hurley, K. Cherkaoui, and H. J. Osten, "High- k -oxide/silicon interfaces characterized by capacitance frequency spectroscopy", *Solid-State Electron.*, vol. 52, iss. 9, pp. 1274–1279, 2008.
- [3] P. K. Hurley, K. Cherkaoui, E. O'Connor, M. C. Lemme, H. D. B. Gottlob, M. Schmidt, S. Hall, Y. Lu, O. Buiu, B. Raeissi, J. Piscator, O. Engström, and S. B. Newcomb, "Interface defects in HfO_2 , LaSiO_x and Gd_2O_3 high- k -metal-gate structures on silicon", *J. Electrochem. Soc.*, vol. 155, no. 2, pp. G13–G20, 2008.
- [4] M. A. Quevedo-Lopez, P. D. Kirsch, S. Krishnan, H. N. Alshareef, J. Barnett, H. R. Harris, A. Neugroschel, F. S. Aguirre-Tostado, B. E. Gnade, M. J. Kim, R. M. Wallace, and B. H. Lee, "Systematic gate stack optimization to maximize mobility with HfSiON EOT scaling", in *Proc. ESSDERC 2006 Conf.*, Montreux, Switzerland, 2006, pp. 113–116.
- [5] G. Lucovsky, Y. Wu, H. Niimi, V. Misra, and J. C. Phillips, "Bonding constraints and defect formation at interfaces between crystalline silicon and advanced single layer composite gate dielectrics", *Appl. Phys. Lett.*, vol. 74, no. 14, pp. 2005–2007, 1999.
- [6] G. Lucovsky, J. P. Maria, and J. C. Phillips, "Interfacial strain induced self-organization in semiconductor dielectric gate stacks. II. Strain relief at internal dielectric interfaces between SiO_2 and alternative dielectrics", *J. Vac. Sci. Technol. B*, vol. 22, iss. 4, pp. 2097–2104, 2004.
- [7] G. Lucovsky and J. C. Phillips, "Defects and defect relaxation at internal interfaces between high- k transition metal and rare earth dielectrics and interfacial native oxides in metal oxide semiconductor (MOS) structures", *Thin Solid Films*, vol. 486, iss. 1–2, pp. 200–204, 2005.
- [8] F. Giustino, A. Bongiorno, and A. Pasquarello, "Equivalent thickness of thin oxide interlayer in gate insulator stacks on silicon", *Appl. Phys. Lett.*, vol. 86, iss. 19, pp. 192901-1–3, 2005.
- [9] P. Broqvist and A. Pasquarello, "Band gaps and dielectric constants of amorphous hafnium silicates: a first principle calculation", *Appl. Phys. Lett.*, vol. 90, iss. 8, pp. 082907-1–3, 2007.
- [10] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. van Benthem, S. J. Pennycook, P. M. Lenahan, and J. T. Ryan, "The effect of interfacial layer properties on the performance of Hf-based gate stack devices", *J. Appl. Phys.*, vol. 100, p. 094108, 2006.
- [11] J. T. Ryan, P. M. Lenahan, G. Bersuker, and P. Lysaght, "Electron spin resonance observations of oxygen deficient silicon atoms in the interfacial layer of hafnium oxide based metal-oxide-silicon structures", *Appl. Phys. Lett.*, vol. 90, p. 173513, 2007.
- [12] B. Raeissi, Y. Y. Chen, J. Piscator, Z. H. Lai, and O. Engström, "Electron traps at $\text{HfO}_2/\text{SiO}_x$ interfaces", in *Proc. ESSDERC 2008 Conf.*, Edinburgh, Scotland, 2008, pp. 130–133.
- [13] K. Iwamoto, Y. Kamimuta, A. Ogawa, Y. Watanabe, S. Migita, W. Mizubayashi, Y. Morita, M. Takahashi, H. Ota, T. Nabatame, and A. Toriumi, "Experimental evidence for the flatband voltage shift of high- k metal-oxide-semiconductor devices due to the dipole formation at the high- k/SiO_2 interface", *Appl. Phys. Lett.*, vol. 92, iss. 13, pp. 132907-1–3, 2008.

- [14] K. Kita and A. Toriumi, "Origin of electric dipoles formed at high-*k*/SiO₂ interface", *Appl. Phys. Lett.*, vol. 94, iss. 13, pp. 132902-1--3, 2009.
- [15] K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, "Defect energy levels in HfO₂ high-dielectric constant gate oxide", *Appl. Phys. Lett.*, vol. 87, iss. 18, pp. 183505-1--3, 2005.
- [16] J. L. Gavartin, D. Muñoz Ramo, A. L. Shluger, G. Bersuker, and B. H. Lee, "Negative oxygen vacancies in HfO₂ as charge traps in high-*k* stacks", *Appl. Phys. Lett.*, vol. 89, iss. 8, pp. 082908-1--3, 2006.
- [17] Y. P. Feng, A. T. Lim, and M. F. Li, "Negative-U property of oxygen vacancy in cubic HfO₂", *Appl. Phys. Lett.*, vol. 87, iss. 6, pp. 062105-1--3, 2005.
- [18] H. D. B. Gottlob, M. Schmidt, A. Stefani, M. C. Lemme, H. Kurz, I. Z. Mitrovic, W. M. Davey, S. Hall, M. Werner, P. R. Chalker, K. Cherkaoui, P. K. Hurley, J. Piscator, O. Engström, and S. B. Newcomb, "Scaling potential and MOSFET integration of thermally stable Gd silicate dielectrics", *Microelectron. Eng.*, vol. 86, iss. 7-9, pp. 1642-1645, 2009.
- [19] H. D. B. Gottlob, A. Stefani, M. Schmidt, M. C. Lemme, H. Kurz, I. Z. Mitrovic, M. Werner, W. M. Davey, S. Hall, P. R. Chalker, K. Cherkaoui, P. K. Hurley, J. Piscator, O. Engström, and S. B. Newcomb, "Gd silicate: a high-*k* dielectric compatible with high temperature annealing", *J. Vac. Sci. Technol. B*, vol. 27, iss. 1, pp. 249-252, 2009.
- [20] I. Z. Mitrovic and S. Hall, "Rare earth silicate formation – a route towards high-*k* for the 22 nm node and beyond", *J. Telecommun. Inform. Technol.*, no. 4, pp. 51-60, 2009.
- [21] O. Engström and A. Alm, "Energy concepts of insulator-semiconductor interface traps", *J. Appl. Phys.*, vol. 54, no. 9, pp. 5240-5244, 1983.
- [22] W. B. Fowler, J. K. Rudra, M. E. Zvanut, and F. J. Fiegler, "Hysteresis and Franck-Condon relaxation in insulator-semiconductor tunnelling", *Phys. Rev. B*, vol. 41, no. 12, pp. 8313-8317, 1990.
- [23] O. Engström and H. G. Grimmeiss, "Vibronic states of silicon dioxide interface traps", *Semicond. Sci. Technol.*, vol. 4, no. 12, pp. 1106-1115, 1989.
- [24] O. Engström, T. Gutt, and H. M. Przewłocki, "Energy concepts involved in MOS characterization", *J. Telecommun. Inform. Technol.*, no. 2, pp. 86-91, 2007.
- [25] M. Johansson, "Silicon device substrate and channel characteristics influenced by interface properties", Ph.D. thesis, Chalmers University of Technology, Göteborg, Sweden, 2005.
- [26] B. Raeissi, "Charge carrier traffic at interfaces in nanoelectronic structures", Ph.D. thesis, Chalmers University of Technology, Göteborg, Sweden, 2010.
- [27] M. Y. A. Yousif, M. Johansson, and O. Engström, "Extremely small hole capture cross sections in HfO₂/Hf_xSi_yO_z/p-Si structures", *Appl. Phys. Lett.*, vol. 90, iss. 20, pp. 203506-1--3, 2007.



Olof Engström received the Ph.D. degree in solid state physics from the University of Lund in 1975 and was later employed by ASEA AB for research on high power thyristors, by AB Rifa for development of MOS technology and by the Swedish Defence Research Institute for sensor research. In 1984, he came to Chalmers Uni-

versity of Technology as a Professor in solid state electronics. Between 1996 and 1999, he served as Dean of Chalmers School of Electrical and Computer Engineering and 1999-2002 he was the Director of the Microtechnology Center at Chalmers (MC2). From 2003 he is back in research as a Professor at the Department of Microtechnology and Nanoscience of MC2. His present research interest is in, high-*k*-materials and quantum dots and Schottky barriers on silicon nanowires. In 1991, he founded Samba Sensors AB, a company for production of fiberoptical pressure sensors. He is a member of the Royal Swedish Academy of Engineering Science, the Finnish Society of Science and the High-*k*-Gang.

e-mail: olof.engstrom@chalmers.se
Chalmers University of Technology
Department of Microtechnology and Nanoscience
SE-412 96 Göteborg, Sweden



Bahman Raeissi received the B.Sc. degree in physics from Isfahan University of Technology, Isfahan, Iran, in 2002 and M.Sc. degree in nanoscale physics and engineering, Chalmers University of Technology, Göteborg, Sweden, in 2005. He is currently a Ph.D. student at the Department of Microtechnology and Nanoscience (MC2),

Chalmers University of Technology. His main research interests are fabrication and characterization of high-*k* dielectrics, semiconductor wafer bonding and characterization of quantum dots.

e-mail: bahman.raeissi@chalmers.se
Chalmers University of Technology
Department of Microtechnology and Nanoscience
SE-412 96 Göteborg, Sweden



Johan Piscator received the M.Sc. degree and the Ph.D. degree in electronic engineering from Chalmers University of Technology, Göteborg, Sweden, in 2003 and 2009, respectively. His main research interests are fabrications and characterization of silicon nanowires and characterization of high-*k* oxides for CMOS applications.

e-mail: johan.piscator@gmail.com
Chalmers University of Technology
Department of Microtechnology and Nanoscience
SE-412 96 Göteborg, Sweden



Ivona Z. Mitrovic received the Ph.D. degree in electronic engineering from the University of Liverpool, UK, in 2007, the M.Sc. degree in materials science from the University of Belgrade in 2002, and Dipl.-Ing. degree in microelectronics from the Faculty of Electronic Engineering, University of Nis, Serbia, Yugoslavia, in 1997. She

took part in a research project concerning BaTiO₃ ceramics (1997–2001), worked as a Research Assistant (2001–2007) and a Research Associate at the University of Liverpool (2000–2009). Since June 2009, she is a Lecturer in the Solid State Electronics Research Group, Department of Electrical Engineering and Electronics, University of Liverpool. Her research interests span materials for beyond 22 nm technological node targeting energy harvesting products for medical, automotive and aerospace applications, as well as emerging technologies for energy conversion and storage.

e-mail: ivona@liverpool.ac.uk

Department of Electrical Engineering and Electronics
University of Liverpool
Brownlow Hill
Liverpool L69 3GJ, United Kingdom



Stephen Hall has been Head of the Department of Electrical Engineering and Electronics at the University of Liverpool, UK, from 2001 to the present date. He has interests spanning materials characterization, device physics and innovative device design and gate level circuits. He has over 200 conference and journal papers in the

area of silicon technology, devices and circuits. These include novel measurements and contributions to the understanding of MOS related interfaces and materials quality. He has successfully designed and built novel MOS and bipolar devices in silicon for about 20 years. More recently, his work encompasses gate level circuits relating to low voltage/low power SOL, micro-power and biologically inspired concepts. He was Technical Programme Chair of ESSDERC 2008, and currently sits on the Steering Committee of ESSDERC/ESSCIRC and INFOS, for which he was vice-Chair in 2009 and is a member of the Steering Committee from 2009.

e-mail: S.Hall@liverpool.ac.uk

Department of Electrical Engineering and Electronics
University of Liverpool
Brownlow Hill
Liverpool L69 3GJ, United Kingdom



Heinrich D. B. Gottlob received his Dipl.-Ing. degree in electrical engineering and information technology from the RWTH Aachen University, Germany, in 2003 and his Dr.-Ing. degree in 2007. In 2003 he joined AMO GmbH as R&D engineer and he is currently leader of the nanoelectronics group and manager of AMO's

nanotechnology lab AMICA. Research topics include novel high-*k* dielectrics and metal gate stacks as well as fully depleted ultrathin body and non-planar SOI devices. He is author and co-author of more than 30 journal papers.

e-mail: gottlob@amo.de

Advanced Microelectronic Center Aachen (AMICA)
AMO GmbH
Otto-Blumenthal st 25
D-52074 Aachen, Germany



Mathias Schmidt received his Dipl.-Ing. degree in electrical engineering from the RWTH Aachen University, Germany, in 2004. He is currently working towards his Dr. Ing. degree at the Advanced Microelectronic Center Aachen (AMICA), AMO GmbH Aachen. His research topics include ultrathin body silicon devices with planar and

non-planar channels with special respect to experimental mobility extraction and integration of novel high-*k*/metal gate stacks and strained channel materials.

e-mail: schmidt@amo.de

Advanced Microelectronic Center Aachen (AMICA)
AMO GmbH
Otto-Blumenthal st 25
D-52074 Aachen, Germany



Karim Cherkaoui received the Ph.D. degree in 1998 from the Institut National des Sciences Appliquées of Lyon, France. During his Ph.D. he gained experience in the spectroscopy of point defects in semi-insulating materials. In 1999 he joined the Tyndall National Institute (formerly NMRC), University College Cork, where he has established and developed several low temperature electrical metrology techniques. His current research interests include the process development and characterization of high dielectric constant materials on Si and III-V materials for future MOS devices.

e-mail: karim.cherkaoui@tyndall.ie
Tyndall National Institute
University College Cork, Lee Maltings
Prospect Row, Cork, Ireland



Paul Hurley received his Ph.D. (1990) and B.Eng. (1985 – first class honors) in electronic engineering at the University of Liverpool, UK. He is a senior research scientist at the Tyndall National Institute, University College Cork, Ireland, where his work focuses on high dielectric constant (high- k) ma-

terials intended for use as gate level insulators in transistors for future integrated circuits. The emphasis of his current research is the formation and characterization of high- k films on silicon and III–V semiconductor substrates. He is a member of the Technical Committee of the Insulating Films on Semiconductors (INFOS) conference and the International Workshop on Dielectrics in Microelectronics (WoDiM). In addition to research activities, he is a part time lecturer in the Department of Micro-electronic Engineering at University College Cork. He has published over eighty papers in the field of microelectronics.

e-mail: paul.hurley@tyndall.ie
Tyndall National Institute
University College Cork, Lee Maltings
Prospect Row, Cork, Ireland