Paper

The Impact of Externally Applied Mechanical Stress on Analog and RF Performances of SOI MOSFETs

Mostafa Emam, Samer Houri, Danielle Vanhoenacker-Janvier, and Jean-Pierre Raskin

Abstract— This paper presents a complete study of the impact of mechanical stress on the performance of SOI MOSFETs. This investigation includes dc, analog and RF characteristics. Parameters of a small-signal equivalent circuit are also extracted as a function of applied mechanical stress. Piezoresistance coefficient is shown to be a key element in describing the enhancement in the characteristics of the device due to mechanical stress.

Keywords— cutoff frequency f_T, intrinsic gain, mechanical stress, piezoresistance coefficient, SOI MOSFET.

1. Introduction

Scaling, channel engineering, high-*k* metal gate, etc., are different technological means to improve digital as well as analog performances of modern metal-oxide-semiconductor field effect transistor (MOSFET). Process induced strain whether tensile or compressive applied to the device during the fabrication process is also receiving increasing attention as another alternative to enhance the MOS transistor performance [1]. However, the impact of mechanical stress on the analog and RF characteristics of the transistor is rarely addressed in the literature [2], [3]. This work provides a complete study of the impact of mechanical stress on the dc, analog and RF characteristics of MOSFET transistors. This investigation is supported by the extraction of the different parameters of a small-signal equivalent circuit as a function of the applied mechanical stress. Piezoresistance coefficient is also calculated based on both dc and RF measurements. The mechanical stress is applied externally by means of a 4-point bending measurement setup coupled with dc and RF probe station.

Externally applied mechanical stress cannot in general reach the high values of process induced stress. However, the external application of mechanical stress provides high precision controllable values of stress, thus providing a valuable tool for the study of the device properties as a function of both tensile and compressive stress. Consequently, the results obtained from this study can easily be extrapolated to higher values of stress, applied either externally or internally.

This approach has been adopted repeatedly in the literature, with different variations in setup [4]–[13] knowing that Colman *et al.* [14] were the first to introduce this measurement setup with a single-points bending.

In this work, detailed investigation and results of strained devices are presented in such a way as to be easy to compare with the literature. Such study, important as it is for the design of analog and RF circuits has not been presented before.

2. Measurement Setup and Devices

A four-point bending setup is used to apply external mechanical stress from compressive (−250 MPa) to tensile (250 MPa), i.e., over a range of 500 MPa. A schematic representation of the 4-point bending setup is shown in Fig. 1.

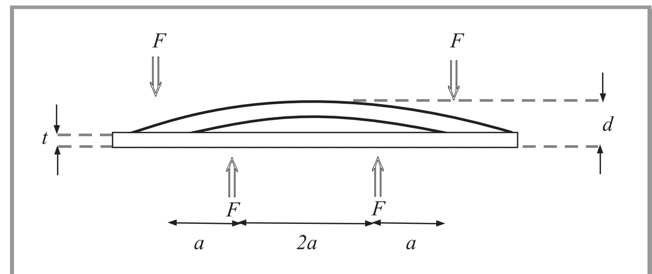

Fig. 1. Four-point bending setup.

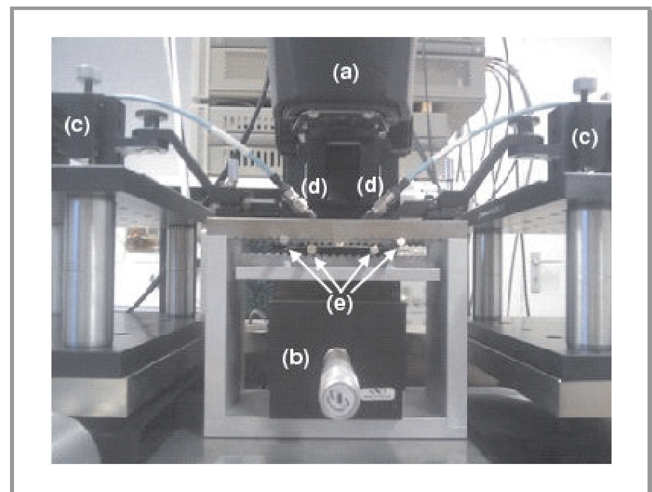

Fig. 2. A photograph of the used four-point bending setup with (a) the microscope, (b) the micrometer screw, (c) the RF probe holders, (d) the RF probes, (e) the metallic rods used to apply the mechanical stress on the 4 inch silicon wafer lying in between.

The value of the applied stress/strain can be calculated using the following formula [10]:

$$\sigma = \frac{3Edt}{8a^2}, \tag{1}$$

where σ is the applied mechanical stress in Pa, E is the wafer's Young's modulus, d is the maximum displacement due to the applied force, t is the wafer thickness, and $2a$ is the distance between the inner contact points.

Displacement is applied through a micrometer screw and measured by an optical microscope thus providing the precision of a few microns (Fig. 2).

Both n- and p-type fully-depleted (FD) silicon-on-insulator (SOI) MOSFETs are studied, bosth featuring 12 gate fingers (each 24 μm wide) connected in parallel. The channel length is 3 μm. The use of long channel devices helps to avoid short channel effects and hence results in a more accurate and less error prone extraction of equivalent circuit parameters.

3. Piezoresistance Coefficient

Piezoresistance coefficient in a transistor has been always defined with regards to the variation of the channel resistivity (or conductivity) as a function of the applied stress [14]–[16]. It was also introduced as the slope of the variation of the transconductance with respect to the transconductance at zero stress ($\Delta G_m/G_{m0}$) [4], [6]. In both cases, the resulting variation with stress is attributed to the dependence of carrier mobility on the applied mechanical stress. As will be shown in the next section, the same values of the piezoresistance coefficient could also be obtained from the variation of the output conductance with respect to the output conductance at zero stress ($\Delta G_d/G_{d0}$). This confirms the fact that the piezoresistance coefficient in a MOSFET device is mainly dominated by the variation of carrier mobility with the applied mechanical stress.

Table 1
Piezoresisitive coefficients π
for $a < 100 >$ wafer [%/kBar] for N- and PMOSFETs
in parallel and perpendicular orientations [7]

NMOS		PMOS	
$\pi \perp$	$\pi \parallel$	$\pi \perp$	$\pi \parallel$
−2.30	−4.97	−4.66	+6.48

The value of the piezoresitance coefficient depends on both the crystalline orientation, and the current orientation with respect to the applied strain [7], this is shown in Table 1 for $a < 100 >$ Si wafer. In this study, the mechanical stress is applied transversally with respect to the direction of the current, while the device channel orientation is <110>.

4. DC Characterization

Based on dc measurements (performed using a HP4145 device parameter analyzer), the piezoresistance coefficient is calculated using the variation in transconductance G_m (at $V_{DS} = \pm 1.2$ V and various V_{GS}, in the saturation regime) and also the variation in output conductance G_d (at V_{DS} = 50 mV and $V_{GS} = \pm 2$ V; i.e., in the linear regime) with the applied mechanical stress, as shown in Figs. 3 and 4. In both cases, a piezoresistance coefficient of 2 and 1 (10^{-4} MPa^{-1}), is found for P- and NMOSFETs, respectively.

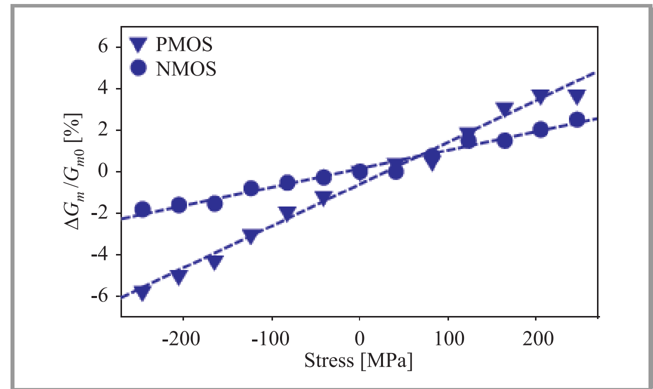

Fig. 3. Relative variation of the maximum dc transconductance G_m in saturation ($V_{DS} = \pm 1.2$ V) for P- and NMOSFETs.

The absolute variation of G_m with the applied mechanical stress shows is a 2.5 and 0.84% per 100 MPa for P- and NMOSFETs, respectively, in the saturation region (V_{DS} = ± 1.2 V and $V_{GS} = \pm 1.5$ V).

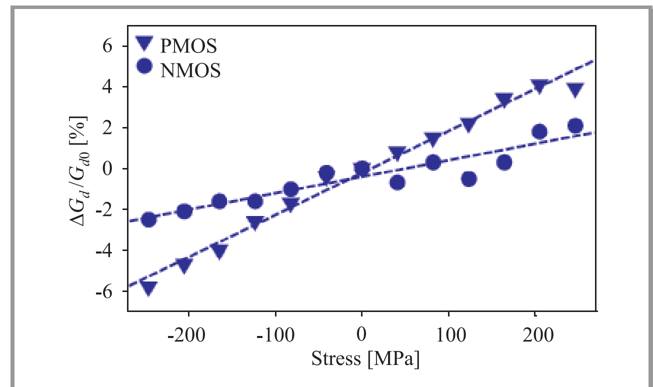

Fig. 4. Relative variation of output conductance G_d in the linear regime (V_{DS} = 50 mV and $V_{GS} = \pm 2$ V) for P- and NMOSFETs.

The dc open-loop gain (A_{V0}) is also improved by applying mechanical stress. This can be seen through the improvement of the early voltage V_{EA} with the applied mechanical stress since [17]:

$$A_{V0} = \frac{g_m}{I_{DS}} \cdot V_{EA}. \tag{2}$$

The first term (g_m/I_{DS}) is constant with stress, since the mobility is canceled out. An increase of ~0.8 and

∼0.7% per 100 MPa is noticed in V_{EA} for P- and NMOSFETs, respectively, at $V_{GS} = \pm 1.8$ V, as shown in Fig. 5. However, this increase drops to ∼0.3 and ∼0.2% per 100 MPa for P- and NMOSFETs, respectively, at $V_{GS} = \pm 0.6$ V. This variation is not dependent on the sensitivity of mobility to the applied mechanical stress, as is the case with the piezoresistance coefficient, since V_{EA} can be approximated by [18]

$$V_{EA} = \frac{I_{DS}}{g_D}, \tag{3}$$

where the effect of mobility is simplified between the numerator and denominator.

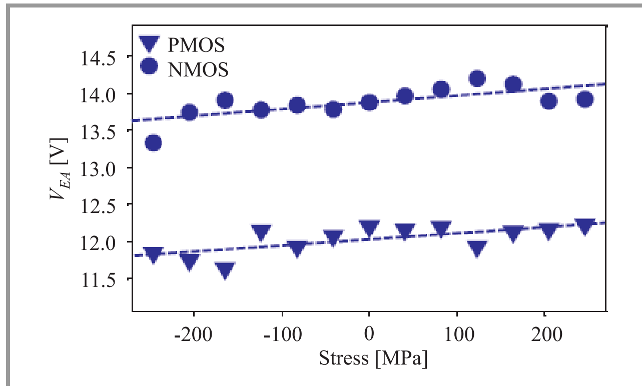

Fig. 5. Variation of early voltage V_{EA} with the applied stress at $V_{GS} = \pm 1.8$ V for P- and NMOSFETs.

It is also worth to notice that the threshold voltage V_{th} is quite constant with the applied mechanical stress, as can be seen from Fig. 6. The same applies to the subthreshold slope S as shown in Fig. 7.

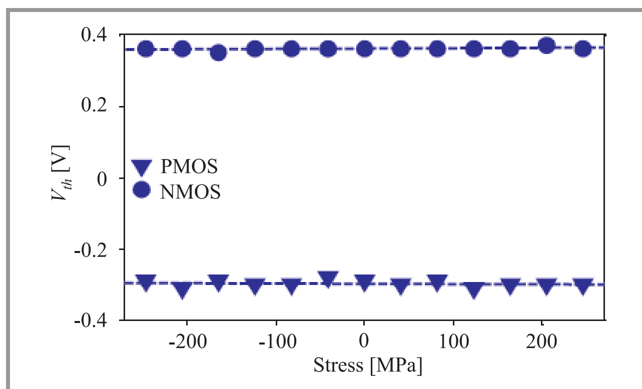

Fig. 6. Variation of threshold voltage V_{th} with the applied stress for P- and NMOSFETs.

The variation of G_m with the applied mechanical stress is also studied as a function of gate voltage V_{GS}. In the saturation region ($V_{DS} = \pm 1.2$ V), the piezoresistance coefficient shows an interesting reduction at V_{GS} values close to V_{th} (−0.3 and 0.36 V for P- and NMOSFETs, respectively). Figures 8 and 9 show values of less than 1 and 0.5% per 100 MPa of the applied mechanical stress for

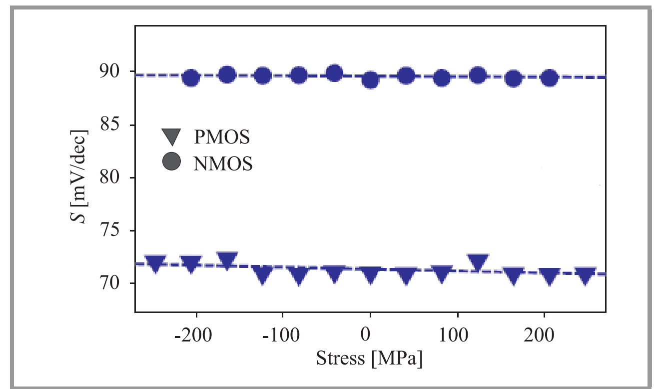

Fig. 7. Variation of subthreshold slope with the applied stress for P- and NMOSFETs.

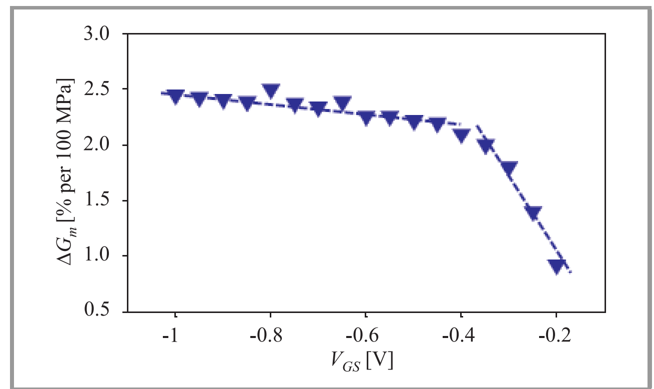

Fig. 8. Variation of dc transconductance G_m with the applied stress for PMOSFETs as a function of V_{GS} at $V_{DS} = -1.2$ V.

P- and NMOSFETs, respectively. These results show a direct relation between the piezoresistance coefficient and the density of carriers in the channel. This relation is further confirmed when studying the variation of G_m in the linear region ($V_{DS} = \pm 50$ mV). When the gate bias passes from $|V_{GS}| > |V_{th}|$ to $|V_{GS}| < |V_{th}|$, the channel passes from inversion to depletion, hence the dominant carriers in the channel change from holes to electrons and from electrons to holes for P- and NMOSFET, respectively. As a direct

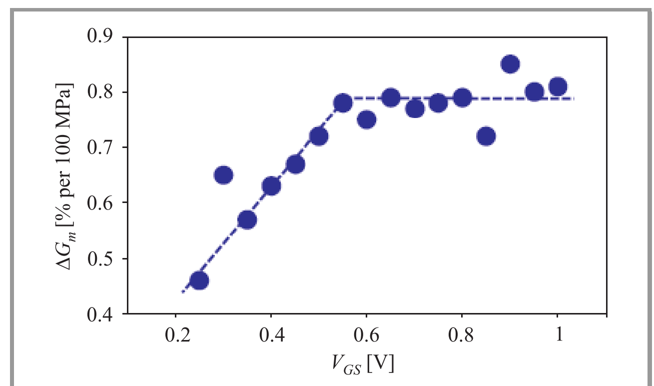

Fig. 9. Variation of dc transconductance G_m with the applied stress for NMOSFETs as a function of V_{GS} at $V_{DS} = 1.2$ V.

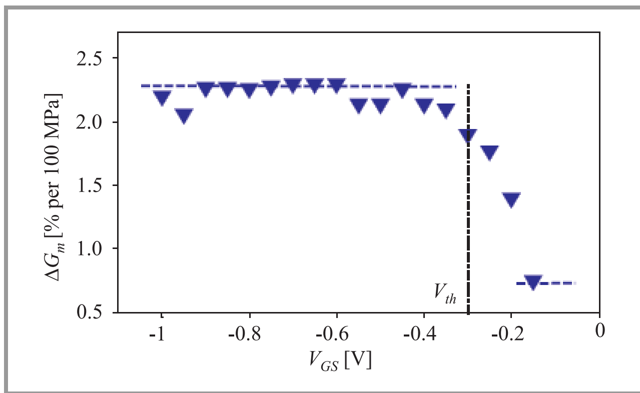

Fig. 10. Variation of dc transconductance G_m with the applied stress for PMOSFETs as a function of V_{GS} at $V_{DS} = -50$ mV.

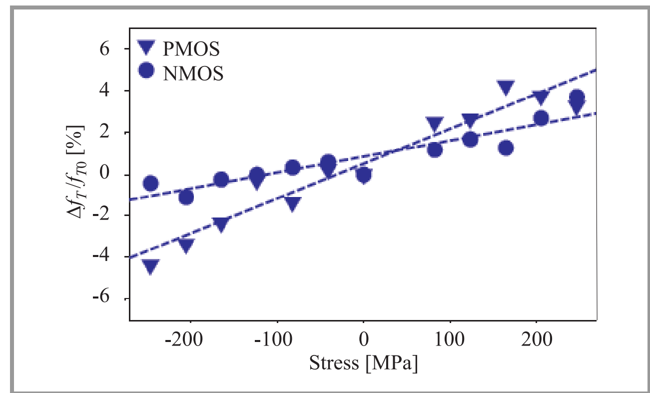

Fig. 12. Relative variation of cutoff frequency f_T with the applied mechanical stress for P- and NMOSFETs.

consequence, the piezoresistance coefficient value follows this transformation of the dominant carrier type in the channel. In PMOSFET (Fig. 10), ΔG_m goes from 2.3 to 0.75% per 100 MPa, with the latter value being close to that calculated earlier for NMOSFET. The inverse can be noticed for NMOSFET as shown in Fig. 11.

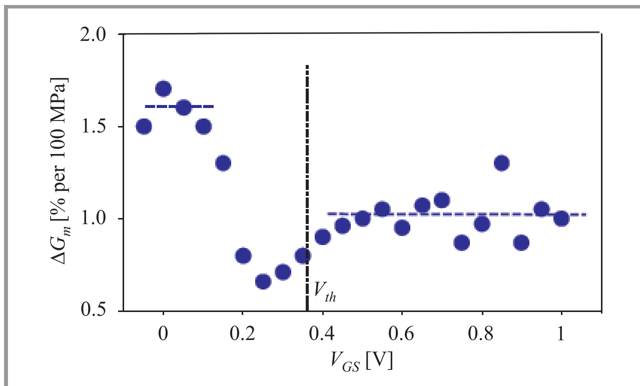

Fig. 11. Variation of dc transconductance G_m with the applied stress for NMOSFETs as a function of V_{GS} at V_{DS} = 50 mV.

This interesting shift in piezoresistance coefficient around V_{th} could be very useful for applications such as piezoresistance gages or switches.

5. RF Characterization

A 2-port Anritsu 37369A^{TM} vector network analyzer (VNA) is used to measure the S-parameters as a function of applied mechanical stress for both the P- and NMOSFETs. An open structure is used for a 1-step de-embedding procedure. Cutoff frequency f_T is extracted from the de-embedded $|H_{21}|$. The maximum of f_T is found at $V_{GS} = \pm 1.6$ V for PMOS and NMOS in the saturation region ($V_{DS} = 1.2$ V). The analysis of the dependence of f_T on the applied mechanical stress is conducted at this maximum f_T point.

Figure 12 shows the relative variation of f_T with respect to f_{T0} as a function of mechanical stress. The slope is found to be 1.7 and 0.8 (10^{-4} MPa^{-1}) for P- and NMOSFETs, respectively. This is slightly lower than the slopes found for $\Delta G_m/G_{m0}$ calculated from dc measurements as shown in Section 4. The absolute variation in f_T is 1.6 and 0.8% per 100 MPa for P- and NMOSFETs, respectively. It is interesting to notice that the ratio is 2:1, which is consistent with the piezoresistance coefficients ratio.

On the other hand, the ratio $f_{\max}/f_T$ shows a negligible variation with the applied mechanical stress, as can be seen from Fig. 13. This important figure of merit [19] depends

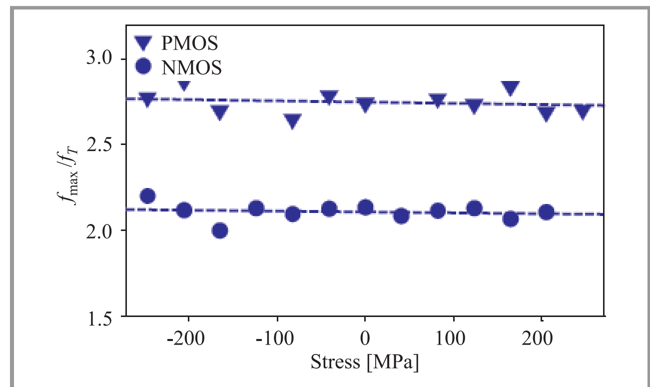

Fig. 13. Variation of (f_{max}/f_T) ratio with the applied mechanical stress for P- and NMOSFETs.

basically on the gate and source resistances (R_g and R_s). As will be shown later, these resistances show very slight variation with the applied mechanical stress.

5.1. Small-Signal Equivalent Circuit

It is of interest at this point to investigate the effect of mechanical stress on the various extrinsic and intrinsic parameters of the small-signal equivalent circuit. A typical small-signal equivalent circuit is shown in Fig. 14, where the elements outside the dashed box are the extrinsic elements whereas the elements inside the dashed box are the intrinsic elements. The term extrinsic refers to those elements which are independent of the bias condition but are scalable with the active zone. The term intrinsic denotes

the elements which are dependent on the bias condition and the size of the active region, thus representing the transistor behavior [20]. Extrinsic capacitances and inductances are neglected. Access elements are removed during the 1-step de-embedding procedure.

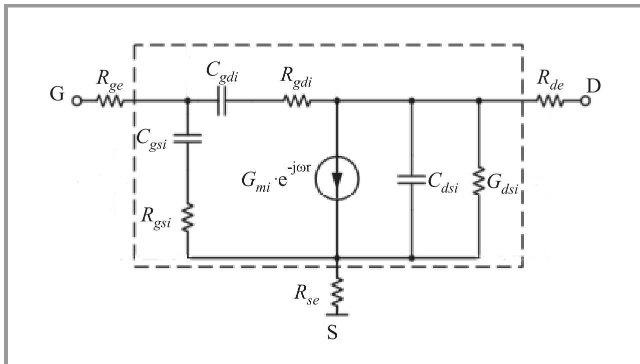

Fig. 14. Small-signal equivalent circuit for MOSFETs. The dashed box contains the intrinsic parameters.

Extrinsic resistances (R_{ge}, R_{se} and R_{de}) are first extracted using the cold-FET method [21]. The variation of these extrinsic resistances with the applied mechanical stress is shown in Fig. 15. Nearly constant behavior with stress can be clearly seen due to the highly doped drain and source areas resulting in low piezoresistance coefficient [22].

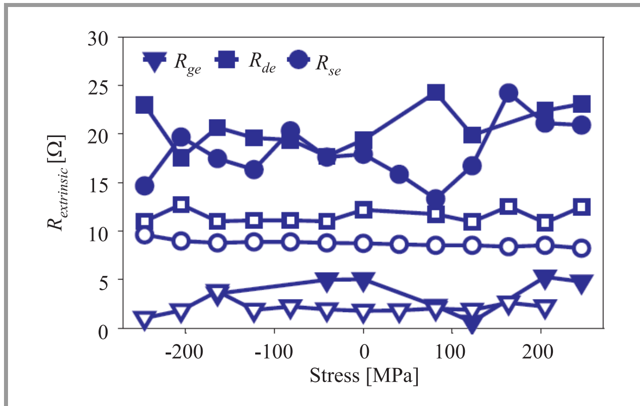

Fig. 15. Variation of extrinsic resistances with the applied mechanical stress for P- (solid symbols) and NMOSFETs (empty symbols).

After removing the effect of extrinsic resistances, the next step is to extract the intrinsic elements of the small-signal equivalent circuit using the direct extraction method proposed in [20]. The extraction is performed in the saturation region at $V_{GS} = \pm 1.5$ V and $V_{DS} = 1.2$ V.

The total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$) shows a slight variation with the applied mechanical stress, namely 0.3% per 100 MPa for both P- and NMOSFETs, as shown in Fig. 16.

The variation of the intrinsic transconductance G_{mi} (extracted from RF measurements) with the applied mechanical stress shows a good agreement with the dc extracted

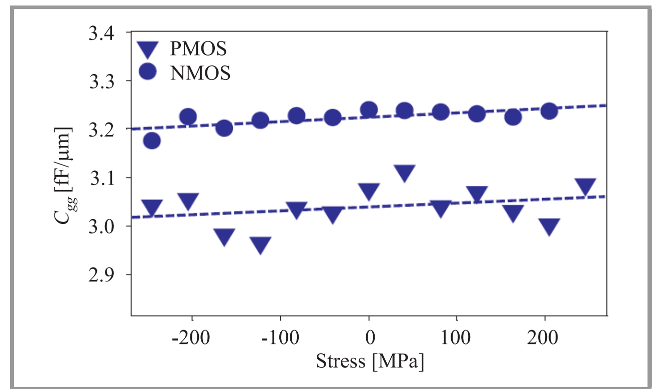

Fig. 16. Variation of intrinsic total gate capacitance C_{gg} with the applied mechanical stress for P- and NMOSFETs.

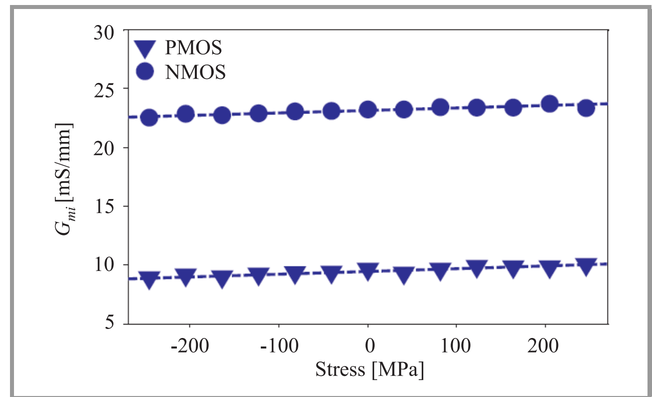

Fig. 17. Variation of intrinsic transconductance G_{mi} with the applied mechanical stress for P- and NMOSFETs.

values, taking into account the errors related to the extraction procedures (extrinsic and intrinsic). A variation of 2.3 and 0.8% per 100 MPa is calculated for P- and NMOSFETs, respectively, as shown in Fig. 17. On the other hand, the intrinsic output conductance shows a slight shift from the values extracted for the transconductance, showing a variation with the applied mechanical stress of 2.5 and 0.65% per 100 MPa for P- and NMOSFETs, respectively, as shown in Fig. 18.

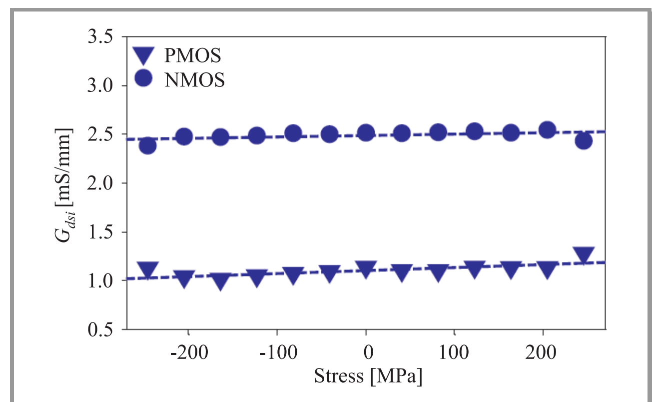

Fig. 18. Variation of intrinsic output conductance G_{dsi} with the applied mechanical stress for P- and NMOSFETs.

The extraction of all intrinsic parameters is performed for devices in saturation, i.e., $V_{DS} = \pm 1.2$ V and $V_{GS} = \pm 1.5$ V. Based on the previous results for C_{gg} and G_{mi}, and knowing that the cutoff frequency f_T is usually approximated by

$$f_T = \frac{G_m}{2\pi C_{gg}} \tag{4}$$

it can be seen that the variation in C_{gg} with the applied mechanical stress is not negligible, however, it is of secondary importance, whereas the major effect comes from the variation in G_{mi}.

5.2. Piezoresistance Coefficient from RF Extraction

The calculation of the piezoresistance coefficient based on RF measurements could be another important tool to characterize the MOSFET behavior under mechanical stress. DC measurements of SOI devices, especially G_m and G_{ds} could suffer from some shift due to the self-heating effect. It is possible to avoid these problems by using the intrinsic parameters, like G_{mi} and G_{dsi}, extracted from RF measured data, as presented in the previous section.

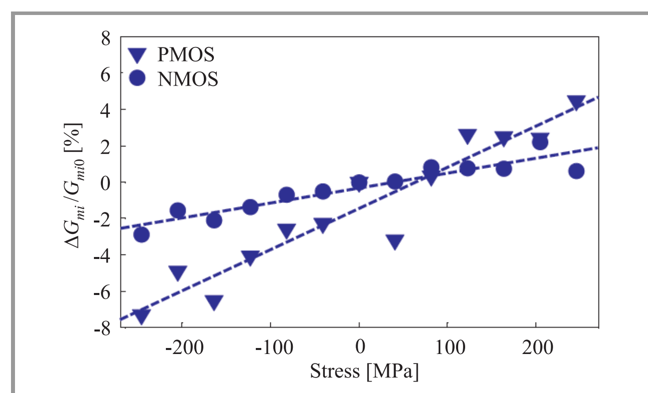

Fig. 19. Relative variation of intrinsic transconductance G_{mi} in saturation ($V_{DS} = \pm 1.2$ V and $V_{GS} = \pm 1.5$ V) for P- and NMOSFETs.

Figure 19 shows the relative variation of the intrinsic transconductance G_{mi} with the applied mechanical stress for both P- and NMOSFETs. A piezoresistance coefficient of 2.25 and 0.82 (10^{-4} MPa^{-1}) for P- and NMOSFETs, respectively, can be calculated from the slope of the corresponding variation. These values are close to the values extracted from dc measurements. The small difference is related to the corrected transconductance by removing the self-heating effect.

6. Conclusion

Based on dc and RF measurements, the mechanical stress is shown to directly affect the dc, analog and RF performances of P- and NMOS transistors. Most of these effects are related to the variation of carrier mobility with the applied mechanical stress, but it was shown that some other effects are also related to the variation of the carrier density inside the channel with the applied mechanical stress.

Cutoff frequencies were shown to vary with the applied mechanical stress as a direct result of the variation of transconductance, while the gate capacitance would still have a slight secondary effect on the variation of cutoff frequency.

On the other hand, the ratio $f_{\max}/f_T$ was shown to slightly vary with stress since it is dominated by the relatively stable extrinsic resistances of the transistors.

The ratio between the performance variation in PMOSFET to the performance variation in NMOSFET with the applied mechanical stress, was shown to be equal to the ratio of piezoresistance coefficients of P- to NMOSFETs.

This characterization methodology being limited in this study to 500 MPa of externally applied mechanical stress, could be extrapolated to higher values of stress/strain, applied internally due to fabrication process steps.

Acknowledgements

This work was supported in part by the Walloon Region (Convention no. 516125 CORMORAN).

References

[1] V. Chan, K. Rim, M. Ieong, S. Yang, R. Malik, Y. W. Teh, M. Yang, and Q. C. Ouyang, "Strain for CMOS performance improvement", in *Proc. IEEE Custom Integr. Circ. Conf.*, San Jose, USA, 2005, pp. 667–673.

[2] D. V. Singh, K. A. Jenkins, J. Sleight, Z. Ren, M. Ieong, and W. Haensch, "Strained ultrahigh performance fully depleted nMOSFETs with f_t of 330 GHz and sub-30 nm gate lengths", *IEEE Electron Dev. Lett.*, vol. 27, no. 3, pp. 191–193, 2006.

[3] S. Houri, M. Emam, and J.-P. Raskin, "RF behavior of strained fully depleted SOI MOSFETs", in *Proc. EUROSOI Conf.*, Cork, Ireland, 2008, pp. 55–56.

[4] A. Hamada, T. Furusawa, N. Saito, and E. Takeda, "A new aspect of mechanical stress effects in scaled MOS devices", *IEEE Electron Dev. Lett.*, vol. 38, no. 4, pp. 895–900, 1991.

[5] C.-L. Huang, H. R. Soleimani, G. J. Grula, J. W. Sleight, A. Villani, H. Ali, and D. A. Antoniadis, "LOCOS-induced stress effects on thin-film SOI devices", *IEEE Trans. Electron Dev.*, vol. 44, no. 4, pp. 646–650, 2004.

[6] R. Degraeve, G. Groeseneken, I. De Wolf, and H. E. Maes, "The effect of externally imposed mechanical stress on the hot-carrier-induced degradation of deep-sub micron nMOSFET's", *IEEE Trans. Electron Dev.*, vol. 44, no. 6, pp. 943–950, 1997.

[7] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, R. Gwoziecki, S. Orain, E. Robilliart, C. Raynaud, and H. Dansas, "Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress", *IEEE Trans. Electron Dev.*, vol. 51, no. 8, pp. 1254–1261, 2004.

[8] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishida, "Future of strained Si/semiconductors in nanoscale MOSFETs", in *Proc. Int. Electron Dev. Meet. IEDM*, San Francisco, USA, 2006, pp. 1–4.

[9] F. Rochette, M. Cassé, M. Mouis, G. Reimbold, D. Blachier, C. Leroux, B. Guillaumot, and F. Boulanger, "Experimental evidence and extraction of the electron mass variation in [110] uniaxially strained MOSFETs", *Solid-State Electron.*, vol. 51, no. 11-12, pp. 1458–1465, 2007.

[10] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (∼1.5 GPa) channel stress", *IEEE Electron Dev. Lett.*, vol. 28, no. 1, pp. 58–61, 2007.

[11] Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, "Impact of mechanical stress on gate tunneling currents of germanium and silicon p-type metal-oxide-semiconductor field-effect transistors and metal gate work function", *J. Appl. Phys.*, vol. 103, no. 64510, pp. 1–5, 2008.

[12] J.-S. Lim, A. Acosta, S. E. Thompson, G. Bosman, E. Simoen, and T. Nishida, "Effect of mechanical strain on $1/f$ noise in metal-oxide semiconductor field-effect transistors", *J. Appl. Phys.*, vol. 105, no. 54504, pp. 1–11, 2009.

[13] Y. J. Kuo, T. C. Chang, P. H. Yeh, S. C. Chen, C. H. Dai, C. H. Chao, T. F. Young, O. Cheng, and C. T. Huang, "Substrate current enhancement in 65 nm metal-oxide-silicon field-effect transistor under external mechanical stress", *Thin-Solid Films*, vol. 517, no. 5, pp. 1715–1718, 2009.

[14] D. Colman, R. T. Bate, and J. P. Mize, "Mobility anisotropy and piezoresistance in silicon p-type inversion layers", *J. Appl. Phys.*, vol. 39, no. 4, pp. 1923–1931, 1968.

[15] G. Dorda, "Piezoresistance in quantized conduction bands in silicon inversion layers", *J. Appl. Phys.*, vol. 42, no. 5, pp. 2053–2060, 1971.

[16] B. Borchert and G. E. Dorda, "Hot-electron effects on short-channel MOSFET's determined by the piezoresistance effect", *IEEE Trans. Electron Dev.*, vol. 35, no. 4, pp. 483–488, 1988.

[17] D. Flandre, J.-P. Eggermont, D. De Ceuster, and P. Jespers, "Comparison of SO1 versus bulk performances of CMOS micropower single-stage OTAs", *IEEE Electron. Lett.*, vol. 30, no. 23, pp. 1933–1934, 1994.

[18] S. M. Sze, *Semiconductor Devices Physics and Technology*. New York: Wiley, 1985.

[19] G. Dambrine, C. Raynaud, D. Lederer, M. Dehan, O. Rozeaux, M. Vanmackelberg, F. Danneville, S. Lepilliet, and J.-P. Raskin, "What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?", *IEEE Electron Dev. Lett.*, vol. 24, no. 3, pp. 189–191, 2003.

[20] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker-Janvier, and J.-P. Colinge, "Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling", *IEEE Trans. Electron Dev.*, vol. 45, no. 5, pp. 1017–1025, 1998.

[21] A. Bracale *et al.*, "A new approach for SOI devices small-signal parameters extraction", *Anal. Integr. Circ. Sig. Process.*, vol. 25, no. 2, pp. 157–169, 2000.

[22] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon", *IEEE Trans. Electron Dev.*, vol. ED-29, no. 1, pp. 64–70, 1982.

Mostafa Emam received the B.Sc. degree in electronics and communication engineering from the Ain Shams University, Cairo, Egypt, in 2001, the Diplome d'Ingénieur degree in electronics and signal processing, and the M.Sc. degree in design of microelectronics circuits and systems both from the Institute National Polytechnique, Toulouse, France, in 2005. He has been working toward the Ph.D. degree in engineering sciences in the Microwave Laboratory, Ecole Polytechnique de Louvain, Université catholique de Louvain, Belgium, since 2006. He worked for the Analog/Mixed Signal Group, Mentor Graphics (2005), George Mason University, Fairfax and AMD, Sunnyvale, USA (2006). His research interests include the characterization and modeling of SOI devices in dc, RF, large-signal, and high frequency noise, for harsh-environment applications and under mechanical stress conditions as well as the design and simulation of RF SOI circuits.

e-mail: mostafa.emam@uclouvain.be
Université catholique de Louvain
Place du Levant, 3, Maxwell Building
B-1348 Louvain-la-Neuve, Belgium

Samer Houri received his B.E. in electrical engineering from the Beirut Arab University, Lebanon, in 2005, and his M.Sc. degree in nano-electronics from the Université de Provence, Marseille, France, in 2006. Currently working towards a Ph.D. degree in engineering sciences in the Université catholique de Louvain, Belgium. Research interests include RF MEMS and devices.

e-mail: samer.houri@uclouvain.be
Université catholique de Louvain
Place du Levant, 3, Maxwell Building
B-1348 Louvain-la-Neuve, Belgium

Danielle Vanhoenacker-Janvier received the electrical engineer degree and the Ph.D. degree in applied sciences from the Université catholique de Louvain (UCL), Belgium, in 1978 and 1987, respectively. She is currently with UCL, where she was an Assistant (1979–1987), a Senior Scientist (1987–1994), an Associate Professor (1994–2000), a Professor (2000–2007), and has been a Full Professor since 2007 with the Microwave Laboratory, where she was the Head (2001–2007). She has been involved in the study of atmospheric effects on propagation above 10 GHz for over 30 years. She was engaged in the analysis, design, and measurement of microwave planar passive and active circuits with a special interest, since 1994, in microwave ICs on SOI. She has authored over 140 technical papers and coauthored a book. She is a Reviewer for various international conferences and IEEE and IET journals. She is a member of the evaluation committee of various Laboratories and Research Centers.

e-mail: danielle.vanhoenacker@uclouvain.be
Université catholique de Louvain
Place du Levant, 3, Maxwell Building
B-1348 Louvain-la-Neuve, Belgium

Jean-Pierre Raskin – for biography, see this issue, p. 17.