Paper

Analysis of the Dispersion of Electrical Parameters and Characteristics of FinFET Devices

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Abstract— Extensive numerical simulations of FinFET structures have been carried out using commercial TCAD tools. A series of plasma etching steps has been simulated for different process conditions in order to evaluate the influence of plasma pressure, composition and powering on the FinFET topography. Next, the most important geometric parameters of the FinFETs have been varied and the electrical characteristics have been calculated in order to evaluate the sensitivity of the FinFET electrical parameters on possible FinFET structure variability.

Keywords— FinFET, line edge roughness, parameter variability, plasma etching, technology computer aided design (TCAD).

1. Introduction

As the dimensions of MOS transistors are shrunk, the close proximity between the source and drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel. Undesirable short channel effects (SCE) induce higher subthreshold slope, threshold voltage roll-off, and punch-through between the drain and source. Multi-gate MOS SOI transistors, e.g., fin field effect transistors (FinFETs), are expected to be promising candidates for the next generation CMOS devices [1]. Because of their structure, FinFETs suppress short channel effects thus leading to further improvement of CMOS circuit performance [2].

However, small-size FinFETs are sensitive to technological process variations, which disturb the electrical characteristics and lower manufacturing yield. Numerical simulation and modeling of the effect of process parameter modifications and random variations becomes a very relevant task. In the presented work, key processes of fin formation, and their influence on manufacturing yield have been discussed. A methodology of plasma modeling and simulation for advanced silicon devices has been presented. Different plasma-related effects (such as loading effects, sidewall bowing and aspect ratio dependent etching) occurring during fin formation and affecting the fin size and shape have also been explained. Finally, the influence of polysilicon overetch on FinFET performance is discussed.

2. Process Simulations

Most plasma etch processes are based on either dc discharge or radio frequency (RF)-excited plasma, typically driven at a frequency of 13.56 MHz. During such discharge, electrons, ions, and reactive species are generated mainly in the bulk of the plasma. Three fundamental reactions may occur when an ion strikes a molecule: electron attachment, ionization and dissociation. The ions are transported towards the surface via a sheath area and impinge on the surface. The fidelity of pattern transfer during etching depends on important process characteristics, that is ion-energy distribution functions (IEDFs) and ion-angular distribution functions (IADFs). Theoretical study of sheath phenomena is therefore critical to developing appropriate models that will increase understanding of the influence of reactor conditions on plasma etching behavior. The IEDFs and IADFs are calculated using the Monte Carlo (MC) method.

A key aspect for fin formation is the anisotropy of the reactive ion etching (RIE) process. It is directly responsible for the shape and size of the fin area. The RIE process conditions have been chosen to etch a fin with the height of 60 nm and width of 20 nm as the reference model shown in Fig. 1(a). We have used CF4 plasma with the composition of gas 69 a.u./ion 19 a.u. under 100 mTr pressure and excited by a 50 V(dc)/55 V(ac) power source. However, the plasma etching process gives rise to a number of undesirable effects, which may be noticed, if the fin sidewall is enlarged (Fig. 1(b)). First, a random distortion of the sidewall edge may be observed. This phenomenon is called surface roughness and may play a significant role in FinFET device performance. The fin surface roughness is caused by charging effects in the plasma. Other plasma-related effects that have to be taken into account during fin formation are the so-called loading effects. They occur when the total area of the material exposed to the etchant decreases. This occurs obviously in the vicinity of the corners between the buried SiO_2 layer and the sidewalls of the projected fin. Then the reactive species become consumed. and the etch rate decreases, making the process lose its anisotropic character. The resulting fin sidewall becomes rounded instead of being perpendicular to the substrate.

The following parameters of the RIE process and their influence on the FinFET profile have been considered: gas pressure, gas composition and plasma powering.

2.1. Gas Pressure

The pressure of the gas in the chamber strongly influences the spatial distribution of the active plasma. As shown in Fig. 2 (obtained using the MC method), at lower pressures
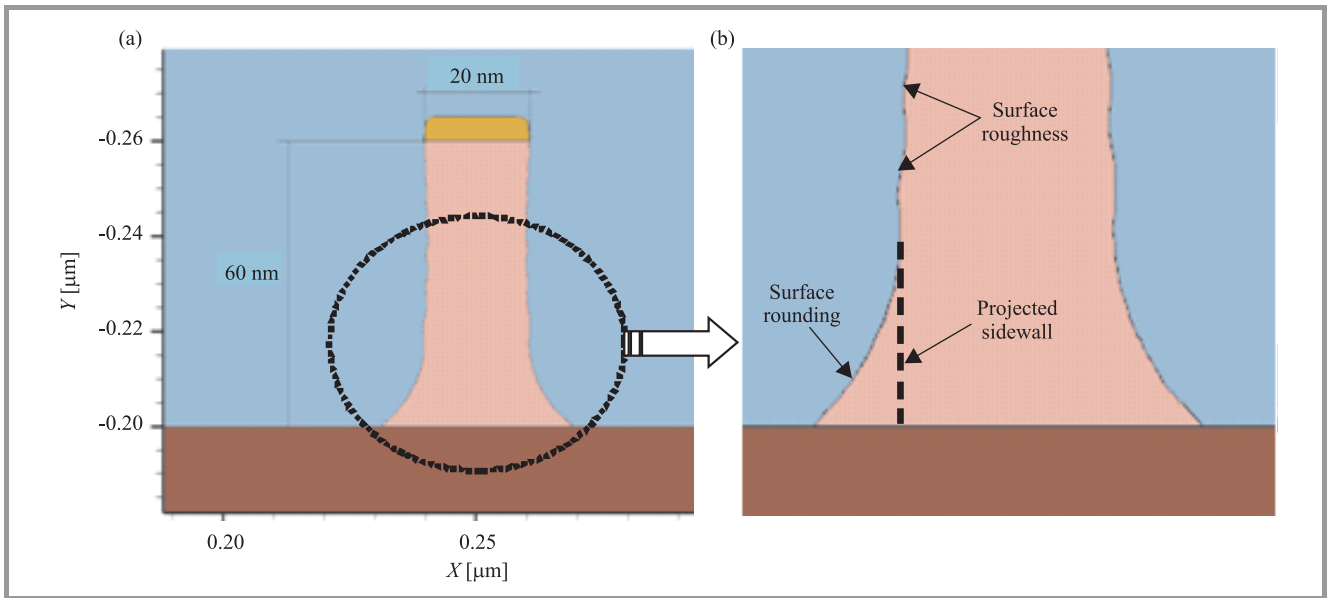
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Fig. 1. Fin cross-section after RIE process: (a) overall view, (b) details of the fin sidewall topography: surface roughness at the sidewalls and surface roundings at the corners.

the gas flow acts as an anisotropic beam while at higher pressures spontaneous ion-molecule collisions make the gas flow more like an isotropic cloud. Apart from weaker etching anisotropy the increased gas pressure lowers the etching rate.
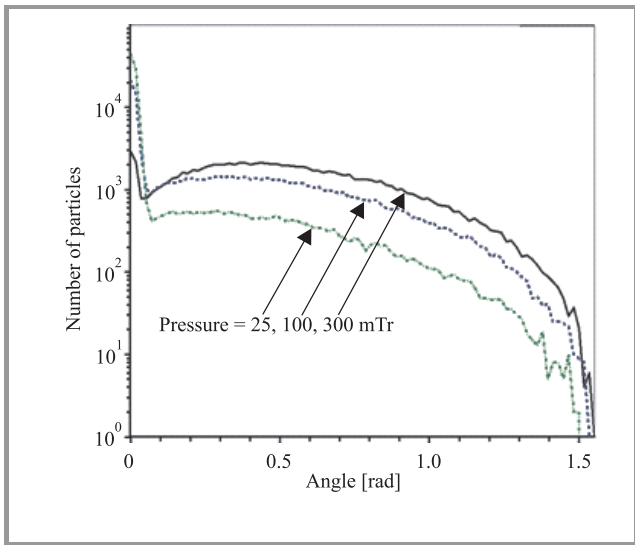

Fig. 2. Ion angular distribution for different chamber gas pressures calculated using the MC method.

The weak anisotropy at higher pressures is followed by lower quality of the patterning. For example, it influences the ratio between the projected fin height and the calculated width of the silicon area etched via the window opened in the mask. However, the effect of the lower etching rate seems to be somewhat ambiguous, because it may be helpful for better control of the total layer thickness etched. In our case the change of plasma pressure from 25 to 100 mTr has had approximately the same effect on the fin

Table 1
Fin_{width} versus chamber gas pressure

Pressure [mTr]	Ratio	Rate [nm/min]	Fin_{width} [nm]
25	3.8	647	25
100	3.46	661	20
300	2.92	587	16

profile as the pressure variation from 100 mTr to 300 mTr. The effect of the gas pressure on the etching rate is illustrated in Table 1.

2.2. Gas Composition

The RIE processes with three types of gas mixtures, i.e., gas 69 a.u./ion 19 a.u. (CF4); gas 96 a.u./ion 19 a.u. (SF6) and gas 80 a.u./ion 80 a.u. (HBr) have been evaluated. The results are shown in Table 2. We have considered the neutral to ion flux ratio: the lower the neutral to ion flux ratio the better the anisotropy thus the fin area obtained using HBr is thicker than the one obtained using SF6 or CF4.

Table 2
Fin_{width} versus gas and ion composition

Gas/ion [a.u.]	Ratio	Rate [nm/min]	Fin_{width} [nm]
69/19	3.46	661	20
96/19	3.03	598	17
80/80	4.86	730	34

In Fig. 3 the fin etch by gas/ion 80/80 a.u. has been shown. The effect of bowing of the sidewalls in the etched profile is visible. It may be induced by ion deflection (ion
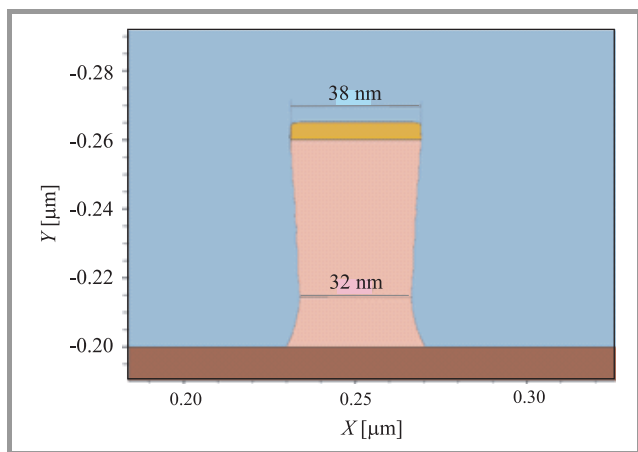
Fig. 3. Fin sidewall bowing.

trajectory distortion) in very narrow spaces between the fins. The angular distribution of ions impacting and subsequently scattered by the etching feature is expected to be the primary cause of non-vertical sidewalls.

2.3. Plasma Powering

Three different powering configurations have been tested. The results are shown in Table 3. In general, increasing power leads to higher etching rate and anisotropy. However, we have found maxima of the etching rate as well as of the anisotropy for $V(dc)$ potential 50 V and $V(ac)$ potential 55 V, respectively. Higher $V(dc)$ and $V(ac)$ potentials result in lower etching rates and ratios. The maximum etching rate is limited either by the chemical reaction rate at the surface or the flow of arriving ions. Higher potentials result in spontaneous collisions thus decreasing anisotropy.

Table 3
Fin_{width} versus power settings

$V(dc)/V(ac)$ [V]	Ratio	Rate [nm/min]	Fin_{width} [nm]
20/25	3.27	615	20
50/55	3.46	661	20
100/105	3.18	611	19

Therefore, anisotropic etch is controlled by the shadowing effect and the directionality of the incoming ions. The lower $V(dc)$ potential is responsible for domination of the isotropic chemical etch.

3. Device Simulations

In order to estimate the variability of fin dimensions in the FinFET caused by the RIE process dispersion Synopsys Sentaurus Structure Editor and Sentaurus Device applications have been used.
A three-dimensional FinFET model has been built (Fig. 4). The structure has been created on a SOI substrate with 60 nm p-type device layer (boron conc.$= 1 \cdot 10^{16}$ cm^{-3}).

Source and drain have been doped with arsenic (conc.$= 5 \cdot 10^{19}$ cm^{-3}). Fin dimensions are as follows: $Fin_{width} = 20$ nm, $Fin_{height} = 60$ nm. Over the fin a thin (2 nm) HfO_2 gate dielectric layer has been deposited. Over the gate dielectric silicon nitride spacers have been formed thus defining $Gate_{length} = 25$ nm. The polysilicon layer has been heavily doped with arsenic (conc.$= 1 \cdot 10^{20}$ cm^{-3}).
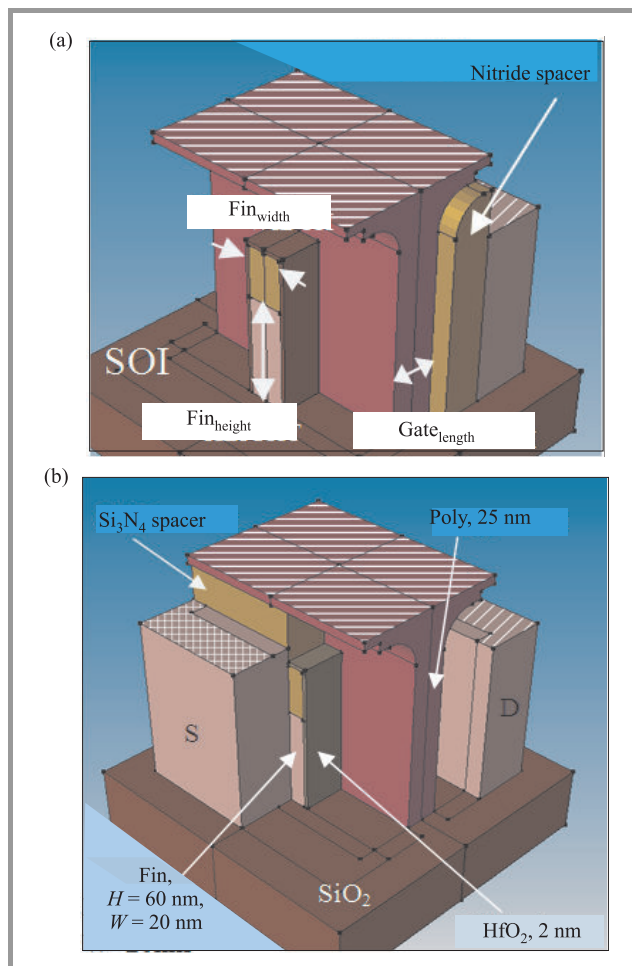

Fig. 4. FinFET structure: (a) details of the fin, (b) details of the spacer.

The electrical characteristics and parameters of the FinFET have been calculated in order to evaluate the influence of RIE dispersion on the device operation as a switch for integrated circuit applications. The FinFET has been biased as follows: gate-source voltage $V_{GS} = -0.5$ V $- 1$ V, drain-source voltage $V_{DS} = 0.1$ V. An example of the obtained $I_D(V_{GS})$ transfer characteristics is shown in Fig. 5.
The following electrical parameters have been taken into account: threshold voltage (V_T), transconductance (g_M), and subthreshold swing (SS). Table 4 presents the variation of the FinFET electrical parameters due to Fin_{width} change. The following remarks may be formulated. Firstly, the threshold voltage values are very low. They result directly from the shape of the $I_D - V_{GS}$ curves and are related to the non-optimized gate stack structure. Due to the very low (in terms of the gate-stack structure) channel doping
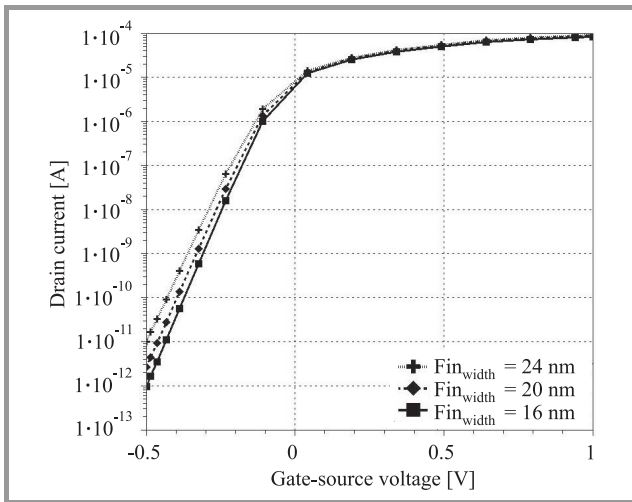
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Fig. 5. FinFET $I_D - V_{GS}$ characteristics for a series of fin widths.

concentration in the fin area the FinFETs can be switched off only by negative gate bias. Nevertheless, one may easily notice an improvement of the subthreshold slope with a decrease of the Fin_{width}. This is most likely due to the fact that in narrow FinFETs the gate control over the channel conduction is better [3].

Table 4
FinFET electrical parameters for different values
of Fin_{width}

Fin_{width} [nm]	V_T [V]	g_M [μS]	SS [mV/dec]
16	-0.102	133.1	67.8
20	-0.104	134.3	70.8
24	-0.106	126.1	73.9

As shown in Fig. 4 the polysilicon gate has been created using the silicon nitride spacers. Spacer lithography technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity and critical dimension (CD) variation. Simulations of the spacer lithography variations causing $Gate_{length}$ variations have been also carried out. The results are shown in Table 5.

Table 5
FinFET electrical parameters for different values
of $Gate_{length}$

$Gate_{length}$ [nm]	V_T [V]	g_M [μS]	SS [mV/dec]
20	-0.109	112.4	73.3
25	-0.104	134.3	70.8
30	-0.088	189.5	69.2

It may be noticed, that as expected a decrease of $Gate_{length}$ leads to the threshold voltage lowering. It may be also stated, that the shortening of the gate induces lowering of the transconductance. This somewhat unexpected FinFET behavior has been caused by the method to generate device

structures considered in this paper. We have assumed that the distance between the heavily doped source and drain areas is constant. Different values of the $Gate_{length}$ parameter have been obtained by the variation of the spacer thickness. However, an increase of the latter (and decrease of the $Gate_{length}$) induces large increase of the series resistance. This, in turn, strongly degrades current conduction and transconductance.

4. Results and Conclusions

The ultra-thin fin formation with good uniformity is still a challenging task for FinFET manufacturing. The uniformity of silicon fin width (Fin_{width}) is especially critical for the FinFET because its variation may cause a change in channel potential and subband structure, which governs short-channel behavior and quantum confinement effects of inversion charges. Also if $Gate_{length}/Fin_{width}$ ratio is smaller than 1.5, drain induced barrier lowering (DIBL), subthreshold swing, and off-state leakage current increase significantly. Thus, a small change of fin width may result in large variation of device characteristics for short gate lengths [4].

It has been shown, that non-optimized FinFET structure leads to a number of undesired effects, e.g., incorrect threshold voltage and degraded $I - V$ characteristics.

It has been also shown in our paper that the uniformity of silicon fin width strictly depends on the RIE parameters, such as pressure, gas composition, and RF power. Therefore, a precise control of these parameters during process is critical.

Acknowledgements

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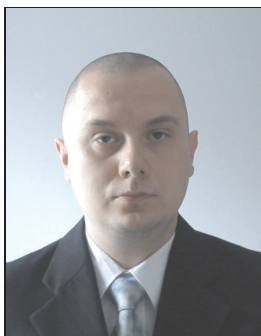
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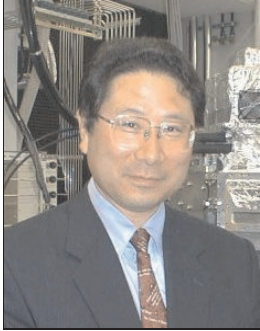
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