Invited paper

Challenges in scaling of CMOS devices towards 65 nm node

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Abstract—The current trend in scaling transistor gate length below 60 nm is posing great challenges both related to process technology and circuit/system design. From the process technology point of view it is becoming increasingly difficult to continue scaling in traditional way due to fundamental limitations like resolution, quantum effects or random fluctuations. In turn, this has an important impact on electrical device specifications especially leakage current and the circuit power dissipation.

Keywords— CMOS devices, gate dielectrics, shallow junctions, silicide, gate stack, lithography, gate patterning, silicon recess, device integration.

1. Introduction

The traditional scaling approach, which has been the base of the semiconductor industry for the last 30 years is beginning to show the fundamental limits of the materials building the modules of a planar CMOS transistor. Significant efforts are being devoted to the introduction of new materials that will replace the existing ones to further extend the device scaling process.

However, even though the new materials and device architectures are being investigated, the gate length scaling below 60 nm has a significant impact on the electrical properties of the devices. The continuous thinning of the gate dielectric layers, the increasing channel doping and the aggressive, abrupt junctions, required to control the short channel effects, start to significantly affect circuit power dissipation.

Nitrided oxides, gate predoping, offset spacers, spike anneal, tilted pocket implants, ultra low energy implants are a few examples of the process steps that were introduced in the 0.13 μm technology generation to enable device gate length scaling. These previous "improvements" will be able to prolong scaling down to 65 nm node. New solutions to device architecture, device substrate, gate stack will have to be introduced to maintain 12% increase in device performance forecasted by ITRS roadmap [1].

This paper gives an overview of the main challenges being faced in the front-end of line (FEOL) technology development for 65 nm node. This includes the gate stack, gate patterning, junction and silicide process.

2. Gate stack

Aggressive scaling of CMOS devices puts severe constrains on the gate dielectric. In order to meet requirements for drive current and off-state leakage set up by ITRS roadmap it is essential to simultaneously scale further gate oxide thickness and limit the gate leakage current. In addition, mobility degradation has to be minimized and gate oxide reliability still has to meet the 10-year lifetime requirements. Despite low gate leakage current as compared to nitrided oxides (Fig. 1), high-k dielectrics are still not ready for device integration due to reliability problems, high mobility degradation and instability of the threshold voltage.

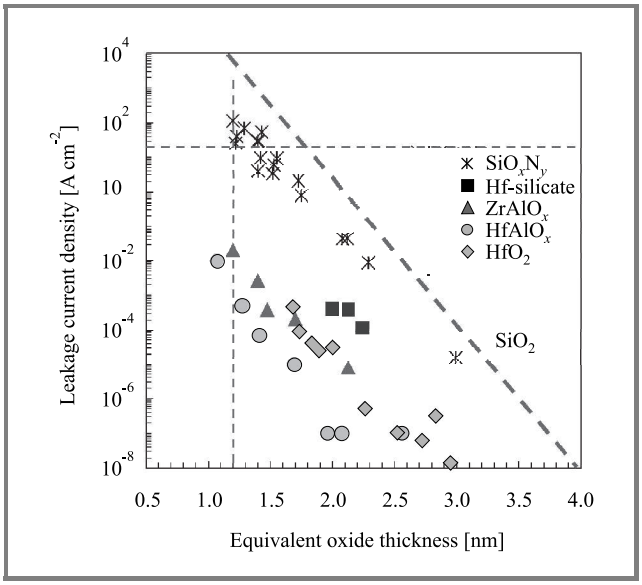

Fig. 1. Comparison of different gate dielectrics with respect to gate leakage and EOT.

Therefore, there is strong motivation to extend the use of oxynitrides to its ultimate limits. Oxynitrides fabricated with a new plasma nitridation techniques such as decoupled plasma nitridation (DPN) [2] or slot plane antenna (SPA) seem to be the best candidates for 65 nm high performance and general purpose CMOS devices (Fig. 1) at least until high-k materials reach their maturity for the gate dielectric applications. Using plasma nitridation it is possible to introduce more nitrogen than with furnace nitridation techniques into thin oxide layer and thus increase the dielectric constant k and scale equivalent oxide thickness without reducing significantly physical oxide thickness [3].

Continued thinning of gate dielectrics and an increase of the interface-state density created by plasma nitridation bring many concerns related to reliability issues. Thorough characterization shows, however, that a careful optimization of the gate dielectric process enables maintaining the maximal operation voltage, at which the device can be operational for 10 years, above the supply voltage [4]. This is possible since oxide reliability is dependent rather on physical oxide thickness than on EOT.

The gate activation, which has direct impact on the drive current, is more and more affected by the reduced thermal budged required in order to control short channel effects. Additional gate implantation called gate predoping is mandatory to maintain low gate depletion. Metal gate seems to be a solution to this problem, however, due to the unsuitability of the work function and highly complex integrity it will not be ready for the 65 nm node.

3. Gate patterning

In order to cope with progressive scaling of CMOS devices new lithography techniques are being investigated. The 157 nm lithography is considered as the leading candidate for semiconductor device manufacturing at the 65 nm technology node [5]. However, development of 157 nm lithography requires considerable effort and effective solutions to resist and reticle materials, lenses, CD metrology, etc. This list of challenges raises fears that the 157 nm lithography will not be ready for the 65 nm node. Therefore, other methods such as resist or hard mask trimming were developed to support lithography in the scaling progress.

In the 65 nm node, where the gate length is in the range of 65–25 nm, depending on applications, the key process step developments are lithography, dry etch, and CD metrology. With respect to lithography, the emphasis is put on the development of thin resist processes (using 193 nm lithography) in combination with alternating phase shift mask (AltPSM) optical extensions. With this combination the lines down to 65 nm with good CD control can be printed (Fig. 2a). Further reduction of the gate length is obtained by subsequent resist or hard mask trimming (Fig. 2b). Trimming techniques allow obtaining gate lengths down to a few nanometers.

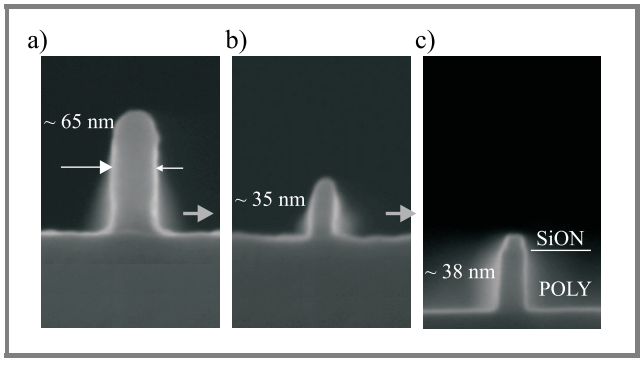

Fig. 2. Visualization of the trim and gate etch: (a) showing the X-section of features after litho; (b) etch trim; (c) gate etch and strip.

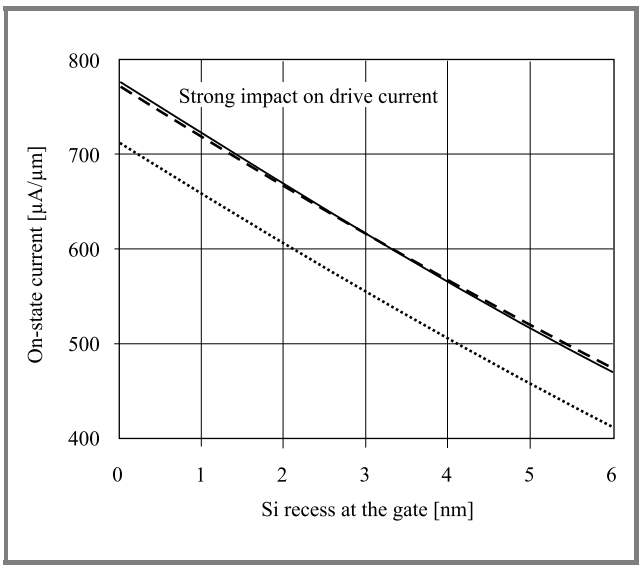

Fig. 3. Impact of Si recess created at the gate patterning on the drive current (simulation results).

An important issue when scaling devices and the gate oxide thickness is silicon recess in source and drain areas which occurs during overetch step in gate electrode patterning. Even small, a few nanometers consumption of Si in the substrate has considerable impact on device performance and leads to increase in the off-state leakage and series resistance (Fig. 3).

4. Junction

Approaching the 65 nm node ITRS requirements for ultrashallow junctions (USJ) has become a great challenge, es-

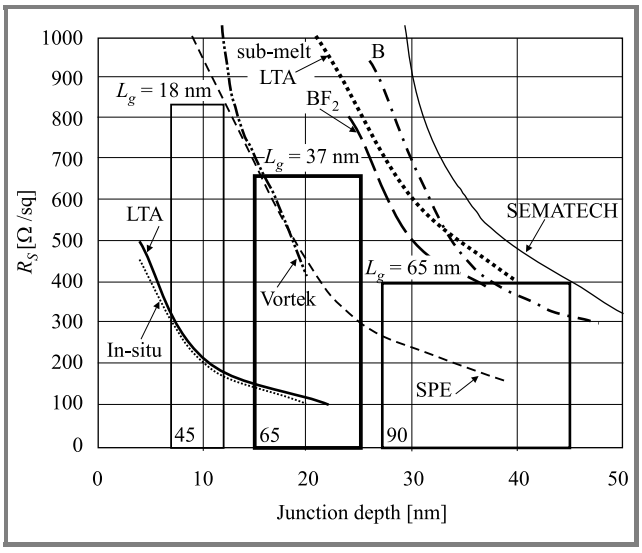

Fig. 4. Summary of p^+/n junctions obtained with different techniques. The boxes indicate the requirements for different technology generations (literature results).

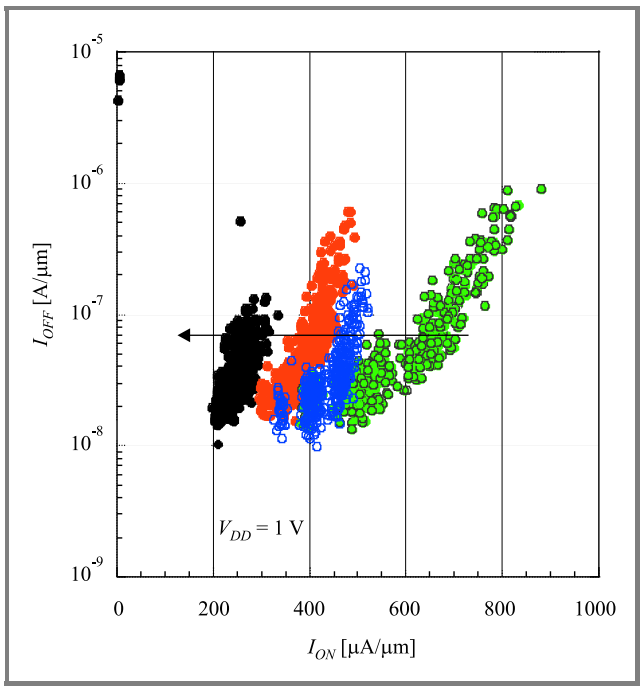

Fig. 5. Drive current versus off-state leakage for NMOS devices with different doses in extensions. The arrow indicates the reduction in the doping concentration in the junctions.

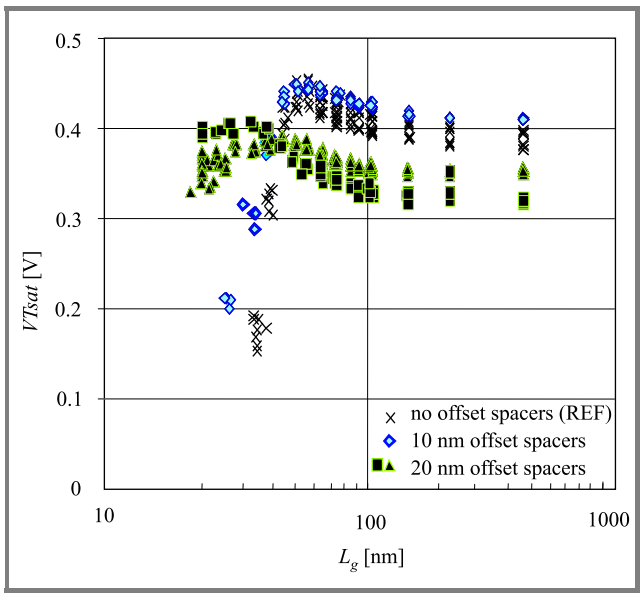

Fig. 6. Impact of offset spacers on control of short channel effects.

pecially for p^+ dopants. With boron, traditionally used for p^+/n junction formation, implanted alone and annealed with conventional methods, the 90 nm node specifications can hardly be reached (Fig. 4). Simple lowering of implantation dose reduces the junction depth but on the other hand leads to high series resistance and degradation of the on-state current (Fig. 5). The literature data shows that only with very sharp spike anneal (high rump-up and rump down using, e.g., Levitor or Vortek tool) the improvement in the trade-off between junction resistance and junction depth can be achieved [6]. Even better results can be obtained with a co-implantation with other elements and/or pre-amorphization implants in conjunction with spike anneal. The combination of Ge pre-amorphization, F co-implantations and fast ramp-up spike anneal appeared to be sufficient to fulfill the 65 nm node requirements [7]. For the next generation other alternative routes of forming the junctions such as solid phase epitaxial re-growth (SPER) [8] or laser anneal (LTA) are investigated.

Introduction of offset spacers allows relaxing the requirements for the extensions without aggravating short channel effects (Fig. 6). This, however, puts very severe constrains on their width control since any small variations in the spacer width may result in huge variation in VT and off-state leakage.

5. Silicide

The scaling of the gate length (below 40 nm) goes in parallel with the reduction in the HDD junction depth. Shallower junctions, in turn, determine more constrained requirements for the silicides. Conventionally used CoSi seems to reach its ultimate limits. For the gate length below 40 nm gate sheet resistance increases dramatically (Fig. 7), which is related to silicide instability and silicide cracking. No improvement is observed when Co is alloyed with Ni. Besides, high Si consumption during the silicide process leads to unacceptable increase in the junction leakage. Therefore, other materials such as NiSi or PtSi were considered as potential candidates for 65 nm technology node [9].

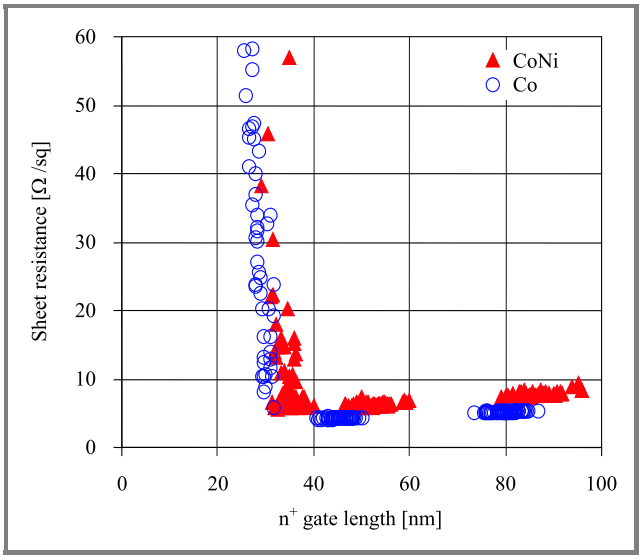

Fig. 7. Gate sheet resistance of Co and CoNi silicided gate as a function of the gate length.

For Ni-silicided poly gates low sheet resistance is obtained down to the narrowest line widths (Fig. 8). The trade-off between junction leakage and silicide sheet resistance is

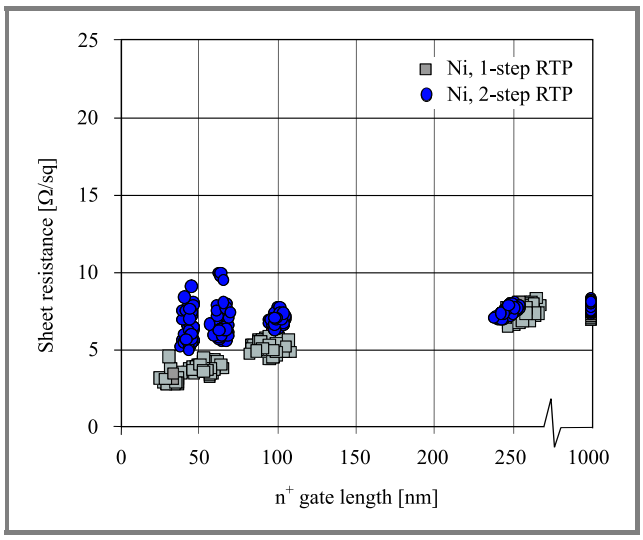

Fig. 8. Gate sheet resistance of Ni silicided gate processed with different annealing steps as a function of the gate length.

in favour of Ni-silicide. Besides, NiSi is known to have smaller contact resistance, which has significant role in total resistance of the junctions in sub-50 nm devices.

6. Conclusions

Conventional bulk scaling reaches its physical limitations. The 65 nm CMOS appears to be the last technology node, where the conventional planar transistor architecture in conjunction with standard modules will be applied. In order to maintain the trend in performance improvement, next technology generations will probably have to deal with more exotic solutions such as strained silicon, metal gate integration, high-*k* dielectrics (mainly for low power applications) and eventually double gate architectures.

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