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Invited paper

Variability of the local ϕ_{MS} values over the gate area of MOS devices

Henryk M. Przewłocki, Andrzej Kudła, Danuta Brzezińska, and Hisham Z. Massoud

Abstract—The local value distributions of the effective contact potential difference (ECPD or the ϕ_{MS} factor) over the gate area of Al-SiO_2-Si structures were investigated for the first time. A modification of the photoelectric ϕ_{MS} measurement method was developed, which allows determination of local values of this parameter in different parts of metal-oxide-semiconductor (MOS) structures. It was found that the ϕ_{MS} distribution was such, that its values were highest far away from the gate edge regions (e.g., in the middle of a square gate), lower in the vicinity of gate edges and still lower in the vicinity of gate corners. These results were confirmed by several independent photoelectric and electrical measurement methods. A model is proposed of this distribution in which the experimentally determined $\phi_{MS}(x,y)$ distributions, found previously, are attributed to mechanical stress distributions in MOS structures. Model equations are derived and used to calculate $\phi_{MS}(x,y)$ distributions for various structures. Results of these calculations remain in agreement with experimentally obtained distributions. Comparison of various characteristics calculated using the model with the results of photoelectric and electrical measurements of a wide range of Al-SiO_2-Si structures support the validity of the model.

Keywords*— *MOS structure, photoelectric measurements, electrical parameters, mechanical stress.

1. Introduction

It has been previously shown (e.g., [1, 2]) that mechanical stress in metal-oxide-semiconductor (MOS) devices influences their electrical parameters. One of these electrical parameters is the effective contact potential difference (ECPD), called also the ϕ_{MS} factor. The dependence of ϕ_{MS} on stress was quantitatively estimated in [3]. On the other hand, it has been shown [2, 4, 5] that usually, mechanical stress is nonuniformly distributed under the gate of a MOS structure. In case of metal gate structures studied in this work, the mechanical stress distribution in the dielectric layer under the gate is characterized by a considerable compressive stress σ_0 in the central part of the gate and abrupt stress changes in the vicinity of gate edges, as shown in Fig. 1. It is therefore expected that ϕ_{MS} will have different values in the vicinity of gate edges and far away from them. This has not been observed until now, since conventional methods used to determine electrical parameters of MOS devices, including ϕ_{MS}, measure the parameter values which are averaged over the gate area. In this work, the lateral distributions of ϕ_{MS} values over the gate area were measured for the first time. A new measurement method was developed for that purpose, which is a modification of the photoelectric ϕ_{MS} measurement method [6], as described below.

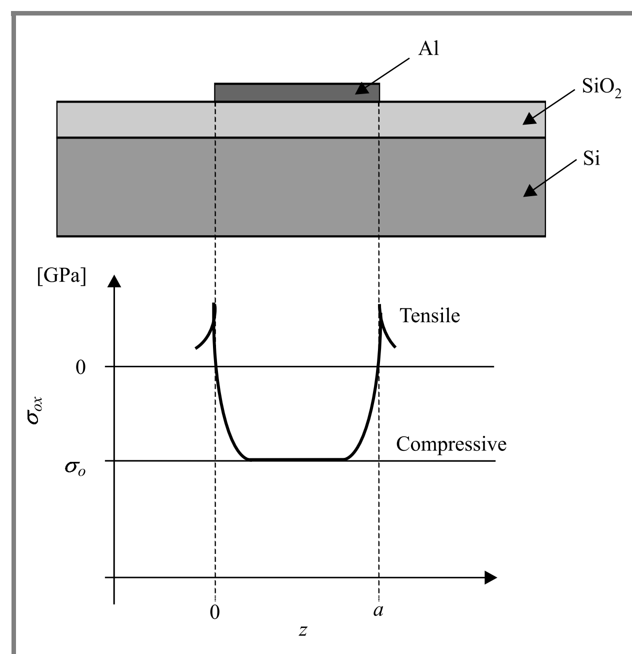

Fig. 1. The expected one-dimensional distribution of stress $\sigma_{ox}(z)$ in the oxide layer under the aluminum gate.

Photoelectric measurement results and their correlation with stress distributions are supported by electrical measurements of various MOS structures. A model of lateral distribution of ϕ_{MS} local values over the gate area has also been developed and is presented later. A range of measurement results fully supports the validity of the model.

2. Experimental

2.1. Measurement methods

Distributions of ECPD local values over the gate area were measured using a newly developed modification of the photoelectric ϕ_{MS} measurement method [6]. The principle of this modified photoelectric method is illustrated in Fig. 2. A focused beam of laser generated UV radiation illuminates a small fragment of the gate area, causing internal

photoemission to take place in this region of the MOS structure. The resulting photocurrent I versus gate voltage V_G characteristics can be taken in the external circuit. Analysis of these characteristics allows determination of the local ϕ_{MS} value in the illuminated region, as described in [6] and references therein. Hence, scanning the gate

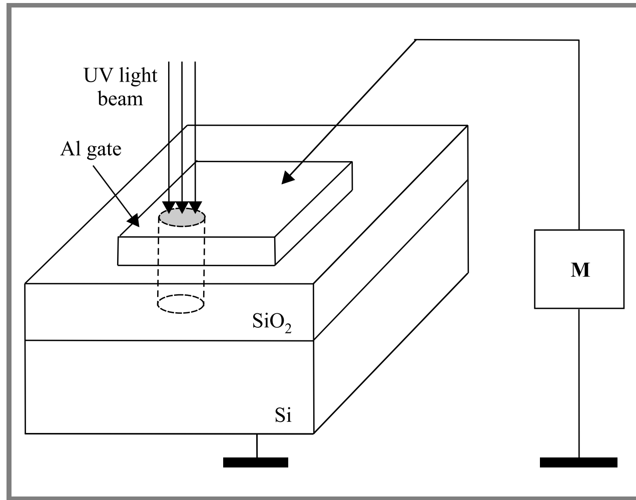

Fig. 2. Illustration of the principle of the modified photoelectric method of ϕ_{MS} determination.

with the UV light beam allows determination of the lateral ϕ_{MS} distribution over the gate area. Results obtained using this method are verified using the purely electrical $C(V)$ measurements and using the photoelectric measurements made on entire MOS capacitors of different shapes and dimensions, as described later.

2.2. Measured structures

In this work, measurements were made on Al/SiO_2/n$^+$-Si ($\rho \cong 0.015$ Ωcm) and on Al/SiO_2/n-Si ($\rho \cong 4$ Ωcm) capacitors of different geometries. MOS capacitors with different gate shape and area were characterized on each of the silicon wafers under investigation. The aluminum gates were either square shaped (SQ), with side $a = 0.1 \ldots 1.0$ mm, or were in the form of sets of narrow aluminum lines (STR). Although SiO_2 layers of current technological interest are thinner than $t_{ox} \cong 3$ nm, we used thicker oxides to optimize the sensitivity of the applied photoelectric methods [6]. MOS structures with three oxide thicknesses $t_{ox} = 20$, 60 and 160 nm, and two aluminum gate thicknesses $t_{\mathrm{Al}} = 35$ and 400 nm were used in this study.

2.3. Measurement results

First, the ECPD values were determined by the standard photoelectric method [6], for MOS capacitors with widely different values of R, where R is the ratio of the gate perimeter P to the gate area A of the MOS structure. Typical results of such measurements are shown in Fig. 3. It can be seen, that ϕ_{MS} values for entire MOS capacitors decrease monotonically with increasing R ratio and

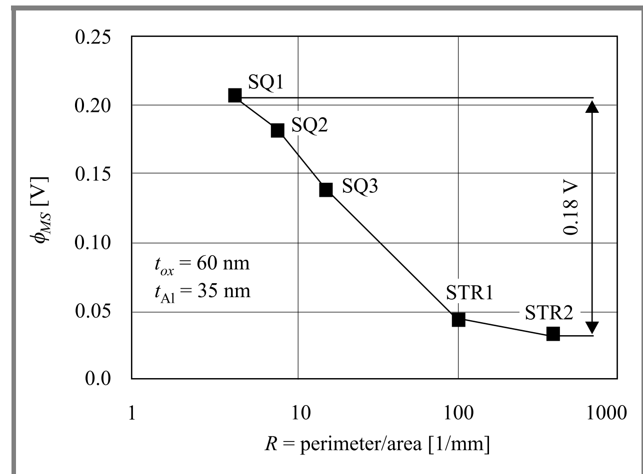

Fig. 3. The ϕ_{MS} measurement results (solid squares) for the entire SQ and STR gate Al-SiO_2-Si capacitors with different R ratios. Lines are drawn for eye guiding purposes.

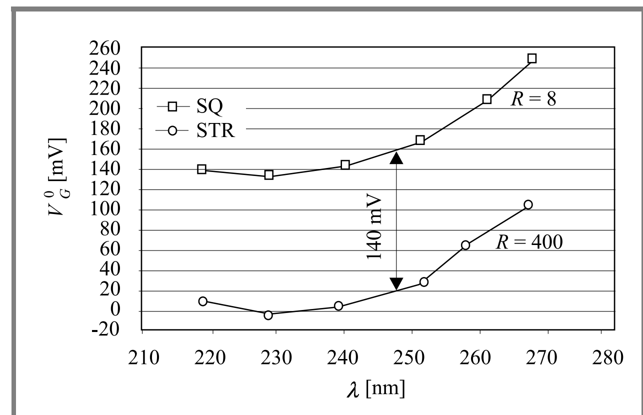

Fig. 4. Spectral characteristics of the zero-photocurrent-voltage $V_G^0(\lambda)$, taken for two Al-SiO_2-Si capacitors with different R values.

tend to saturate for large values of R. It was also found that the spectral characteristics of the zero-photocurrent-voltage $V_G^0(\lambda)$, taken for capacitors of different R values, are shifted in parallel against each other along the voltage axis, as shown in Fig. 4. Since for any MOS structure: $V_G^0(\lambda) = \phi_{MS} + \mathrm{const}(\lambda)$; [6], this result shows that for two structures with different R ratios, the difference between their ϕ_{MS} values can be determined at any wavelength λ within the used UV range. The $\phi_{MS}(R)$ dependence, illustrated in Figs. 3 and 4, suggests, although indirectly, that ϕ_{MS} values in the vicinity of gate edges are lower than far away from these edges. The direct proof of this property requires the use of measurement techniques, which allow determination of local ϕ_{MS} values in the regions, which are small in comparison with the overall dimensions of the gate. Hence, the modified photoelectric method, described above and illustrated in Fig. 2, was used for that purpose. The typical $V_G^0(z)$ characteristics (where z is a coordinate in the gate surface plane), taken using this method, are shown in Fig. 5, which proves that indeed ϕ_{MS} values at gate edges

are lower than in the middle of the gate, and that in the vicinity of gate corners the ϕ_{MS} values are still lower than near the gate edges.

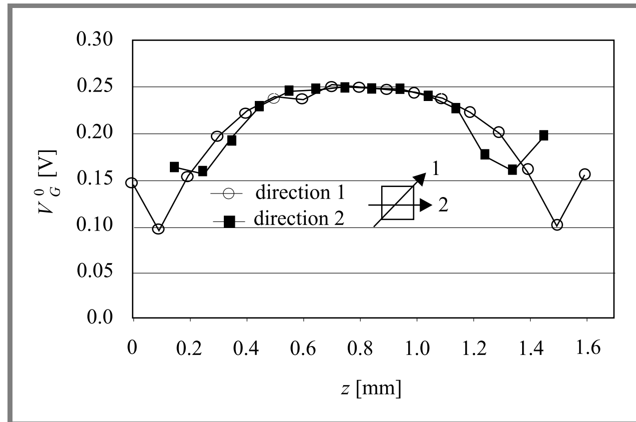

Fig. 5. Typical results of $V_G^0 = \phi_{MS} + \text{const.}$ local value measurements versus distance z, for SQ Al(35 nm)-SiO_2(60 nm)-Si(n^+) structure. Distance z is measured: 1) along the diagonal of the gate; 2) parallel to gate edges and through the middle of the gate.

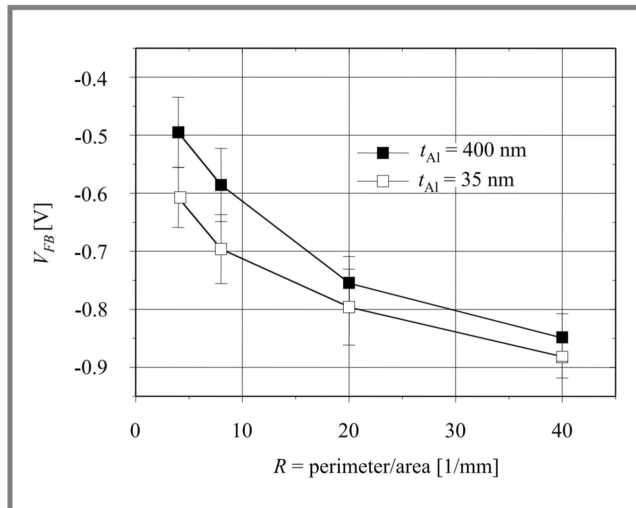

Fig. 6. Average V_{FB} values (squares) and their standard deviations (error bars) measured on SQ gate Al-SiO_2-Si capacitors with different R ratios. The solid squares are for thicker aluminum gate structures ($t_{Al} = 400$ nm), and the open squares are for thinner aluminum gate structures ($t_{Al} = 35$ nm). Lines are drawn as eye guides.

All the evidence of nonuniform ECPD distributions over the gate area, presented above, is based on photoelectric measurements. To exclude the possibility that the observed results are due to some unidentified optical effect, taking place when UV radiation illuminates the edges and corners of the gate, the results were confirmed by electrical measurements which do not involve the use of radiation. Taking into account that the ϕ_{MS} value directly influences that of the flat-band voltage V_{FB}, capacitance – voltage $C(V_G)$ characteristics were taken for MOS capacitors with different R ratio, and V_{FB} values were determined from these characteristics. This way V_{FB} values were obtained for thousands of Al/SiO_2/n-Si capacitors, with different R ratio, which were identically processed as the Al/SiO_2/n^+-Si structures measured by photoelectric methods, as described above. Results of these measurements consistently show that flat-band voltage values decrease with increasing values of R. Typical results of such measurements made on square gate (SQ) capacitors, with $R = 4$, 8, 20 and 40 mm^{-1} are shown in Fig. 6, for structures with aluminum gate thicknesses $t_{Al} = 35$ and 400 nm, fully confirming the conclusions drawn from results obtained by photoelectric methods.

3. Model

Stress distribution in the SiO_2 layer under the gate of a MOS capacitor, such as the distribution shown in Fig. 1, can be modeled in one dimension as:

$$\sigma(z) = \sigma_0 + \Delta\sigma(z) \tag{1}$$

with:

$$\Delta\sigma(z) = \Delta\sigma\left\{\exp(-z/L) + \exp[-(a-z)/L]\right\}, \tag{1a}$$

where σ_0 is the compressive stress in the central part of the gate, $\Delta\sigma = \Delta\sigma(0) = \Delta\sigma(a)$ is the maximum deviation of $\sigma(z)$ from the σ_0 value which occurs at gate edges (for $z = 0$ and $z = a$), a is the width of the gate in z-direction, and L is the characteristic length of the stress distribution. Assuming that the lateral ϕ_{MS} distribution, discussed above, is caused by lateral stress distributions, in such a way that $|\Delta\phi_{MS}(z)|$ is proportional to $\Delta\sigma(z)$, the one dimensional $\phi_{MS}(z)$ distribution can be expressed as:

$$\phi_{MS}(z) = \phi_{MS_0} + \Delta\phi\left\{\exp(-z/L) + \exp[-(a-z)/L]\right\}, \tag{2}$$

where ϕ_{MS_0} is the ϕ_{MS} value far away from gate edges, $\Delta\phi = \Delta\phi(0) = \Delta\phi(a)$ is the deviation of $\phi_{MS}(z)$ from the ϕ_{MS_0} value which occurs at gate edges (for $z = 0$ and $z = a$), and as results from experiment $\Delta\phi$ is negative. The average ϕ_{MS} value for the entire MOS capacitor, designated $\overline{\phi_{MS}}$ is given by:

$$\overline{\phi_{MS}} = \frac{1}{a}\int_0^a \phi_{MS}(z)\mathrm{d}z \tag{3}$$

and is a function of the a/L ratio.

The one dimensional analysis, presented so far, can be applied to some of the MOS capacitors of practical interest, e.g., to structures with gates in form of long and narrow stripes (STR), used in our experiments. However, in most of the cases, the problem considered is not of a one dimensional nature. For instance, for structures with square gates (SQ), of side length a, lying in the x, y plane, the $\Delta\sigma(x)$ and $\Delta\phi_{MS}(x)$ distributions are equally important as $\Delta\sigma(y)$ and $\Delta\phi_{MS}(y)$. Assuming that the properties

of the MOS system are isotropic in the x, y plane, these distributions can be expressed by Eqs. (1) and (2), with the z variable replaced by x and y. Assuming further that the principle of superposition can be applied to stress and ECPD distributions in the x, y plane, one obtains:

$$\Delta\phi_{MS}(x, y) = \Delta\phi_{MS}(x) + \Delta\phi_{MS}(y) \tag{4}$$

and

$$\phi_{MS}(x,y) = \phi_{MS_0} + \Delta\phi_{MS}(x,y)\,. \tag{5}$$

Equations (5) and (4), together with expressions for $\Delta\phi_{MS}(x)$ and $\Delta\phi_{MS}(y)$, analogous to Eq. (2), determine the $\phi_{MS}(x,y)$ distribution in the x, y plane of the gate area. Examples of $\phi_{MS}(x, y)$ distributions, calculated using the above equations, for structures with square gates (SQ) of different side lengths a are shown in Fig. 7.

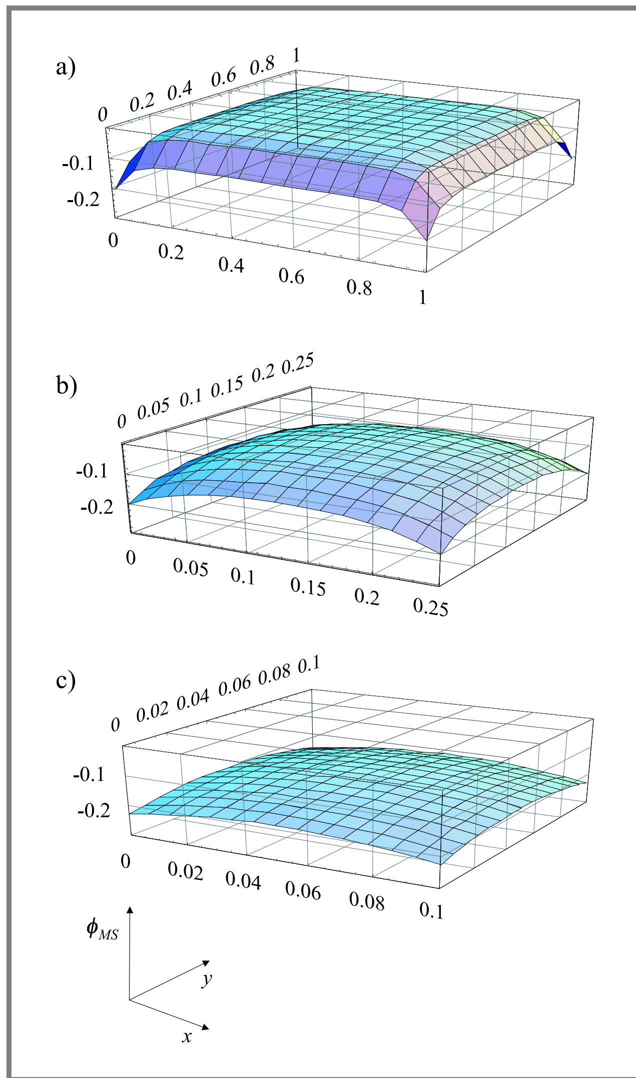

Fig. 7. The $\phi_{MS}(x, y)$ distribution calculated using the model, for SQ gate Al-SiO_2-Si capacitors of different side length a: (a) $a = 1$ mm; (b) $a = 0.25$ mm; (c) $a = 0.1$ mm, and using $\phi_{MS_0} = 0$ V, $\Delta\phi = -0.1$ V, $L = 0.05$ mm in the expressions for $\Delta\phi_{MS}(x)$ and $\Delta\phi_{MS}(y)$.

For such structures the average ϕ_{MS} value, designated $\overline{\phi_{MS}}$, is given by:

$$\overline{\phi_{MS}} = \frac{1}{a^2}\int_0^a\int_0^a \phi_{MS}(x, y)\mathrm{d}x\mathrm{d}y\,. \tag{6}$$

The integration of Eq. (6) yields:

$$\overline{\phi_{MS}} = \phi_{MS_0} + 4\frac{\Delta\phi \cdot L}{a}\left[1 - \exp\left(-\frac{a}{L}\right)\right] \tag{7}$$

showing that $\overline{\phi_{MS}}$ is a function of a/L, as clearly seen in Fig. 7. Equation (7) can be transformed to explicitly give the dependence of $\overline{\phi_{MS}}$ on the previously introduced R ratio:

$$\overline{\phi_{MS}} = \phi_{MS_0} + \Delta\phi \cdot L \cdot R\left[1 - \exp\left(-\frac{4}{L \cdot R}\right)\right]. \tag{8}$$

For capacitors with gates in form of long and narrow stripes of width a and length l, ($l \gg a$), similar reasoning leads to:

$$\overline{\phi_{MS}} = \phi_{MS_0} + \Delta\phi \cdot L \cdot R\left[1 - \exp\left(-\frac{2}{L \cdot R}\right)\right]. \tag{9}$$

The dependence of $\overline{\phi_{MS}}$ on R should be reflected in the dependence of the flat-band voltage $\overline{V_{FB}}$ (as measured on the entire MOS structure) on R. Assuming that the effective charge of the MOS system does not significantly depend on R, the $\overline{V_{FB}}(R)$ dependence for square gate structures is:

$$\overline{V_{FB}} = V_{FB_0} + \Delta V \cdot L \cdot R\left[1 - \exp\left(-\frac{4}{L \cdot R}\right)\right], \tag{10}$$

where V_{FB_0} is the local $V_{FB}(x, y)$ value far away from the gate edges, and $|\Delta V|$ is maximum deviation of $V_{FB}(x, y)$ from the V_{FB_0} value (ΔV is negative). Equations (8)–(10) are the equations of the model which can be used to determine $\overline{\phi_{MS}}(R)$ and $\overline{V_{FB}}(R)$ dependencies in MOS structures, as shown below.

4. Verification

To verify the model, experimental results were fit with the model equations. The best fit of model equations to the measurement results yields the model parameters for a given set of experiments, i.e., the values of ϕ_{MS_0}, $\Delta\phi$ and L, or V_{FB_0}, ΔV and L. As an example, model Eqs. (8) and (9) were fit to the ϕ_{MS} measurements illustrated in Fig. 3, and the result is shown in Fig. 8. The fit is good both for the square (SQ) gate structures (Eq. (8)) and for the (STR) structures with gates in form of narrow aluminum stripes (Eq. (9)). It should be noted that in both cases the fit is obtained for the same values of ϕ_{MS_0} and $\Delta\phi$ which strongly support the validity of the model. The (effective) L value is different for SQ and STR structures, since for STR structures L is comparable to the width a of the aluminum lines and the influences of both line edges overlap.

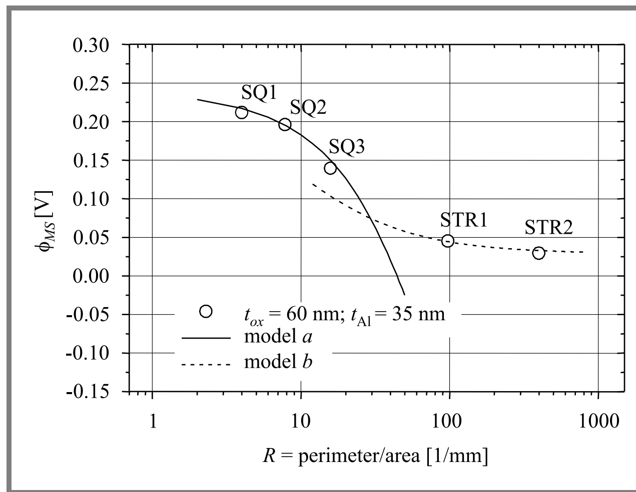

Fig. 8. Curves calculated using Eqs. (8) and (9) fit to the measurement results shown in Fig. 3, obtained for Al-SiO_2-Si capacitors with SQ and STR gates. Both curves are calculated using $\phi_{MS_0} = 0.236$ V, and $\Delta\phi = -0.106$ V in Eqs. (8) and (9). The curve calculated for SQ structures (model *a*) uses $L = 0.056$ mm in Eq. (8), and the curve calculated for STR structures (model *b*) uses $L = 0.090$ mm in Eq. (9).

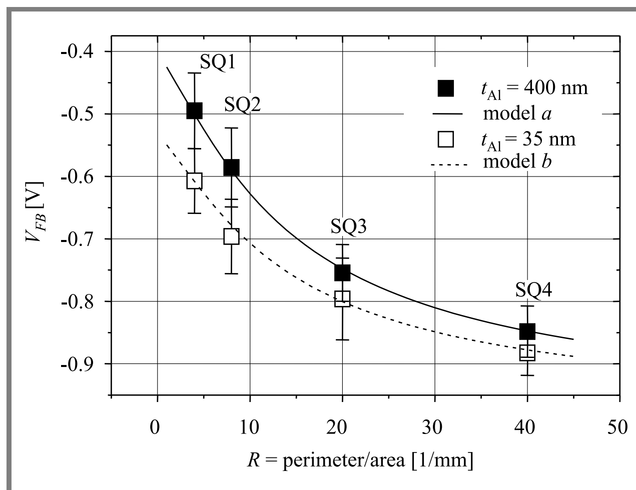

Fig. 9. Curves calculated using Eq. (10) fit to the V_{FB} measurement results shown in Fig. 6, for SQ gate Al-SiO_2-Si capacitors with different *R* ratio and different aluminum gate thickness. The upper curve (for $t_{Al} = 400$ nm) is calculated using $V_{FB_0} = -0.400$ V, $\Delta V = -0.148$ V, and $L = 0.170$ mm in Eq. (10). The lower curve (for $t_{Al} = 35$ nm) is calculated using $V_{FB_O} = -0.530$ V, $\Delta V = -0.115$ V, and $L = 0.170$ mm in Eq. (10).

As a result, the shape of the $\phi_{MS}(z)$ distribution is quite different in this case from the distributions obtained in case when $a \gg L$ (e.g., for large SQ structures).

The model was further verified by fitting Eq. (10) to the V_{FB} measurement results. As an example, Eq. (10) is fit to the measurement results illustrated already in Fig. 6, as shown in Fig. 9. The fit is good, both for the capacitors with thicker and the ones with thinner aluminum gates. It should be noted that the best fit gives higher values of both V_{FB_0} and $|\Delta V|$ for structures with thicker gates. This is the result that was expected since thicker aluminum layers cause higher compressive stresses σ_0 in the SiO_2 layer and larger $\Delta\sigma$ deviations at gate edges, supporting the assertion that the lateral distributions of ϕ_{MS} and V_{FB} values are caused by lateral distributions of stress σ_{ox} in the plane of the gate. Further support for this assertion was gained from an experiment based on the following reasoning. Any change in the stress distribution under the MOS system gate, should be reflected in changes of ϕ_{MS} and V_{FB} distributions. A change of stress distribution can be introduced if a gate of another MOS structure is placed close enough to the gate of investigated structure. Hence, a comparison was made between the $V_{FB}(R)$ characteristics of square gate capacitors, which were not surrounded by other capacitors in their immediate vicinity, with the characteristics of identical capacitors surrounded by protective aluminum rings of the same thickness $t_{Al} = 400$ nm, at a distance of 10 μm. The result

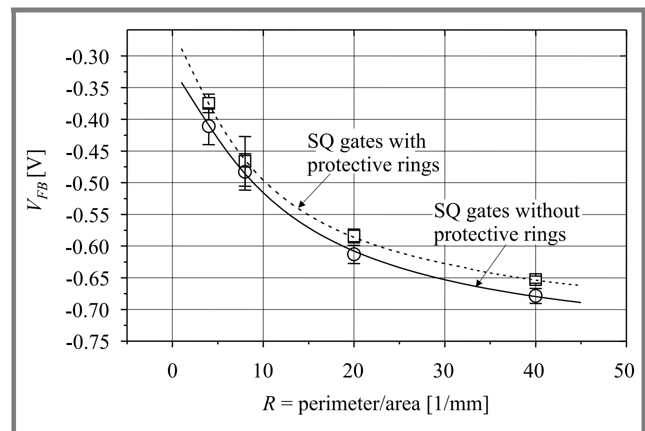

Fig. 10. The V_{FB} versus *R* measurement results obtained for SQ gate structures with and without the protective aluminum rings (open squares and open circles). Curves calculated using Eq. 10) are fit to measurement results for both types of structures. The upper curve (for SQ gates with protective rings) is calculated using $V_{FB_0} = -0.259$ V, $\Delta V = -0.119$ V and $L = 0.249$ mm in Eq. (10). The lower curve (for SQ gates without protective rings) is calculated using $V_{FB_0} = -0.319$ V, $\Delta V = -0.115$ V, and $L = 0.197$ mm in Eq. (10).

of this comparison is shown in Fig. 10. Similarly as in the case of capacitors with different aluminum gate thickness (see Fig. 9), a considerable shift is observed between the $V_{FB}(R)$ characteristics of structures with and without the protective aluminum rings.

5. Conclusions

The lateral distribution of local ECPD values in the plane of MOS structure's gate was studied for the first time. Photoelectric and electrical measurement methods were used in this investigation. It was found that ϕ_{MS} has a characteristic distribution over the gate area, with local ϕ_{MS} values being

highest in the middle of the gate, lower at gate edges, and lowest at gate corners. To study these ECPD distributions, the photoelectric ϕ_{MS} measurement method was modified to allow determination of local ECPD values over dimensions that are small in comparison with the dimensions of the MOS structure. The lateral distributions of ECPD are attributed to lateral distributions of mechanical stress under the gate of a MOS structure. A simple model has been proposed of the distribution of local ϕ_{MS} values over the gate area. The $\phi_{MS}(x, y)$ distributions calculated using the model remain in agreement with the ones determined by the photoelectric method. The validity of the model is further verified by electrical measurements of the flat-band voltage V_{FB} values of a range of Al-SiO_2-Si capacitors, differing in the ratio R, of the gate perimeter to gate area.

References

[1] C. H. Bjorkman, J. T. Fitch and G. Lucovsky, "Correlation between midgap interface state density and thickness-averaged oxide stress and strain at SiO_2 interfaces formed by thermal oxidation of Si", *Appl. Phys. Lett.*, vol. 56, pp. 1983–1985, 1990.

[2] S. M. Hu, "Stress related problems in silicon technology", *J. Appl. Phys.*, vol. 70, pp. R53–R80, 1991.

[3] H. M. Przewłocki and H. Z. Massoud, "The effects of stress annealing in nitrogen on the effective contact potential difference (ECPD), charges and traps at the Si/SiO_2 interface of MOS devices", *J. Appl. Phys.*, vol. 92, pp. 2198–2201, 2002.

[4] I. De Wolf, H. E. Maes, and S. K. Jones, "Stress measurements in silicon devices through Raman spectroscopy: bridging the gap between theory and experiment", *J. Appl. Phys.*, vol. 79, pp. 7148–7156, 1996.

[5] K. F. Dombrowski, I. De Wolf, and B. Dietrich, "Stress measurements using ultraviolet micro-Raman spectroscopy", *Appl. Phys. Lett.*, vol. 75, pp. 2450–2451, 1999.

[6] H. M. Przewłocki, "Theory and applications of internal photoemussion in the MOS system at low electric fields", *Sol. St. Electron.*, vol. 45, pp. 1241–1250, 2001.

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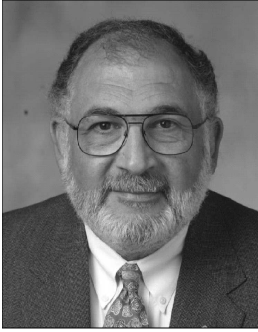

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