Paper

# TSSOI as an efficient tool for diagnostics of SOI technology in Institute of Electron Technology

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**Abstract—This paper reports a test structure for characterization of a new technology combining a standard CMOS process with pixel detector manufacturing technique. These processes are combined on a single thick-film SOI wafer. Preliminary results of the measurements performed on both MOS SOI transistors and dedicated SOI test structures are described in detail.**

***Keywords*— *SOI CMOS technology, pixel detector, test structure.***

## 1. Introduction

In typical silicon-on-insulator (SOI) technologies a thick substrate acts only as a mechanical support for the active silicon film. However in the specific application concerning the SUCIMA (Silicon Ultra Fast Camera for Electron and Gamma Sources in Medical Applications) project [1], the low-doped substrate detects ionized particles. This sensor is monolithically coupled to the readout electronics manufactured in the SOI device layer over the BOX (buried oxide) layer (Fig. 1). This is a solution unique in the world.

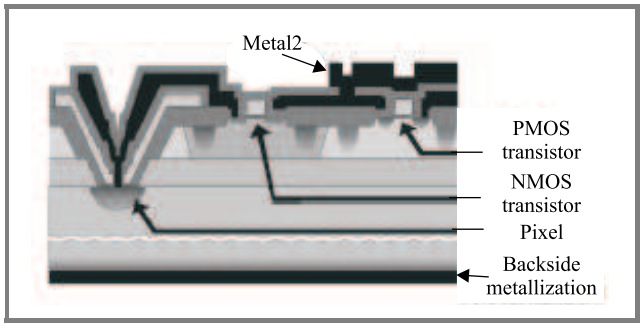


***Fig. 1.*** A cross-section of a SOI pixel sensor.

So far sensors of ionizing radiation have not been fabricated on SOI wafers.

This challenging task requires a new technology of silicon processing at both sides of BOX layer [2, 3]. Interactions between these processes must be carefully taken into account. The following critical requirements for a sequence of individual operations can be mentioned:

- dielectric layers, doping profiles and junctions depths in the silicon body must be optimized for proper operation of read-out electronics;
- $p^+$-n pixel junctions should be shallow, because low-energy beta radiation must be detected;
- high quality of the substrate silicon, i.e. minority carrier life-time on the order of milliseconds, must not be degraded;
- metallization paths between pixel junctions (in deep cavities) and read-out electronics must be reliable.

A TSSOI test structure has been prepared and fabricated for development and characterization of the new technology, as well as for validation of the design. In this paper the individual elements implemented in the TSSOI structure will be described. Preliminary results of measurements of the test elements will be discussed.

## 2. Test structure specification

The TSSOI structure consists of two parts, namely a process-characterization substructure and a functional substructure. The process-characterization substructure of the TSSOI chip contains standard devices like resistors, capacitors, diodes, transistors and chains of contacts. Moreover, several special devices have been implemented. These are MOSFET arrays for threshold voltage variation measurements, and devices for the investigation of the influence of body contact configuration (layout) on the quality of the bias applied to the body of SOI MOSFETs. The functional substructure of the TSSOI structure contains sets of dedicated MOS transistors and numerous special devices. These are current mirrors dedicated to the mismatch measurements, devices dedicated to the capacitor mismatch measurements, specialized amplifying stages and read-out matrices. The two substructures of the TSSOI chip mentioned above are described in the next section.

### *2.1. Test elements for process characterization*

The process-characterization substructure of the TSSOI chip was developed for the following purposes:

– extraction of parameters of SOI MOSFETs and other device models for SPICE-type simulator;

– characterization of SOI CMOS process;

– monitoring of quality and reliability of Metal1 and Metal2 connecting paths.

This substructure covers an area of $6.5 \times 4.0$ mm$^2$. It consists of $500 \times 800$ $\mu$m$^2$ modules, arranged in 5 rows and 13 columns. A $2 \times 4$ probe pad array is used throughout the chip for the purpose of automatic and/or manual testing. The size of several test modules exceeds the standard area of $500 \times 800$ $\mu$m$^2$. There are 46 probe pad arrays (i.e., 46 test modules) in the process-characterization vehicle.
The process-characterization substructure contains transistors with very long, very wide and standard-size channels, sets of diffused p$^+$-n junctions, poly-Si and p well resistors, capacitors with different area/perimeter ratios and different dielectric layers. A more detailed description of these modules is presented below.

#### 2.1.1. Standard MOSFET arrays

These modules are illustrated in Fig. 2. There are two arrays of the so-called medium-size n- and p-channel MOSFETs. There are also another two arrays containing standard-size n- and p-channel devices, as well as devices with dimensions more critical from the point of view of the Institute of Electron Technology (IET) line.
The first set of wide-enough and long-enough transistors is used to extract the parameters of the DC models of standard wide- and long-channel transistors (threshold voltage VTO, substrate doping concentration NSUB, body factor GAMMA, Fermi voltage PHI) [4]. This set may also be used for the estimation of the variations of device dimensions *LD* (total channel shortening) and *DW* (channel narrowing) due to the limitations of the fabrication process (e.g., lithography). Standard DC parameters are extracted from transistor *I-V* characteristics, whereas *LD* and *DW* parameters are extracted through a comparison of *I-V* data obtained from devices with different dimensions.
Standard-size devices found in the second array are used for the extraction of DC model parameters of shorter transistors that are to be used in read-out electronics of the pixel detector in the SUCIMA project. These parameters include carriers mobility parameters (UO, UEXP, UCRIT), saturation velocity of carriers VMAX and several other parameters describing second-order effects. These parameters are estimated using the *I-V* characteristics of standard-size transistors [4]. The second array contains also devices of critical sizes. Electrical characteristics of these devices are

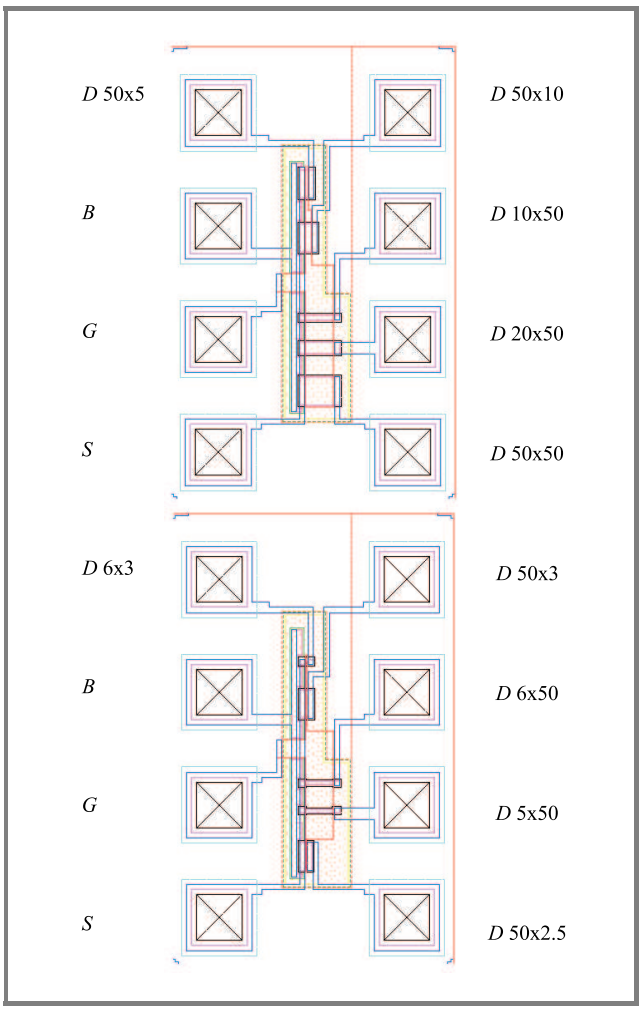


***Fig. 2.*** A layout of n-channel MOSFET arrays used to extract DC model parameters; numbers following the drain pad symbol are channel dimensions (in micrometers).

used mainly for the improvement of devices performance in the presence of strong electric field.

#### 2.1.2. Arrays of very wide and very long MOSFETs

The layout of the array of very wide MOSFETs is presented in Fig. 3. These transistors are used mainly for the extraction of the fringing gate-source (CGSO) and gate-drain (CGDO) capacitances. Moreover, they may be used for the estimation of gate oxide thickness (TOX) and/or gate oxide capacitance per unit area (COX). Also the channel shortening *LD* can be estimated using *C-V* data of these devices. The CGSO and CGDO parameters are extracted from the *C-V* characteristics in accumulation. The procedure of the extraction of the parameters mentioned above is based on a comparison of *C-V* data obtained from devices with different gates widths [5].
Very long MOSFETs have no source and drain areas, therefore they are capacitors. They are used to extract the fringing gate-substrate (CGBO) capacitance. Moreover, they

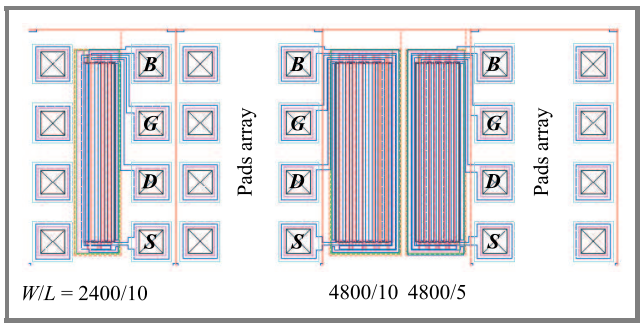


***Fig. 3.*** A layout of wide n-channel MOSFETs array used for extraction of fringing capacitances CGSO, CGDO; the layout of p-channel MOSFETs is analogous.

may be used to estimate the values of TOX and channel narrowing *DW*. The CGBO parameter may be extracted from the *C-V* characteristics in inversion. COX and *DW* parameters may be obtained through a comparison of *C-V* data in accumulation and weak inversion obtained from devices with different dimensions. The extraction procedure is based on a comparison of *C-V* data obtained from devices with different gate lengths.

### 2.1.3. MOSFET arrays for the estimation of threshold voltage variations

The TSSOI structure contains also a set of twelve modules of n- and p-channel MOSFETs for the estimation of the threshold voltage mismatch. It is important to keep the value of this mismatch low, particularly for analog applications of MOS transistors. Each of these modules

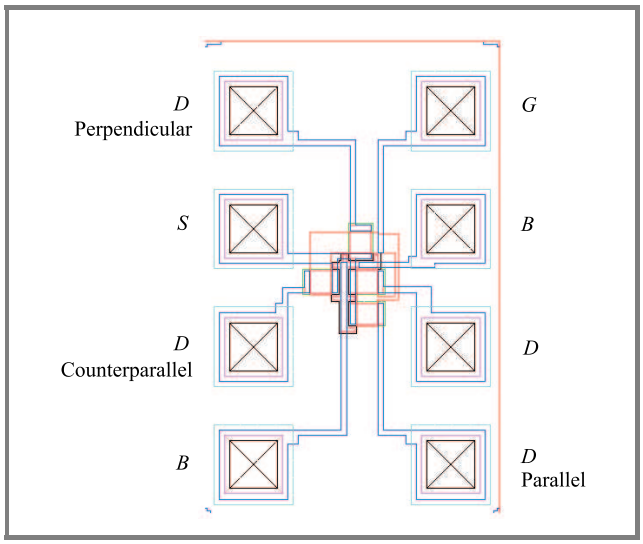


***Fig. 4.*** The layout of one cell of p-channel MOSFETs for estimation of threshold voltage mismatch and its dependence on gate area.

contains four transistors of the same size placed very close to one another and arranged in parallel, counterparallel and perpendicular pairs (Fig. 4).

### 2.1.4. Cells for the estimation of the quality of the bias applied to the body of a SOI MOSFET

In the case of partially-depleted and thick-film SOI MOSFETs parasitic effects like "kink-effect" may be avoided if the silicon body is not floating. This solution requires an additional body contact. It may be expected that the position of this contact relative to the active part of the body may be relevant for MOSFET operation. This may be crucial particularly in the case of analog applications.

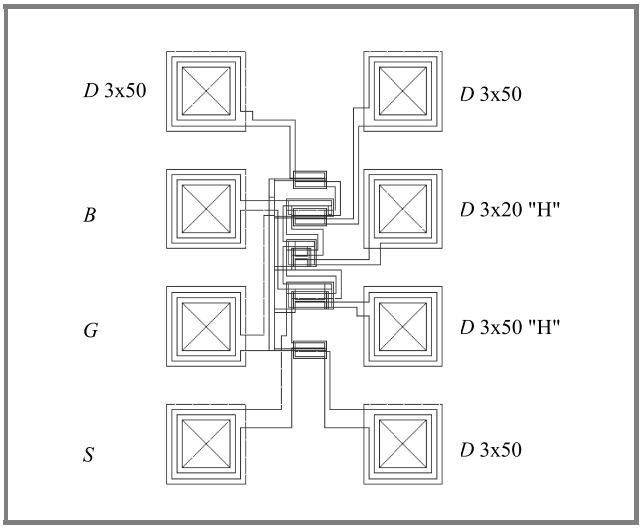


***Fig. 5.*** The layout of one cell of p-channel MOSFETs for the optimization of body bias.

In order to investigate this problem two dedicated modules are included in the TSSOI structure (Fig. 5). They contain 5 n-channel MOSFETs with different p-well (body) contact configurations, as well as 5 p-channel MOSFETs with similar body contact configurations. The gates of two transistors are H-shaped. This will help to estimate the influence of parasitic edge transistors on the device characteristics.

### 2.1.5. Resistor modules for the extraction of the parameters of resistive paths

The TSSOI structure includes three modules containing sets of $n^+$-diffused, $p^+$-diffused and p-well resistors. These modules enable the parameters of resistive paths to be extracted, such as sheet resistance $R_s$, contact resistance $R_c$ and width narrowing *DW*. These parameters can be extracted through a comparison of the resistance of resistors with different dimensions.

### 2.1.6. Diode modules for the extraction of p-n junction capacitance and leakage current parameters

Junctions p-n are extremely relevant for the operation of CMOS circuits. They strongly influence MOSFET operation in weak-inversion, as well as small-signal and transient operation. Thus the extraction of leakage currents

and capacitances of p-n junctions is important. The TSSOI structure contains three modules consisting of square and rectangle p well/n substrate, $n^+$/p-well and $p^+$/n-substrate diodes. The layout of the modules is illustrated in Fig. 6.

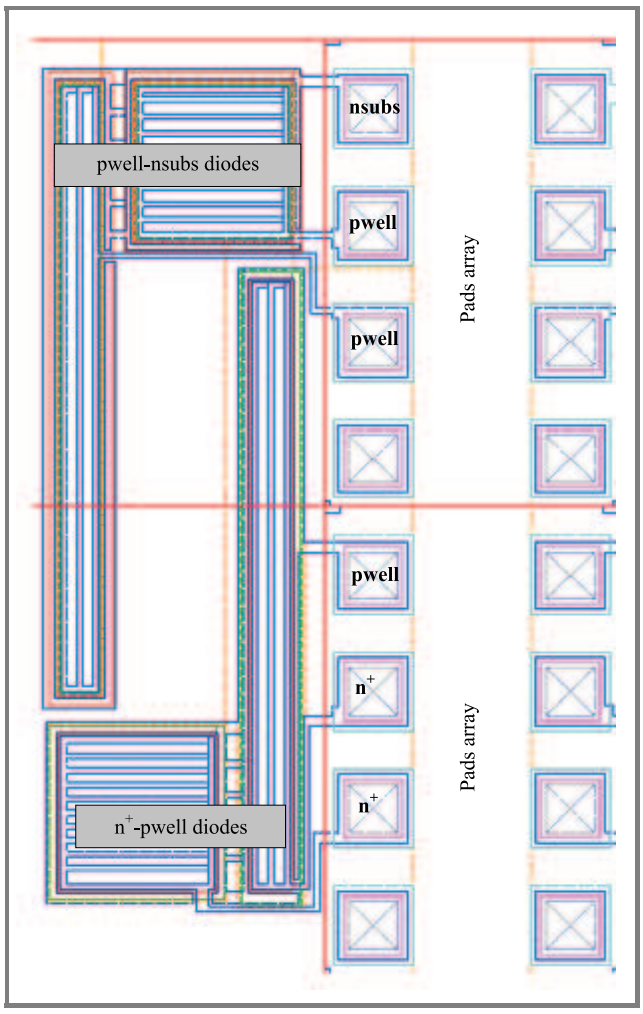


***Fig. 6.*** A layout of modules containing different diodes with two area/perimeter ratios ($W \times L = 260 \times 260$, $65 \times 1040$ $\mu m^2$); they may be used to extract p-n junction capacitances and the volume and surface components of junction leakage.

A comparison of *I-V* and/or *C-V* characteristics of diodes with different dimension allows bulk and edge components of the considered parameter to be extracted. This may be very useful for the characterization and improvement of technology. It is also necessary for the proper extraction of p-n junction capacitance parameters for the SPICE simulator (CJ, MJ, PB, CJSW, MJSW).

### 2.1.7. Capacitor modules for the extraction of interlayer capacitances

The TSSOI structure contains a set of modules for the characterization of dielectric layers. The following capacitors (layout is the same as in the case of p-n junctions – see Fig. 6) are included in the structure:

- poly-Si/FOX/n-substrate, poly-Si/FOX/p-well,
- poly-Si/TOX/n-substrate, poly-Si/TOX/p-well,
- Metal1/FOX/n-substrate, Metal1/FOX/p-well,
- Metal1/DOX/poly-Si, Metal1/DOX/n-substrate,
- Metal2/DOX/Metal1.

where: TOX – thin (gate) oxide, FOX – field oxide, DOX – deposited (passivation) oxide.

The comparison of *C-V* data for capacitors of different dimensions allows vertical and lateral components of capacitances to be extracted. This may be important for the estimation of dielectric layer quality.

### 2.1.8. Modules for monitoring reliability of Metal1 and Metal2 conducting lines

The TSSOI structure contains a set of modules for monitoring of levels 1 and 2 (Metal1 and Metal2, respectively) of conducting metal lines, as well as vias between them. These modules consist of the following structures:

- a series of crossovers of Metal1 strip on poly-Si strips,
- a series of crossovers of Metal2 strip on Metal1and poly-Si strips,
- a series of double crossovers of Metal2 strip on Metal1 and poly-Si strip pairs drawn in accordance or violation of the design rules,
- a series of crossovers of Metal2 on Metal1 and poly-Si strip sandwich,
- a chain of VIA contact windows,
- chains of Metal1/$p^+$ and Metal1/$n^+$ contact windows,
- chains of Metal1/poly-Si($p^+$) and Metal1/poly-Si($n^+$) contact windows.

### 2.1.9. Modules for characterization of pixel p-n junctions and monitoring of contact reliability

The TSSOI structure contains modules for characterization of detector p-n junctions and for monitoring the reliability of contacts to these junctions. These modules are very important, when p-n junctions are to be formed in high-resistivity substrates below buried oxide layer, in deep cavities (see Fig. 1). Pixel properties and reliability of the connections are extremely important for detector operation. The structure contains the following modules for monitoring of contact reliability:

- a chain of contact windows for pixel detectors,
- a Metal1 serpentine over extremely deep detector contact windows.

These test elements as well as the elements mentioned above are very important as a tool for the diagnostics of conducting path reliability in the IET laboratory.
The structure contains also a module for the extraction of pixel p-n junction parameters in deep cavities. The module consists of 2 detector diodes of different area/perimeter ratios. A comparison of the *I-V* characteristics of these diodes is necessary for the extraction of lateral and vertical components of p-n junction current and thus for pixel characterization.

### *2.2. Test elements for verification of front-end electronics operation (functional substructure)*

The functional test structure contains numerous elements. The main part consists of functional blocks that are described below. Among other devices they include several modules with individual MOSFETs (also with different body contact layout).

#### 2.2.1. Blocks for mismatch measurements

The test structure includes two modules that are dedicated to the measurements of mismatch in the devices fabricated using SOI technology. The first one is a large set of PMOS and NMOS current mirrors (Fig. 7). In this unit some of the current mirrors have the transistors with the dimensions nominally exactly the same. As the consequence, the threshold voltage mismatch of the transistors can be evaluated by measuring the output currents $I_{out}$ for a fixed value of the injected current $I_{inj}$. Additionally, this unit makes it possible to compare the output currents from transistors with the same $W/L$ ratio but different dimensions and to observe the short channel effect in current sources.

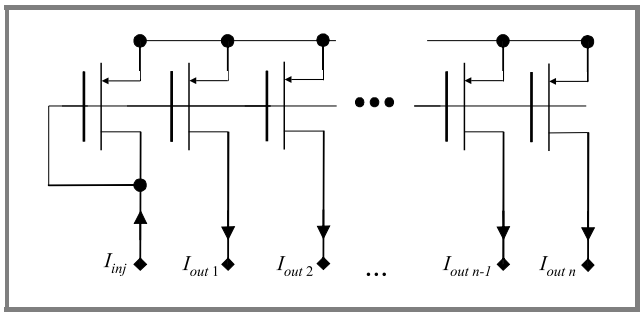


***Fig. 7.*** Threshold voltage mismatch measurement in current mirrors unit.

The next module is dedicated to the measurements of capacitance mismatch. The designed test circuit allowing capacitance ratios to be measured consists of a couple of two capacitors ($C_X$ and $C_Y$) that are nominally identical and a source follower.
The principle of capacitance mismatch measurements using this circuit is presented in Fig. 8. First the output signal is measured at the $X$ pin connected to the signal generator and the $Y$ pin grounded. The obtained value $S_X$ is proportional to $C_X/(C_X+C_Y+C_p)$, where $C_p$ is a parasitic capacitance. Next the same procedure is performed while the $Y$ pin is connected to the signal generator and the $X$ pin is grounded. This time the output signal value $S_Y$ is proportional to $C_Y/(C_X+C_Y+C_p)$. Hence the ratio of $S_X$ over $S_Y$ signals is equal to the ratio of $C_X$ over $C_Y$ capacitances and does not depend on the input parasitic capacitance of the source follower.

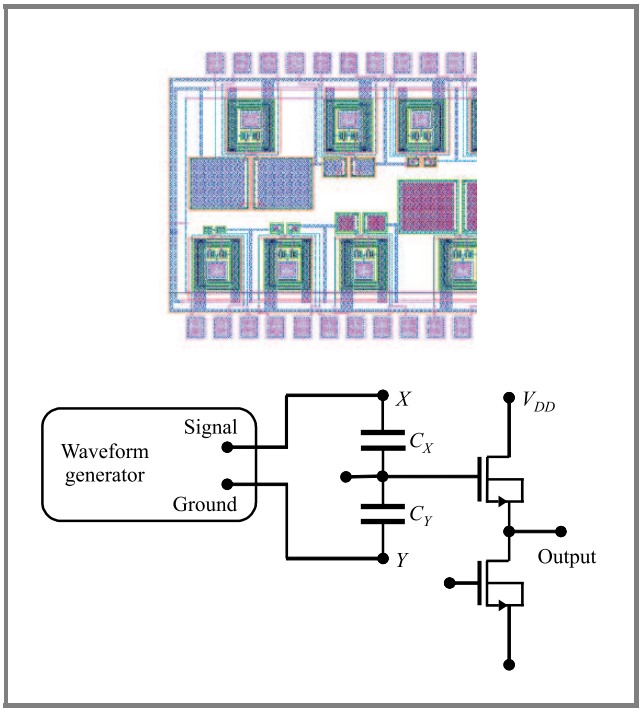


***Fig. 8.*** Module and principle of capacitance mismatch measurements.

The next module of the test structure – two matrices of precise ratio capacitors – may be measured in a similar way. Apart from capacitance mismatch measurements, two different kinds of capacitors (Metal1-Metal2 and polySi-Metal1) may be compared using this module.

#### 2.2.2. Blocks of amplifying stages

The block includes three simple amplifying stages: two common source OS stages and one cascode OS-OG stage. The layouts and schematics of those circuits are presented in Fig. 9. This part of the test chip not only allows the behavior of the new technology to be observed in an analog application, but also makes it possible to compare the measurement results with simulations.

#### 2.2.3. Blocks with digital cells

Several basic digital gates and data flip-flops with asynchronous reset are implemented in the test structure (Fig. 10). Such important parameters, as rising and falling

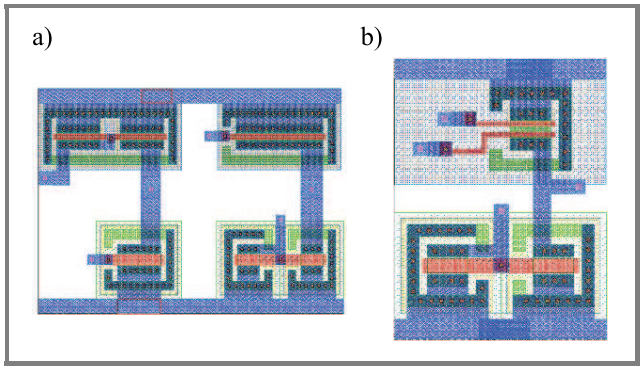


***Fig. 9.*** Schematic layouts of amplifying stages: (a) OS; (b) OS-OG.

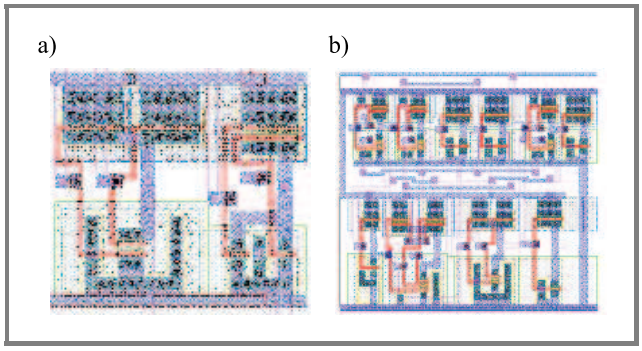


***Fig. 10.*** Layouts of digital cells: (a) NAND, NOR gates; (b) data flip-flop cell.

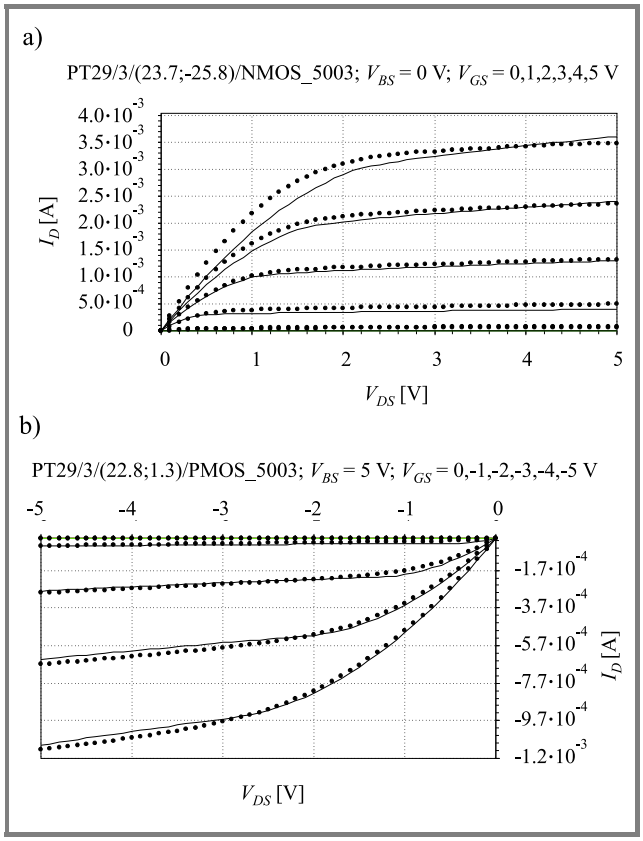


***Fig. 11.*** Measured *I-V* characteristics of (a) n- and (b) p-channel MOSFETs (dots) and those simulated using SPICE LEVEL = 2 MOSFET model after parameters extraction (solid line).

times, propagation times, noise margins and other ones may be measured using these cells and compared with the simulation results. These measurements will also enable the maximum readout speed to be estimated for the readout electronics and the optimum bias voltage to be found for the digital circuits used in the SUCIMA project.

## 3. Measurements

In this section selected results of the measurements of individual transistors and functional blocks are shown.
The *I-V* characteristics of MOSFETs have been measured using both manual and semi-automatic probe-stations [6] combined with the METRICS software. Next the measured *I-V* characteristics were used to extract SPICE model parameters [4]. The results are shown in Fig. 11. Moreover, measurements of the functional blocks have been carried out. Certain results are shown in Figs. 12 and 13. These preliminary results suggest that the functional blocks work

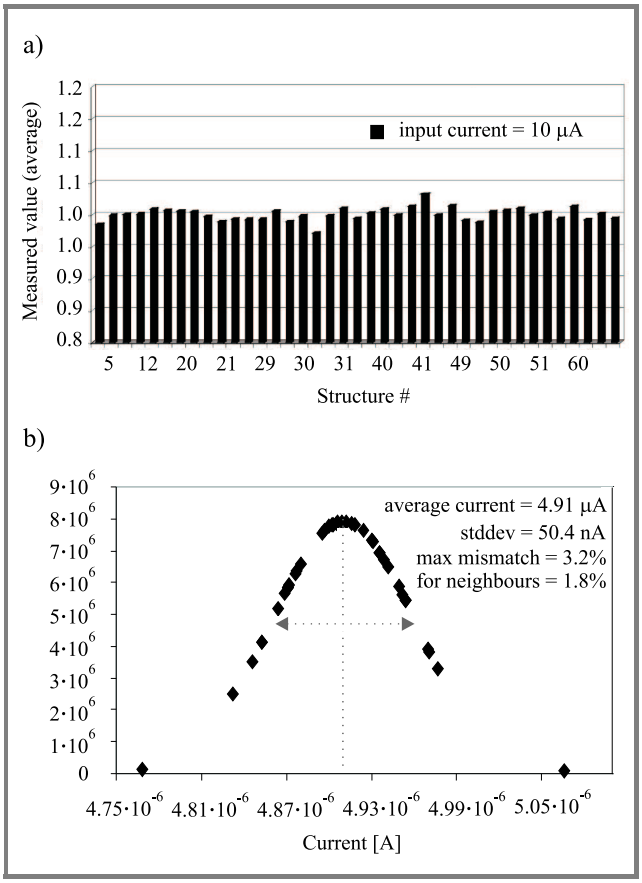


***Fig. 12.*** Matching properties of the NMOS transistor with the dimensions of 50 $\mu$m/10 $\mu$m: (a) normalized output current at different wafer locations; (b) normal fit of measured current values – the current deviations between different structures on the same wafer are ca. 1% of the average value.

properly. The uniformity of the electrical parameters within wafers is satisfactory and proves that the technology under test is mature.

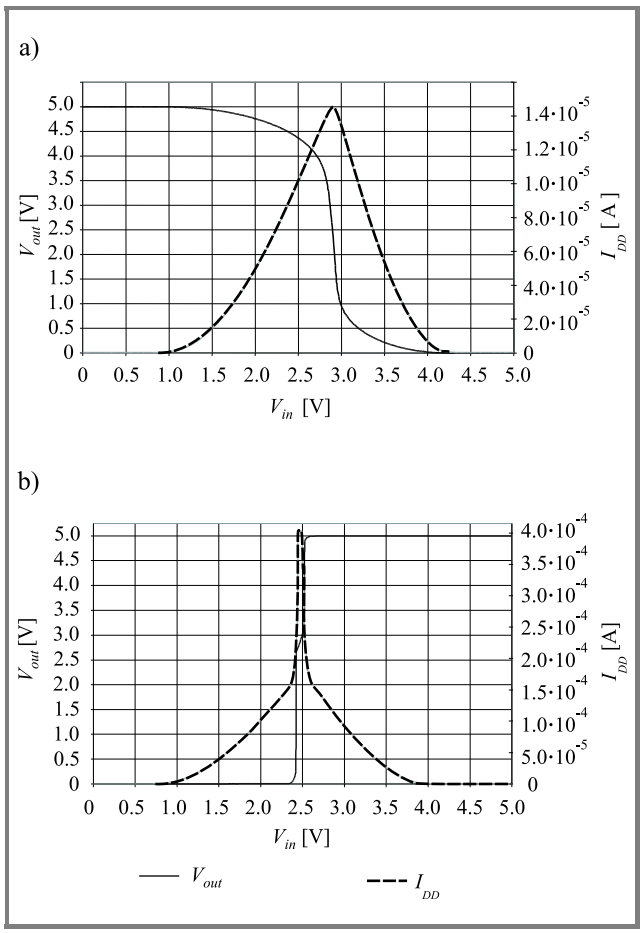


***Fig. 13.*** Transfer characteristics and supply currents of different digital cells: inverter (a); digital buffer (b).

## 4. Conclusion

The TSSOI test structure is a versatile tool for future optimization of SOI-based pixel detectors. The proposed set of devices provides a basis for detailed studies of both process sequence and design.

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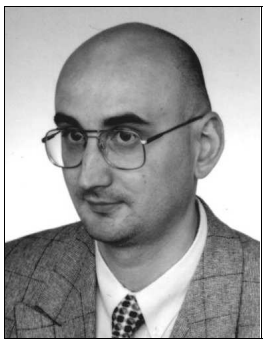

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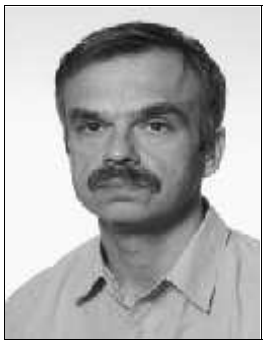

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