

Modeling, Simulation and Calibration of Silicon Wet Etching

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Abstract— The methods of parameter optimization in Etch3D™ simulator and the results of the comparison of simulations of silicon etching in KOH with experiments are presented. The aim of this study was to calibrate the tool to a set of process conditions that is offered by Institute of Electron Technology (ITE). The Taguchi approach was used to analyze the influence of every remove probability function (RPF) parameter on one or more output parameters. This allowed tuning the results of simulation to the results of real etching performed in ITE.

Keywords— anisotropic wet etching, KOH, silicon technology.

1. Introduction

Anisotropic wet chemical etching of single crystalline silicon (Si) in KOH/TMAH is the standard process technology to fabricate three-dimensional structures for microelectromechanical devices. However, the etch process is depends on the crystal orientation, etching temperature, etchant concentration, and the length of time the wafer remains in the etchant [1]. The final structure determined by Si anisotropic etching is difficult to predict precisely. Etch3D™ simulator addresses this challenge by wet etching simulation [2]. Performing simulations with Etch3D™ prior to going to the fab helps users reduce the time-consuming and expensive process of iteratively refining the masks and processing parameters.

The Etch3D™ is a silicon wet etching simulator based on a first-principles, atomistic simulation method [3]. The wafer is represented by a matrix of “atoms” arranged with the same geometry and connectivity as the 18-atom cells in crystalline silicon. The simulator uses a “voxel” (volumetric pixel) based process emulation tool that takes 2D masks and a description of the fabrication process, to build highly detailed, realistic-looking virtual prototypes. The cell size that is used in an Etch3D™ simulation is determined from the resolution, in voxels per micron. Scale invariance means that the simulations can be run with the cell arbitrarily larger size than the size of the actual silicon crystal cells (which is 0.543 nm) and produce the same macroscopic behavior, at least up to the size required to resolve macroscopic features of the wafer surface.

After initialization, which usually involves applying a mask to one or both sides of the wafer, the simulation goes through a series of time steps (also called frames). During each frame, the simulator computes the removal probability for each atom on the wafer surface that is exposed to the etchant (i.e., not masked). The simulator uses a Monte

Carlo approach – it compares the removal probability to a random number between 0 and 1. Using this approach, it is possible to duplicate certain microscopic topographies that occur in actual anisotropic etching [2].

However, the primary purpose of Etch3D™ is to model the macroscopic evolution of the wafer surface geometry. The atomistic method, as currently implemented, does not explicitly account for etchant concentration. Rather, it is assumed that the etch rates of all crystal planes vary linearly within a range of concentration. Etch3D™ includes several sets of recommended parameter values for specific concentration ranges of KOH and TMAH. Users can further tune these parameter values for a specific concentration level.

The remove probability function (RPF) defines the probability p of removing an atom with n_1 first neighbors (in the crystal lattice) and n_2 second neighbors by the function

$$p(n_1, n_2) = p_0(n_1) \frac{1 + e^{\varepsilon(-n_2^0)/k_B T}}{1 + e^{\varepsilon(n_2 - n_2^0)/k_B T}}, \quad (1)$$

where: ε is the average energy of interaction between second neighbors, and where for $n_1 = 2, 3$ the constants $p_0(n_1)$, and $n_2^0 = n_2^0(n_1)$ are parameterized as follows:

$$p_0(2) = \frac{a_{21}(1 + e^{-a_{22}a_{23}})}{1 + e^{a_{22}(c - a_{23})}}, \quad (2)$$

$$n_2^0(2) = b_{21} - b_{22}c, \quad (3)$$

$$p_0(3) = \frac{1.0 - a_{31}(1 + e^{-a_{32}a_{33}})}{1 + e^{a_{32}(c - a_{33})}}, \quad (4)$$

$$n_2^0(3) = b_{31} - b_{32}c. \quad (5)$$

These values were obtained by a curve-fitting approach by Coventor, but these parameters require further adjustment in order to match the user-measured data.

2. Fabrication and Measurement of Test Structures

A dedicated mask for test etching was designed and manufactured (Fig. 1). The mask contains several structures, designed so as to represent a variety of geometries that allow exposition of multiple crystallographic planes, enabling the analysis of crystallographic planes of etched silicon. N-type (resistivity 2 – 4 Ω -cm) single crystal $\langle 100 \rangle$ silicon substrates with 4-inch diameter were used for

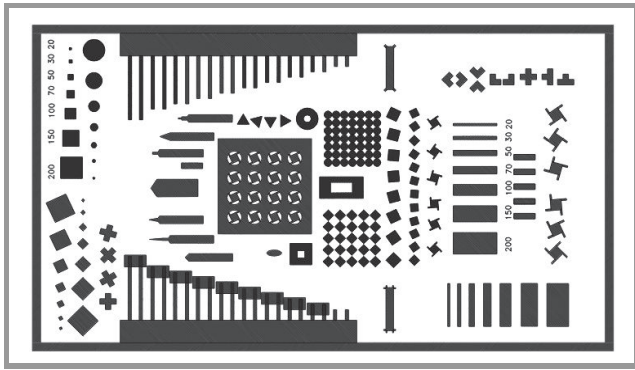


Fig. 1. Test structure for KOH etching.

anisotropic etching. Initially, a 50-nm silicon dioxide layer was grown thermally. Thereafter a 100 nm thick silicon nitride layer was deposited and photolithographically patterned. Before insertion of the wafers in etching solution, native oxide was removed. The wafers were etched in KOH (concentration 30%) at 60°C for 10, 20, 30 and 40 min. Etch depth was measured using a profilometer (typical results are given in Table 1).

Table 1
Etch depth versus time for KOH etching carried out in ITE

Time [min]	Etch depth [μm]
10	3.22
20	7.00
30	10.05
40	13.43

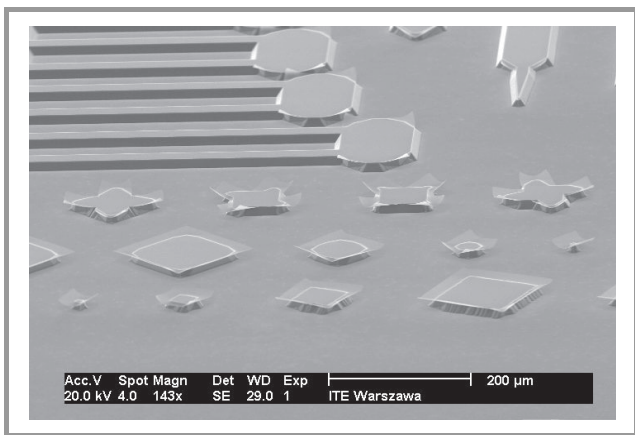


Fig. 2. SEM microphotograph of test structures after 40 min etching in KOH.

The structures were then subjected to scanning electron microscope (SEM) observations. A SEM micrograph of test structures after 40 min etching in KOH is shown in Fig. 2. The etch depth as well as characterized shapes of etched structures were used as an input to Etch3D™.

3. Simulation and Calibration of Etch3D™

Due to the high number of test structures, simulating the whole mask would take a very long time. In order to reduce the overall simulation time, only a subset of the structures was selected for initial simulations. The simulation results were then compared in detail with the experimentally fabricated structures, making use of SEM techniques. The Etch3D™ simulation software gives the user access to 10 so-called RPF parameters. It turned out that tuning all parameters in order to find the optimal values, for different etching times, concentrations and temperatures and using different test structures would result in a huge amount of data to be processed.

As a first step, in order to reduce the amount of data, a set of four crosses, rotated at different angles, was selected for tuning the RPF parameters (Fig. 3). This structure offers several interesting etching angles and is also quite simple, allowing time-effective simulations. This decision allowed the number of voxels, and thus the resolution of simulation, to be increased, which results in an improved quality of the simulation.

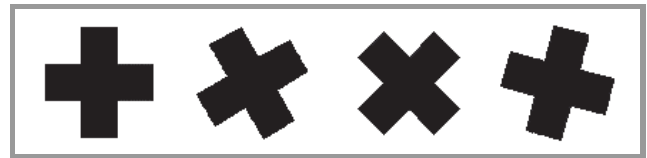


Fig. 3. Layout of the selected 4-cross test structure.

We have selected separate sets of input and output parameters for the experiment in order to allow comparison not only in quality but also quantity:

- input parameters: 10 RPF parameters, concentration and temperature of bath;
- output parameters: 5 selected geometry details revealing selected crystallographic planes (Fig. 4).

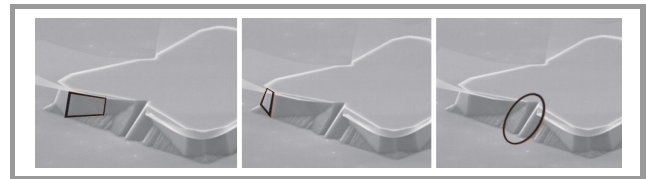


Fig. 4. Example of geometry details defined as output parameters.

The first set of simulations resulted in an enormous amount of data to analyze mainly due to the fact that:

- the 10 RPF input parameters had to be modified for each process setup;
- each input parameter affected the results in a different way;
- one input parameter influenced more than one output parameters.

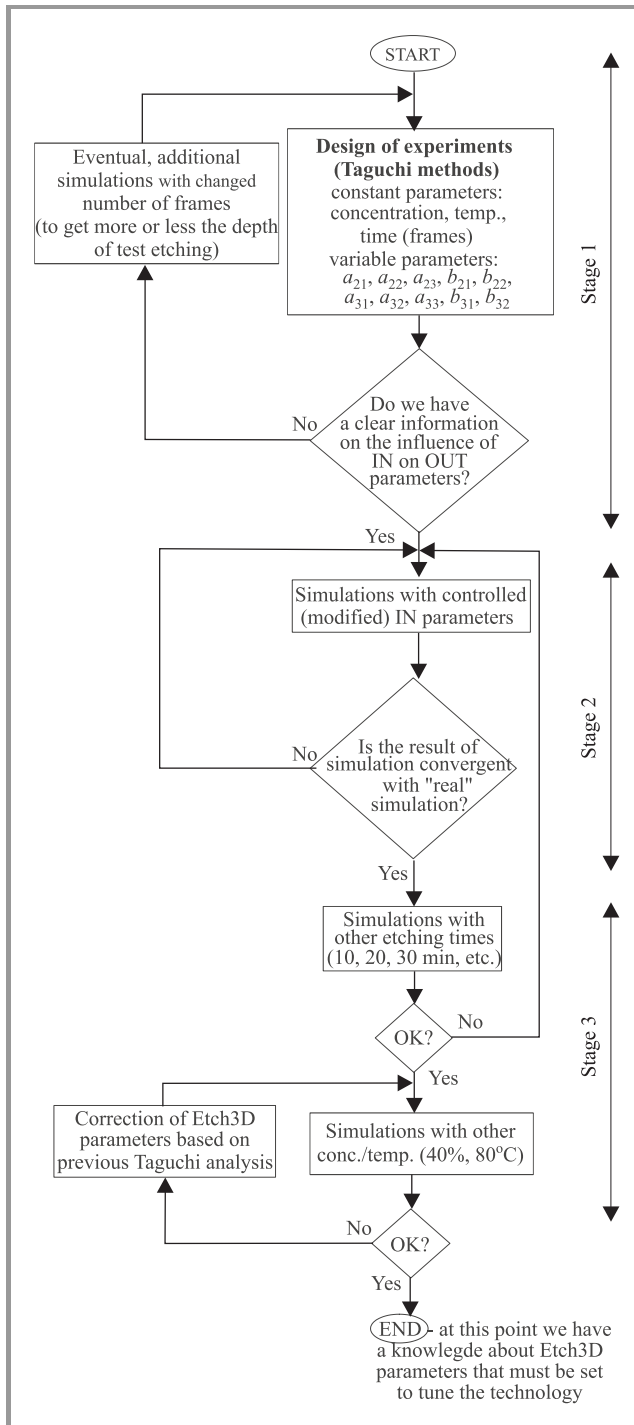


Fig. 5. Algorithm of tuning Etch3D™ RPF parameters to existing KOH/TMAH technology.

Due to a high number of possible parameter combinations, a reliable statistical method of planning further simulations was necessary. The Taguchi approach was proposed to design a sequence of simulations and analyze results. The Taguchi method [4], [5] is an approach to designing experiments using statistical analysis. It allows for the process and product design to be improved through the identification of controllable factors and their settings, minimizing the variation of a product around a defined tar-

get response. The Taguchi approach in Etch3D™ was used to analyze the influence of every RPF parameter on one or more output parameters. This allowed tuning the results of the simulation to those of real etching performed in ITE.

To solve this calibration problem, a simulation optimization procedure was developed (Fig. 5). The whole tuning sequence was divided into three stages.

In stage 1 the Taguchi table was created and a set of simulations was performed. The purpose of this stage is to get the information on the influence of input parameters on the results of simulation (Fig. 6).

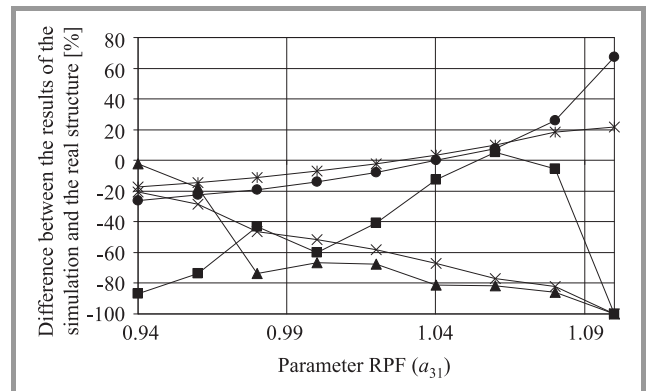


Fig. 6. Graphs presenting dependence of various geometrical details on the RPF parameter (a_{31}).

In stage 2, based on the information from stage 1, a new set of simulations was designed. The purpose of this stage was to perform more detailed simulations with modified input parameters (however, concentration, temperature and number of frames remained constant).

At this stage the results of the simulations are tuned to the results of etched test structures. The results of the simulations of test structures with tuned parameters of Etch3D™ are presented in Figs. 7–11.

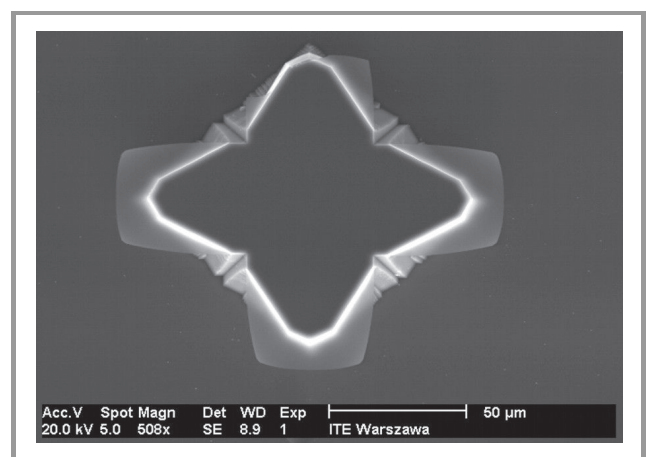


Fig. 7. SEM microphotograph of the real structure (top view).

Comparing the results obtained with default and tuned parameters good agreement with the crystallographic planes

of the etched test structures may be noticed (higher-order crystallographic planes marked in Fig. 4). Moreover, the difference in the depths of the simulated and etched groove is below 5%.

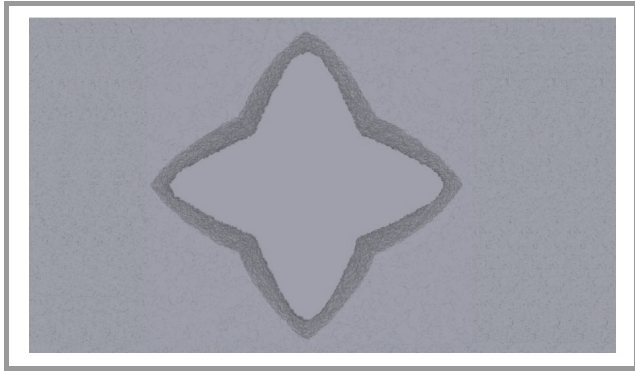


Fig. 8. Results of the simulations using the default a_{ij} , b_{ij} coefficients.

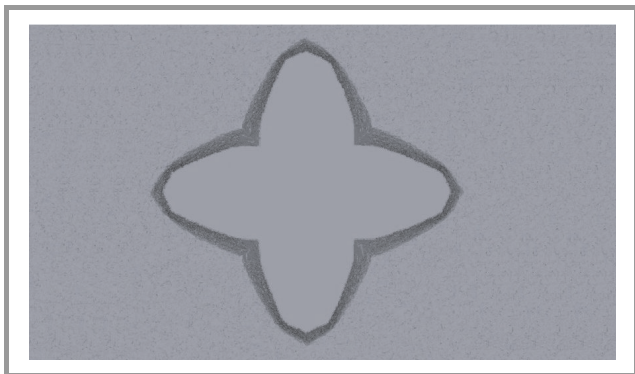


Fig. 9. Results of the simulations – using tuned Etch3D™ RPF parameters.

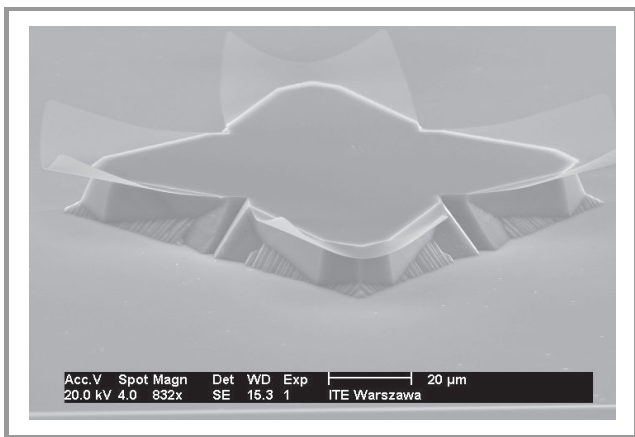


Fig. 10. Main view of the real structure.

It was found that some of the parameters have significant influence on the output parameters (angles, etch depth, etc.). For example, changing the b_{31} parameter results in the greatest increase of the etch depth than any other RPF parameter.

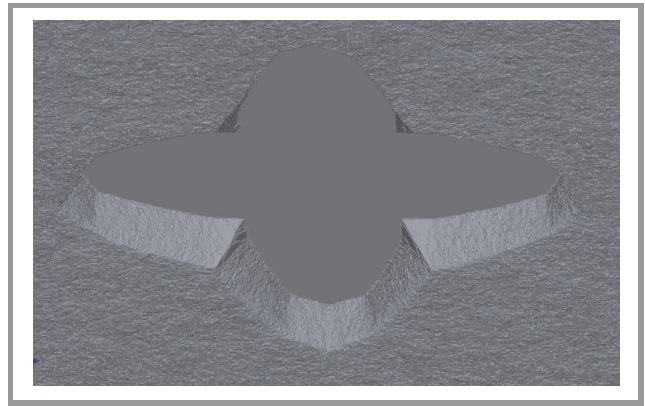


Fig. 11. Main view of the simulated structure with tuned Etch3D™ RPF parameters.

Finally, tuning of only 5 out of 10 parameters was necessary for tuning. In the case of the remaining 5 parameters their default values could be treated as sufficiently accurate.

Table 2
Remove probability function parameters

RPF parameter	Default	Tuned
a_{21}	0.5	0.35
a_{22}	25.0	25.0
a_{23}	0.7	0.7
b_{21}	7.0	7.0
b_{22}	0	1.2
a_{31}	1.0	0.94
a_{32}	7.5	7.5
a_{33}	0.5	0.5
b_{31}	7.3	7.7
b_{32}	0.6	0.1

The values of RPF parameters used for tuned simulations are presented in Table 2.

4. Process Emulation of MEMS and IC structures

The Etch3D™ is intended to be used in conjunction with SEMulator3D™-MEMulator™ [2]. The results of virtual manufacturing of silicon accelerometer using both programs [6] are shown in Fig. 12.

MEMulator™ is useful for preprocessing or postprocessing a wafer, and for visualizing the results of an Etch3D™ simulation. Preprocessing with MEMulator™ may entail creating a wafer, then using one or more of the available etch steps in MEMulator™ to create some initial features on the wafer, or using one or more of the available deposition steps to create etch stops. The material that is deposited on the wafer with MEMulator™ may be etched

in Etch3D™, but this would be unusual because the actual process steps (other than wafer bonding) do not produce crystalline silicon. Postprocessing with MEMulator™, on

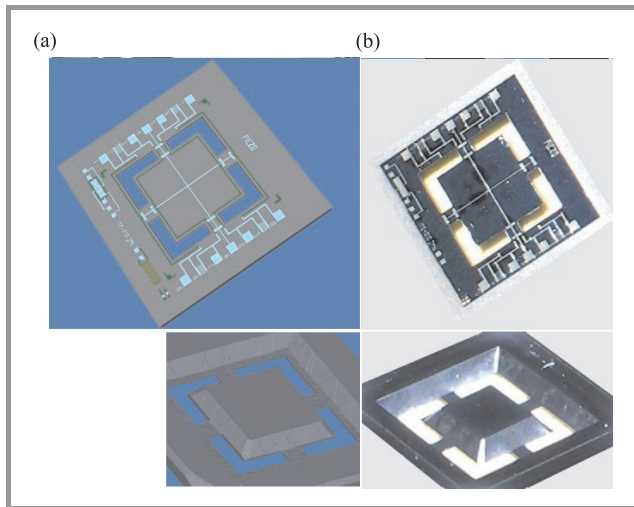


Fig. 12. Emulation of fabrication steps of piezoresistive accelerometer. Results of virtual manufacturing (a) and real structure (b).

the other hand, may entail an arbitrary series of deposition and etch steps on top of the wet-etched surface that was produced by Etch3D™.

5. Conclusions

The presented modeling, simulation and real etching results demonstrate successful calibration of wet silicon etching processes. Using the Taguchi method it is possible to tune the etch process to the fab reality and a given technology specification.

Tuned software like Etch3D™ is a perfect tool to optimize the wet etching of silicon processes and use it for virtual, rapid prototyping. The precise 3D model generated using described approach may be further analyzed using finite element method.

Virtual prototyping is a powerful tool that may be used to reduce the time consuming and expensive process of refining masks and many processing parameters. This is of great importance since TTM (time to market) is a key parameter of the MEMS product development process.

References

- [1] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgartel, "Anisotropic etching of crystalline silicon in alkaline solutions", *J. Electrochem. Soc.*, vol. 137, no. 11, pp. 3612–3625, 1990.
- [2] "Etch3D User Guide Version 2006.5", Sept. 2006 [Online]. Available: <http://www.coventor.com>
- [3] M. A. Gosalvez, R. M. Nieminen, P. Kilpinen, E. Haimi, and V. Lindroos, "Atomistic wet chemical etching of crystalline silicon: atomistic Monte-Carlo simulations and experiments", *Appl. Surf. Sci.*, vol. 178, pp. 7–26, 2001.
- [4] P. J. Ross, *Taguchi Techniques for Quality Engineering*. New York: McGraw-Hill, 1988.
- [5] G. Z. Yin and D. W. Jillie, "Orthogonal design for process optimization and its application in plasma-etching", *Solid-State Technol.*, vol. 30, no. 5, pp. 127–132, 1987.
- [6] P. Janus, T. Bieniek, A. Kociubiński, P. Grabiec, and G. Schröpfer, "Modeling and co-simulation of integrated micro- and nanosystems", in *14th Int. Conf. MIXDES 2007*, Ciechocinek, Poland, 2007.



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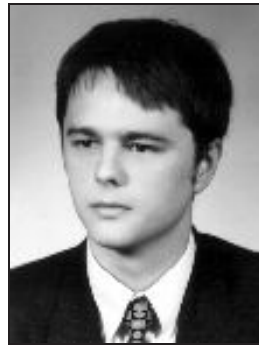
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