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Rare Earth Silicate Formation: A Route Towards High-k for the 22 nm Node and Beyond

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Abstract— Over the last decade there has been a significant amount of research dedicated to finding a suitable high-*k*/metal gate stack to replace conventional SiON/poly-Si electrodes. Materials innovations and dedicated engineering work has enabled the transition from research lab to 300 mm production a reality, thereby making high-*k*/metal gate technology a pathway for continued transistor scaling. In this paper, we will present current status and trends in rare earth-based materials innovations; in particular Gd-based, for the high-*k*/metal gate technology in the 22 nm node. Key issues and challenges for the 22 nm node and beyond are also highlighted.

Keywords— gadolinium silicate, interfacial layer, lanthanides, rare earth oxides.

1. Introduction

A 32 nm process technology, including a high-k dielectric and metal-gate has been announced [1]–[5]. The equivalent oxide thickness (EOT) of the high-k dielectric has been reduced from 1.0 nm on 45 nm node to 0.9 nm [1] on the 32 nm process, while gate length has been reduced to 30 nm. Transistor gate pitch continues to scale $0.7\times$ every two years – with 32 nm providing the tightest gate pitch in the industry. The key industrial players are Intel Corporation, IBM alliance (with AMD, Chartered, Freescale, Infineon, Samsung, ST and Toshiba), TSMC, NEC, Panasonic in collaboration with Renesas. Different integration strategies have been employed by various parties involved, namely a replacement gate [6], [7] or a conventional gate-first approach [8], [9]. In the latter, the gate stack is formed before the source and drain, as in a conventional complementary metal oxide semiconductor (CMOS) process, while the former is a gate-last approach. Moving beyond the planar transistor, IBM, AMD, Freescale and Toshiba have recently presented a fin field effect transistor (FinFET) with high-k and metal gates for the 32 nm node and beyond [3].

A static random access memory (SRAM) cell was devised at areas down to 0.128 μm^2. Using 22 nm design rules, the cell was fabricated using a CMOS process flow and e-beam lithography. In the cell, fin pitch was 80 nm, gate pitch 110 nm and physical gate length 30 nm. To enable high-k and metal gates, chemical vapour deposition (CVD)-based HfO_2, physical vapour deposition (PVD) TiN and polysilicon were deposited on the fin portion of the device. TSMC has also announced a 32 nm process [4], which includes a high-k/metal-gate scheme based on a gate-first technology. A 0.15 μm^2 SRAM cell was developed by using a Hf-based material and 193 nm immersion lithography with a numerical aperture of 1.35. The high-k material has been scaled to 1 nm, at 30 nm physical gate length and 130 nm gate pitch. The team of NEC and Toshiba Corporation has developed a 32 nm process, with a single-exposure lithography technology and a gate-first high-k/metal-gate process [5]. They demonstrated a SRAM cell of 0.124 μm^2 and a gate density of 3650 KGate/mm^2. From the relevant publications and press releases, it is evident that Hf-based dielectrics are retained for the 32 nm node leaving other dielectrics for consideration at further technology nodes. Physical gate length scaling, from 35 nm, in the 45 nm generation, to 30 nm in the 32 nm generation, is enabled by high-k dielectric scaling and shallow junction engineering [10].

Low standby power (LSTP) technology requirements in the near term years according to the International Technology Roadmap for Semiconductors (ITRS) [11] are listed in Table 1. As can be seen, more aggressively scaled EOT is required in order to reach the specification for the 22 nm node. This leads to stringent control of interfacial oxide layer, either by reducing its thickness or by increasing its k-value. A good interface requires either that the oxide is amorphous, or that it is epitaxial and lattice-matched to the underlying silicon [12]. Amorphous oxides represent a low-cost solution; nonetheless, the challenge is to keep these materials amorphous even after post-deposition high temperature processing in order to avoid increased surface roughness and additional leakage due to the formation of grain boundaries, as shown in many investigations [13]–[16]. Another approach is based on the development of epitaxial metal oxides grown directly on silicon surfaces [12]. It is known that for given values of MOS leakage current and insulator thickness, the dielectric constant, k, and the offset value between oxide and silicon energy bands, ΔE, are bound roughly by a hyperbolic relation $k \cdot \Delta E = C_E$, where C_E is a constant. Engstrom *et al.* [17] have suggested that a value of $C_E \approx 70$ eV is necessary for the 22 nm bulk LSTP node, while the corresponding figure for silicon-on-insulator (SOI) technology is in the range of 30–40 eV. Rare earth (RE) oxides offer interesting properties to fulfil such requirements: a high dielectric constant [17], a high band gap and suitable band offsets with respect to Si [18], sufficiently high breakdown strength,

Table 1
Low standby power technology requirements – near term years [11]

Year in production	2008	2009	2010	2011	2012	2013	2014	2015
MPU/ASIC metal $1\frac{1}{2}$ pitch [nm] (contacted)	59	52	45	40	36	32	28	25
Physical length gate for high performance logic [nm]	29	27	24	22	20	18	17	15
Physical gate length for LSTP (Lg)								
Extended planar bulk and DG [nm]	38	32	29	27	22	18	17	15
UTB FD [nm]	*	*	*	*	*	20	18	17
EOT								
Extended planar bulk [nm]	1.6	1.5	1.4	1.3	1.2	1.1	*	*
UTB FD [nm]	*	*	*	*	*	1.2	1.1	1.0
DG [nm]	*	*	*	*	*	*	*	1.1
Maximum gate leakage current density ($J_{g,\text{limit}}$)								
Extended planar bulk [mA/cm^2]	81	94	110	120	140	150	*	*
UTB FD [A/cm^2]	*	*	*	*	*	150	170	180
DG [A/cm^2]	*	*	*	*	*	*	*	190

* delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling.

extremely low leakage current, and well-behaved interface properties. Their key advantages for advanced CMOS are:

- thermal stability;
- a feature to shift the work function of a metal gate towards n-type and thus engineer a transistor threshold voltage [19], [20];
- a reduction of the low-*k* interfacial layer (IL) thickness.

An important consideration in choosing an alternative high-*k* dielectric is its compatibility with Si, and metal silicates have attracted much recent attention [21]–[23]. The presence of silicon leads to improved metal oxide/silicon interface stability and reduced leakage currents. This in turn has generated interest in the deposition of lanthanide silicates, such as Gd-silicate [24], La-silicate [25], Pr-silicate [26], [27]. A silicate formation is known to occur when a rare earth oxide is in contact with a Si-containing dielectric or a silicon substrate in the presence of oxygen [23]. As such, it can be used to consume the typical SiO_2-like interfacial layer between high-*k* and silicon substrate or to enhance its *k*-value. In this paper, we will show that RE silicate formation is one of the possible pathways towards scaling beyond the 22 nm node. In particular, our recent work on optimization of GdSiO-based gate stack is reviewed and results presented on thermal stability and mechanisms of silicate formation.

2. Rare Earth Oxides and Silicates

Rare earth oxides are attractive materials for gate dielectric application, and in particular the lanthanide oxides group (LnO's). Lanthanides refer to a series of 15 elements from La to Lu in the periodic table, which have similar but gradually changing characteristics [28]. The LnO's can have different stoichiometries due to the multiple oxidation states (+2, +3, and +4) of the metals. This leads to oxides with different structural phases including two cubic phases, namely, the calcium fluoride structure for the Ln(IV) only, and the bixbyite structure for Ln(III) [29]. Lanthanide oxides with more than one valence state are not the best choice for CMOS processing because of the coexistence of phases with different oxygen contents and possible transformations between them, or even the occurrence of mixed valence-state structures [30], [31]. A summary of the key properties of RE LnO's is given in Table 2 ([17], [29] and references therein). Those deemed suitable for application are now described.

The RE oxides, such as La_2O_3 [32], [33], Pr_2O_3 [34]–[37], Gd_2O_3 [38], and Nd_2O_3 [39], [40] have been investigated. They are good insulators due to their large band gaps, high dielectric constants (13–16 for Gd_2O_3, 25–30 for La_2O_3 [17], 15–25 for Pr_2O_3 [41]) and good thermodynamic stability on silicon even at high temperatures, i.e., when heated in contact with silicon will not directly react to form silicide, metal, or silicon oxide [42]. Another attractive feature of Pr_2O_3, Gd_2O_3, and Nd_2O_3 is their relatively close lattice match to silicon ($2a_{Si} = 1.090$ nm), which offers the possibility of epitaxial growth, eliminating problems related to grain boundaries in polycrystalline films.

Silicate formation of binary lanthanide oxides in contact with SiO_2 has been the subject of many studies [24], [40], [43]–[46] whereby the SiO_2 IL is consumed during a high temperature step. The process has been demonstrated for La_2O_3 [47], [48] or Gd_2O_3 [49], [50] deposited on SiO_2.

Table 2
Properties of RE Ln_2O_3 oxides [17], [29]

Compound	Structure	a[Å]	c[Å]	Band gap [eV]	Dielectric constant
Er_2O_3	Bixbyite	10.548		5.3, 5	13
La_2O_3	Bixbyite	11.327		5.5, 6	25, 27–30
La_2O_3 A type polymorph	Hexagonal	3.937	6.129	5.5	25
Nd_2O_3	Bixbyite	11.08		4.4	16
Nd_2O_3 A type polymorph	Hexagonal	3.829	5.997	4.4	16
Sm_2O_3	Bixbyite	10.92		5	13, 11.4–15
Ho_2O_3	Bixbyite	10.606		5, 5.2	13.1
Gd_2O_3	Bixbyite	10.813		5.3, 6.4	13.7, 13.6
Dy_2O_3	Bixbyite	10.665		4.9	13.1
Lu_2O_3	Bixbyite	10.391		5.4, 6	12.5
Pr_2O_3	Hexagonal	3.857	6.916	4.6	14.9, 25.4 [41]

The extent of silicate formation depends on temperature, time (spike anneal) and the ion radius of the RE element [31], [51], [52]. A unique property of RE elements is "lanthanide contraction", a term which refers to the observation that the ion radii of rare earth elements decrease gradually as the atomic number increases. The quantity of Si-O-Ln bonds increases as the post-annealing temperature rises, and this increase depends strongly on the ion radii of the RE elements. As a result, metal-oxides with larger ion radii easily form LnSiO (silicate) layers. An alternate explanation can be deduced from thermodynamic arguments [52]. Furthermore, the quantity of Si-O-Si bonds increases after annealing independent of the element.

Rare earth oxide and silicate films have been deposited by various methods including atomic and electron beam evaporation [24], [38], [49], [50], [53], molecular beam epitaxy (MBE) [40], metal organic chemical vapour deposition (MOCVD) and atomic layer deposition (ALD) [33], [35], [54], [55]. CVD and ALD techniques allow the controlled growth of highly conformal films on planar and high-aspect ratio substrates. Recent developments in precursors for the MOCVD and ALD of lanthanide oxides LnO_x and silicates $LnSi_xO_y$ (Ln = Pr, Gd, La and Nd) have been described in [55], with emphasis on the effect of the precursors molecular structure on process chemistry and layer purity.

3. GdSiO: High-*k* Material for the 22 nm Node

3.1. Gd_2O_3 Studies

The Gd_2O_3 layers have been studied extensively [38], [52], [56]–[58]. Gd_2O_3 has been deposited by MOCVD [57], anodic oxidation [59], thermal oxidation [60], [61], MBE [62], [63], e-beam evaporation [49], [50] and ALD [55], [64], [65]. The use of Gd_2O_3 dielectric layers has been reported for Si [52], [63] and III-V compounds, such as GaN [66], [67] and GaAs [68], [69]. Based on thermodynamic consideration, Gd_2O_3 formed according to equation $2Gd_2O_3 + 3\,Si = 4Gd + 3SiO_2$ with $\Delta G > 100$ kJ, is expected to be stable on Si up to 1000°C [42]. Furthermore, Gd is a single valence metal ion (+3); therefore it forms only a single oxide (Gd_2O_3) from the reaction with oxygen. This oxide does not exhibit any intermediate metastable states while reacting with oxygen. The effective dielectric constant of the Gd_2O_3 films is in the range of 7–23 [57]. The reported values for a band gap vary from 5.2 eV [70], [71], 5.3 [29], to 6.4 [17]. The conduction and valence band offsets to Si are larger than 2 eV [62], [71]. The lattice parameter of Gd_2O_3 in its bixbyite phase is 1.081 nm (Table 2), while Si has a lattice constant a_{Si} of 0.545 nm, where $2 \times a_{Si}$ is 0.4% larger than $a_{Gd_2O_3}$, which allows for epitaxial growth.

There are reports on electrical properties of epitaxial Gd_2O_3 thin films grown by MBE [62], [72], with EOT< 1 nm and leakage current density below 1 mA/cm^2. As can be seen from Table 1, these numbers exceed the requirements for LSTP application predicted for 2012. A careful control of the thermodynamic parameters, such as oxygen chemical potential allows the interface layer change from oxide-like to a silicate-like, and thus leads to larger *k* and lower leakage for the latter one [62]. The impact of rapid thermal anneal (RTA) on structural and electrical properties of crystalline Gd_2O_3 layers grown on Si has been discussed in [73]. Any degradation of the layers can be significantly reduced by capping with amorphous-Si prior to RTA.

3.2. Academic Cluster Work

The so-called Academic Cluster comprises of four member institutions, namely – Chalmers University of Technology (Sweden), AMO GmbH (Germany), Tyndall National Institute (Ireland) and Liverpool University (UK). We have recently reported an optimized process based on GdSiO for the gate dielectric, consistent with the 22 nm LSTP target [49]. The Gd_2O_3 layers are deposited by

e-beam evaporation [49], [50] and atomic layer deposition [64], [65] on different interfacial silicon dioxide layers (thermal ∼1–4 nm, and native ∼1 nm). Detailed material properties of the layers are assessed by variable angle (65–75°) spectroscopic ellipsometry (VASE), medium energy ion scattering (MEIS), X-ray diffraction (XRD), high resolution transmission electron microscopy (HRTEM) and X-ray photoelectron spectroscopy (XPS). Electrical characterization including capacitance-voltage and current-voltage techniques is conducted on metal insulator semiconductor (MIS) capacitors with TiN and Au electrodes. The formation of gadolinium silicates has been achieved by RTA annealing of various Gd_2O_3/SiO_2 gate stacks in the temperature range of 800 to 1050°C and anneal time 1–100 s.

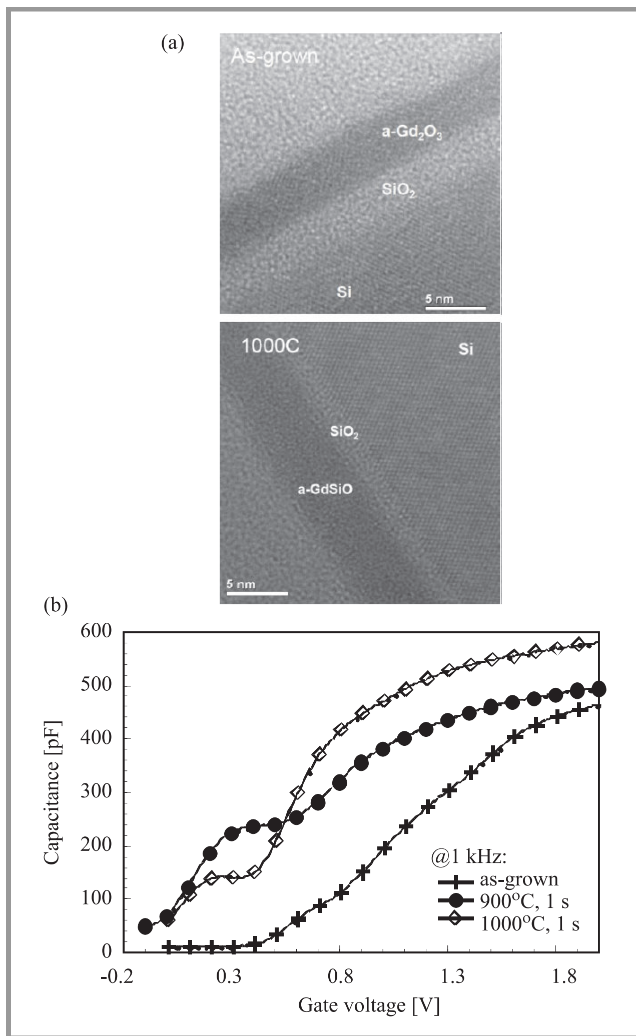

Fig. 1. (a) HRTEM images of Gd_2O_3/SiO_2 gate stacks as-deposited by ALD (top) and after RTA at 1000°C for 1 s in N_2 (bottom); (b) *C-V* plots of corresponding MIS devices (Au/*hi-k*/SiO_2/Si(100)).

The HRTEM images of ALD Gd_2O_3/SiO_2 gate stacks as-deposited and after the RTA @1000°C are shown in Fig. 1(a). The high-*k* dielectric is deposited in amorphous form. Following a 1000°C anneal for 1 s, the intermixing is complete resulting in a 4.6 nm amorphous GdSiO layer. The consumption of interfacial SiO_2 layer is evident after RTA anneal. More importantly, the silicate reaction causes an increase of accumulation capacitance in the associated $C-V$ plots (Fig. 1(b)), and hence the capacitance equivalent thickness (CET) of the gate stack is reduced after RTA. Furthermore, k is ∼ 16 and amorphization of the film annealed at 1000°C reduces the leakage current density ($9.9 \cdot 10^{-7}$ Acm^{-2}) by an order of magnitude compared to the 900°C sample [65].

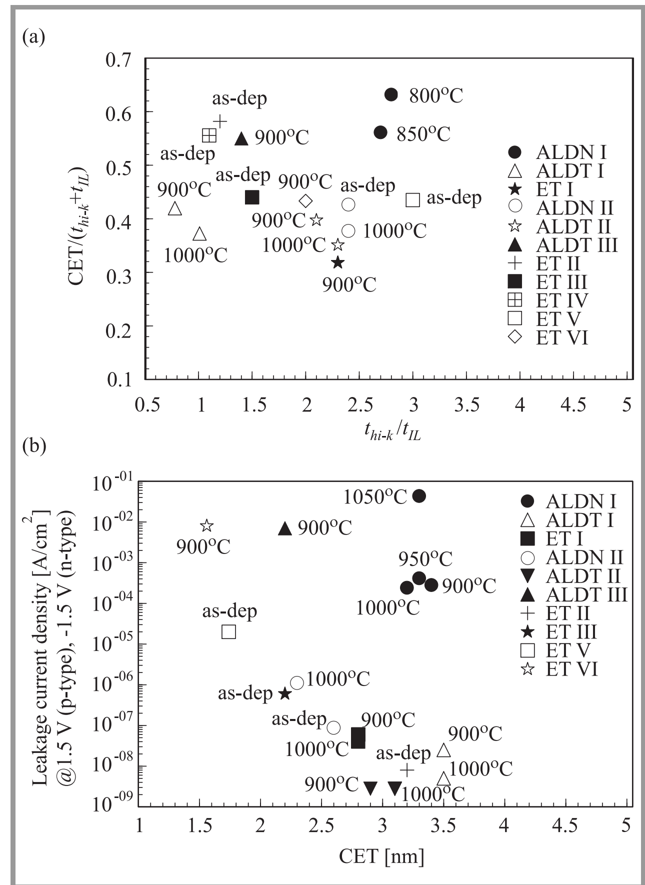

Fig. 2. (a) CET/total deposited thickness versus t_{hi-k}/t_{IL} ratio and (b) leakage versus CET for various Gd_2O_3/SiO_2 gate stacks deposited by ALD and e-beam evaporation, on thermal (T) or native oxide (N). I-VI refer to different runs, i.e., various t_{hi-k}/t_{IL} ratios.

Various ratios of the physical thicknesses of the Gd_2O_3/SiO_2 (t_{hi-k}/t_{IL}) gate stack have been explored [64] as shown in Fig. 2. By plotting CET/($t_{hi-k}+t_{IL}$) versus t_{hi-k}/t_{IL} for 1 s anneal time, it can be seen that a value $t_{hi-k}/t_{IL} \sim 2-2.5$ gives the optimal scaling, that is, the smallest CET of the GdSiO gate dielectric stack. However, this observation needs to be taken equally with the effects of mechanisms involved during RTA anneals on scaling, that is, the way the RTA is performed has shown to be of crucial importance [49]. Specifically, for the same thickness ratios achieved by two deposition processes, e-beam evaporation and ALD, different scaling/CET can be seen after RTA from Fig. 2(b). For ALD processes, RTA was performed in an inert ambient (N_2 or Ar) – RTA1, while

for e-beam evaporation in addition to RTA1, an inert gas is used but with open vacuum valve referred to as RTA2 [49]. GdSiO formation at 900°C by RTA1 results only in slight reduction of CET and this is found to be due to residual oxygen in the process chamber that can diffuse through the films and react at the Si/SiO_2 interface. This is a parasitic effect rather than an intrinsic feature of RTA1; as a result, CET cannot be further reduced as IL re-growth counteracts the consumption due to silicate formation. This explains an increased CET for ALD deposited stacks. The use of RTA2 with open vacuum valve was seen to cause significant reduction of IL re-growth and thus consumption of the IL dominates during silicate formation which further enhances scaling. Using the RTA2 in combination with a preceding post deposition annealing (PDA) treatment enabled to achieve GdSiO gate stack with an EOT of 1.3 nm and $j = 0.02$ Acm^{-2}, in line with ITRS LSTP targets for the 22 nm node [49]. This stack can be optimized further for scaling requirements beyond the 22 nm node as GdSiO has been successfully introduced into fully functional SOI n-MOSFETs with TiN metal gate electrodes [74].

3.2.1. Thermal Stability and Mechanism of GdSiO Formation

The thermal behavior of these Gd_2O_3/SiO_2 gate stacks can be assessed by plotting MIS device leakage current and CET versus RTA process temperature as shown in Fig. 3(a) and Fig. 3(b), respectively. It can be seen that very low leakage currents ($< 10^{-7}$ A/cm^2) are obtained for stacks deposited by both techniques (evaporation and ALD), in particular when there is a thermal oxide as an IL. Furthermore, an increase from 900°C to 1000°C does not compromise the leakage current; it is further reduced. The observed trend is a significant reduction of the capacitance equivalent thickness after annealing as outlined in Fig. 3(b). When observing the RTA time series, very low leakage currents of $\sim 10^{-9}$ A/cm^2 were obtained for 10 s and 100 s anneal time (Fig. 3(a)), however the CET is largely increased after 100 s anneal (Fig. 3(b)). The CET is reduced further when anneal time varies from 1 to 10 s.

Oxygen has been found to diffuse into the film eliminating oxygen vacancies, but Si diffusion was absent after oxygen and vacuum annealing at temperatures up to 800°C for GdSiO films on Si(100) [75]. It has been suggested [23] that silicate formation for rare earth based materials occurs through inter-diffusion with underlying SiO_2 to form silicates, rather than by diffusion of Si and subsequent oxidation, as this can explain absence of silicates when capped structures are used [76]–[78]. It seems that excluding oxygen and preventing the oxidation of the silicon substrate can prevent silicate formation. There are also reports on GdSiO gate dielectric films deposited on Si(001) substrates using UHV (ultra high-vacuum) e-beam evaporation from pressed-powder targets [24]. These films were amorphous as deposited and remained amorphous when annealed to temperatures up to 900°C, and showed $k \sim 16$ and low leakage currents of $5.7 \cdot 10^{-3}$ A/cm^2 at 1 V.

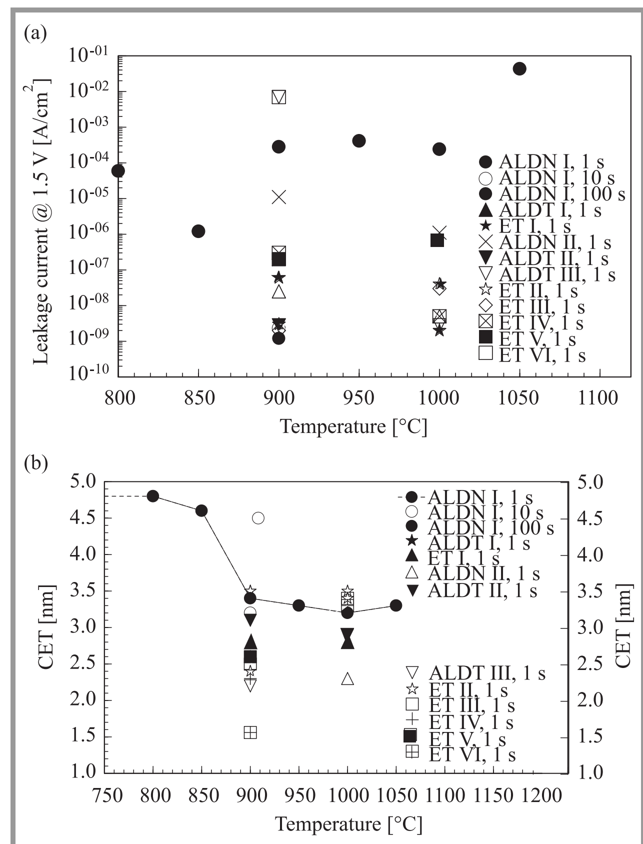

Fig. 3. (a) Leakage current and (b) CET versus anneal temperature for various Gd_2O_3/SiO_2 gate stacks deposited by ALD and e-beam evaporation.

For the ALD Gd_2O_3/SiO_2 gate stacks discussed here, annealing causes substantial reordering of the layers and the effects are apparent by plotting the MEIS energy spectra as depth profiles for Gd, Si and O shown in Fig. 4(a). It can be seen that higher temperatures drive more silicon into the high-k layer. The source of the incorporated Si is likely to be from inter-diffusion with the native SiO_2 layer, with some contribution from the substrate [65]. Diffraction patterns (XRD) from samples annealed in the temperature range from 800–1050°C contain a peak at 28.6° referring to cubic Gd_2O_3. The most pronounced peaks, corresponding to the highest level of crystallinity in the films, occur around 900°C to 950°C. The MEIS and XRD results suggest that two competing mechanisms occur during annealing [65]. The ALD Gd_2O_3 layer crystallizes into the cubic phase at all temperatures studied and the extent of crystallinity increases with increasing temperature. The second mechanism is the diffusion of Si into the layer. As Si is swept into the polycrystalline Gd_2O_3 the crystalline grains become amorphised. This reduces the thickness of the crystalline layer and thus the intensity of the XRD diffraction features. Crystallisation dominates at lower temperatures and silicate formation dominates at higher temperatures. It follows that the final state of a film after annealing depends on the film thickness as well as the anneal temperature and duration, as expected for a diffusion driven process [23].

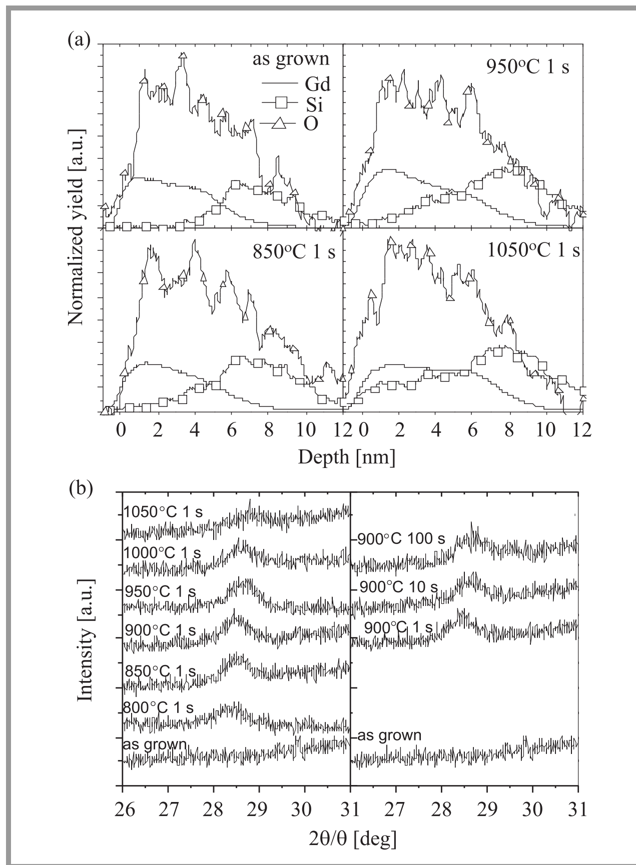

Fig. 4. (a) MEIS and (b) XRD profiles for ALD grown Gd_2O_3/SiO_2 gate stacks under different RTA conditions [65].

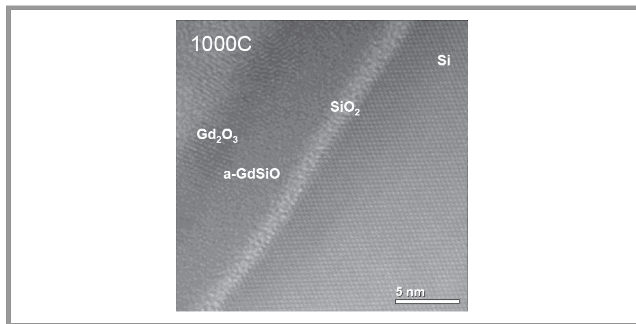

Fig. 5. HRTEM image of ALD bi-layer structure Gd_2O_3/GdSiO/SiO_2 after RTA at 1000°C for 1 s in N_2.

Figure 5 depicts the case when, even after 1000°C anneal, the layer is not fully transformed into the silicate but contains bi-layer structure due to the initially deposited thicker (∼ 8 nm) Gd_2O_3 film. Note also that the interfacial SiO_2 layer is present after the anneal. Similar has been observed for other RE based silicates [23], [50], [52].

3.2.2. Band Offsets for GdSiO

An insight into the energy band line-ups of ALD GdSiO gate stacks is provided by XPS measurements. The onset of the excitation from the valence to conduction bands can be observed at an energy corresponding to the band gap energy below the XPS O 1 s core signal [79], [80]. From the threshold energy of an energy loss spectrum for O 1 s photoelectrons, the bandgap of GdSiO is determined to be 6.3 eV [81]. The measured XPS valence band spectrum for GdSiO/SiO_2/Si is shown in Fig. 6(a). The valence band offset between GdSiO and Si is determined by evaluating the energies of the valence band maxima of GdSiO and Si. These energies were determined by analytically finding the intersection of the regression-determined line segment defining the leading edge of the valence band and the flat energy distribution curve [82], and taking into account charging effects on the XPS spectra [83], [84].

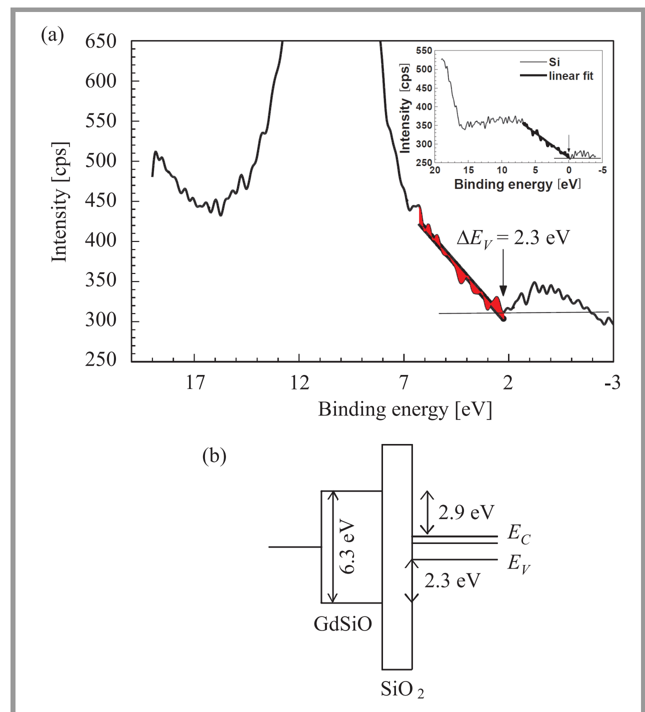

Fig. 6. (a) The XPS valence band spectrum and (b) the band diagram of ALD GdSiO/SiO_2/Si(100) structure.

The values of 2.31 eV for GdSiO and 0.01 eV for Si(100) are estimated. The difference of these values corresponds to a valence band offset of 2.3 eV. Thus the conduction band offset is 2.9 eV. The resulting energy band alignment for a GdSiO/SiO_2/Si(100) is shown in Fig. 6(b). The results are comparable to the ones published by Hattori *et al.* [85] for Gd_2O_3/silicate/SiO_2/Si, where $E_g = 6.4$ eV, $\Delta E_V = 2.2$ eV and $\Delta E_C = 3.1$ eV. For advanced CMOS application, the band offsets to Si above 2 eV and roughly equal ($\Delta E_C \approx \Delta E_V$) represent one of the most desirable features for future gate stack.

4. Beyond the 22 nm Node

Recent reports indicate that lanthanum-based ternary oxides are likely to have major role in meeting the ITRS requirements for scaling beyond the 22 nm node [86]. The growth methods proposed include molecular beam deposition (MBD) [87], [88], pulsed laser deposition (PLD) [89], or ALD [90]. The interfacial layers can be avoided when

ternary rare earth oxide films ($La_xM_{2-x}O_3$, M = Sc, Lu, or Y) are deposited on Si by ALD from metal amidinate precursors and H_2O [86]. Both $LaScO_3$ and $LaLuO_3$ films are found to be amorphous and free of interfacial layers, with high dielectric constants (~ 23 for $LaScO_3$ and 28 ± 1 for $LaLuO_3$), low leakage current density, and are scalable to EOT$<$ 1 nm. $La_{1.23}Y_{0.77}O_3$ films have polycrystalline structures with moderately high $k = 17 \pm 1.3$ and low leakage current [86]. The growth of stoichiometric and smooth $LaLuO_3$ films ($C_E \sim 65$ eV) that remain amorphous up to 1000°C has been reported [89]. The band gap has been found to be 5.2 ± 0.1 eV, with symmetrical conduction and valence band offsets of 2.1 eV, a dielectric constant of ~ 32, and low leakage current density levels. Amorphous $GdScO_3$ films have also demonstrated a high permittivity of 22, the EOT of ~ 1 nm, and the leakage current density less than 2 mA/cm^2 [91].

$LaAlO_3$-based heterostructures are also expected to fulfil the requirements of ITRS beyond 22 nm [92]. Very aggressive scaling <1 nm EOT with reasonable leakage currents can be achieved for amorphous $LaAlO_3$ (LAO) films on Si(001), but interfacial SiO_2 grows at anneals above 400°C. The addition of an Al_2O_3 interlayer increases the thermal stability up to 600°C. Both a-$LaAlO_3$/Si(001) and a-$LaAlO_3/\gamma-Al_2O_3$/Si(001) systems should be appropriate for gate-first processes, when optimized. Suzuki *et al.* at Toshiba Labs have reported [93] 0.3 nm EOT for amorphous $LaAlO_3$ grown by PLD. It should be noted that LAO often exhibits structural instability and interface reaction during high temperature treatment [94], [95].

There are few publications about ultra-thin high-*k* films with EOTs lower than 1 nm on crystalline Gd_2O_3 grown by MBE [62], [72]. There has been a recent attempt to grow epitaxially ternary $(Nd_{1-x}Gd_x)_2O_3$ (NGO) thin films, with the idea that a combination of Gd_2O_3 and Nd_2O_3 would create a system exhibiting exact lattice matching with Si [96]. The NGO films show promising electrical features, the CET of 0.9 nm and leakage currents below 1 mA/cm^2. The key parameter for IL control is found to be oxygen partial pressure during the interface formation and/or MBE growth; it prevents silicide inclusions, while avoiding the formation of interfacial SiO_x [63], [71]. GdSiO material, grown by e-beam evaporation or ALD, as discussed in this paper, has potential for further scaling and is also contender as a high-*k* material beyond the 22 nm node.

Although there seem to be several possibilities to engineer the gate stack for ultimate scaling, most of the high-*k* materials reported above show high mid-gap density of interface states ($D_{it} = 3 \cdot 10^{11}$ eV^{-1}cm^{-2} [91], $1.4 \cdot 10^{12}$ eV^{-1}cm^{-2} [96], $5 \cdot 10^{12}$ eV^{-1}cm^{-2} [95]), and bulk fixed charge density $> 10^{11}$ cm^{-2} [91], [96]. On the pathway of scaling, it is critical to obtain an optimal high-*k*-Si interface with acceptably low $D_{it} < 10^{11}$ eV^{-1}cm^{-2} and mobility in MOSFET channels approaching the universal curve. At the same time, the problem of reliability and stability (charge trapping) [97], [98] of these new dielectrics still remains acute and requires further studies.

5. Summary

In this paper, recent work on rare earth based oxides and silicates has been reviewed with an emphasis on materials suitable for integration according to the ITRS LSTP targets for the 22 nm node and beyond. Understanding the mechanisms that create interfacial layers is a key requirement for further scaling of these high-*k* dielectrics. There are several approaches to achieve elimination of the interfacial SiO_2 layer and thus ultimate scaling, employed by various research labs worldwide. Reaction of the SiO_2 with a RE oxide causes an effective increase for the *k*-value of the interfacial layer. Furthermore, full reaction of the interfacial layer with cap can be used to form a higher-*k* dielectric, or the formation of epitaxial high-*k* dielectrics can be utilised. The scaling potential of GdSiO-based gate stacks which exhibit excellent thermal stability, low leakage currents and sufficiently high band offsets to be employed in the devices for technological nodes beyond 22 nm has been demonstrated.

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