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Invited paper

Recent developments in vertical MOSFETs and SiGe HBTs

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Abstract — There is a well recognised need to introduce new materials and device architectures to Si technology to achieve the objectives set by the international roadmap. This paper summarises our work in two areas: vertical MOSFETs, which can allow increased current drive per unit area of Si chip and SiGe HBT's in silicon-on-insulator technology, which bring together and promise to extend the very high frequency performance of SiGe HBT's with SOI-CMOS.

Keywords — vertical MOSFET, HBT, SOI.

1. Introduction

The ITRS roadmap recognizes the need for innovative device concepts and architectures in addition to the more predictable scaling of MOSFETs. Furthermore, the incorporation of the heterojunction bipolar transistor (HBT) into CMOS processes and further scaling of MOSFETs opens up the r.f. market to mainstream silicon technology. In this paper, we report the status of our work in two related areas. Firstly, we consider innovative vertical MOSFET architectures and secondly, we address work on SiGe HBT's on silicon-on-insulator (SOI).

One vertical MOST device concept features a so-called dielectric pocket (DP) which sits on top of a Si turret. The pocket serves a number of functions; it reduces greatly the influence of the large area parasitic bipolar transistor in the vertical structure and also prevents encroachment of the doping from the extrinsic drain, so reducing electrical bulk punch-through effects. Perhaps most importantly, it reduces charge-sharing effects (SCE) associated with the reverse biased drain and so improves threshold voltage control. The device offers dual channel or gate all around for high current drive with reduced footprint and can be readily scaled to the decananometer regime. We consider also strategies for reducing parasitic capacitance using thickened oxide regions and inhibiting parasitic bipolar transistor action using a poly-SiGe extrinsic source contact.

The SiGe HBT (on SOI) process has the advantage that all the device layers (collector base and emitter) are realized in a single epitaxial growth stage. This involves selective and non-selective growth. We will briefly review our work and report the results of a recent study concerning high injection effects and associated current crowding in the low-doped emitter region of the device. A major showstopper for SiGe HBT's is the transient enhanced diffusion of boron from the very heavily doped base. The incorporation of carbon in substitutional sites during growth of the base has been shown to suppress TED very effectively. Various growth techniques are usually used, with conditions far from equilibrium so leading to metastable alloys with C concentrations exceeding the equilibrium solubility (C supersaturation). Further post growth device processing requires that the structural properties and alloy compositions remain stable during any annealing steps. We comment here on out proposed methodologies to address this new area of activity.

2. Vertical MOSFETs

It is recognised that vertical transistors can overcome scaling problems due to lithography resolution, whereby decananometer channels can be realised with relaxed lithography as the channel length is determined by the accuracy of ion-implantation or epitaxial growth. Vertical transistors also allow double gate or gate all-around structures thus increasing current drive albeit at the expense of increased device capacitance. The architectures are however compact and hence give a high drive with reduced footprint compared to an equivalent lateral architecture, as demonstrated in [1]. Much of the work reported previously is concerned with discrete device fabrication often using fabrication techniques that could not be easily integrated into an advanced CMOS process [2–5]. Rather than present a detailed account of the large body of work gathered on vertical MOSFETs and double gate MOSFETs, we choose to summarise the key developments by identifying three basic approaches to vertical MOSFET realization and these are depicted in Fig. 1.

In the first approach, the device is realised by epitaxy [2]. This is the easiest way to realise devices but has a number of important disadvantages. Perhaps most importantly, the approach does not easily allow the production of p- and n-channel devices required for CMOS. Furthermore, parasitic overlap capacitances are very high and there is a strong parasitic bipolar transistor. The gain of this transistor can be high because the effective base will be very thin (set by the channel length) and also the currents themselves will be high as the effective emitter/collector regions extend across the turret. The device features very deep source/drain junctions and the body region must be highly doped. It will suffer from severe short channel effects. The second approach uses selective epitaxy [3, 4] and by this means parasitic capacitances can be reduced, particularly in the replacement gate approach of Hergenrother *et al.* [4]. Parasitic bipolar gain and currents remain high, however, short channel effects remain severe and there may be reliability problems with the gate oxide which is re-

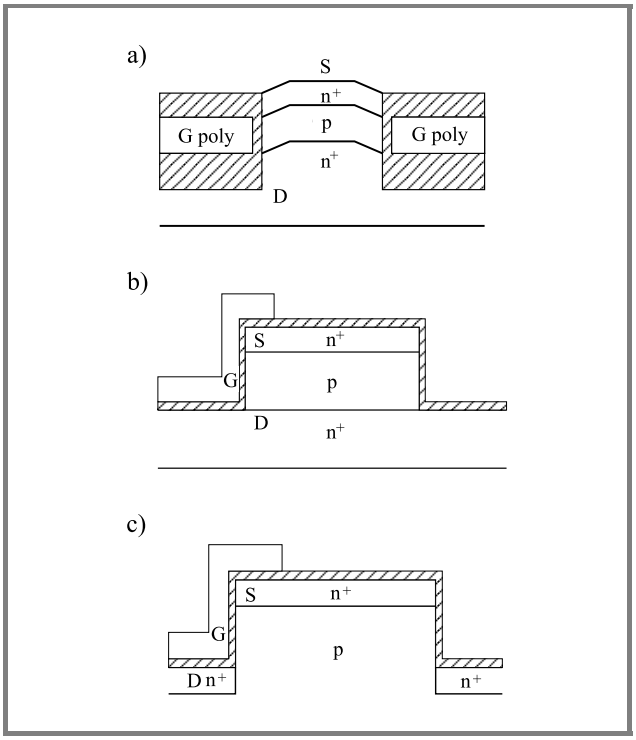

Fig. 1. Vertical MOSFET types: (a) epitaxy; (b) selective epitaxy; (c) ion-implanted.

alized in a non-standard way. The third approach employs ion implantation [5] and allows the realisation of architectures with reduced parasitic bipolar gain and improved short channel effects but the parasitic capacitances remain high. A key advantage of this approach is the ability to devise CMOS comparable processes.

We identify therefore three important research issues for VMOS transistors namely reduction of parasitic capacitance, control of short channel effects and reduction of parasitic bipolar gain. We now investigate the means of addressing these three key issues.

We have reported a novel vertical transistor architecture incorporating a so-called dielectric pocket [6, 7] for control of

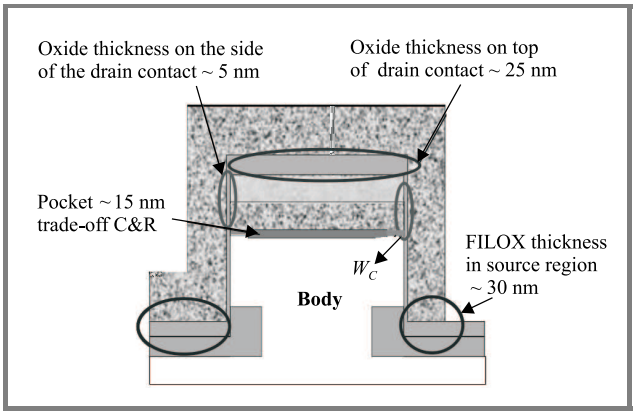

Fig. 2. Vertical MOSFET architecture, featuring the dielectric pocket and thickened oxide regions to minimise parasitic capacitance.

short channel effects. This concept was first demonstrated successfully within a lateral architecture [8], but implementation in a vertical architecture is considerably simpler. The structure is compatible with strategies reported previously to reduce parasitic capacitances in the device [7, 9].

The basic structure of the VMOST device concept featuring the dielectric pocket is shown in Fig. 2. The pocket serves a number of functions; it reduces greatly the influence of the large area parasitic bipolar transistor in the vertical structure and also prevents encroachment of the doping from the extrinsic drain, so reducing electrical bulk punch-through effects. Perhaps most importantly, it reduces charge sharing effects associated with the reverse biased drain and so improves threshold voltage control. Note the silicidation of the top contact, which we designate the drain, to reduce significantly the associated parasitic resistance. The intrinsic drain contact is formed by out-diffusion from the poly-Si extrinsic drain contact in a manner not unlike that of a poly-emitter on a bipolar transistor process. Care is required with the thermal budget to ensure that only slight out-diffusion occurs from this extrinsic drain contact such that there is no encroachment of drain dopant below the DP into the channel region. Such encroachment would remove the electrostatic influence of the DP on the channel and so mitigate its influence on the SCE. Notice that dual channel operation is achieved by the gate poly-contact running over the pillar width which is set to the minimum feature size to reduce drain/body overlap capacitance.

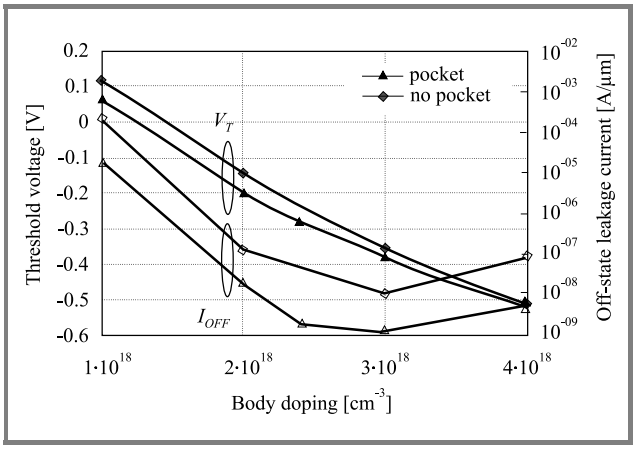

Fig. 3. Threshold voltage and off-state leakage current versus body doping for 50 nm vertical MOSTs with and without dielectric pocket. The gate oxide thickness was 2 nm.

The ISE device simulator was used to obtain electrical characteristics for the DP-VMOST. The Van Dort quantum correction model, hydrodynamic model, avalanche and band-to-band tunnelling were all switched on to provide self-consistent data for short-channel, highly doped devices. The dielectric pocket thickness was set at 15 nm to minimise its parasitic capacitance [7]. The gate oxide thickness was set at a conservative value of 2 nm as the formation of gate oxides on sidewalls with associated corners is likely to prove problematic. The body doping was then varied to

produce electrical characteristics for the PMOS with and without the DP, as summarised in Fig. 3.

The leakage current is seen to be at minimum for a body doping of $3 \cdot 10^{18}\,\mathrm{cm}^{-3}$; band-to-band tunnelling becomes increasingly dominant beyond the minimum whereas punch-through causes the increase in leakage for lower doping levels. A body doping of $2.4 \cdot 10^{18}\,\mathrm{cm}^{-3}$ results in a threshold voltage of -0.28 V and a leakage current of 1.5 nA/μm at a drain to source voltage of -1 V.

Further simulations serve to investigate the influence of the spacing between the pocket and the gate oxide (referred to as the contact region width, W_C) on the threshold voltage. The DP serves to increase the absolute magnitude of threshold voltage because it inhibits charge sharing by the drain. For $W_C = 50$ nm, the V_T equals that of the non-DP device indicating that the DP no longer exerts electrostatic influence. The results are summarised in Fig. 4, where it is

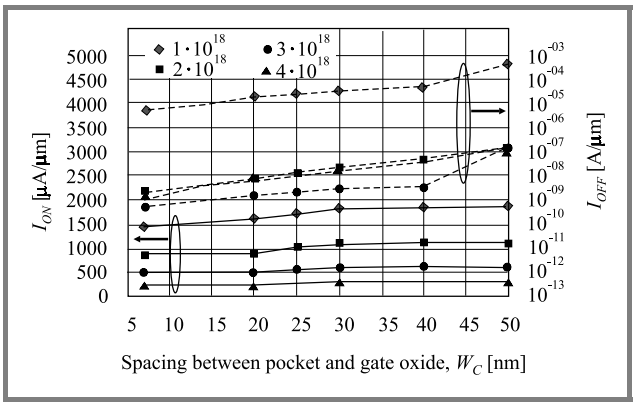

Fig. 4. I_{ON} and I_{OFF} for different contact widths, W_C.

shown that decreasing W_C results in significant reduction in I_{OFF} with little reduction in I_{ON}. The latter arises because of the influence on V_T. For $W_C = 20$ nm and a body doping of $2 \cdot 10^{18}\,\mathrm{cm}^{-3}$, an on-current of 1 mA/$\mu$m and off-current 10 nA/$\mu$m is obtained. Simulated transistor characteristics (not shown) reveal a DIBL of 80 mV for a body doping of $2.4 \cdot 10^{18}\,\mathrm{cm}^{-3}$. Repeating the simulations with a gate oxide thickness of 1.2 nm results in a DIBL of 30 mV, $I_{OFF} = 7$ nA/μm, $I_{ON} = 1.2$ mA/μm.

3. Parasitic capacitance reduction

The approaches to reduce the parasitic capacitances are indicated in Fig. 1 and involve thickening oxide regions using the following techniques. Reduction of gate-source overlap capacitance (bottom of pillar) is achieved by a LOCOS type process FILOX [9, 10]. Incorporation of a deposited oxide region on top of the pillar and the thicker oxide grown on the highly doped poly-Si extrinsic drain contact can reduce significantly the gate-drain capacitance. A previous study using MOS-capacitors has demonstrated a 5-fold reduction in parasitic overlap capacitance using FILOX and a thick top oxide [10].

A semi-analytical transient model has been developed to assist in the optimization of the device with regard to parasitic capacitances [7]. The methodology is to consider an inverter loaded by n other inverters. A unity fan-out CMOS inverter circuit is shown in Fig. 5, where the parasitic capacitances are identified. These capacitive components of the device structure are readily related to the device geometries and physical parameters – doping levels, oxide thicknesses, etc. using standard equations.

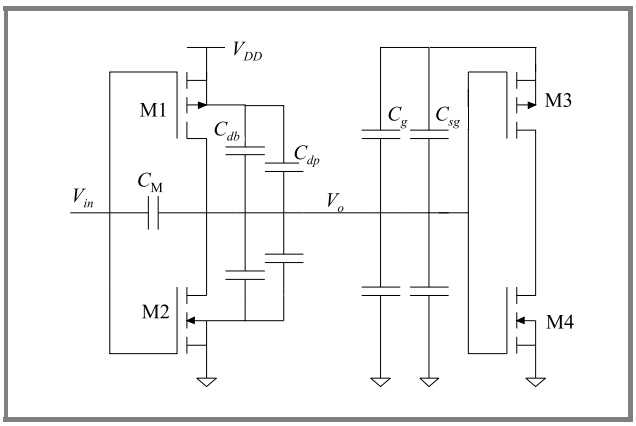

Fig. 5. Circuit used as a test bench.

The capacitances can be lumped together into one single capacitor, C_T assigned to the output node, V_o by recognising series and parallel configurations and treating V_{in} and V_{DD} as virtual earths. As the gate to source/drain overlap capacitances (C_{gso}/C_{gdo}) are responsible for a significant portion of C_T in a vertical structure, these capacitances were isolated from the total gate source/drain capacitance, (C_{gs}/C_{gd}). Other capacitances considered were gate to substrate (included with C_{sg}), drain to bulk depletion region C_{db}, dielectric pocket capacitance, C_{dp} taking into account depletion under the oxide, and finally the capacitance due to the drain contact. The voltage dependence of depletion capacitance is linearised in the usual manner. Note that vertical devices benefit from being operated "source down" because this reduces the switched depletion capacitance compared to "drain down", i.e. source at the top of the turret.

We define a circuit performance metric $\tau = 3\tau_f$ where τ_f is the fall time of V_o following an abrupt input voltage step. The fall time can be calculated by considering the discharge of the effective load capacitance, C_T, via the NMOS pull-down transistor, between 10 and 90% of the full voltage swing as indicated in the model equations below, where $i(t)$ is the transient current through the NMOS and other symbols have their usual meaning. Gate field dependence of mobility is included also:

$$\tau = 3\left(\tau_{fs} + \tau_{fus}\right) = -3C_T(V_o) \int_{0.1\,V_{DD}}^{0.9\,V_{DD}} \frac{dt}{i(t)},$$

$$\tau_{fs} = \frac{C_T}{2C_{ox}W v_{sat}}\left(1+\frac{L\cdot\xi_{sat}}{V_{DD}-V_{th}}\right)\int_{V_{Dsat}}^{V_H}\frac{1}{(V_{DD}-V_{th})(1+\lambda V_o)}dV_o,$$

$$\tau_{fus} = \frac{C_T L}{2C_{ox}W\mu_{eff}(V_{DD})}\int_{V_{Lt}}^{V_{Dsat}}\frac{1}{(V_{DD}-V_{th})V_o-\frac{V_o^2}{2}}\,dV_o\,.$$

The latter two equations represent the time the device is saturated and unsaturated, respectively. The equations are easily solved numerically. To validate the model, a unity fan-out inverter circuit was simulated using the SpectreS simulator in Cadence v4.4.3 and a production 350 nm lateral device SPICE deck. The simulated fall time was equal to 58 ps while the calculated fall time was equal to 49 ps, an error of 15% that represents reasonable agreement for a comparative study.

Using this methodology, we have identified the approximate thicknesses of dielectric regions required to optimise the VMOST. The results of the study are indicated in Fig. 1 (thickness values quoted).

4. Reduction of parasitic BJT gain

The DP concept brings the added benefit of reducing considerably the area of the effective emitter and collector formed by the source and drain of the VMOSFET and so reduces the magnitude of base and collector currents of the PBT. The DP device is however inherently "drain up".

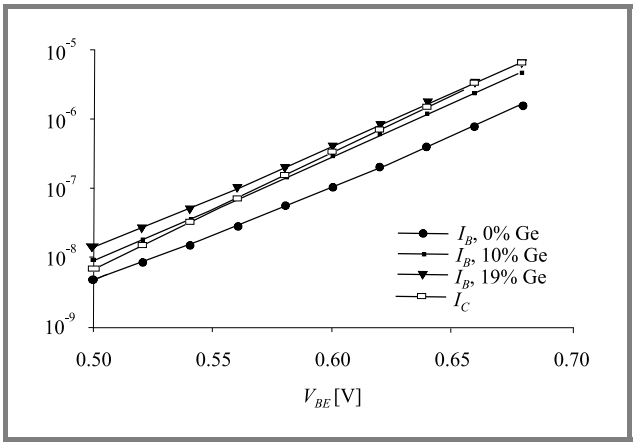

Fig. 6. Increase in base current as a result of Ge incorporation into the emitter.

An alternative approach to minimise parasitic bipolar transistor gain for drain-down configurations (source at the top), is to include a poly-SiGe extrinsic source contact [11]. This serves to steepen the profile of minority carriers injected into the parasitic emitter so increasing the base current and reducing the gain. Figure 6 shows Gummel plots from test bipolar transistors where a considerable reduction in BJT gain is evident.

A theoretical model for the base current of such a poly-SiGe emitter has been developed, which combines the effects of the poly-SiGe grains, the grain boundaries and the interfacial layer at the poly-SiGe/Si interface into an expression for the effective surface recombination velocity of a poly-SiGe emitter [11]. The model is equally valid for the parasitic BJT in vertical MOSFETs. Silicon bipolar transistors were fabricated with 0, 10 and 19% Ge in the poly-SiGe emitter and the variation of base current with Ge content characterised. The measured base current for a poly-SiGe emitter was seen to increase by a factor of 3.2 for 10% Ge and 4.0 for 19% Ge compared with a control transistor containing no germanium, in good agreement with the theoretical predictions. The competing mechanisms of base current increase by Ge incorporation into the polysilicon and base current decrease due to an interfacial oxide layer were investigated. The size of the base current increase with Ge content depends on the thickness of the interfacial layer, with larger increases being obtained for thinner interfacial layers. The introduction of germanium into a polysilicon emitter therefore allows the base current, and hence the gain, to be controlled by means of the Ge content in the poly-SiGe parasitic emitter of a vertical MOSFET.

5. Test transistors

Both p-channel and n-channel vertical MOS transistors have been successfully fabricated to demonstrate some of the concepts outlined above. Figure 7 shows a field effect SEM of a vertical transistor, demonstrating the FILOX concept whereby thickened oxide regions are achieved in the source and drain gate overlap regions, to minimise overlap capacitance. Both pillar top and bottom have a 60 nm thick FILOX oxide as visible under the gate electrode and this oxide encroachment reduces the gate to top electrode capacitance. Calculations based on the electron micrographs, and process and device simulations give an estimate for capacitance reduction of a factor of 3.

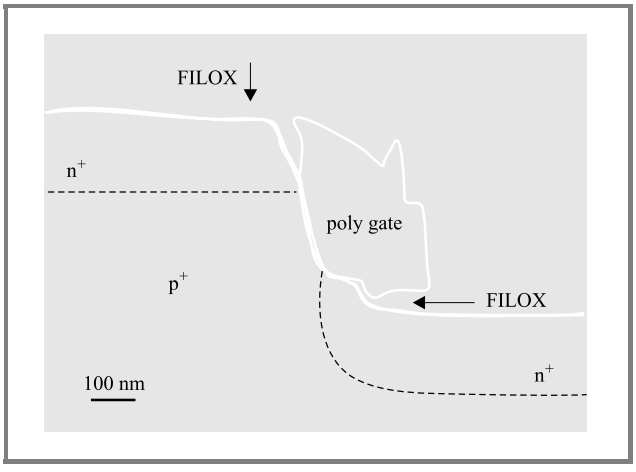

Fig. 7. Field emission SEM cross-section of a surround gate ion-implanted vertical NMOS.

Figure 8 shows transfer characteristics of vertical NMOS transistors similar to those shown in Fig. 7. Gate ox-

ide thickness is 3 nm and channel length is estimated to be 100 nm. Characteristics on the right employ a single gate whereas those on the left have a surround gate and hence considerably higher drive.

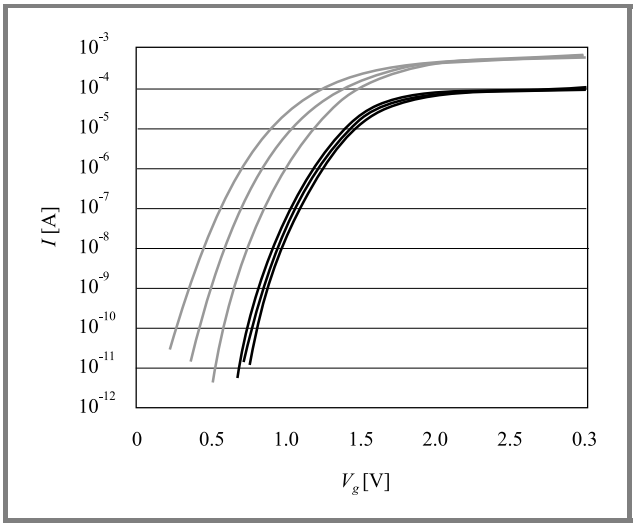

Fig. 8. Transfer characteristics of vertical n-channel transistors.

Transfer characteristics of surround gate vertical PMOS transistors are shown in Fig. 9. The threshold voltage is higher than normal since the gate oxide thickness of 10 nm was chosen very conservatively to prevent shorts in the corners of the transistors. Otherwise the transistors are of very high quality with negligible variation over the wafer.

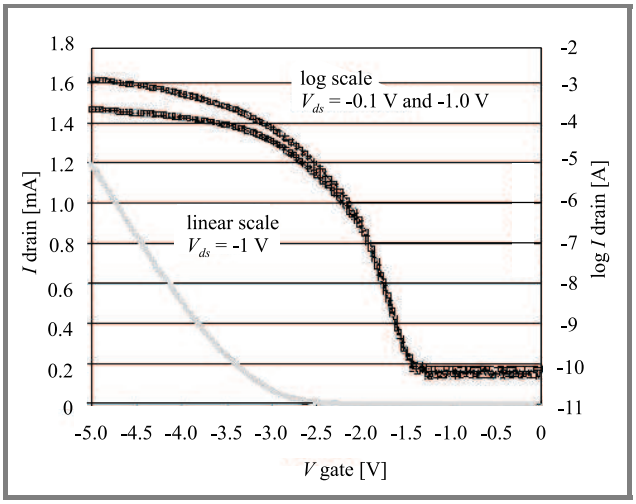

Fig. 9. Transfer characteristics of a 300 nm surround gate ion-implanted vertical PMOSFET.

6. Performance appraisal

The VMOS inverter with 2 nm gate oxide was compared to equivalent minimum sized lateral CMOS inverters taken from ITRS 2001. The width of the PMOST, W_p was set to 2 W_n. The source and drain resistances of the VMOST

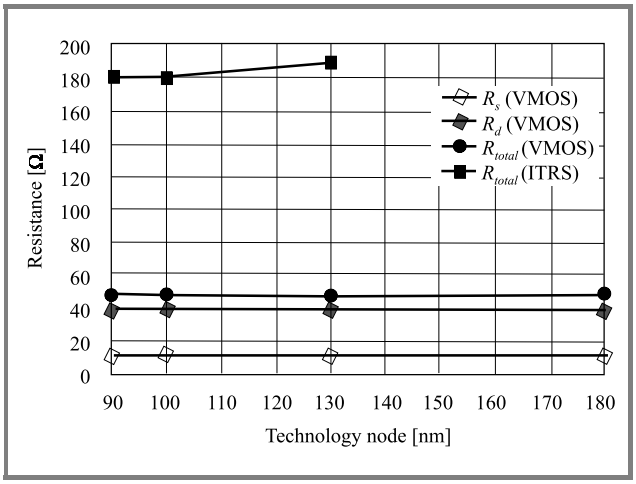

Fig. 10. Scaling of series resistance.

(extracted from ISE simulation) are 3 to 4 times smaller than the ITRS values and these resistances do not significantly increase when the device is scaled as shown in Fig. 10. This arises essentially because the dielectric pocket precludes the need for pockets or extensions.

Figure 11 serves to quantify the performance of the optimised VMOS up to the 45 nm technology node, using the delay metric $C_T V_{DD}/I_{ON}$. The capacitance C_T obtained

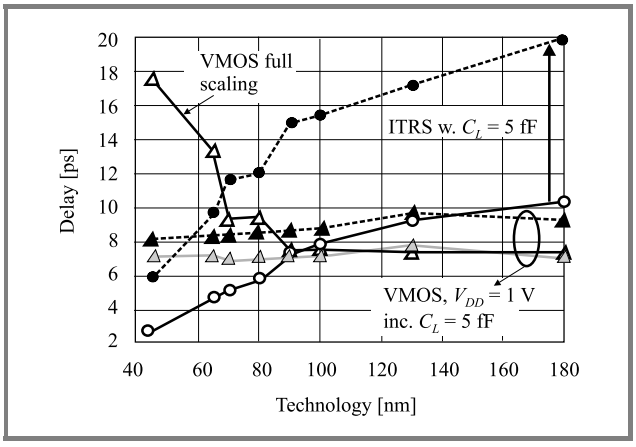

Fig. 11. Projected performance of VMOS in context of the roadmap. Delay approaching that of the 40 nm ITRS node can be realised with earlier generation rules for loaded inverters (5 fF).

from ISE simulations includes gate overlap and depletion capacitances [7]. The VMOS shows a clear advantage down to the 90 nm node (note that the channel length of the VMOS is not scaled). Thereafter the performance deteriorates largely because of the reduced V_{DD}. The effect of maintaining V_{DD} for the VMOST is shown also. Beyond the 100 nm node, we can say that load capacitance due to interconnections will have a very dominant role and so the additional drive capability of the VMOS should continue to offer considerable advantage. We demonstrate this by including a fixed load capacitance of 5 fF in the calculation

of delay. In this context, the smaller relative degradation in performance of the VMOST compared with the ITRS roadmap demonstrates the potential of the latter device.

7. Heterojunction bipolar devices

Silicon-germanium heterojunction transistors allow Si technology to penetrate lucrative radio-frequency application markets of mobile communications and local area networks. For the bipolar transistor, the silicon-on-insulator technology brings advantages of reduced collector capacitance and reduced cross-talk for mixed signal circuits. In the context of BiCMOS, the CMOS circuitry gains much advantage from SOI; namely simplified process flow and latch-up immunity together with enhanced MOSFET device performance. In particular, the lower threshold voltage and low junction capacitance associated with SOI-CMOS is particularly suited to low-voltage, low power applications. The SiGe HBT also offers enhanced performance at lower current levels due to the collector current enhancement thus there are overall benefits for lower power, high performance SOI-BiCMOS circuits. Bond and etch back SOI (BESOI) is preferred for HBT application due to the better Si and SiO_2 quality.

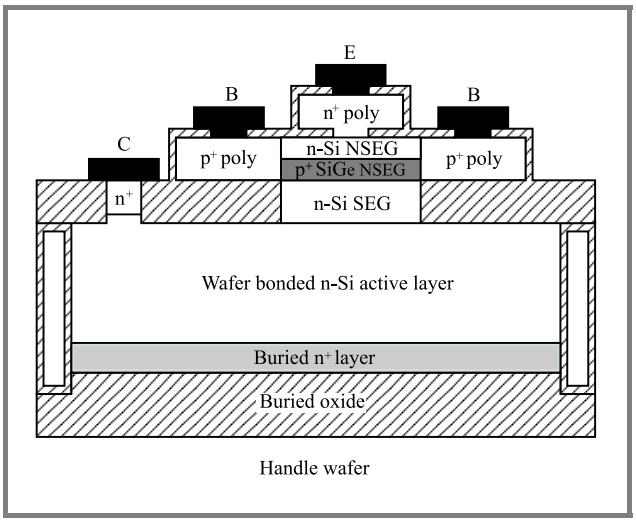

Fig. 12. Schematic diagram of the bonded wafer SOI device architecture.

A schematic diagram of the SiGe HBT on SOI is shown in Fig. 12. The bonded SOI wafers used feature a 1 μm buried oxide layer with the surface Si layer thinned to a nominal thickness of 1.5 μm. Deep, poly-Si filled trenches provide isolation through to the buried oxide layer. The patterned SOI layer is used to provide the heavily doped buried collector as well as the crystalline seed layer for subsequent epitaxial layer growth of the silicon collector and SiGe base layers. Before the silicon epitaxial growth the SOI layer is implanted with a $5 \cdot 10^{15}\text{cm}^{-2}$ dose of arsenic ions at an energy of 160 keV to form the buried collector contact layer. The transistor layers are grown using selective epitaxial growth (SEG) for the Si collector, followed in the same growth step by non-selective epitaxial growth (NSEG) for the p+ SiGe base (nominally 12% Ge) and the n-Si emitter cap [12]. The selective Si collector was grown at 900°C and the non-selective SiGe base and Si emitter cap at 750°C.

The advantages of this approach are that the basic transistor structure is grown in a single epitaxy step and the growth interface is kept away from the transistor active regions. Transistor characteristics show good uniformity across the wafer implying good control of the Ge and B concentrations across the wafer during the non-selective SiGe growth.

Achieving full optimisation of HBT's is facilitated by this growth of collector, base and emitter layers in the same growth step. The incorporation of a low-doped emitter (LDE), however, implies a propensity for high emitter resistance particularly in devices where the emitter overlay is large. Furthermore, issues arise as to the realisation of the buried layer and associated collector resistance for HBTs on SOI. We have identified a new parasitic mechanism whereby we explain anomalies in SOI-HBT device characteristics to be the result of current confinement caused by high lateral resistance in the low doped emitter region of the device.

Figure 13 shows sets of Gummel plots for SiGe HBTs (a) and Si controls (b), where the parameter b is varied. Considering first the SiGe HBTs (a), for $b = 0$, we observe high leakage current which we have explained earlier [12]. For small b, we observe correlated turn-over of collector and base current at relatively low values of $V_{BE} (\approx 0.64\ \text{V})$ presumably due to series resistance induced, lateral voltage drops. As the base current level is small, we suggest at this stage that the turn-over is a result of resistive drops in the emitter due to the high collector current. At higher bias levels $(0.88 - 1.0\ \text{V})$, pronounced I_B-kinks and hard limiting of I_C are evident. The onset of the base current kinks correlate with the hard limiting of I_C, suggesting quasi-saturation due to internal forward biasing of the collector-base junction due to collector series resistance.

Alternatively, the kinks may be due to a combination of emitter resistance and modified kink effect (MKE) [14]. The MKE is an effect associated with the collector-base junction. At high collector current densities, the image charge of holes accumulating at the collector end of the base become sufficiently large to cause the band-bending in the base depletion region to change sign. This has the effect of "mirroring" the valence band edge discontinuity into the conduction band thus causing the appearance of a potential barrier, which results in quasi-saturation of I_C. We will discuss further, which of these two effects (collector resistance or MKE) is the likely explanation. Turning to the Si devices of Fig. 13b, I_C is of course lower than that of the HBT's for a given V_{BE} so collector resistance induced kinks might not be evident. MKE is of course not to be expected in homojunction devices. For higher b-values (5.5, 6 μm), I_C is seen to turn-over at $V_{BE} \approx 0.7$ V and exhibit an ideality factor (m) of two with coincident severe limiting of the base current. This latter trend is evident in both SiGe and Si base devices.

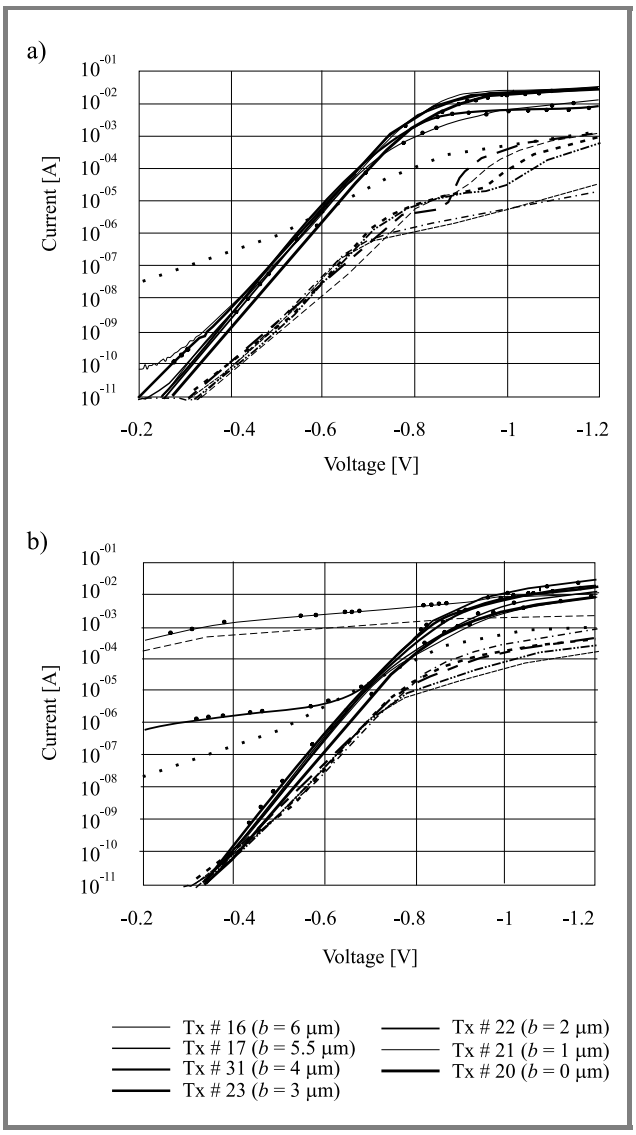

Fig. 13. Measured Gummel characteristics from (a) SiGe HBT (wafer # 6); (b) Si base (wafer # 9).

Figure 14 shows a plot of the collector current dependence of devices with large values of b. It is seen that at low bias the current exhibits an areal dependence with relation to the emitter polysilicon (EP): for these devices the active area is set by the emitter polysilicon. However, at approximately 0.6 V for the HBT and 0.7 V for the BJT the current dependence changes from an EP areal dependence to an emitter window (EW) areal dependence. This bias level corresponds to the onset of the $m = 2$ regime. For devices with smaller b, the emitter polysilicon areal dependence is maintained until higher biases.

We have shown in previous work [13] that the collector current in the $(m = 2)$ – regime shows an activation energy of half the band-gap and the current gain β shows a negative coefficient of temperature. These latter three properties are strong indicators of high injection. The bias level at which the proposed high injection effect occurs is not consistent with the doping levels in either base or emitter so the $(m = 2)$ – region on the characteristics and the (presumably) associated turn over in base current can be considered anomalous.

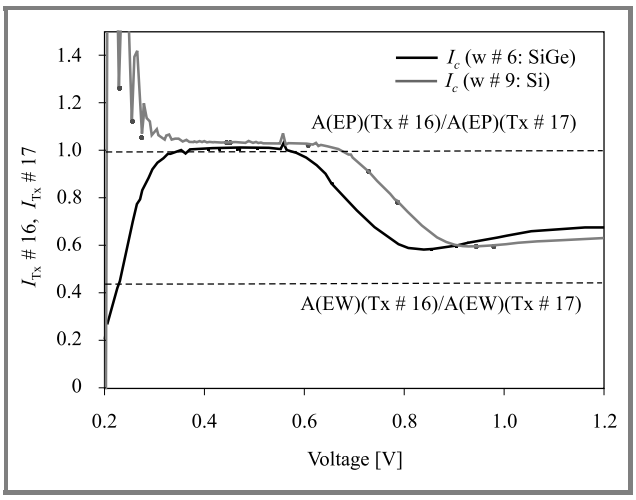

Fig. 14. Device dimensional collector current dependence for devices with large values of b.

Silvaco ATLAS was used to simulate devices with $b = 2\ \mu$m and $b = 6\ \mu$m. The emitter and collector regions were set at uniform doping level and the base was set as a Gaussian function, with a peak doping of $4 \cdot 10^{18}\,\mathrm{cm}^{-3}$. The collector doping was $1 \cdot 10^{17}$ and the emitter doping $N_E = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$. The collector contact was placed at the back of the device. We consider simulations for $V_{BE} = 0.8$ V, $V_{BC} = 0$ V. This is the bias level at which simulated Gummel pots begin to show the turn-over in I_B. (Note that our simulator is not fully calibrated against experimental results.) For the device with $b = 2\ \mu$m the current flow was seen to be uniform across the whole of the active area at this bias level. Figure 15 shows the simulated electron current density for a device with $b = 6\ \mu$m. Confinement of the current to the centre of the device is clearly evident.

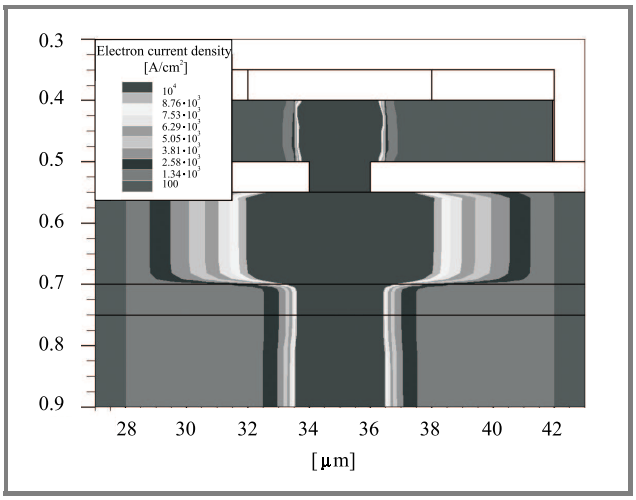

Fig. 15. Simulated electron current density with device biased at $V_{be} = 0.8$ V for $b = 6\,\mu$m.

Figure 16 shows emitter resistance extracted using the Ning-Tang technique [15]. The results for larger b-values will be in error (by about a factor of 2 from Fig. 13) because of the increasing lack of areal dependence. A linear extrapolation from the small values gives an indication of the likely emitter spreading resistance for large b-values.

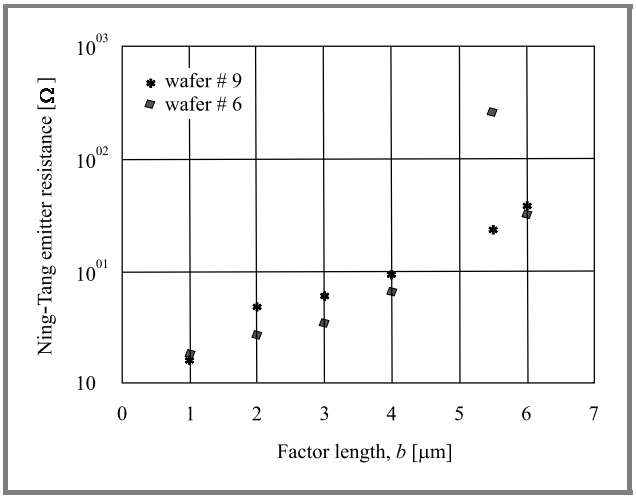

Fig. 16. Emitter resistance extracted using the Ning-Tang technique.

Next, we resolve the issue as to the nature of the kinks for devices with smaller b-values. Applying the methodology of [14] to the $b = 1\ \mu$m curve in Fig. 13, does not produce an ideal I_C and I_B curve with quasi-saturation of I_C. We conclude that the kinks arise from quasi-saturation due to R_C, therefore. This is consistent with the high value of I_C and the estimated value of R_C ($\sim 100\,\Omega$). This highlights the problems of realising low resistance access to the collector for SOI-HBTs. Wafer bonding offers the possibility of buried silicide layer to address this issue [16].

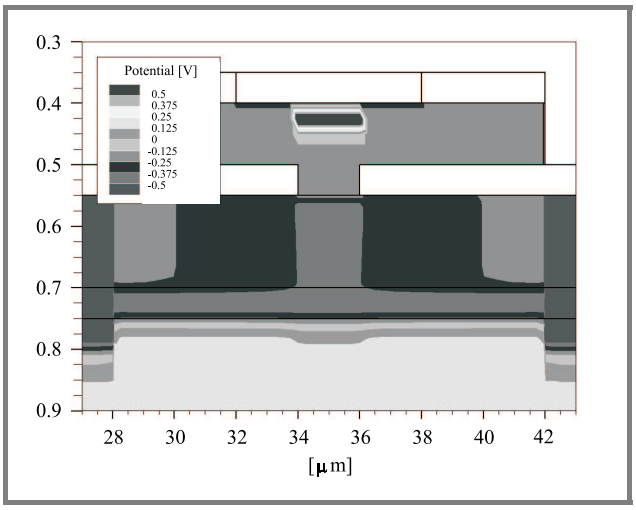

Fig. 17. Simulated potential with device biased at $V_{be} = 0.8$ V for emitter overlay $= 6\ \mu$m.

Finally, Fig. 17 shows a 2D potential distribution, and the de-biaisng effect of the emitter resistance is clearly evident.

8. SiGeC HBT technology

In addition to the parasitic mechanism of the previous section, a major issue with HBTs is parasitic barrier formation by the out-diffusion of boron from the heavily doped base. This is exacerbated by the flow of interstitials arising from implant damage or oxidation of the surface: "transient enhanced diffusion". A strategy to limit this effect is to introduce a small percentage of substitutional carbon (C_s) into the lattice, which allows band engineering and strain control. However, carbon has low solubility in Si and 2D growth conditions must be maintained to achieve substitutional rather than interstitial carbon (C_i) incorporation whilst increasing the critical thickness, decreasing the strain and improving the bandgap shift. The SiGeC layer can be obtained at low temperatures using MBE and CVD epitaxial growth techniques but we are concerned with further processing steps, such as thermal oxidation, and post implant activation anneals. The challenge then is to obtain an alloy layer (SiGeC) with sufficiently high C_s content and to ensure that this is maintained during the subsequent HBT process. Thus thermal budget and Si cap thickness play an important role as well as any source or sink sites formed by interstitials as these have a strong influence on the diffusion and clustering behaviour of carbon. For instance, an oxidation process will generate higher carbon loss rates than a vacuum or inert gas annealing. Redistribution or complete loss of carbon from the SiGeC layer can occur due to C-diffusion and clustering can result in interstitial carbon (C_i) leading to the formation of β – SiC precipitates. The situation is further complicated because these processes are inter-dependent.

The total concentration of carbon inside the alloy can be measured with secondary ion mass spectrometry (SIMS) whereas C_s is typically obtained from high resolution X-Ray diffraction (HRXRD), phonon based techniques such as Raman and Fourier transform infra-red (FTIR) spectroscopy. Cluster formation can be viewed using high resolution TEM (HRTEM), HRXRD, FTIR and Raman spectroscopy. No single technique provides all the necessary information therefore and so we adopt the following methodology. We characterise the layers post-growth, using SIMS for carbon, boron, and germanium total concentration profiles, scanning ellipsometry (SE) which yields layer thickness and carbon concentration (as well as optical properties), FTIR with the C_s line at 610/cm, O_i line at 1100/cm, Si-C lines 700–900/cm, and XRD. Figure 18 shows initial results from SE and XRD showing a disparity between C concentrations, which can be interpreted in terms of C_s and C_i.

Figure 19 shows corresponding layer thickness derived from SE and XRD. Further calibration will be sought from HRTEM.

The results from the various techniques are correlated to provide a self-consistent assessment of layer content and morphology in particular the I/S ratio. If the XRD and if the results from the various techniques are correlated to

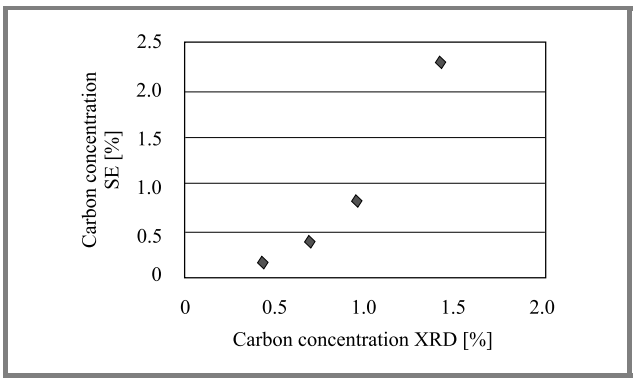

Fig. 18. C concentration derived from SE and XRD.

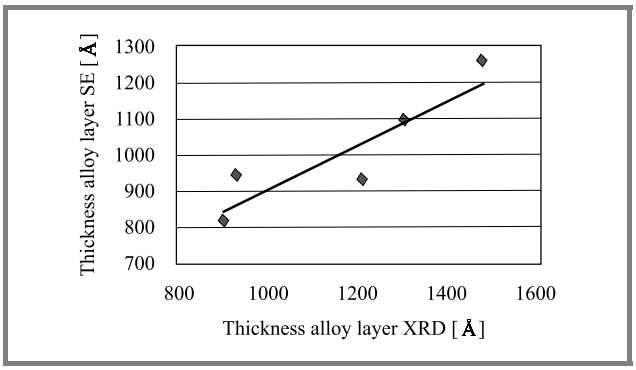

Fig. 19. Layer thickness derived from SE and XRD.

provide a self-consistent assessment of layer content and morphology. If the XRD and SIMS results do not remain correlated during subsequent heat treatments, we look for evidence of carbon clustering using HRTEM. Further correlation is sought with electrical results from test transistors. The ultimate aim of the experiments is to optimise the thermal budget.

9. Conclusions

In this paper we, have summarised our recent work in two areas: the first relates to novel vertical transistor concepts whereby we have demonstrated by simulation and experimentally some potential advantages of our ideas and concepts. The second area concerns explanation and modelling of some anomalous effects in experimental characteristics of SiGe transistors on SOI substrates and a discussion of our strategy for realising SiGeC layers into HBTs.

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