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Paper

Electrical characterization of ISFETs

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Abstract— Methodology of electrical characterization of ISFETs has been described. It is based on a three-stage approach. First, electrical measurements of ISFET-like MOSFETs and extraction of basic parameters of the MOSFET compact model are performed. Next, mapping of the ISFET channel conductances and a number of other characteristic parameters is carried out using a semi-automatic testing setup. Finally, ISFET sensitivity to solution pH is evaluated. The methodology is applied to characterize ISFETs fabricated in the Institute of Electron Technology (IET).

Keywords—ISFET, CMOS, electrical measurements, I-V characteristics, characterization, parameters extraction.

1. Introduction

Ion-sensitive MOS transistors (ISFETs) operate as depletion-mode devices. Their electrical characterization must combine techniques typical for CMOS evaluation and those necessary for description of mechanisms specific to depletion-mode MOS transistors. In the electrical characterization of these devices it must be taken into account, that there are no gates in the functional devices. Thus the characterization must be done using first of all the ISFET-like MOS transistors with gates. The functional ISFETs are also tested and evaluated. The paper reports methods and selected results of electrical characterization of these devices.

2. Devices

Fabrication of ISFETs is partially based on the standard CMOS process. Device parameters are given in Table 1, whereas their structure is shown in Fig. 1. Also the topology of an ISFET-like MOSFET is shown in Fig. 2. The specific features of ISFET structure are as follows:

Table 1
Ion-sensitive MOS transistor parameters

Parameters	Values
Total area	4.9×4.9 mm^2
Channel width (W)	600 μm
Channel length (L)	16 μm
Gate oxide thickness (T_{SiO_2})	65 nm
Silicon nitride thickness ($T_{Si_3N_4}$)	65 nm
p-well junction depth ($X_{J\text{-}well}$)	6 μm
Source/drain junction depth ($X_{J\text{-}S/D}$)	1.5 μm

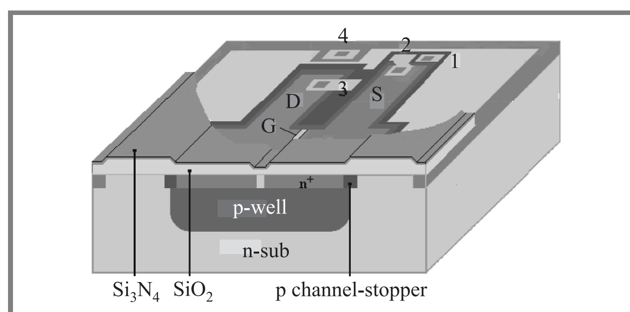

Fig. 1. Cross-section of a p-well ISFET; numbers denote the electrodes: p-well (1), source (2), drain (3), substrate (4).

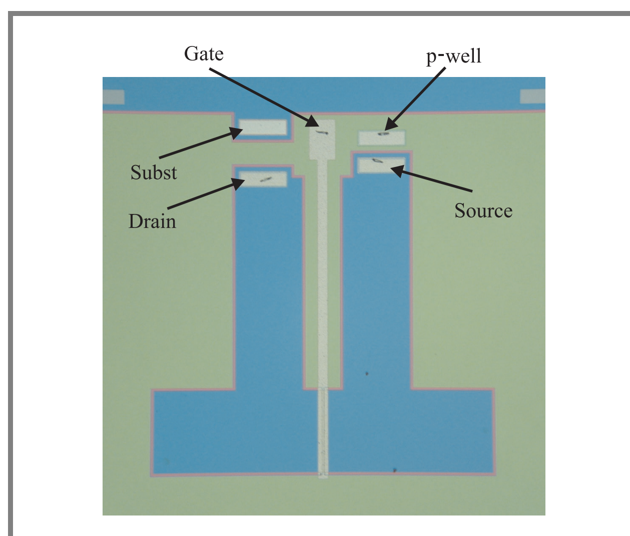

Fig. 2. A photo of an ISFET-like MOSFET. An Al-gate covers the active area of the device. The electrodes are seen clearly.

– p-well insulation of active areas (relevant mainly in the case of ISFET arrays); such insulation is necessary for ISFETs to operate in a typical application, that is as a source and drain follower [1, 2];

– long source/drain leads designed for the purpose of sufficient separation between the pads and the active area exposed to the solution-under-test; the separation is particularly necessary in the case of front-side contacted ISFETs; this obviously results in increased S/D series resistance.

3. Measurements

A Keithley System 93 IV controlled by METRICS software is used for electrical characterization of ISFETs and ISFET-like MOSFETs. In the case of wafer-scale measurements this system works concurrently with a semi-automatic probe station. The system is used for the following tests:

- measurements of *I-V* characteristics of ISFET-like MOSFETs;
- evaluation of ISFETs on a semi-automatic probe station;
- investigation of the insulation between ISFETs arranged as arrays of devices fabricated in the same substrate;
- measurements of *I-V* characteristics of ISFETs exposed to pH-solutions.

Selected measurement (subthreshold *I-V* characteristics of the ISFET-like devices and measurements of dark currents of the p-n junctions) are performed using a shielding box.

3.1. Measurement and characterization of ISFET-like MOSFETs

A measurement setup typical for MOSFET characterization is used (Fig. 3). Below, characterization procedures are described in more detail.

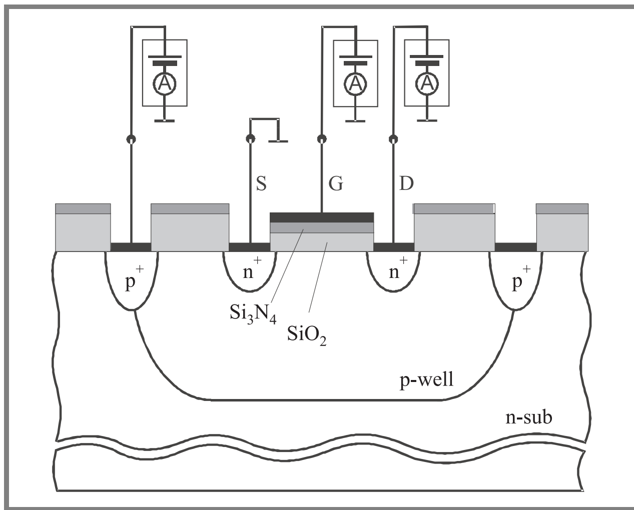

Fig. 3. Measurement setup used for characterization of ISFET-like MOSFETs.

3.1.1. Overall evaluation of electrical characteristics of the MOSFETs based on the *I-V* data

This procedure is based on the simple model of MOSFETs *I-V* characteristics, given by Eq. (1), where the symbols have their standard meanings:

$$I_D = \frac{W}{L_{eff}} \mu_{eff} C_I \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} . \qquad (1)$$

It should be mentioned that oxide capacitance C_{OX}, used commonly in models of MOSFET *I-V* characteristics, has been replaced by insulator capacitance C_I. This is due to the fact that the dielectric layer in ISFETs consists of oxide and nitride layers (see Fig. 1).

3.1.2. Extraction of basic parameters of MOSFETs

Transconductance coefficient $KP = \mu_{eff} C_I$, threshold voltage at $V_{BS} = 0$ V VTO, body factor $GAMMA$ and Fermi voltage PHI are evaluated through analysis of $I_D(V_{GS})$ data measured at constant V_{DS} voltage and a set of V_{BS} values. First, $I_D(V_{GS})$ data is differentiated to obtain $G_m(V_{GS})$ curves. Next, $I_D(V_{GS})$ and $G_m(V_{GS})$ data is used to extract KP and threshold voltage V_T. Threshold voltage corresponds to an abscissa of intersection point between a tangent line of the $I_D(V_{GS})$ curve and the V_{GS} axis. A position of the tangent line is determined by the coordinate of this $G_m(V_{GS})$ curve maximum. This method is illustrated in Fig. 4. It should be mentioned, that in the case

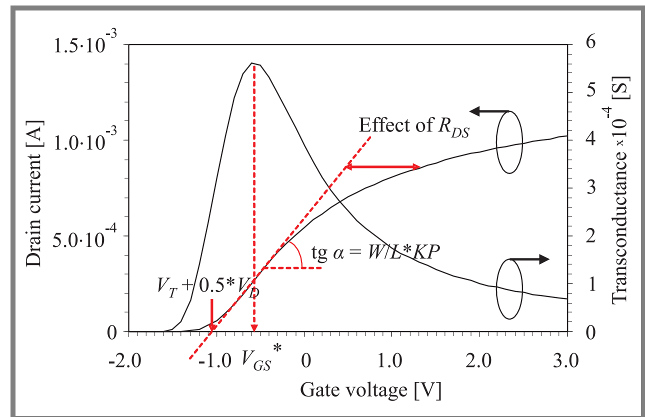

Fig. 4. Extraction of threshold voltage and transconductance coefficient ($V_D = 0.5$ V, $V_B = 0$ V).

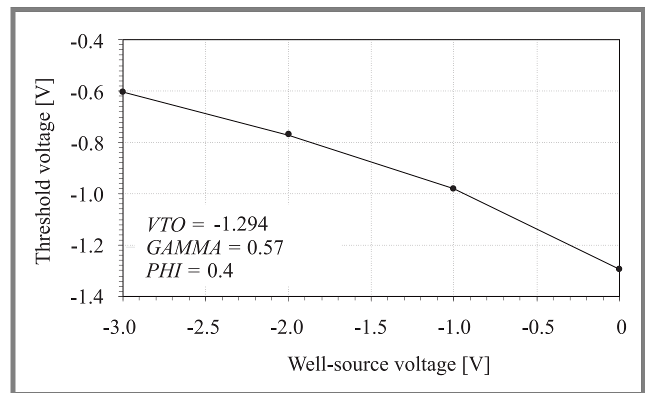

Fig. 5. Extraction of threshold voltage parameters ($V_{DS} = 0.5$ V).

of ISFETs a significant $I_D(V_{GS})$ degradation range can be observed in strong inversion. This is due to series resistance (from the devices topology), rather than mobility degradation. Both effects have a similar influence on the $I_D(V_{GS})$ data. Next, the calculated $V_T = f(V_{BS})$ characteristics are used to evaluate VTO, $GAMMA$ and PHI.

For this purpose a well-known square-root formula given by Eq. (2) is used:

$$V_T = VTO + GAMMA\left(\sqrt{PHI - V_{BS}} - \sqrt{PHI}\right). \qquad (2)$$

Figure 5 illustrates the methods used for extraction of these parameters.

3.1.3. Extraction of the weak inversion parameters of MOSFETs: *S*, *NFS*

This method is based on the MOSFET model of *I-V* characteristics in the subthreshold range presented in [3]:

$$I_D = I_{D,ON}\exp\left(\frac{V_{GS}-V_{ON}}{n\frac{kT}{q}}\right) = I_{D,ON}\exp\left(\frac{V_{GS}-V_{ON}}{S/\ln 10}\right), \qquad (3)$$

where:

$$S = n\frac{kT}{q}\cdot\ln 10\,,$$

$$n = 1 + \frac{q\cdot NFS + C_D}{C_I}\,,$$

$$C_D = \frac{\varepsilon_{Si}}{W_D} = \frac{GAMMA\cdot C_I}{2\cdot\sqrt{PHI - V_{BS}}}\,.$$

The capacitance C_D is understood here as the capacitance per unit area of the gate-induced depletion region at the onset of strong inversion. The *NFS* parameter denotes the density of fast surface states at the insulator-silicon interface. The capacitance of the interface traps degrades the slope of the $I_D(V_{GS})$ curve *S*, which is reflected in the non-ideality factor *n* [3]. Other parameters have standard meanings. The estimation procedure is illustrated in Fig. 6.

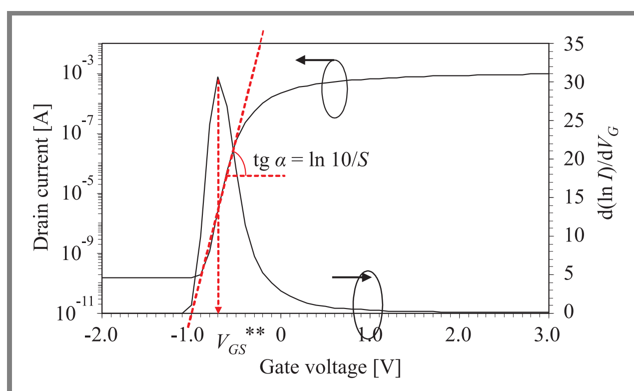

Fig. 6. Extraction of the subthreshold slope ($V_D = 0.5$ V, $V_B = -3$ V).

First, $\ln I_D(V_{GS})$ data is differentiated and a sharp peak is found. The coordinate of this peak determines a position of the subthreshold slope.

3.1.4. Estimation of ISFET current in the off-state, evaluation of the insulation between devices

As mentioned earlier, ISFETs operate as depletion-mode devices. However, for the purpose of characterization it is also necessary to evaluate the true dark current of S/D junctions. This test is performed by measurement of $I_D(V_{DS})$ characteristics for a set of negative gate voltages. The characteristics are measured both in the reverse and forward bias range. The junction dark current under reverse bias can be determined by measurement at the gate voltages below –1 V. Then the channel leakage current is switched off. Under these conditions *I-V* characteristics of the forward biased drain junction may be observed, too. The measurement results are shown in Fig. 7.

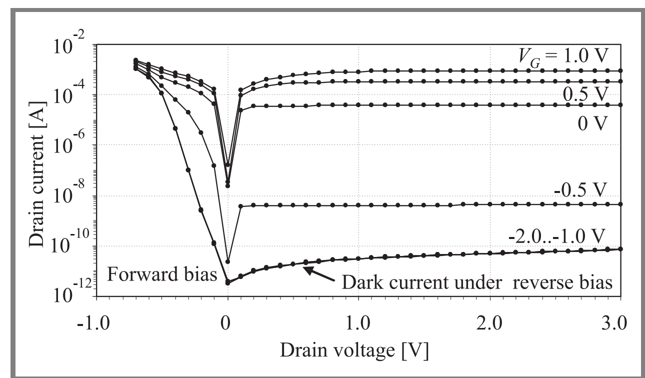

Fig. 7. Extraction of the dark current of the drain-well junction.

Perfect insulation between ISFETs is a very important requirement for their application in ISFET matrices. The devices operate independently, therefore any interaction, resulting, e.g., from a high well-substrate leakage and/or poor encapsulation, leads to degradation of the matrix functionality. The dark currents of adjacent devices have been measured in two configurations: separately and simultaneously. The results indicate that there is no interaction between the devices. The p-well insulation used in the presented technology is satisfactory.

3.2. Evaluation of ISFETs on a semi-automatic probe station

A semi-automatic measurement system is used in order to evaluate the fabricated ISFETs and to determine whether the measured parameter values are uniform over the wafer area. The measurements require multiplexing, therefore a Keithley 707A/7072 switching matrix is also used. The following parameters are measured:

- current of the forward-biased drain-well n^+-p junction;
- current of the reverse-biased drain-well n^+-p junction;
- source-drain current/source-drain resistance.

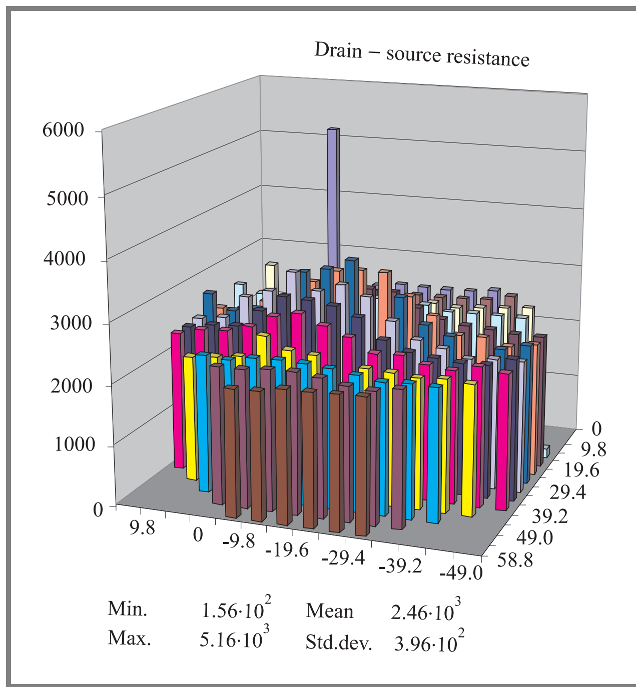

Fig. 8. On-wafer distribution of channel resistance of ISFETs in the on-state.

Post-processing of the measured data is done automatically including filtering, statistical processing (calculation of mean value, standard deviation, frequency) and smoothing. The output data is presented as discrete contour maps and bar charts. Figure 8 illustrates this set of measurements. The result show a satisfactory process uniformity.

3.3. Characterization of ISFETs exposed to pH-solutions

These measurements complete ISFET characterization. Operation of ISFETs with different p-well doping densities has been tested. Three calibrated buffer solutions with pH = 4.0, 6.694, and 8.358 have been used. The measurement setup configuration is shown in Fig. 9.

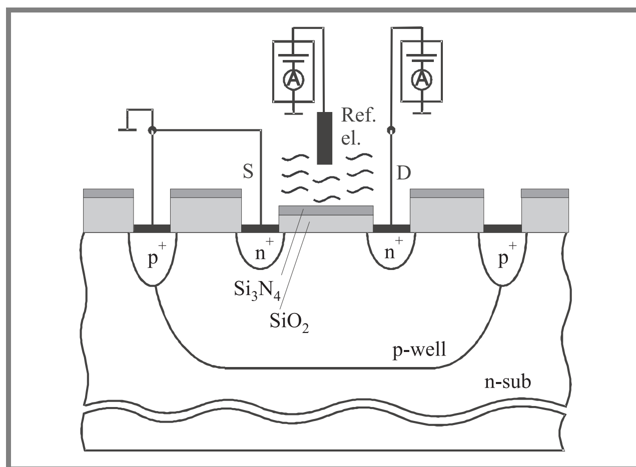

Fig. 9. Measurement setup for testing ISFETs exposed to pH-solution.

Characteristics $I_D(V_{GS})$ have been measured and threshold voltages have been calculated using the transconductance data. In accordance with the theory the experimental results show linear V_T(pH) dependence with sensitivities of the order of 50 mV/pH (Fig. 10). The increase of sensitivity

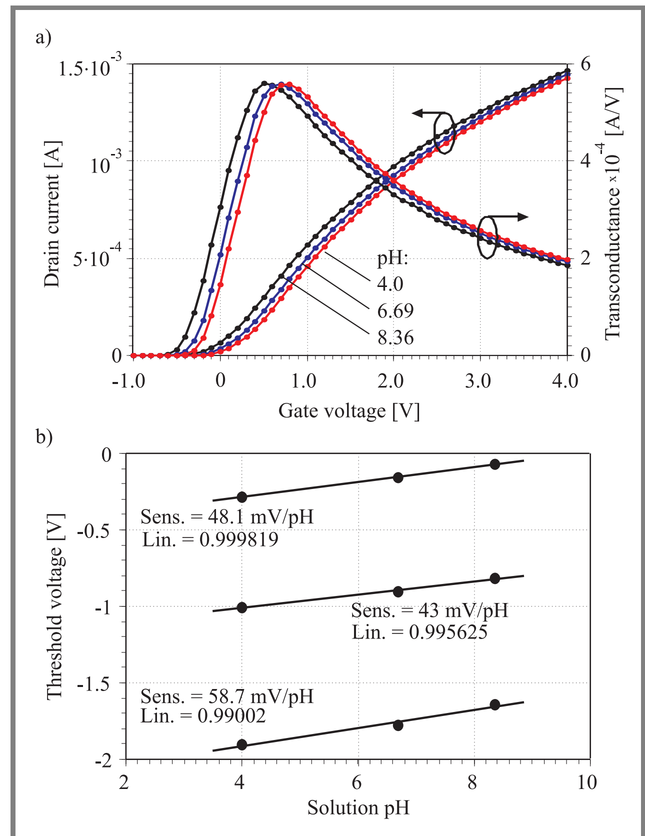

Fig. 10. Influence of pH on ISFETs characteristics: (a) a shift of the $I_D(V_{GS})$ and $G_m(V_{GS})$ characteristics; (b) a resulting ISFET-like MOSFETs threshold voltage variation due to the pH change.

of sample with DHF (diluted HF) dip up to 58.7 mV/pH results from a native oxide removal. Moreover, it has been determined, that the subthreshold slope of ISFETs increases for increasing pH values. In the case of these devices it has changed between 115 and 130 mV/dec.

4. Summary

A methodology of electrical characterization of ISFETs has been presented. It is based on a concept of CMOS characterization system. The presented measurement and parameters extraction methods have been used for evaluation of the devices manufactured in the Institute of Electron Technology.

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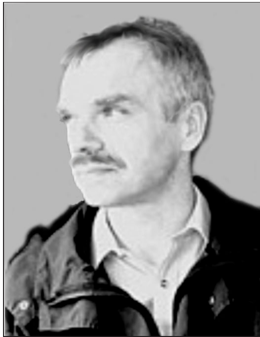

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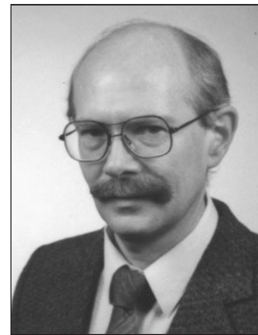

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