Paper

Arbitrary waveform generator for charge-pumping

Marcin Iwanowicz, Zbigniew Pióro, Lidia Łukasiak, and Andrzej Jakubowski

Abstract—The paper presents a new signal generator for charge-pumping. Modular structure of the generator is discussed with special emphasis on signal-generation module consisting of five independent signal channels. Digital signal synthesis is chosen to minimize inaccuracies. Noise analysis is performed to demonstrate the validity of the design of signal channel. Calibration procedure is also discussed.

Keywords— arbitrary waveform generator, calibration, charge-pumping, digital synthesis, noise.

1. Introduction

A new signal generator for charge-pumping (CP) is presented. Charge-pumping is one of the most versatile methods to estimate the quality of the Si-SiO_2 interface of MOS structures. It enables determination of such parameters as: average density of interface traps, energy distribution of interface traps and capture cross-sections, distribution of interface traps along the channel, rough estimation of flat-band and threshold voltages. New generations of MOS structures impose new requirements on CP measurements. For example, due to reduced gate-oxide thickness, gate-voltage amplitude has to be lower, thus voltage resolution becomes of importance.

2. Charge-pumping

Charge-pumping is widely used to characterize interface traps in MOS devices. It consists in measuring substrate DC current induced by repeated switching of a MOS transistor between strong inversion and accumulation as shown in Fig. 1. The main component of the measurement set-up is signal generator. The main task of this generator is to provide gate pulses that switch the investigated structure between accumulation and strong inversion, but also to generate appropriate bias voltages for the source and drain, and possibly for the back gate of silicon-on-insulator (SOI) devices. The density of interface traps is described as [1]:

$$D_{it} = \frac{I_{cp}}{qAf\Delta E}, \qquad (1)$$

where: I_{cp} – measured charge-pumping current, q – elementary charge, A – gate area, f – gate signal frequency, ΔE – energy range of traps participating in charge-pumping.

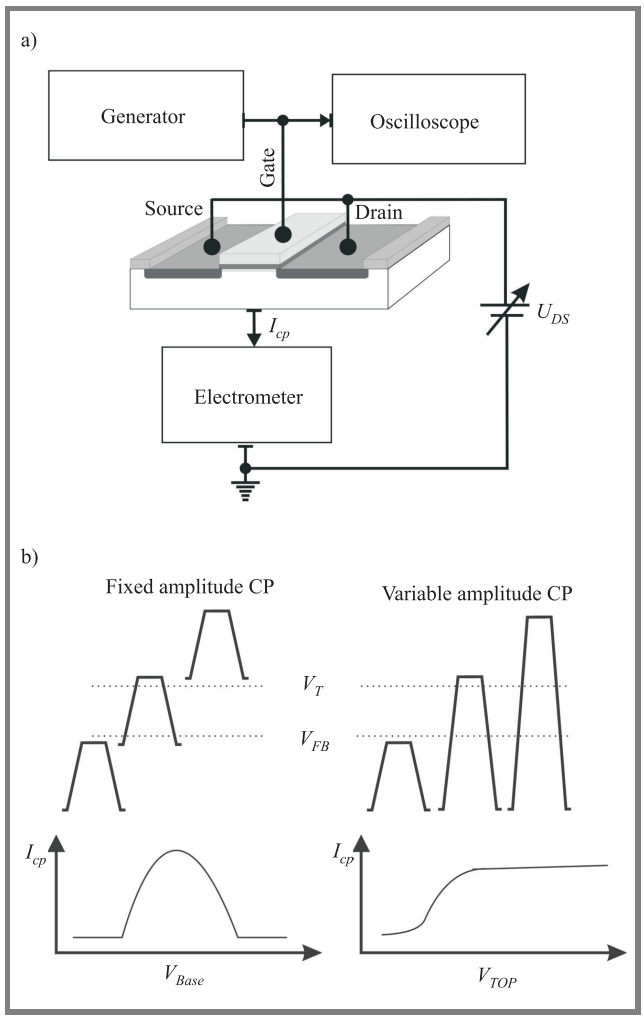

Fig. 1. The principle of charge-pumping: (a) measurement setup, (b) charge-pumping current versus base voltage [11].

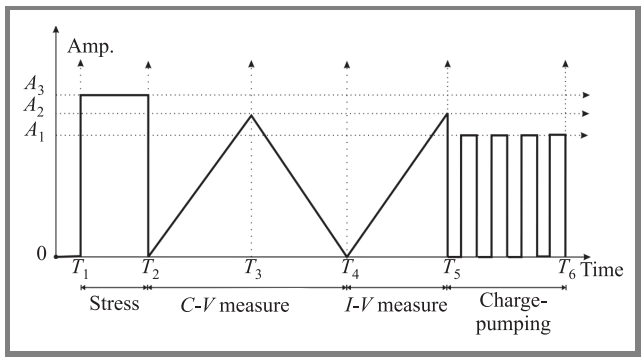

Fig. 2. Waveform of the applied voltage versus time for a "stress and sense" measurement [11].

Many different versions of charge-pumping method have been developed, such as [1, 2]:

- two-level method (square pulses) with constant amplitude, gate-voltage base level or top level;
- two-level method (trapezoidal pulses) with variable rising/falling time;
- two-level method (symmetrical or non-symmetrical triangular pulses) with variable frequency;
- three-level method (square pulses with additional middle level) with variable pulse duration;
- and "stress and sense", composition (see Fig. 2) charge-pumping and other methods (*C-V*, *I-V*) with pulse stress [11].

3. Generator parameters

The available generators have usually high output noise (up to 70 mV_{pp}) [3]. The obtained measurement results are therefore averaged over several kT/q, which may shade the details of the shape of the measured quantity. This undesirable effect may be further intensified by low resolution and very low precision.
The generator must provide several synchronous multiphase voltage signals. In the case of a typical SOI structure at least four channels are necessary: two for independent biasing of source and drain and two for front and back gate. A fifth channel is added for future applications. The electrical parameters of the generator should be suitable for measurement of modern semiconductor devices with small geometry and thin gate dielectric. It should be remembered, though, that the final values of these parameters are, to a large extent, determined by electronic components used to build the generator (DAC, FPGA, etc.). The parameters of the presented generator are shown in Table 1.

Table 1
Basic parameters of the generator

Parameters	Values
Number of channels	5
Maximum rising/falling rate of the output voltage	10^8 V/s (100 V/1 μs)
Output voltage range	$\pm$5 V_{pp} (into 50 Ω) $\pm$10 V_{pp} (into open circuit)
Phase duration	min –50 ns max –20 s
Triggering	internal and external
Trigger pulses for other equipment	2 per channel
Voltage resolution	0.15 mV (into 50 Ω) 0.30 mV (into open circuit)
Resolution of phase duration	5 ns
Noise (with 50 Ω load)	$\pm$1 mV_{RMS}

4. Arbitrary waveform generator (AWG)

In the vast majority of cases charge-pumping does not require truly arbitrary signals but vector ones [4]. Limiting the generator to this class of signals results in considerable simplification of the design and enables digital synthesis to be used to shape the output signal.
The generator consists of three modules: main module, power module and signal-generation module (5 channels), see Fig. 3 [4]. They have been defined to ensure the highest possible autonomy of each module. In this way the amount of data exchanged between modules is minimized.

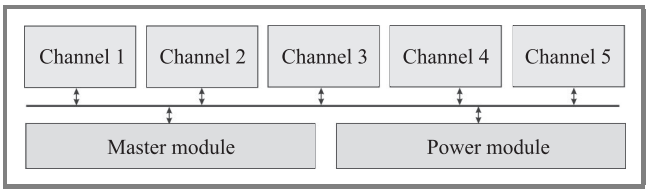

Fig. 3. Diagram of signal generator.

The task of the main module is to ensure communication between the channels of the signal-generation module and the outside world (usually a PC). Moreover, the module checks and updates the status of each channel of the signal-generation module. The role of the power module is obvious. It provides the supply bias necessary for the operation of the whole device. The signal-generation module (5 channels) is the most important module of the generator as it produces the desired signals necessary for characterization of semiconductor devices. Each channel is in the form of EURO CARD 3U.

4.1. Main module

The main module programs/controls all signal channels as well as provides communication between the generator and external computer. The module reads the status of each signal channel and sends this information to the computer. It also reads the information on signal parameters from the computer and sends it to the appropriate signal channel. The generator is seen by the computer as a USB mass-storage device.

4.2. Power module

The power module provides supply bias necessary for correct operation of the whole generator. It protects the generator from overvoltage and monitors the supply bias. In the case of inappropriate supply bias the module may turn the generator off to avoid damage.

4.3. Signal-generation module

As it was mentioned before, the signal-generation module consists of 5 independent signal channels. A channel consists of (Fig. 4.):

- synthesis block (FPGA structure);
- analog block;
- control block with SiLabs C8051F064 microcontroller;
- calibration circuit with two analog-to-digital converters (ADC) integrated in the microcontroller.

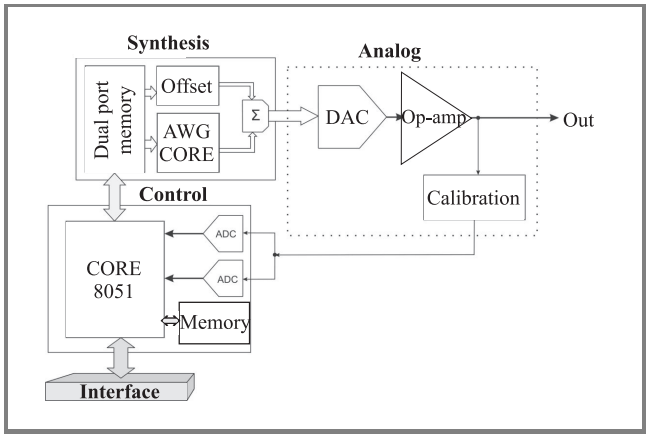

Fig. 4. Block diagram of the signal channel.

4.3.1. Synthesis block

As it was mentioned before, the class of the generated signals was narrowed to vector signals. Therefore each phase of the generated signal may be described with three parameters, i.e., offset, duration and slope (in the case of constant voltage the slope is zero).

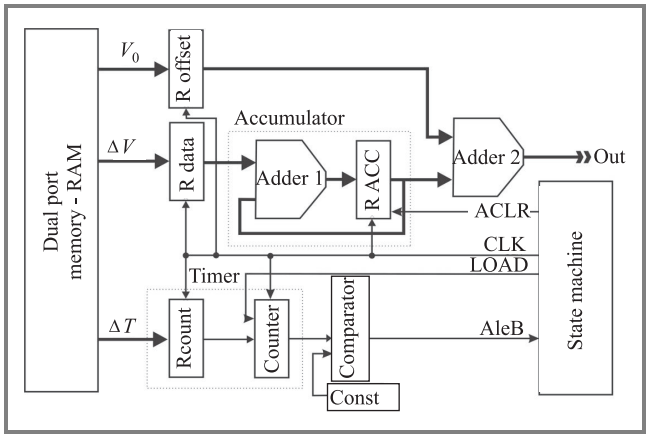

Fig. 5. Diagram of the synthesis block.

Signal synthesis is performed using two components: an accumulator and a timer (Fig. 5). Synthesis of a ramp phase of the pulse consists in adding an appropriate voltage increment ΔV to the accumulator every elementary time increment ΔT (period of CLK clock) until the timer signals the end of the phase. In the case of a constant voltage the value contained in the accumulator does not change [4]. The signal may be additionally modified by an offset voltage V_0. To ensure smooth transition between signal phases, the control block starts preparation of the next phase a certain period of time (9 clock periods) before the current phase is completed. This is achieved by means of comparing the time measured by the timer with the phase duration as shown in Fig. 5. The accumulator data is 32-bit long with the upper 16 bits representing the integer part of the voltage to be obtained and the lower 16 bits representing the fractional part. Only the upper 16 bits are connected to the digital-to-analog converter (DAC) input, therefore the errors associated with addition do not exceed 1LSB.
The input data for the offset, accumulator and timer (V_0, ΔV and ΔT in Fig. 5) are held in a dual-port RAM (Fig. 6). The memory receives data describing the signal

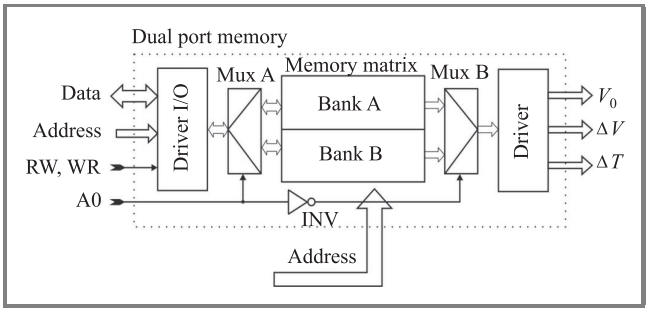

Fig. 6. Diagram of dual-port static RAM.

to be generated from external circuits and provides this data to the signal-synthesis block. Due to the fact that the memory is equipped with two ports, the accumulator and timer may read the data while the parameters of the new signal shape are written to the memory. The synthesis block was designed and implemented in a CYCLONE FPGA from Altera.

4.3.2. Analog block

The analog block consists of a DAC (with all components necessary to ensure its proper operation) and two operational amplifiers Op1 and Op2 (Fig. 7). The first is operating as a differential amplifier (with gain $G_1 = 2$). The second op-amp is an amplifier output buffer ($G_2 = 5$).
The noise at the output of the DAC results from arithmetic errors (mentioned in the description of the synthesis block), non-linearity, temperature drift and quantization errors. To calculate the total noise at the output of the analog block the noise of both operational amplifiers has to be taken into account. For this purpose we assume that the clock frequency is 200 MHz and bandwidth is 30 MHz.
The RMS noise V_{NA} of the DAC (MAX 5888) resulting form arithmetic errors is 35 μV_{RMS} (1 LSB). Its non-

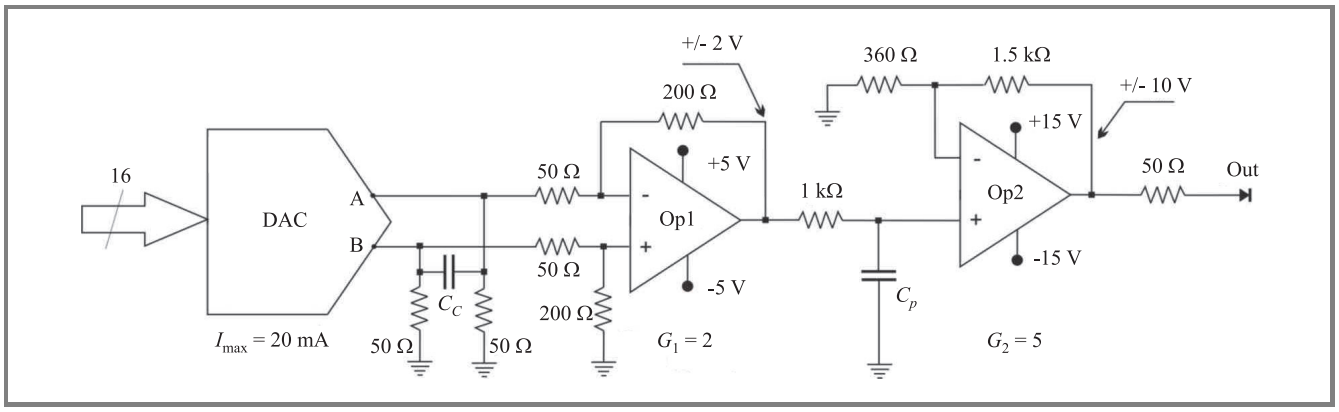

Fig. 7. Circuit diagram of analog block.

linearity V_{NNL} is ±0.003% FS (i.e., ±2 LSB) [5], thus the quantization noise may be estimated as 50 μV_{RMS} (2 LSB). The total RMS noise at the DAC output is therefore:

$$V_{NDAC} = \sqrt{V_{NA}^2 + V_{NNL}^2} = 61\ \mu V_{RMS}\,. \tag{2}$$

To continue noise analysis the circuit illustrated in Fig. 7 should be transformed as shown in Fig. 8. The input components of noise density calculated based on Fig. 8 are listed in Table 2.

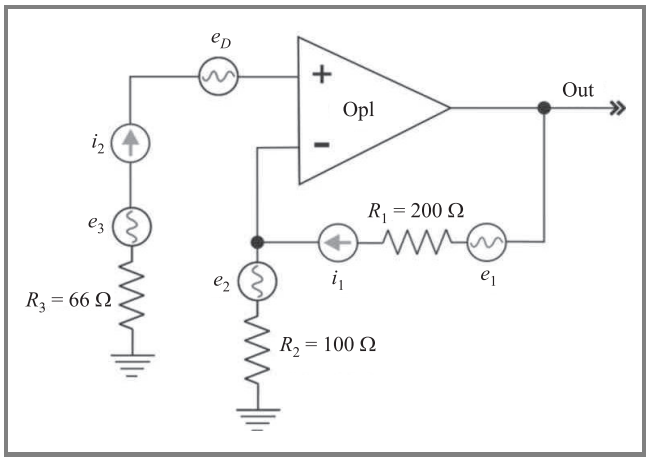

Fig. 8. Analysis of the noise generated by the operational amplifier Op1.

To calculate voltage components of noise density associated with e_1, e_2 and e_3 the widely-known formula was used [6]:

$$V_{Ni} = \sqrt{4kTR_iB}, \tag{3}$$

where: k – the Boltzmann constant, T – absolute temperature [K], R_i – resistance, B – bandwidth [Hz].

It is assumed that current components of noise density associated with i_1 and i_2 are 1 pa/$\sqrt{\text{Hz}}$ [7] and the voltage component of noise density associated with e_D is 5.2 nV/$\sqrt{\text{Hz}}$ [8]. The noise density components identified in Fig. 8 are listed in Table 2.

Table 2
Noise density components
($T = 20°C$, $B = 30$ MHz, $G_{Op1} = 2$)

Input component of noise voltage/current	Noise density before amplification	Gain factor of input components of noise density	Noise density at output [nV/$\sqrt{\text{Hz}}$]
$e_D = \text{Op1}_{NOISE}$	5.2 nV/$\sqrt{\text{Hz}}$	$G = 2$	10.4
e_3	1.2 nV/$\sqrt{\text{Hz}}$	$G = 2$	2.4
e_2	1.4 nV/$\sqrt{\text{Hz}}$	$G-1 = 1$	1.4
e_1	2 nV/$\sqrt{\text{Hz}}$	1	2
i_1	1 pA/$\sqrt{\text{Hz}}$	R_1	0.20
i_2	1 pA/$\sqrt{\text{Hz}}$	$R_3 \cdot G$	~0
Σ			16.4

The total noise density SND_{Op1} at the output of Op1 is 16.4 nV/$\sqrt{\text{Hz}}$ and the total RMS noise is

$$V_{NOp1} = SND_{Op1}\sqrt{B} = 90.18\ \mu V_{RMS}\,. \tag{4}$$

At the output of amplifier Op2 ($G_{Op2} = 5$) one obtains:

$$V_{NOp2} = V_{NOp1}\,G_{Op2} = 450\ \mu V_{RMS}\,. \tag{5}$$

The total noise of the analog block is therefore:

$$V_{Ntotal} = \sqrt{V_{NOp2}^2 + V_{NDAC}^2} = \sqrt{(450)^2 + (61)^2} \approx 455\ \mu V_{RMS}\,. \tag{6}$$

As a result of a 16-bit DAC and appropriate arithmetic the "digital" noise is totally negligible in comparison with the noise generated by the analog part of the block. Since RMS noise at the output of signal generator is ~455 μV_{RMS} we may assume that the accuracy of the generated signal is ±1 mV.

4.3.3. Control block

The control block is based on SiLabs C8051F064 microcontroller equipped with two 16-bit analog-to-digital converters that are used for calibration and on-line correction of the signal. The main task of this block is to provide communication with the main module in the SCPI standard (over internal RS-232 interface).
Moreover, the control block is responsible for preparation of the necessary data for the signal-synthesis block. The parameters of the generated signal are calculated based on the data received from the main module and calibration table and then written to the dual-port RAM implemented in FPGA.

4.3.4. Calibration block

Temperature drifts of the MAX5888 16-bit DAC used in the analog block are quite substantial (offset drift: ±50 ppm/°C, gain drift: ±50 ppm/°C). This means that the accuracy of the generated signal will be less than 14 bits if the temperature changes even by 1°C. If we assume that

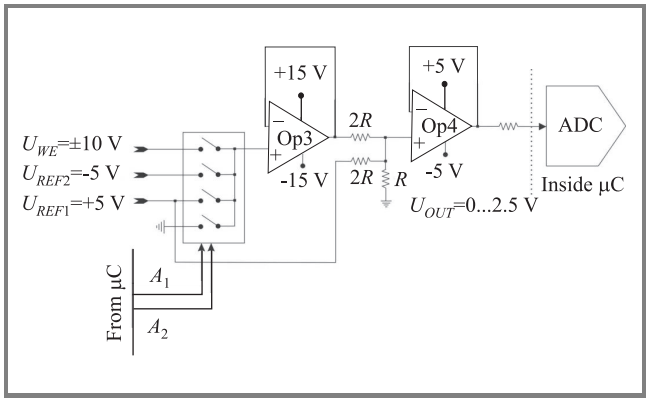

Fig. 9. Circuit diagram of the calibration block.

the output voltage range is 10 V (±5 V) and the accuracy of the generated output voltage is to be ±1 mV, 15-bit resolution is required (total error at the level of 30 ppm). Such parameters may be obtained if at least 16-bit ADC is used for calibration.
The calibration block consists of:

- two 16-bit unipolar analog-to-digital converters integrated in the C8051F064 microcontroller of SiLabs [9];
- precision voltage reference ±5 V VRE405 of THALER CORPORATION with the total thermal drift < 3 ppm/°C [10];
- multiplexer (controlled by the microcontroller) with inputs connected to +5 V reference voltage, −5 V reference voltage, ground and signal taken directly from the generator output (see Fig. 9.);
- voltage-level converter from ±5 V to 0/2.5 V, according to Fig. 9.

Calibration consists of three processes:

Autocalibration – the self-calibration of the calibration block – the inputs of the ADC are successively connected to the minimum and maximum voltage (from reference) and calibration coefficients A_1 and B_1 (see Fig. 10) are calculated based on the obtained results:

$$A_i = \frac{Y_1 - Y_2}{X_1 - X_2}, \tag{7}$$

$$B_i = Y_2 - \frac{(Y_1 - Y_2)X_2}{X_1 - X_2}, \tag{8}$$

where: X_1, X_2 – digital representation of the minimum and maximum voltage (0000h i FFFFh), Y_1, Y_2 – results of conversion. This procedure is performed every time the generator is switched on.

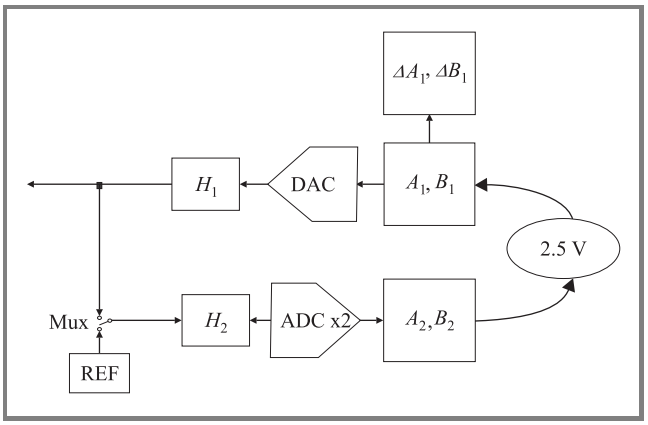

Fig. 10. Diagram of calibration.

Calibration of the analog block – two digital representations corresponding to the extreme values of the voltage range are written to the DAC inputs. The obtained voltages are then measured by the ADC. Calibration coefficients A_2, B_2 (see Fig. 10) are determined as in the previous case with X_1 and X_2 being the values written to the DAC and Y_1 and Y_2 being the values read from the ADC. This routine is performed every time correction indicates the error exceeding a selected threshold (ΔA_1, ΔB_1, see Fig. 10). The generator must be warm and the measurement set-up fixed.

Correction – in-flight calculation of corrections to calibration coefficients. This stage is necessary due to ambient changes (temperature, humidity, etc.). Calibration coefficients are calculated again, the difference being that the digital representations fed to the inputs of the DAC are now the levels of the currently generated signal, not extreme values. One ADC cannot measure two levels of the output voltage because its sampling and conversion time is too long. Therefore, correction is performed by two ADC's. The routine is triggered at user's request at selected levels of the generated signal. If the difference between the previous and current calibration coefficient exceeds an admissible threshold, calibration procedure should be performed.

5. Summary

Progress in the area of semiconductor devices requires measurements with ever smaller voltage amplitudes, therefore digital synthesis is the best way to design a signal generator. Even though a digital generator yields a starcase signal, it is not necessarily worse than a fully analog generator. This is because the quantization noise is almost an order of magnitude lower that the thermal Johnson noise introduced by the components used to build the analog block. Digital synthesis allows the analog block (the biggest source of noise) to be minimized, therefore generators with digital synthesis are pushing analog generators out of the market.

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Marcin Iwanowicz was born in Białystok, Poland, in 1979. He received the B.Sc. and M.Sc. degrees in electronics in 2003 and 2005, respectively, both from the Faculty of Electronics and Information Technology of Warsaw University of Technology (WUT). He is currently working toward the Ph.D. degree at the Institute of Microelectronics and Optoelectronics, WUT. His research interests include characterization of semiconductor devices and design of advanced measurement equipment.
e-mail: M.Iwanowicz@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

Zbigniew Pióro was born in Nadkole, Poland, in 1948. He received the M.Sc. and Ph.D. degrees from Warsaw University of Technology (WUT) in 1971 and 1975, respectively, both in microelectronics. He joined the Institute of Microelectronics and Optoelectronics of Warsaw University of Technology in 1971. In the years 1994–2001 he held the position of R&D Director of AB-micro s.c., a company involved in automation of industrial processes. His research interests include metrology, digital signal processing and microprocessor techniques.
e-mail: pioro@imio.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

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