Invited paper

Review and perspective of high-*k* dielectrics on silicon

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Abstract— The paper reviews recent work in the area of high-*k* dielectrics for application as the gate oxide in advanced MOSFETs. Following a review of relevant dielectric physics, we discuss challenges and issues relating to characterization of the dielectrics, which are compounded by electron trapping phenomena in the microsecond regime. Nearly all practical methods of preparation result in a thin interfacial layer generally of the form SiO_x or a mixed oxide between Si and the high-*k* so that the extraction of the dielectric constant is complicated and values must be qualified by error analysis. The discussion is initially focussed on HfO_2 but recognizing the propensity for crystallization of that material at modest temperatures, we discuss and review also, hafnia silicates and aluminates which have the potential for integration into a full CMOS process. The paper is concluded with a perspective on material contenders for the "end of road map" at the 22 nm node.

Keywords— high-k dielectrics, dielectric constant, interfacial layer, hafnia, aluminates, silicates.

1. Introduction

The challenges around the search for a replacement for silicon dioxide as the gate dielectric in the ubiquitous CMOS technology are well known to the community. The unique and excellent intrinsic properties of SiO_2 together with its compatibility with high temperature manufacturing process and the natural abundance of silicon, have underpinned the entire development of the $200B silicon industry. However, the relentless miniaturization or scaling of the MOS transistor and associated infrastructure on chip create the demand for ever thinner gate oxides. There is a school of thought that the rate of technology scaling is exceeding the rate at which circuit designers can fully exploit the advantages of a given technology node but the momentum behind the industry and the customer demand for ever faster processing, sets the paradigm. The well-known issue for the gate oxide then, is that it must become vanishingly thin to control adequately the electrostatics of the MOSFET channel and so win in the competition with the drain voltage encroachment, to minimise undesirable short channel effects. In fact, the International Technology Roadmap for Semiconductors (ITRS) predicts equivalent oxide thicknesses of 1 nm in 2007, reducing to 0.35 nm for the 22 nm node [1]. Notwithstanding other issues, at least three mono-layers of SiO_2 are required so that "bulk" like properties can be achieved giving a lower limit for the native oxide in any event, of about 0.7 nm [2]. Such oxide thickness reduction comes at a price as the quantum mechanical current leakage through the gate becomes prohibitively high and so therefore is the stand by power dissipation in chips containing a billion individual transistors. The gate leakage must be reduced without compromising the current drive (I_{ON}) of the transistor so materials with higher dielectric constant (k) are sought to allow a thicker oxide for the same gate capacitance, so mitigating the leakage problem.

Silicon dioxide is a hard act to follow and any contender must satisfy stringent requirements. We can summarize the requirements [3] as relating to:

- thermodynamic stability in contact with Si;
- a high enough k to warrant the cost of R&D – including a propensity to be scaled;
- band offsets for electrons and holes > 1 eV which translates to band gap energies $(E_g) > 5$ eV taking into account the inverse relationship between E_g and k;
- stability through a high temperature CMOS manufacturing process and finally, acceptable reliability and wear-out attributes.

With these constraints in mind, the periodic table reveals (perhaps not surprisingly) relatively few contenders. In the short to medium term, taking account of ITRS performance requirements, the metallic oxide HfO_2 is the main contender and its silicates and aluminates can reduce the tendency for crystallization occurring at temperatures beyond about 450°C, at the expense of a slight reduction in the k values. Looking at the requirements for the 22 nm node, contenders such as Pr, La look to be promising, while Gd, Ce and Sm oxides are also worthy of consideration in many respects.

A vast array of metrological techniques has been developed over the years for characterizing SiO_2 both in terms of very fundamental physics and also engineering perspectives. The techniques represent a self-consistent methodology for engineering highly reliable gate oxides in a mass production environment and there is considerable confidence in this technology. It soon became clear that the new dielectrics have properties that require the experimental techniques to be reexamined and recalibrated. Taking the case of HfO_2, the rapid electron trapping which gives rise to a significant threshold instability has required the establishment of high bandwidth measuring systems with data capture times of the order of microseconds or less. Turning to physical characterization, spectro-ellipsometry (SE) represents a very powerful tool for obtaining fundamental parameters and properties such as oxide thickness, dielectric

constant and band gap. Studies of the losses (complex part of the permittivity or absorption coefficient) can provide information regarding defect levels in the oxide band gap and importantly, at the band edges. The SE together with standard C-V and I-V measurements can provide powerful self-consistent, non-destructive schemes for characterizing these materials.

To address the above points, we have structured the paper as follows. In Section 2 we outline the dielectric physics that underpins the engineering of the k value and in Section 3 we discuss methodologies for accurately determining experimental k values from C-V, spectroscopic ellipsometry and complementary techniques. We present a brief overview of trapping effects in high-k materials in Section 4. Section 5 contains a review and appraisal of aluminates and silicates of hafnia that allow for higher process temperatures. Section 6 presents the case for likely materials for the 22 nm node and the paper is concluded in Section 6.

2. How to increase k – dielectric physics

Figure 1 presents a useful description of the frequency dependence of the dielectric function over a wide range of frequencies. In general, the "zero frequency" value of the dielectric constant can be seen to have two components: a "high – frequency" one, where the contribution of electronic polarization dominates and one related to the ionic

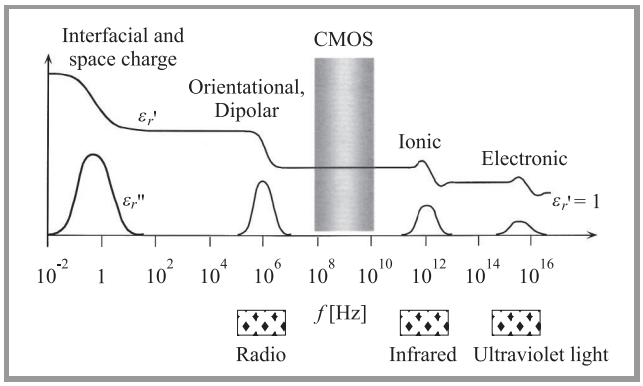

Fig. 1. The frequency dependence of the dielectric function ($\varepsilon_r = \varepsilon_r' + j\varepsilon_r''$, where ε_r' is the real part and ε_r'' – imaginary part of the complex dielectric permittivity) [4].

contribution [5]. In the CMOS frequency window, we can see that electronic and ionic processes contribute to k and we consider that the permittivity is given by the relation:

$$\varepsilon_{ox} = \varepsilon_\infty + \varepsilon_{latt}\,, \tag{1}$$

where ε_{ox} is equivalent to k.

The electronic component, which arises from simple polarization of the atoms, is the main component for SiO_2 and the simple relationship $n \sim \sqrt{\varepsilon_\infty}$ links the refractive index, readily measurable in ellipsometry, to the permittivity, giving $\varepsilon_{ox} \sim \varepsilon_\infty$. The essence of increasing k then is to choose materials that can contribute a large lattice component. Table 1 shows some values of these parameters for different crystalline forms of hafnia. We can see that ε_{latt} can vary from about 2 to over 25 depending on

Table 1
The electronic (ε_∞) and lattice (ε_{latt}) permittivity components for different crystalline forms of hafnia [5]

Crystalline phase	ε_∞	ε_{latt}	$\varepsilon_{ox}(k)$
c-HfO_2	5.37	20.80	26.17
t-HfO_2: parallel	5.13	14.87	20.00
t-HfO_2: perpendicular	5.39	27.42	32.81
m-HfO_2: yy	–	10.75	10.75
m-HfO_2: xx	–	11.70	11.70
m-HfO_2: zz	–	7.53	7.53
m-HfO_2: xz	–	1.82	1.82

the crystalline form. Without going into details of the crystallography, we can simply make the point that the permittivity can vary over a wide range depending on the form of the material and hence the method used to prepare it. Furthermore, amorphous forms are preferred for processing in any event. The variability of k with the structure of various metallic oxides is pointed out from another perspective in [6], by consideration of the Clausius-Mossotti (C-M) theory which links the k to the polarizability α, and the volume of the unit cell, V_m as described in Eq. (2):

$$\varepsilon_r = \frac{\left(1 + \frac{2}{3} 4\pi \frac{\alpha}{V_m}\right)}{1 - \frac{1}{3} 4\pi \frac{\alpha}{V_m}}\,. \tag{2}$$

In essence, larger atoms yield more polarization and hence higher k values. The C-M equation reveals that k raises steeply as the ratio α/V_m increases demonstrating the strong connection with the structure and nature of the material.

3. How to measure k – methodologies

The simplest, most convenient and appropriate way to measure k is from a C-V plot although care is required to ensure that a genuine response is obtained which usually means adjusting the data for a variety of frequency dependent parasitic phenomena such as series resistance [7], leakage current [8] and lossy interfacial capacitance [9]. Furthermore, in the case of ultra-thin gate dielectrics, the accumulation capacitance does not readily saturate to the oxide capacitance C_{ox}, because the oxide capacitance is large compared to that of the space charge in accumulation and also due to the quantization of energy levels in the accumulation layer. The difference between the measured accumulation capacitance and the true oxide capacitance must be taken into account in the extraction of capacitance equivalent thickness (CET) and the effective dielectric constant.

The Maserjian technique [10] provides a simple method to extract the oxide capacitance from a C-V plot under accumulation conditions. Computer code is available to account for accumulation layer related quantum mechanical effects and oxide leakage [11]. Having obtained a genuine accumulation and hence oxide capacitance, C_{ox} (considered here per unit area) and if no transition layer (SiO_x) is present, the permittivity can simply be obtained from the relation that $k = C_{ox} t_{ox}$, where t_{ox} has been measured from ellipsometry (see later). In practice, and usually intentionally, a so-called transitional layer (TL) is present between the substrate and the high-k layer and a two-capacitor model (with perfect, planar interfaces, i.e., no roughness) can be used to analyse the MOS structure which may be written:

$$\frac{EOT}{\varepsilon_{SiO_2}} = \frac{t_{TL}}{\varepsilon_{TL}} + \frac{t_{hi-k}}{k}, \tag{3}$$

where we extend the definition of equivalent oxide thickness (EOT) to incorporate the TL. The electronic properties of TL are dependent on the nature of its formation and it can be designated SiO_x in general where often $x = 2$ is used and the permittivity of 3.9 is then considered. However, it is important to note that x-values greater or less than 2 can arise therefore affecting the permittivity value; for instance, $x > 2$ for oxides that are heavily strained, and $x < 2$ for "unintentional" oxides that grow after an HF dip treatment. It is important therefore to understand the nature of the oxide and if possible measure its electrical and optical properties independently. We have illustrated the importance of this issue in a recent publication [12] and the main points are summarized here. We considered four samples of varying Hf stoichiometry with TLs produced by rapid thermal oxidation (RTO) and so-called chemical oxidation associated with SC1/SC2 cleaning procedures. The chemical nature of the TL plays a major role in the growth dynamics of the HfO_2 layer; it has been shown that the use of chemical oxides, which are characterized by higher OH concentration, results in almost linear growth, while obtaining a two-dimensional uniform coverage with HfO_2 [13]. The thickness of the TL was measured in situ prior to the deposition by angle resolved X-ray photoelectron spectroscopy (ARXPS), that of the hafnia layer by spectro-ellipsometry and the Hf content by Rutherford backscattering spectrometry (RBS). The SE measurements were performed in the 184–1700 nm spectral range, at three various angles of incidence (65°, 70°, and 75°) for an increased sensitivity. A simple model was used for establishing the thickness of the HfO_2 film. The model incorporated a Si substrate and a TL for which the optical properties were established on a control sample together with a Cauchy layer for describing the hafnia layer. The thickness of the hafnia layer was extracted in the spectral region where the HfO_2 layer was transparent.

The maximum capacitance was measured and the model of [12] used to extract k using four values for ε_{TL}, in the 3–4.3 range. This choice of values for the ε_{TL} has been observed in TL's in our experience and also reported in the literature. Figure 2 shows the results of the extraction and it is striking that the spread of the k-values is relatively large (10.6–19). When increasing the [Hf] concentration in the layers, the spread of results is reduced significantly from factors of ~ 7 to ~ 1. Furthermore, for the same thickness of TL and nearly the same concentration of Hf, the samples with the chemical oxide TL have significantly higher relative dielectric constant: (14–19), as compared to 12–15. These results demonstrate the sensitivity of

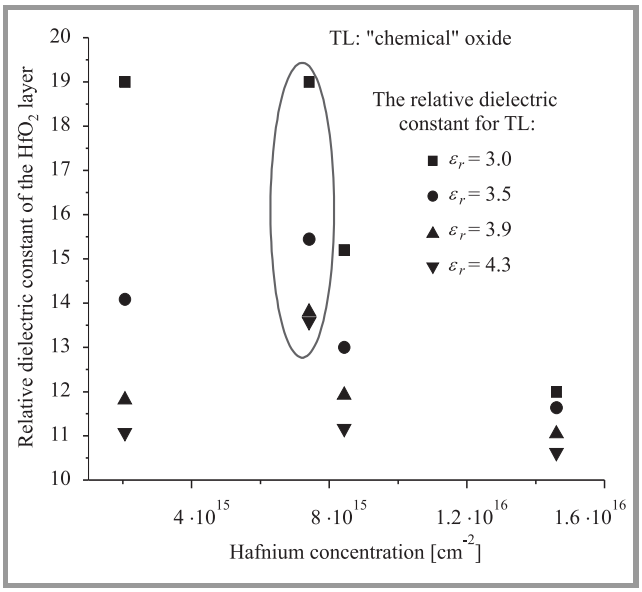

Fig. 2. Relative dielectric constant of the HfO_2 layer versus Hf content calculated for different values of relative permittivity of transitional layer [12].

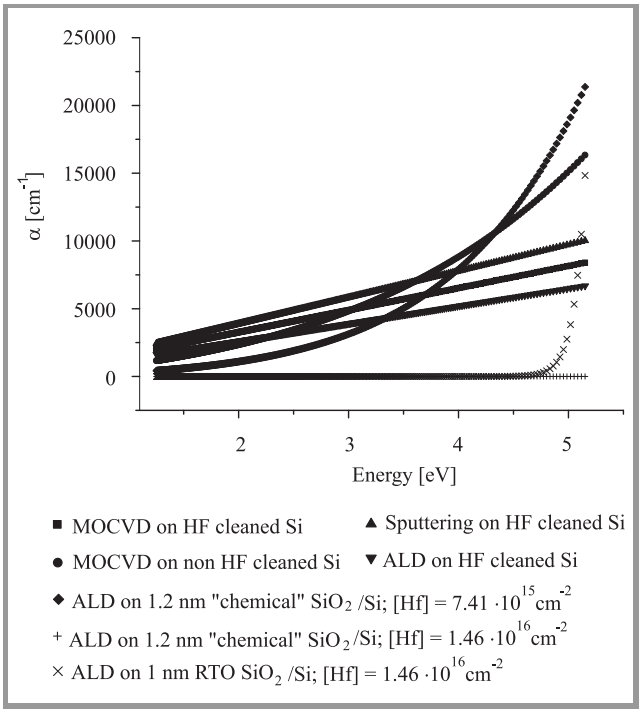

Fig. 3. The absorption coefficient α versus energy for hafnia layers prepared by different techniques [14].

the extraction technique to the TL characteristics. Clearly for low Hf density, there is doubt that the model of Eq. (3) is valid and suggests a non-uniform or mixed TL and possible poor morphology of the hafnia layer. This point was pursued in the study of [14] where the effects of pre-treatment were investigated. Figure 3 shows the absorption coefficient (α) extracted from the imaginary part of the complex permittivity, measured with SE. The best result (lowest α) is obtained with atomic layer deposition (ALD) on chemical oxide TL with ALD on RTO exhibiting a sharp increase in absorption at an energy E $\sim$ 4.7 eV. There is some evidence that such an energy level is associated with the oxygen vacancy in hafnia films [15]. The worst case is for a film on chemical oxide with sub-stoichiometric Hf. Other samples in the study incorporated HF surface preparation and inferior properties are apparent for both ALD and metal organic chemical vapour deposition (MOCVD) hafnia deposition.

We can summarise this section by reinforcing the importance of taking careful consideration of the TL when extracting k from C-V data and would advocate the use of error bars and a clear description of methodology when quoting experimental values.

4. Parasitic charges: measurement challenges

A key advantage of the SiO_2 system is the excellent electrical properties in terms of electron and hole traps. As-grown and appropriately annealed thermal oxide contains very low trap levels with relatively small capture cross-sections. As well as being virtuous for integrated circuit engineering, it has made far easier the characterization and study of the properties of these traps. Investigation of trapping in SiO_2 has been a major activity for nearly 50 years with specialist conferences (e.g., INFOS, SISC) over much of this time. It soon became apparent, when studying hafnia and other high-k dielectrics, that electron trapping in particular was extremely severe and there was a need for specialized measurement configurations to characterize the extremely fast trapping kinetics. An analogue based technique whereby the drain current is monitored across a small drain load resistance and fed to an oscilloscope is a typical set-up [16] although the technique has been refined further [17].

A study by Zhao *et al.* [18] illustrates effectively the trapping time constants and it can be seen that data capture of the order of 10's of microsecond are required to capture the full extent of the trapping, as shown in Fig. 4. Translating the time-dependence of the voltage shifts with first order trapping theory reveals for as-grown electron traps, two effective capture cross-sections of the order of 10^{-15} cm^2 with concentrations of the order of 10^{12} cm^{-2}; these being very large values relative to SiO_2. It is important to point out that such trap concentrations confined within such thin films imply very closely spaced traps – of the order of nm's which makes the use of first order trapping theory controversial. However, the values at least convey the rapid nature of the trapping and are useful for providing a representation of the time constants associated with the phenomenon.

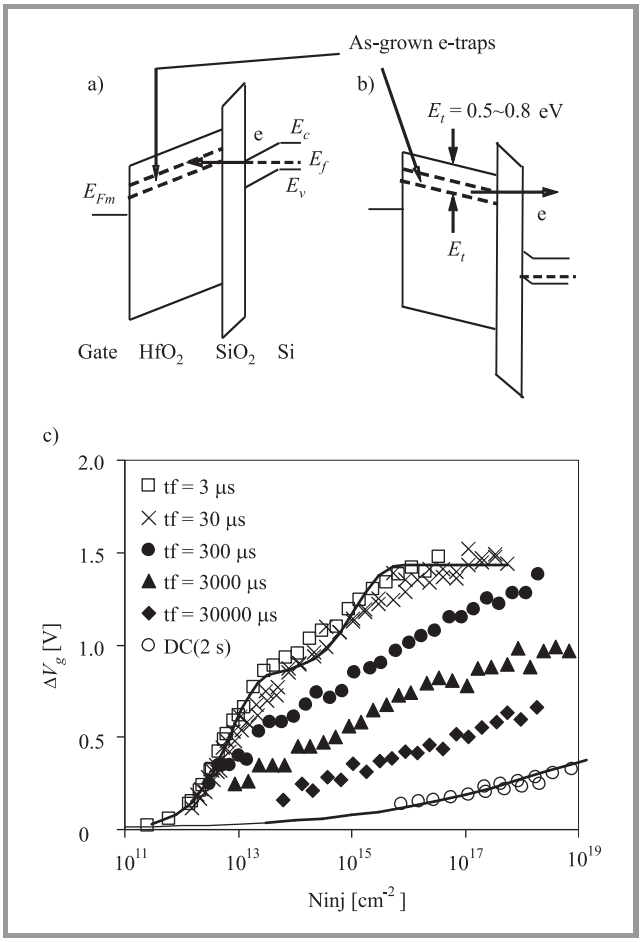

Fig. 4. Energy band diagrams of as-grown e-traps in HfO_2. (a) e trapping at $V_g > 0$ V. (b) e detrapping at $V_g < 0$ V. (c) Dynamic behavior of electron trapping measured by different techniques. The data represented by symbol "o" was measured by the traditional DC $I_d - V_g$ with V_g increasing with a step of 0.1 V for each point. The data in other symbols were obtained by the pulsed $I_d - V_g$ technique [18].

Other trapping studies show also that the films are rich in fixed positive charge with similar concentrations, as shown in Fig. 5. It is possible also to create positive charge by stressing, with similar concentrations to the as-grown ones [19]. The measurements are usually carried out on MOSTs but there is a great advantage to employing MOS capacitors due to the simplicity of the structure. Capacitor based measurements can be employed for rapid screening of new materials. We have developed a novel measurement system based on pulsing MOS capacitors [20]. Using this technique, which involves a deep-depleting voltage step, we can observe a positive

charge which would not readily be apparent from transistor based measurements which involve an inverted surface with a ready supply of minority carriers. The rapid removal of compensating electrons in the film reveals the influence of positive charge and the associated centroid induces an image charge in the substrate which is realized by a further extension of the depletion region.

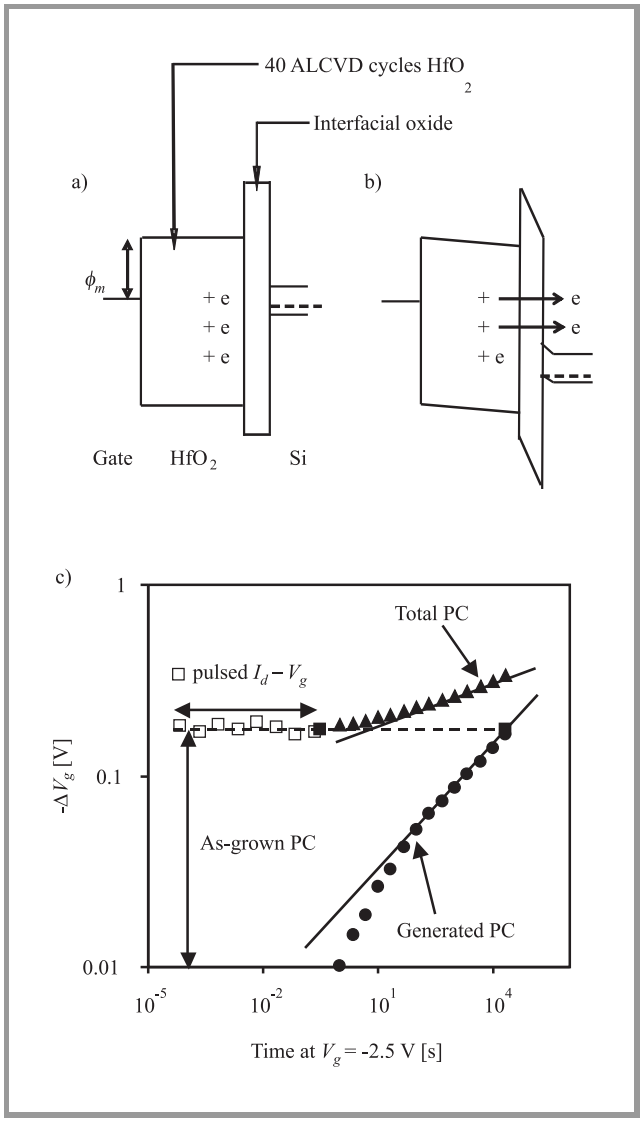

Fig. 5. A schematic illustration of the defect and physical process responsible for the ΔV_{th} of PMOSFETs. (a) Under $V_g = 0$ V, the donor-like defects are neutral. (b) Under $V_g < 0$ V, electrons tunnel away, leaving positive charges in the dielectric. (c) As-grown positive charge (PC) and generated PC. As-grown PC was measured by pulsed $I_d - V_g$ technique and generated PC was measured by traditional DC $I_d - V_g$ technique (after C. Z. Zhao *et al.*, unpublished).

This image charge then manifests itself as an extension to the depletion edge causing an undershoot in the capacitance (see Fig. 6b). The undershoot region can be further interrogated to reveal the rate at which the electrons are de-trapped; that is to say, the rate at which the positive charge is uncovered. As time progresses, the capacitance relaxes as electron-hole pairs are created in the depletion region. The oxide field also increases during the relaxation as the voltage across the depleted semiconductor is transferred to the oxide allowing tunnelling of minority

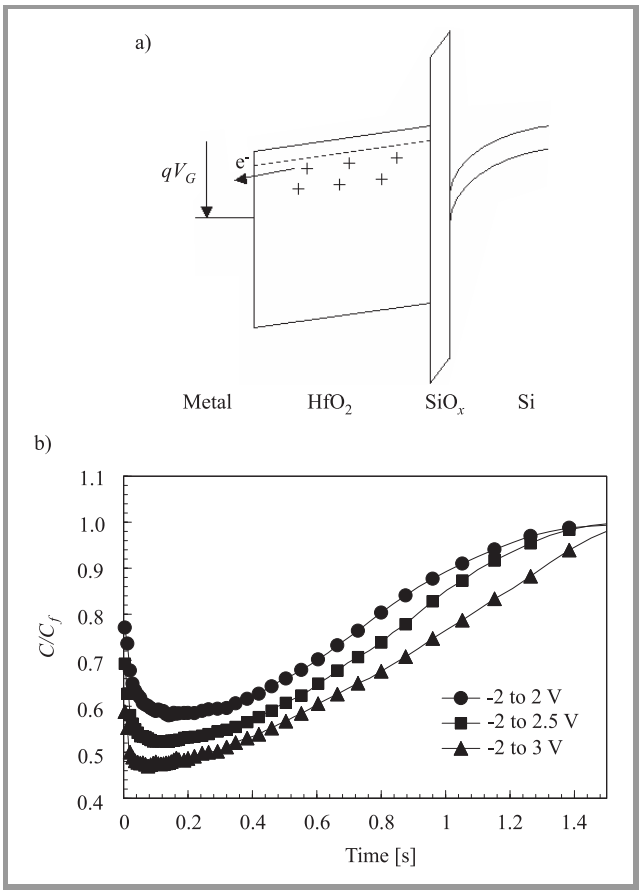

Fig. 6. (a) Energy band diagram showing positive charges are generated by electrons detrapping from pre-existed oxide defects. (b) Capacitance-transient curves of an HfO_2 sample showing undershoots [20].

carriers into the oxide and associated compensation of the positive charge. The method could be easily employed in "stress and sense" methodologies, for investigating trap creation.

5. Materials for manufacturability

Despite the advantages that HfO_2 possesses as a candidate for alternative high-k dielectric, one major problem associated with HfO_2 is the thermal instability. To minimise electrical and mass transport along grain boundaries and stabilise the interface between Si and metal oxide, it is preferable that the gate oxide remains amorphous throughout CMOS processing. Unfortunately, HfO_2 films crystallize at low temperatures of 450°C when deposited by molecular beam epitaxy (MBE) [21] to 530°C when deposited by ALD [22].

5.1. Aluminates

It has been reported that the crystalline temperature of HfO_2 can be increased by the incorporation of Al_2O_3 to form an HfAlO alloy, which will still have a relatively high dielectric constant (typically $k \sim 15$) whilst remaining amorphous up to high processing temperatures [23, 24]. It has been shown that Hf-aluminate film with 7% Al deposited by MOCVD remains amorphous up to 900°C [24]. Another group [25] also reported that Hf-aluminate film deposited by ALD can stay amorphous up to 1000°C rapid thermal anneal.

When incorporating Al_2O_3 into HfO_2, the large band gap of Al_2O_3 (~ 9 eV) also increases the band gap of the compound. Yu *et al.* [26] showed that the band gap of the HfAlO films (estimated by XPS) varies linearly from 5.25 to 6.52 eV with Al concentration from 9.6 to 33.9%. Using the spectro-ellipsometry we demonstrated that the band gap of HfAlO films deposited by MOCVD can be increased up to 7.9 eV with 38% Al [27]. When combined with electrical measurements, the ellipsometry data can provide valuable information related to the relative dielectric constant of the layers. Our results demonstrated the possibility of adjusting the relative dielectric constant of the layers in a wide range (9–17), when the aluminium concentration varies between 4.5% and 38%. This result is consistent with the results of Zhu *et al.* [28], who also reported the dielectric constant of HfAlO films deposited by jet vapour deposition decreases from 19.6 for HfO_2 to 7.6 for Al_2O_3.

Another feature for HfAlO is the high density of fixed oxide charge. Results reported by Bae *et al.* [29] show negative fixed charge of $1.5 \cdot 10^{12}$ cm^{-2} for HfAlO with 38% Al and $1 \cdot 10^{12}$ cm^{-2} for HfAlO with 20% Al. Our results [30] extended this relationship to HfAlO with Al concentration from 4.5 to 38%; the fixed charge density varies almost linearly from $4.8 \cdot 10^{11}$ to $1.1 \cdot 10^{12}$ cm^{-2}. This feature shows the possibility to adjust the threshold voltage simply by adjusting the ratio of precursors. Recent work [31] successfully demonstrated the attainment of symmetry threshold voltage in HfAlO based complementary MOSFETs by adjusting the Hf/Al ratio.

A few papers [24, 32] have reported large amounts of hysteresis observed in C-V measurements, indicating high densities of oxide traps in the HfAlO films. The measurements of the Doppler broadening spectra of annihilation radiation and the lifetime spectra by Uedono *et al.* [33] shows strong oxygen deficiency in the compound. Driemeier *et al.* [25] found that the oxygen deficiency increases with increasing Al/Hf ratio. The oxide traps may induce additional leakage and therefore the advantages of larger band gap and thermal stability may be traded off. In [27], the HfAlO film with 31.7% Al shows significant higher leakage than the film with 6.8% Al at as-deposited status. However after anneal in N_2 at 700°C, the film with 6.8% Al shows a sudden increase in leakage current. The leakage current of the HfAlO with 31.7% Al remains low due to the improved thermal stability by higher density of Al introduced. Our results [30] showed that HfAlO film with 22% Al has the lowest leakage current (@–1 V); further increase of Al concentration results in excessive leakage.

Hong *et al.* [34] conducted annealing studies on 7.3–7.8 nm thick HfAlO films with 14% Al deposited by thermal sputtering. They annealed the samples in an N_2 ambient for 5 min at temperatures from 500 to 900°C. The HRTEM images showed the interfacial layer growth between the HfAlO film and the Si substrate after anneal.

Cho *et al.* [35] carried out the annealing studies of ultra thin (1.3 nm) HfAlO films. The films were first deposited by ALD and subsequently annealed at 700°C for 60 s in an NH_3 atmosphere. They found that the near-edge x-ray absorption fine structure spectra of the HfO_2 components remained the same while the spectra of Al_2O_3 were changed after the anneal. This result indicates that the change in the bonding characteristics as the result of N incorporation is mainly caused by N incorporation into Al oxide.

Torii *et al.* [36] proposed the employment of HfAlO/SiON stack as gate dielectric and demonstrated successful integration into a standard CMOS process. The transistor achieved encouraging properties such as low EOT (1.1 nm), low leakage ($\sim 10^{-2}$ A/cm^2), low interface density ($2 \cdot 10^{11}$ eV^{-1}cm^{-2}), symmetrical threshold voltage and 92% electron mobility ($V_g = 1.1$ V) of those for SiO_2.

5.2. Silicates

Hafnium silicate films, $(HfO_2)_x(SiO_2)_{1-x}$, are being studied as an alternative to pure hafnium oxide due to comparable advantages such as an increased crystallization temperature [4], stable amorphous structure [37–39] which also resists oxygen diffusion [4, 37], reduced growth of interfacial layers at the silicon/high-k interface and higher values of band gap and effective electron rest mass resulting in reduced leakage [37]. Hafnium silicate films do however have the disadvantage of having a lower k value ($\sim 11-15$) [40, 41] than the pure oxide ($\sim 21-25$) [42, 43] reducing the scalability of the material.

Takeuchi and King in 2004 [44] compared the compositional dependency of the electrical properties of hafnium silicate films from published studies and found that there was a nonlinear dependency of the permittivity of the film with the permittivity decreasing with increasing concentration of incorporated silicon. The same work also reviewed experimental band gap results for hafnium silicate films of varying composition and observed that the compositional dependence of the band gap of hafnium oxide films has two distinct regions. The band gap of hafnium silicate films decreases linearly at a an approximate rate of 50 meV/% when the hafnium oxide content is increased, until the hafnium oxide content reaches 64%. At this stage the band gap becomes independent of hafnium oxide content and stays

constant at a value of 5.7 eV. The theoretical conduction and valence band offsets for an $Hf_{0.5}Si_{0.5}O_2$ film were shown to be 1.5 eV and 3.4 eV, respectively.

Cho *et al.* in 2005 [45] studied the dependence of hafnium silicate phase separation on the composition of the film using XPS finding that a silicon-dioxide-rich hafnium silicate sample ($x = 0.25$) could withstand temperatures greater than 900°C for 1 min in a nitrogen ambient without phase separation but that a hafnium rich hafnium silicate sample ($x = 0.75$) phase-separates at a temperature of 800°C. Thermal stability is a required property for high-k dielectrics due to current processes requiring the gate oxide to remain unaffected by an annealing temperature of 1000°C for 5 s to activate the polysilicon gate [46]. Wilk, Wallace, and Anthony in 2000 [47] were able to anneal silicon-rich (i.e., $x = 0.2$) hafnium silicate samples of thickness 3 nm for 20 s at temperatures of 1050°C in nitrogen without visible grain boundaries formation and proposed the resistance to crystallization may continue even for hafnium silicate films of hafnium content up to 30%.

Nitrogen incorporation into hafnium silicate films is known to be beneficial to their electrical properties such as further increase of the phase separation temperature of hafnium silicates [48], increased permittivity [43] and reduced boron penetration [49]. Cho *et al.* [45] annealed hafnium rich ($x = 0.75$) ~ 3.5 nm thick hafnium silicate samples for 1 min at 900°C in either NH_3 or N_2. The sample annealed in pure nitrogen was seen to phase-separate to contain monoclinic HfO_2 grains, whereas the sample annealed in NH_3 remained stable with no visible phase separation [50]. It was seen that annealing in both atmospheres increased the Si/high-k interfacial layer by less than 1 nm, however annealing in N_2 caused the growth of a 1.4 nm overlayer which seriously increased the effective oxide thickness (EOT) of the film. In the same paper, Cho *et al.* showed results from 3 nm hafnium silicate samples of hafnium content ($x = 0.5$) annealed for 60 s in either NH_3 at a temperature of 750°C or N_2 at a temperature of 950°C. Cho *et al.* also reported that N_2 increased the EOT compared to the as-deposited film whereas NH_3 reduced the EOT compared to the as-deposited film. The samples annealed in N_2 however had superior electrical qualities having leakage currents an order of magnitude ($\sim 10^{-9}$ A/cm^2) lower than those of the NH_3 annealed samples ($\sim 10^{-8}$ A/cm^2) and having a higher effective mobility [43].

Nitrogen incorporation has, however, also been reported to reduce the conduction band and valence band offsets for a $(HfO_2)_{0.40}(SiO_2)_{0.60}$ by 0.33 eV and ~ 1.2 eV, respectively, and reduce the band gap of the film by ~ 1.50 eV [49]. The reduction in band offsets is not serious enough to affect the viability of nitrogen incorporating films, however leakage current will increase through such a film.

In our own laboratories, $(HfO_2)_x(SiO_2)_{1-x}/SiO_2$ $(0 < x < 1)$ gate stacks grown by MOCVD at IMEC were investigated using spectroscopic ellipsometry and electrical characterization techniques [51]. The optical constants, thickness of the layers and optical band gap for hafnium silicates of four concentrations were assessed using UV – NIR and deep UV spectral regions. The permittivity was seen to decrease from ~ 21 for HfO_2 layer to ~ 8 for Hf-silicate with $x = 0.3$. The results suggest that an Hf content above 60% is required to yield a permittivity higher than 10.

6. The way forward to the 22 nm node

Nag [52] explored the relationship between the mean atomic number of atoms constituting different semiconductors, $|Z|$, and the dielectric constant of these materials.

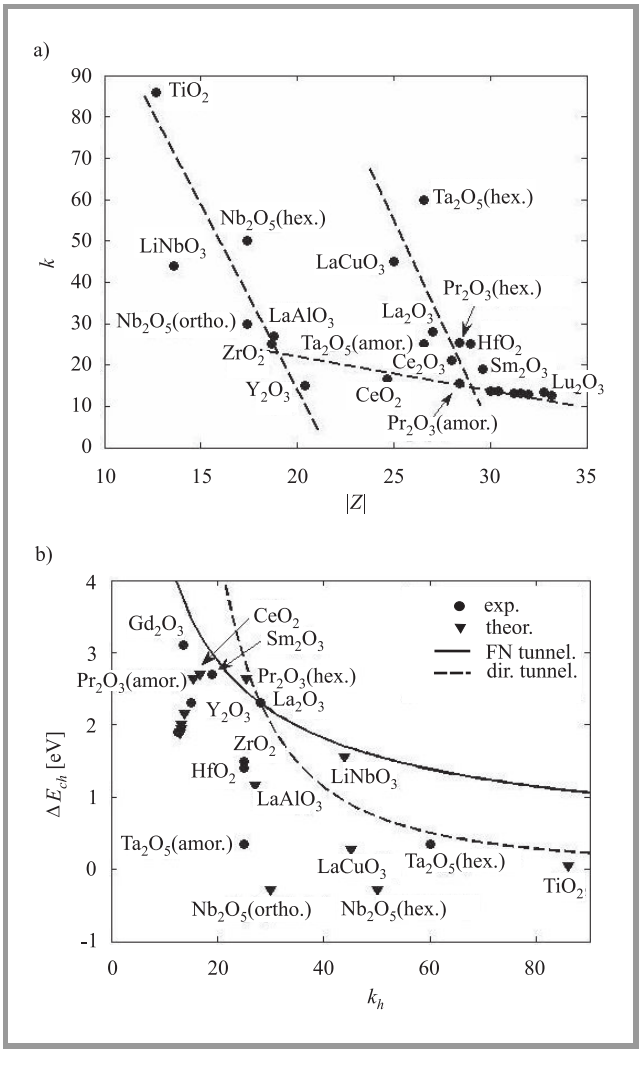

Fig. 7. (a) Experimental relative permittivity for some experimental gate dielectrics plotted against their mean atomic number [6]. (b) Conduction band offset versus the relative permittivity for experimental high-k dielectrics [6].

Busani and Devine [53] and Xue *et al.* [54] also pointed out corresponding relations for the rare earth oxides, but

beside any changes in polarizability, α, both cases suggested that a change in the molecular volume, V_m, was responsible for the relationship between the permittivity value and $|Z|$. Both cases modelled the relative permittivity value using the Clausius-Mossotti equation (see relation (2)).

Figure 7a shows the relative permittivity values versus the mean atomic number of some well-known and potentially suitable metal oxides, after Engstrom *et al.* [6]. In the same work, Pauling electronegativities were considered to allow prediction of the conduction band offsets for the oxides for which values were experimentally unknown, allowing predictions of conduction band offsets versus relative permittivity, as shown in Fig. 7b. Boundaries were established assuming the most stringent requirements for the 22 nm node, namely EOT = 0.5 nm and leakage $< 10^{-2}$ A/cm^2 at 1 V, considering both purely direct tunnelling and Fowler-Nordheim and are included on the plot. By assuming the most pessimistic scenario, which was that any materials with relative permittivity lower than that of lanthanum would suffer from direct tunnelling and above this Fowler-Nordheim tunnelling, it was predicted that only a few materials would be able to meet the requirements for the 22 nm node, namely Pr_2O_3 in the hexagonal phase, La_2O_3 and $LiNbO_3$. It was also suggested that Sm_2O_3, Ce_2O_2 and Gd_2O_3 were worthy of consideration. Of the lanthanides, La_2O_3 has been extensively studied by Iwai *et al*. and is perhaps the most serious contender for this node [55].

Kwo *et al.* [56] reported encouraging results of amorphous Gd_2O_3 films. The films were attained by electron beam evaporation using powder packed ceramic Gd_2O_3 sources. The scanning transmission electron microscopy (STEM) results showed that the film was 4.5 nm thick and no interfacial layer was observed. The C-V and I-V measurements showed the EOT of the film was 1.65 nm and the leakage (@ 1 V) was 10^{-4} A/cm^2, much lower comparing with SiO_2 with similar EOT. They also showed that these amorphous dielectrics could withstand annealing tests to a temperature of 850°C, as corroborated by the XPS analysis.

Ohmi *et al.* [57] made a comparative study of rare earth oxides grown by E-beam deposition. They found La_2O_3 possessed the lowest leakage and smooth interface among the rare earth oxides investigated. Other material such as Dy_2O_3 and Lu_2O_3 also showed good electrical properties but highly dependent on deposition processes [57].

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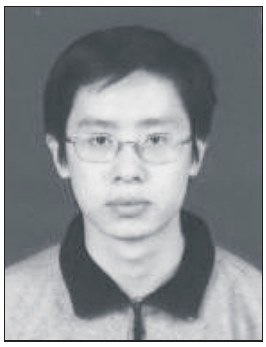

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