Invited paper

Special size effects in advanced single-gate and multiple-gate SOI transistors

Akiko Ohata, Romain Ritzenthaler, Olivier Faynot, and Sorin Cristoloveanu

Abstract— State-of-the-art SOI transistors require a very small body. This paper examines the effects of body thinning and thin-gate oxide in SOI MOSFETs on their electrical characteristics. In particular, the influence of film thickness on the interface coupling and carrier mobility is discussed. Due to coupling, the separation between the front and back channels is difficult in ultra-thin SOI MOSFETs. The implementation of the front-gate split C-V method and its limitations for determining the front- and back-channel mobility are described. The mobility in the front channel is smaller than that in the back channel due to additional Coulomb scattering. We also discuss the 3D coupling effects that occur in FinFETs with triple-gate and Ω-gate configurations. In low-doped or tall fins the corner effect is suppressed. Narrow devices are virtually immune to substrate effects due to a strong lateral coupling between the two lateral sides of the gate. Short-channel effects are drastically reduced when the lateral coupling screens the drain influence.

Keywords— MOSFET, SOI, ultra-thin silicon, multiple-gate, mobility, coupling effect, thin gate oxide, gate-induced floating body effect, drain-induced virtual substrate biasing.

1. Introduction

As CMOS is scaled down, the introduction of silicon-on-insulator (SOI) structures is inevitable for improving the short-channel effects, speed, and subthreshold swing. The SOI thickness should be 3–4 times smaller than the channel length and, therefore, stands as a critical parameter for the integration. On the other hand, thin-gate oxides are also necessary for improving the device performance. In this paper, we discuss a number of issues related to the downsizing of planar SOI transistors, focusing on the problems induced by the body thinning and thin gate oxide. A more advanced approach is to use multiple-gate SOI transistors like FinFETs [1] (Fig. 1a), triple-gate FETs [2] (Fig. 1b) or existing variants [3–5] (Fig. 1c). We demonstrate that interesting coupling effects in longitudinal, lateral and vertical directions arise leading to new phenomena. Due to the electrostatic influence of the top and bottom gates, the surface potential and threshold voltage can vary along the lateral gate. Then a bi-dimensional threshold voltage may be observed, depending on the location in the channel. The influence of the back-gate and drain potential, detrimental for single-gate short SOI structures, is also expected to be modified using triple-gate structures because of the three-dimensional coupling.

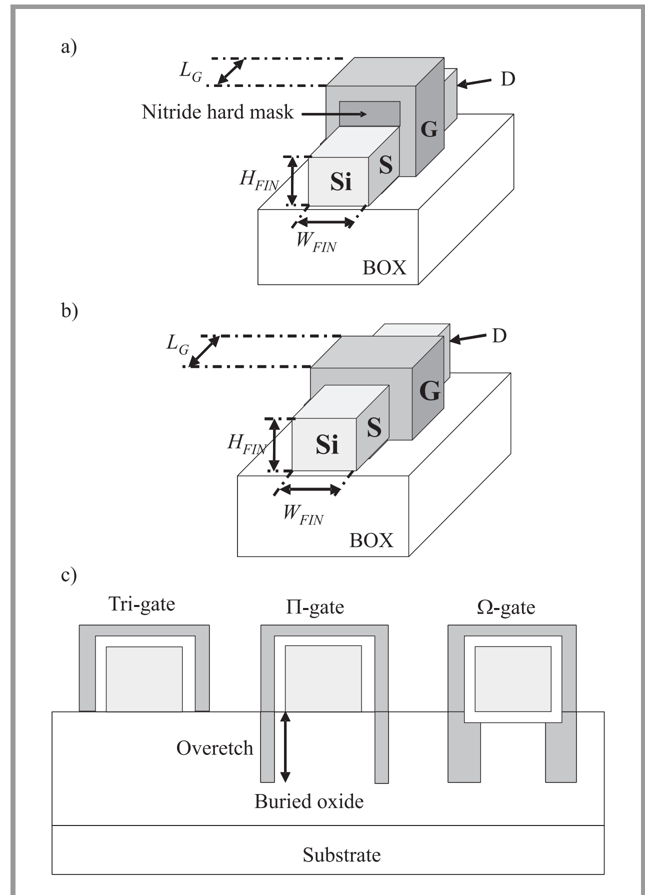

Fig. 1. FinFET (a) and triple-gate FET (b) structures. Variants of triple-gate FETs such as Π- and Ω-gate FETs (c).

2. Ultra-thin SOI MOSFETs

The SOI film thinning improves the electrostatic control and the device scalability, but also causes special coupling and transport effects.

2.1. Coupling effect

An investigation of the coupling effect between the front and back interfaces (i.e., the front-channel threshold voltage V_{T1} as a function of the back-gate voltage V_{G2}, and vice-versa $V_{T2}(V_{G1})$ [6, 7]) can provide useful information for determining whether one or two channels are created in an SOI film. This is an important point for designing double-gate MOSFETs or FinFETs, since their electrical

characteristics are affected by volume inversion [8]. Furthermore, the coupling effect is an essential operation principle for devices in which the threshold voltage is controlled by several gates.

Figures 2a and 2b show the coupling effect between the front and back interfaces in long- and short-channel SOI NMOSFETs. The transconductance curves of a short channel exhibit a single peak (Fig. 2a); however, a plateau appears for a long channel (Fig. 2b) due to the formation of a back inversion layer at the film-BOX interface before the front-channel inversion is created [9]. The back-channel characteristics at various front-gate biases are similar, i.e., the transconductance of a short channel exhibits a single peak [10].

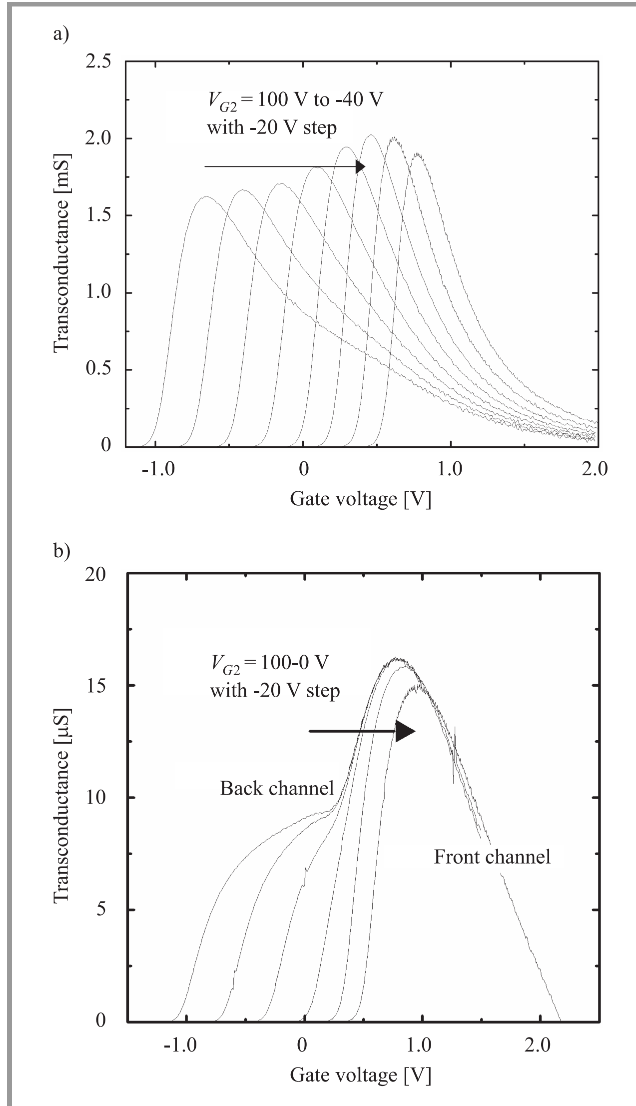

Fig. 2. Transconductance ($\delta I_d/\delta V_{G1}$) in SOI NMOSFET versus gate voltage V_{G1} with the back-gate bias V_{G2} as a parameter for (a) a short SOI MOSFET ($L = 0.5$ μm) and (b) a long SOI MOSFET ($L = 100$ μm). The plateau due to the back-channel activation is evident for a long transistor. In both cases, $T_{Si} = 15$ nm, $T_{BOX} = 400$ nm, $T_{ox} = 2$ nm, $W = 100$ μm, and $V_D = 50$ mV. The doped body ($N_A \approx 4 \cdot 10^{17}$ cm^{-3}) was thinned by sacrificial oxidation, except in the source/drain regions.

Another interesting feature is that the V_{T1} (V_{G2}) curve is superimposed on the V_{G1} (V_{T2}) one for a short channel (Fig. 3a) while the two curves are different for a long channel (Fig. 3b). The coupling curves for a long channel are described by [7]:

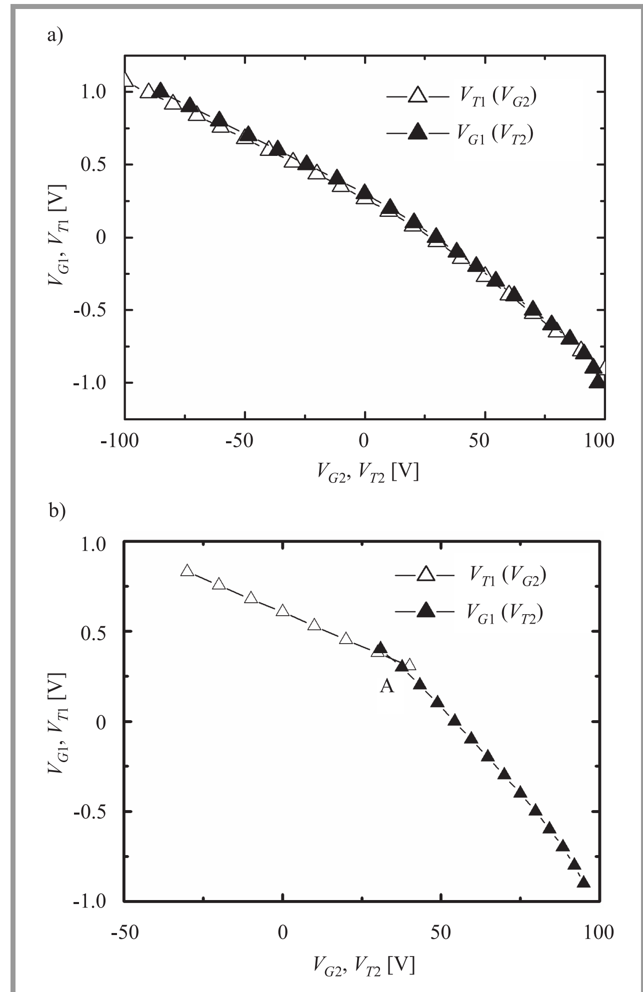

Fig. 3. (a) Front-channel threshold voltage V_{T1} versus back gate bias V_{G2} and back-channel threshold voltage V_{T2} versus front-gate bias V_{G1}. Threshold voltages were extracted from the transconductance peak. In a short channel, the two curves are different. (b) In a long channel, the two curves are different. At point A, both the front and back channels are simultaneously inverted.

$$\Delta V_{T1} \approx -\frac{C_{BOX}}{C_{ox}}\Delta V_{G2}\,, \tag{1}$$

$$\Delta V_{G1} \approx -\frac{C_{BOX}}{C_{ox}}\frac{C_{si}+C_{ox}}{C_{si}}\Delta V_{T2}\,, \tag{2}$$

where $C_{si} = \varepsilon_{si}/T_{Si}, C_{ox} = \varepsilon_{ox}/T_{ox}$, and $C_{BOX} = \varepsilon_{ox}/T_{BOX}$ represent the capacitances of the depleted film, gate oxide and buried oxide (BOX), respectively.

The cross-point of these curves (point A in Fig. 3b) indicates the voltage condition at which the front and back

channels are simultaneously inverted [11]. If V_{G2} is larger than this value, when sweeping V_{G1}, the back channel is inverted before the front channel. On the other hand, if V_{G2} is smaller than this value, only the front channel is inverted by sweeping V_{G1}. Thus, the inverted channel can clearly be identified from point A.

In the case of an extremely thin SOI layer ($C_{si} >> C_{ox}$), Eq. (2) can be rewritten as:

$$\Delta V_{G1} \approx -\frac{C_{BOX}}{C_{ox}} \Delta V_{T2} . \qquad (3)$$

Since the slope of this equation is the same as that of Eq. (1), it is difficult to separate the two curves.

Furthermore, for high series resistance once the back channel is inverted, the formation of the front channel could be masked: the transconductance curve obtained by sweeping V_{G1} shows a single-peak structure due to the back channel only [10]. Thus, the results in Fig. 2a and Fig. 3a can be understood as follows: for a short channel, the back-channel plateau transforms into a peak. When measuring $V_{T1}(V_{G2})$, the beginning of the plateau appears as a peak and can be mistaken as V_{T1}. This peak shows the threshold of the back channel; it actually corresponds to $V_{G1}(V_{T2})$ as confirmed by our direct back-channel measurements $V_{T2}(V_{G1})$. The point where the slope of the curve changes (around $V_{G2} = 20$ V in Fig. 3a) corresponds to the voltage condition at which the front and back channels are simultaneously inverted.

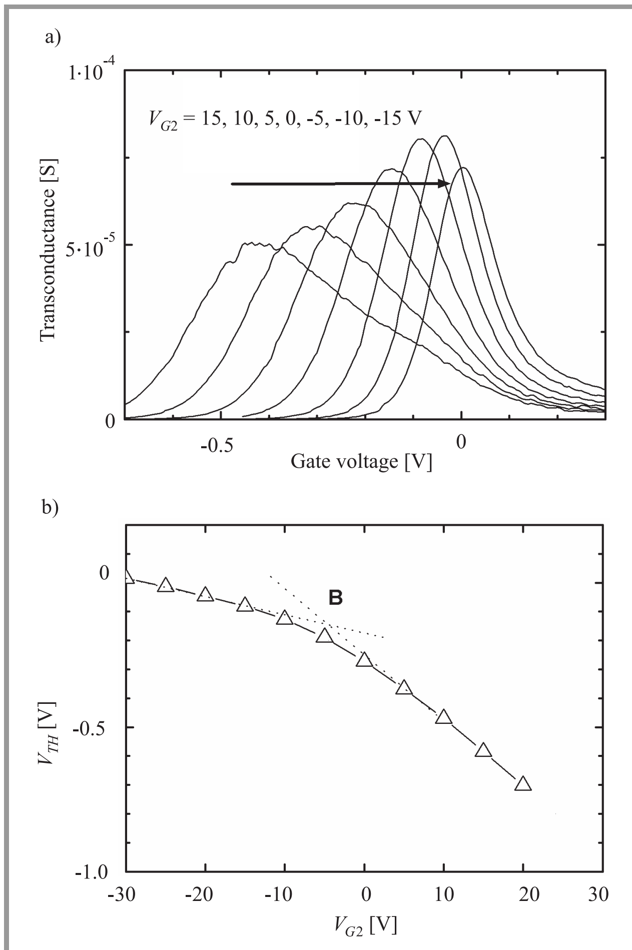

Fig. 4. (a) Transconductance ($\delta I_D/\delta V_{G1}$) versus front-gate voltage with the back-gate bias as a parameter for the undoped thin-SOI (initial wafer doping was $N_A = 5 \cdot 10^{14}$ cm^{-3}) NMOSFET. $V_D = 10$ mV, $W = 10$ μm, $L = 0.05$ μm. The average SOI thickness was 9 nm on the wafer. The gate oxide thickness is approximately 1 nm. (b) Threshold voltage V_{th} versus back gate voltage V_{G2}, $V_D = 10$ mV. At point B where the slope changes, both sides are inverted simultaneously.

As the SOI thickness or channel area decreases, the point where the slope of the coupling curve changes is useful to determine which channel is actually inverted; this identification is impossible from the transconductance curves due to their single-peak shape [12]. Figure 4a reproduces the transconductance curves exhibiting a single peak at various V_{G2} applied to a short-channel SOI NMOSFET. Figure 4b shows that the threshold voltage is due to the front channel when V_{G2} is smaller than point B, and to the back channel when V_{G2} is larger than point B. Note that V_{G2} at point B is less than 0 V. Hence, the transconductance peak at $V_{G2} = 0$ V occurs due to the back channel. Transconductance and subthreshold slope deteriorate because the channel is controlled through the gate oxide and silicon body. Thus, this device is not suitable for operation at $V_{G2} = 0$ V. On the other hand, the transconductance peak reaches a maximum value near the condition where both channels are simultaneously inverted ($V_{G2} \approx -5$ V in Fig. 4b).

As the SOI thickness decreases below 10 nm, the coupling effect theory should be revisited [13]. Figure 5 shows the simulated results of the surface potential variation with the front-gate voltage for a negative back-gate bias. In a thick-body MOSFET, as V_{G1} increases, the front channel is gradually inverted whereas the back-surface potential does not change, remaining in accumulation. By contrast,

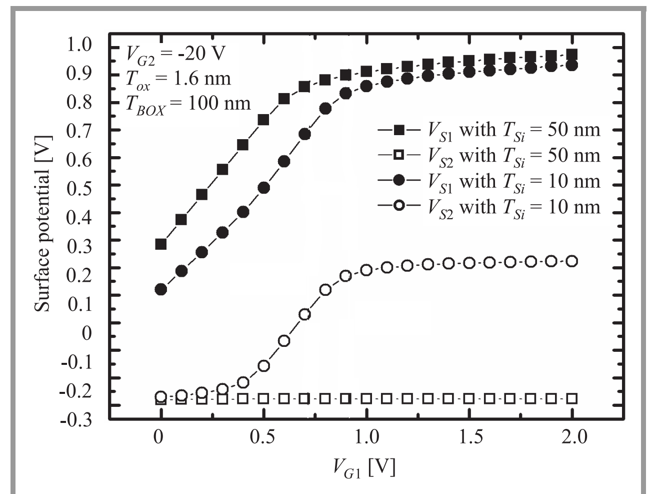

Fig. 5. Surface potential of the front (V_{S1}) and back (V_{S2}) interfaces versus front-gate voltage (V_{G1}) in the case of thick (50 nm) and thin (10 nm) SOI. Back gate voltage $V_{G2} = -20$ V.

in an ultra-thin body, both the front and back potentials increase with V_{G1}. This means that it becomes difficult to keep one channel in accumulation while inverting the opposite channel. Additional simulations show that the potential distribution in a 5 nm thick body is quasi-flat. The two channels merge in a single channel that covers the whole film volume [13]. Ultra-thin SOI devices are also subject to quantum effects: sub-band splitting which leads to an increase in the threshold voltage and a modification of the effective mass and scattering mechanisms.

2.2. Carrier mobility

The effect of the film thickness on mobility is important for further CMOS performance and scalability. Figure 6 shows the mobility-thickness correlation in 10–20 nm thick NMOSFETs with a 2-nm SiO_2 gate oxide, in which SOI thickness variations were locally caused by process fluctuations. In short-channel MOSFETs, the mobility decreases for thinner films, whereas in long MOSFETs the thickness effect is insignificant. This difference is essentially due to the series resistance. This argument applies to both the front and back channels [14].

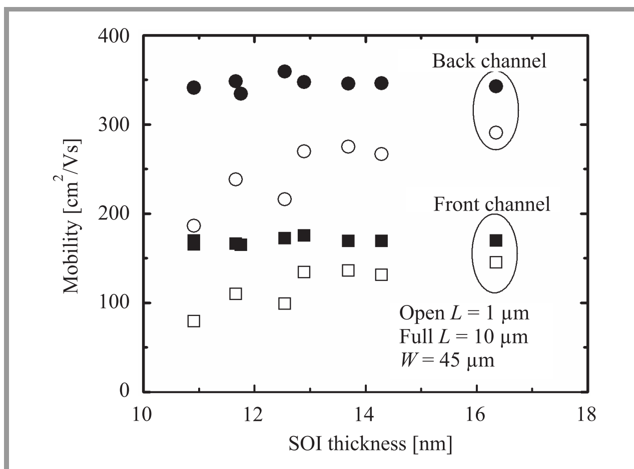

Fig. 6. Front- and back-channel field-effect mobilities versus SOI film thickness for short (1 μm) and long (10 μm) channels. The field-effect mobility was determined from the transconductance peak. All the devices were probed on the same wafer. The local film thickness was measured by ellipsometry and verified by analyzing the coupling between the front and back channels. $T_{ox} = 2$ nm and $T_{BOX} = 400$ nm. The doped body ($N_A \approx 4 \cdot 10^{17}$ cm^{-3}) was thinned by sacrificial oxidation, except in the source/drain regions.

The mobility is systematically lower at the front channel than at the back channel, even after correcting for a lowered gate-oxide capacitance due to polysilicon depletion and quantum capacitance of the inversion layer. Comparing the effective mobility at the front and back channels makes the origin of the mobility difference clear.

The front-gate split C-V method was used for determining the carrier mobility and density, N_s, at both the front and back channels. As shown in Fig. 7, a plateau is observed in

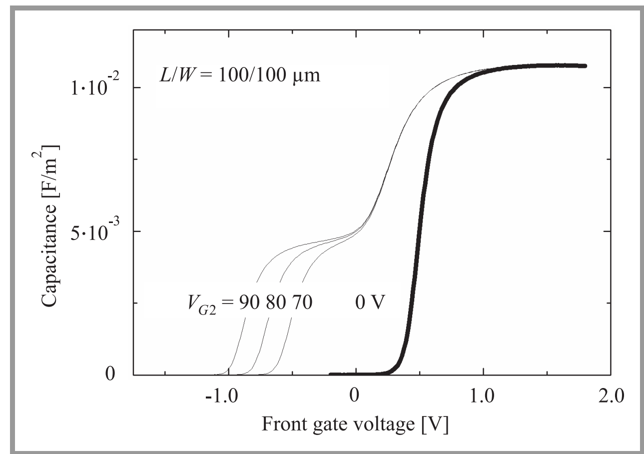

Fig. 7. Front-gate split C-V measurements for various substrate voltages. $T_{Si} \approx 16$ nm. The frequency for split C-V measurement is 5 kHz.

the C-V plot at large substrate voltages due to the creation of the back channel [15]. The carrier density N_s of the back channel can be obtained by integrating the capacitance values specific to this region [16, 17]:

$$qN_{s\,Back}\left(V_{G1}, V_{G2}\right) = \int_{-\infty}^{V_{G1}} C_{gc}\, \mathrm{d}V_{G1}\,. \tag{4}$$

The effective field is determined from the equations for thin SOI [18, 19]. The threshold voltage is calculated by defining a corresponding inversion charge density [17].

There is, however, a limitation in this front-gate split C-V method for evaluating the carrier density in the back channel [17]. Figure 8 shows the relationship between the back-channel threshold voltage V_{T2} and front-gate volt-

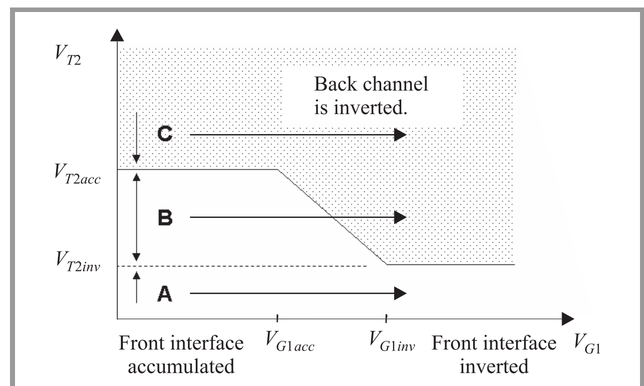

Fig. 8. The relationship between the threshold voltage of the back channel (V_{T2}) and the front-gate voltage (V_{G1}) by the model of Lim and Fossum. When the front interface is accumulated (V_{T1acc}), the threshold voltage of the back channel becomes constant. When the back gate is in region A and the front gate is swept, only the front channel is inverted. When the back gate is in region B and the front gate is swept, the back channel is turned off and on by the front gate voltage. When the back gate is in region C and the front gate is swept, the back channel cannot be turned off by the front gate voltage because of the accumulation layer at the front interface.

age V_{G1} as modeled by Lim and Fossum [7]. For the back gate bias in region A, only the front channel is activated by applying the front-gate voltage. Thus, the carrier density at the front channel can be evaluated by the front-gate split C-V method. For the back gate bias in region B, the back channel can be turned on and off by sweeping the front-gate voltage. Thus, the carrier density at the *back* channel can be evaluated by the front-gate split C-V method. On the other hand, for the back gate bias in region C, when V_{G1} is swept, it is impossible to cut off the back channel since V_{T2} becomes constant when the front interface is accumulated. Furthermore, in this region C, a careful examination is required for getting the correct C-V curves. The front-interface accumulation layer is not formed instantly as there is no source for the majority carrier in SOI films. A hysteresis in C-V and I-V is therefore observed [15, 20]. Thus, the front-gate split C-V method cannot be used for determining the carrier density at the back channel in region C.

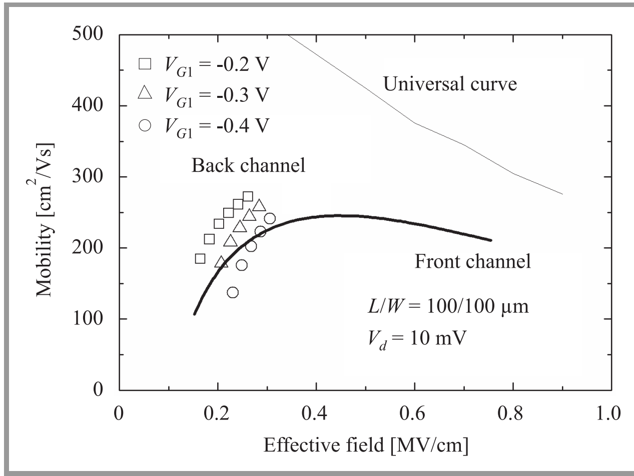

Fig. 9. Front-channel effective mobility (for $V_{G2} = 0$ V) and back-channel effective mobility (for $V_{G1} = -0.2$, -0.3, and -0.4 V) versus effective field.

Figure 9 shows the effective mobility of the front ($\mu_{eff,F}$) and back ($\mu_{eff,B}$) channels evaluated by $I_D - V_G$ and front-gate split C-V method for our devices of Fig. 6. For low $|V_{G1}|$, $\mu_{eff,B}$ is clearly higher than $\mu_{eff,F}$ at the same effective field E_{eff}. The mobility components μ_{Fl} and μ_{Bl} which indicate the deviation from the "universal mobility" curve were estimated by Matthiessen's rule:

$$\mu^{-1}_{Fl,Bl}(N_s) = \mu^{-1}_{eff\,F,eff\,B}\big(N_s(E_{eff})\big) - \mu^{-1}_{universal}(E_{eff})\,. \quad (5)$$

This procedure removes the impact of phonon scattering. Figure 10 shows that these mobility components depend on N_s, which suggests the role of Coulomb scattering. V_{G1} dependence of $\mu_{eff,B}$ in Fig. 9 is explained by the change in N_s. At a constant E_{eff}, N_s decreases with a more negative V_{G1}, which results in a reduced charge-screening effect.

Furthermore, since $\mu_{Fl} < \mu_{Bl}$, an additional scattering mechanism would affect only the front channel. We extract μ_{add} on the basis of the mobility difference between the two channels as follows:

$$\mu^{-1}_{add}(N_s) = \mu^{-1}_{Fl}(N_s) - \mu^{-1}_{Bl}(N_s)\,. \quad (6)$$

Note that the mobility limited by Coulomb scattering on film impurities is now eliminated. The dependence of μ_{add} on N_s (Fig. 10) suggests that the presence of Coulomb scattering centers at the front channel is responsible for the mobility difference between the two channels. Remote scattering centers from the polysilicon gate are possible candidates and should be considered for thin-gate oxides [21].

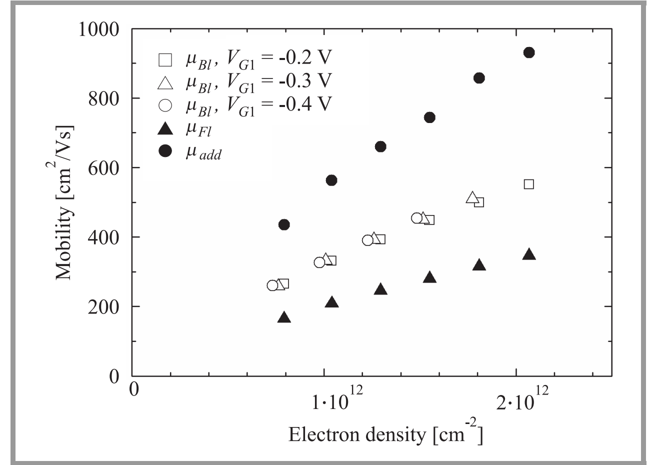

Fig. 10. Mobility-lowering components of the front channel μ_{Fl} and back channel μ_{Bl} determined from Eq. (5). The additional mobility-lowering component μ_{add} of the front channel was derived from Eq. (6).

2.3. Thin gate oxide

An important effect in SOI MOSFETs with ultra-thin oxides is the gate-induced floating-body effect (GIFBE) [22]. This effect is caused by the tunneling current from the valence band of the SOI film into the gate [23], which charges the body with majority carriers. The body potential is determined by the balance between the body charging via direct tunneling current and the carrier recombination in the body or junctions. Due to the GIFBE, the transconductance curve becomes distorted giving rise to a second peak, as shown in Fig. 11.

The GIFBE occurs even in FD MOSFETs, especially when the back interface is biased close to accumulation [24]. The standard method to determine the mobility in FD SOI MOSFETs consists of eliminating the interface coupling by accumulating the opposite channel. Figure 11 shows that the second peak of transconductance due to the GIFBE becomes larger than the genuine peak. If the "maximum" transconductance is misused, then the field-effect mobility is overestimated.

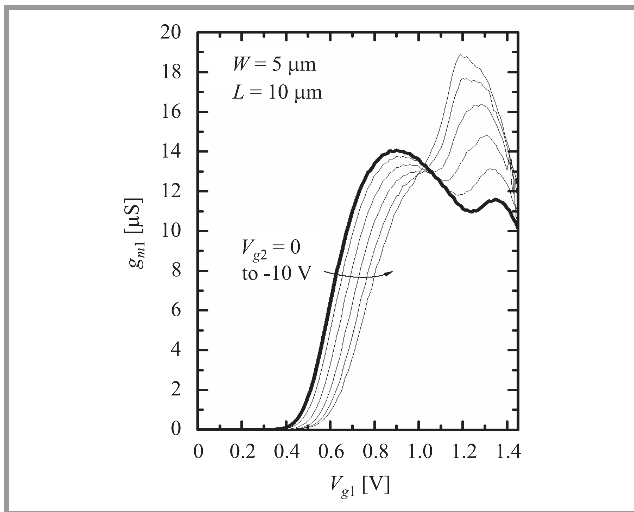

Fig. 11. Transconductance as a function of the front gate voltage for different back-gate biases from 0 V to –10 V in a FD SOI MOSFET. $T_{BOX} = 145$ nm, $T_{ox} = 1.6$ nm, and $T_{Si} = 17$ nm. The "second peak" appears due to the GIFBE.

3. Non-planar multiple-gate SOI transistors

3.1. Corner effects

Triple-gate devices feature a non planar silicon/oxide interface involving corners (Fig. 1b). In each corner region (Fig. 12a), the coupling between the adjacent gates induces a local lowering of the threshold voltage. This parasitic channel may cause an increase of the off-state leakage current. In order to characterize the threshold voltage inhomogeneity, we performed numerical simulations. The "local" threshold voltage of the different channel regions was extracted from the electrical characteristics. First, the "global" threshold voltage V_{TG} was determined from the second derivative of the drain current versus gate voltage curve. Then, the electron density for $V_G = V_{TG}$ was calculated all along the channel. Finally, using the relationship between the threshold voltage and the inversion charge, a "local" threshold voltage was calculated:

$$V_T^{LOCAL} = V_{TG} - \frac{Q_{INV}}{C_{OX}}. \quad (7)$$

The local threshold voltage along the vertical channel for undoped FinFET and triple-gate (TriGate) transistors is plotted in Fig. 12b. The threshold of a triple-gate structure is found to decrease near the top gate. For FinFETs, the deactivation of the top channel by the nitride hard mask suppresses the drop of the threshold voltage and the profile is roughly flat along the channel.

The ΔV_T is defined as the maximum threshold lowering along the vertical axis. In Fig. 13, ΔV_T is plotted as a function of the fin height for FinFETs and triple-gate FETs, with low and high doping. As expected, tall fins

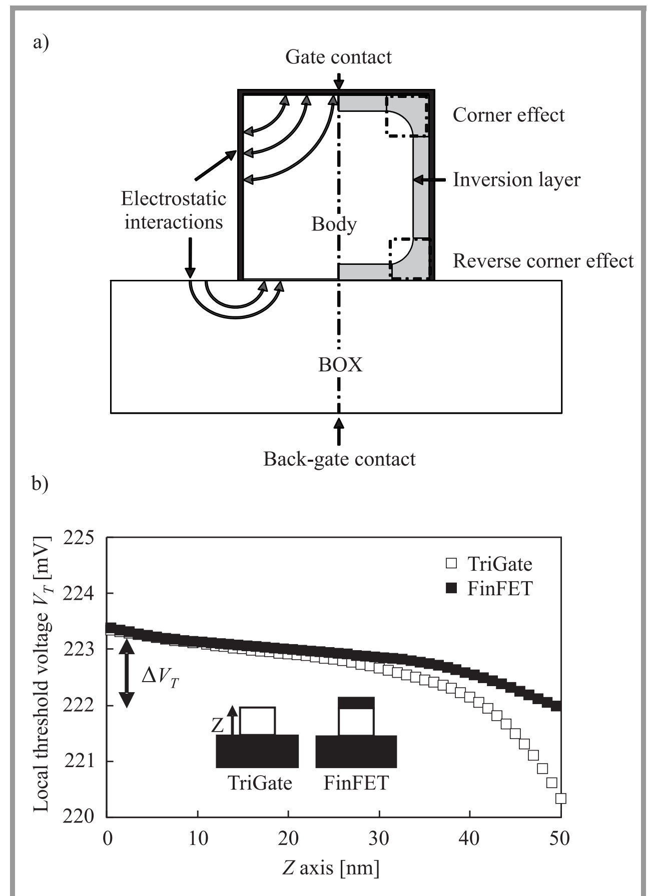

Fig. 12. (a) Cross-section of a triple-gate structure showing the electrostatic interactions leading to corner effects. (b) Local threshold voltage along the vertical channel for low doped ($N_A = 10^{15}$ cm^{-3}) FinFET and triple-gate FET with $W_{FIN} =$ 50 nm, $H_{FIN} = 50$ nm, and $L_G = 0.5$ μm.

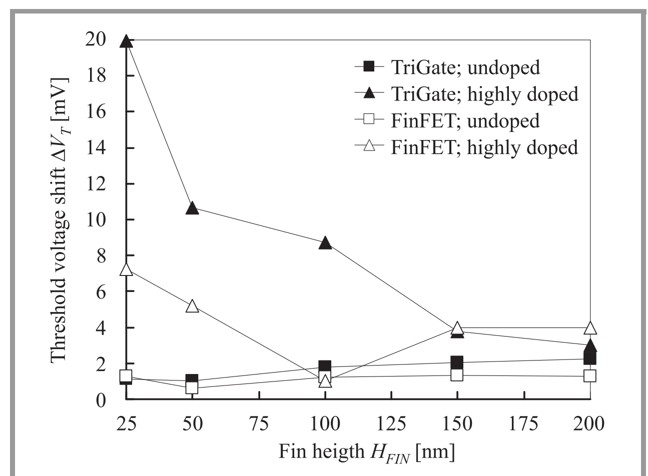

Fig. 13. ΔV_T versus fin height H_{FIN} for FinFET and triple-gate structures with low ($N_A = 10^{15}$ cm^{-3}) and high ($N_A = 10^{18}$ cm^{-3}) body doping. $W_{FIN} = 50$ nm, $L_G = 500$ nm.

exhibit a lower ΔV_T because of a smaller top-gate influence. In FinFETs the threshold voltage shift is efficiently reduced due to their quasi-double gate operation. A low

doping clearly attenuates the threshold voltage shift for both FinFET and triple-gate architectures. Although the threshold voltage non-uniformity increases with the doping level, ΔV_T shift due to the non-planar triple-gate configuration is smaller than 25 mV, indicating a weak impact of the corners.

3.2. Lateral versus vertical coupling

The ΩFETs are triple-gate transistors where the lateral gates penetrate within the BOX (Fig. 1c) [5]. A wide ΩFET behaves as a single-gate fully depleted (FD SOI) device rather than a FinFET. Changing the back-gate bias V_{G2} from -15 to $+15$ V results in a lateral shift of the current and transconductance characteristics (Fig. 14a). The back-channel activation is visible on transconductance curves as a plateau (for $V_{G2} = +15$ V and $V_G = -0.5$ V, see also Fig. 2b).

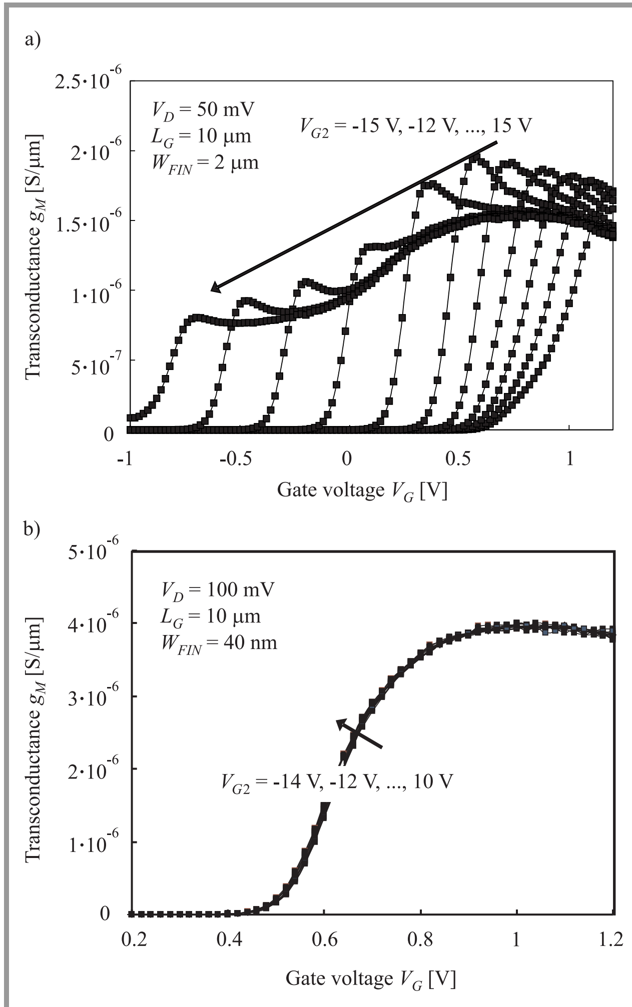

Fig. 14. (a) Transconductance g_M versus gate voltage V_G for a wide ($W_{FIN} = 2\ \mu$m) ΩFET. The back-gate voltage V_{G2} varies from -15 to 15 V. (b) Transconductance g_M versus gate voltage V_G for a narrow ($W_{FIN} = 40$ nm) ΩFET. The back-gate voltage V_{G2} varies from -14 to 10 V.

For narrow devices (Fig. 14b), the substrate bias is no longer effective. The silicon-BOX interface becomes controlled by the fringing electric field penetrating from the lateral gates into the channel (horizontal coupling) and into the BOX. For instance, when the front gate is in accumulation, it is impossible to invert the back channel even for high back-gate bias.

The threshold voltage variation with substrate bias is shown in Fig. 15. For *wide* devices, the change from substrate accumulation to substrate inversion is reflected by a linear decrease of the threshold voltage, followed by a more rapid drop due to the activation of the back channel (1D Lim and Fossum model, see also Fig. 3 [7]). As noted above, the lateral gates can screen the narrow silicon body from the back-gate influence. In Fig. 15, it is seen that for devices with very small fin width the threshold voltage is rather insensitive to back-gate voltage. In ΩFET devices, the control of the body and back channel by the main gate is better than in FinFETs.

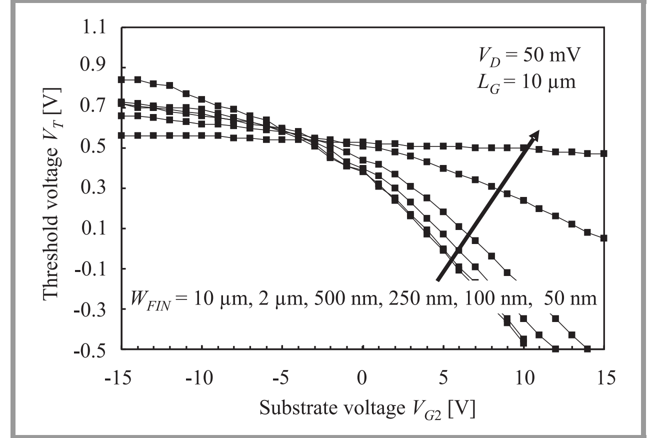

Fig. 15. Threshold voltage V_T versus back-gate bias V_{G2} for n-channel ΩFETs with various fin widths. V_T was extracted using a constant current method.

The potential distribution in the channel of a triple-gate structure can be analytically calculated by adapting the model proposed for four-gate FETs [25]. The variation of the threshold voltage when the back-gate is biased into depletion (vertical coupling: Eq. (1)) can then be rewritten to take into account the influence of the lateral coupling:

$$\alpha(W,H) = \frac{\partial V_{T1}}{\partial V_{G2}} = \left[\frac{2\sqrt{2}}{\sinh\left(2\sqrt{2}\dfrac{H}{W}\right)}\right] \frac{\dfrac{C_W(W)}{C_{ox}}}{1+\dfrac{2\sqrt{2}}{\tanh\left(2\sqrt{2}\dfrac{H}{W}\right)}\dfrac{C_W(W)}{C_{BOX}}}, \tag{8}$$

where $C_W = \varepsilon_{Si}/W_{FIN}$, C_{ox} and C_{BOX} are respectively the lateral silicon film capacitance, front and back oxide capacitances.

In Fig. 16, the 2D coupling coefficient α, which generalizes Fossum's model [7], is plotted as a function of the channel width. For a narrow triple-gate the coefficient is close to zero; this corresponds to the situation where the lateral gates control perfectly the body, screening the influence of the back-gate. For a fully depleted SOI configuration, i.e., $W >> H$, the coupling coefficient α is close to the classical value T_{ox}/T_{BOX}, given in Eq. (1).

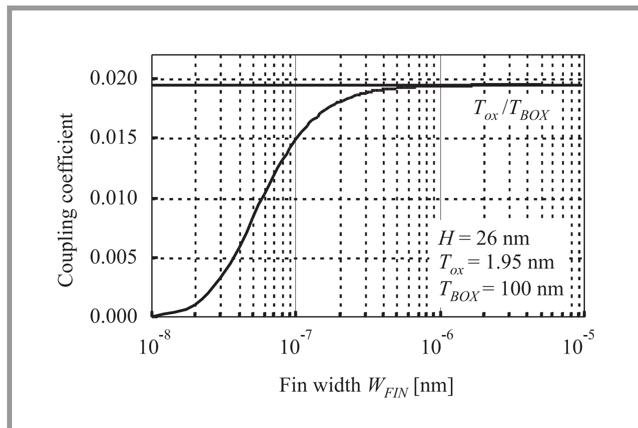

Fig. 16. Coupling coefficient $\Delta V_{T1}/\Delta V_{G2}$ (back-gate biased into depletion) as a function of the fin width in a triple-gate transistor.

Practical implications of back-gate coupling in multiple-gate FETs are related to resistance to harsh environment with radiation or hot carrier injection, where charges trapped into the BOX can modify the electrostatic potential of the back interface. Radiation tests on ΩFET devices [26] have shown that wide devices exhibit a 200 mV threshold voltage shift after 500 krad exposure. By contrast, narrow devices (50 nm) experience a quasi-null threshold voltage variation. Narrow ΩFETs are therefore intrinsically immune to radiation effects and could operate in very harsh conditions.

3.3. Lateral versus longitudinal coupling – DIVSB

A dramatic short-channel effect in fully depleted SOI structures is the penetration of the electric field from the drain into the buried oxide and underlying silicon substrate (Fig. 17a). This fringing field tends to increase the surface potential at the back interface (film-BOX). Because of the existing vertical coupling between the front and back interfaces, the properties of the front channel are degraded.

The potential profile in the buried oxide can be resolved by conformal mapping [27]. Deriving the potential at the body/BOX interface, the expressions of the back-channel transverse field components can be calculated. The source/body $C_{BS}(x)$ and drain/body $C_{BD}(x)$ capacitances

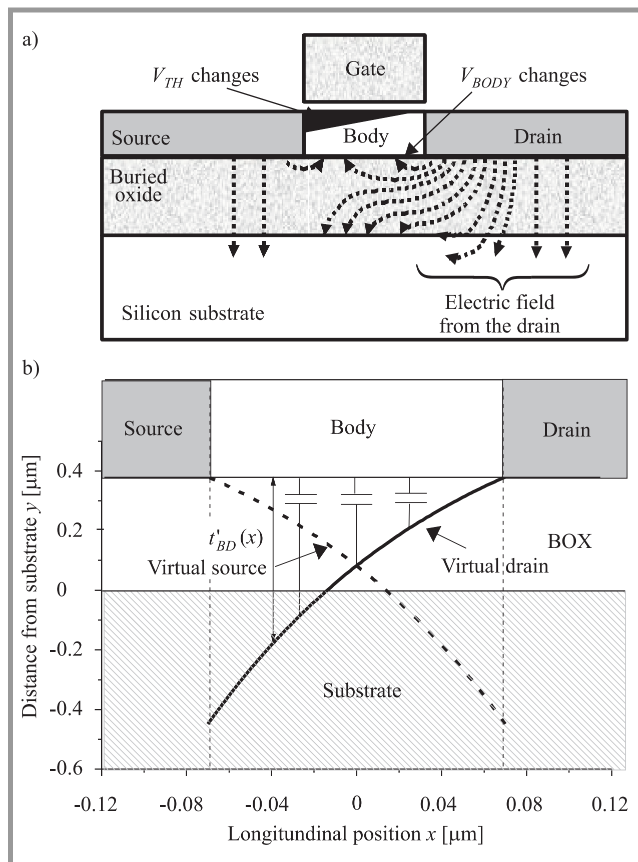

Fig. 17. (a) Schematics of the fringing fields leading to DIVSB effect and (b) equivalent representation of buried oxide fringing capacitances and source/drain virtual electrodes.

summarize the back-channel charge control by the source and drain:

$$C_{BS/BD}(x) = \frac{\varepsilon_{ox}}{T_{BOX}} \frac{1}{\exp\left[\frac{\pm\pi}{T_{BOX}}\left(x \pm \frac{L}{2}\right)\right] - 1}. \tag{9}$$

A very interesting feature of this formalism is the fact that the fringe capacitances C_{BD} and C_{BS} behave like the BOX capacitance C_{BOX}. This means that drain and source influence can be described by *virtual* electrodes located at a varying distance from the body/BOX interface (Fig. 17b). This is why the phenomenon is named DIVSB (drain induced virtual substrate biasing) [27].

The 3D simulations were carried out to investigate the evolution of DIVSB effect as a function of fin width. The vertical potential profiles taken in the centre of the device (at $L_G/2$ and $W_{FIN}/2$) are presented in Fig. 18. At low drain voltage (10 mV, Fig. 18a) the potential depends exclusively on the fin width. For narrow ΩFETs, the BOX region located between the two lateral gates is totally under control and the potential exhibits a peak. For wide devices, the lateral gates have no influence. For high drain voltage (1.2 V, Fig. 18b) DIVSB effect is directly visible in a short and wide device, where the potential in the BOX is increasing as compared to a long and wide device. This

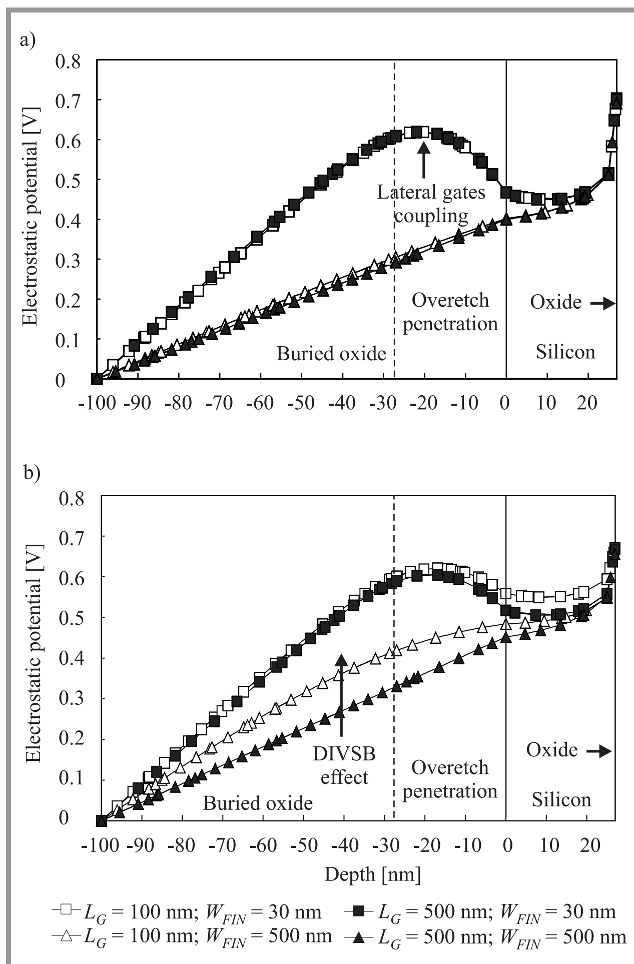

Fig. 18. Vertical potential profiles in the centre of the fin. Simulations are for short (open symbols) and long (closed symbols), as well as for narrow (squares) and wide (triangles) devices; (a) is simulated with a low drain voltage ($V_D = 10$ mV) and (b) with a high drain voltage ($V_D = 1.2$ V); $V_G - V_T = 300$ mV, and $V_{G2} = 0$ V.

critical problem is solved for narrow fins, where the potential profile in the BOX is roughly the same for long and short devices.

4. Summary

Several dimensional effects taking place in modern SOI MOSFETs have been reviewed. In planar transistors, the film thickness plays a crucial role. The coupling effects are amplified in ultra-thin films preventing the separation between the front and back channels. The coexistence of accumulation in the back channel with inversion in the front channel becomes equally difficult. In addition, the high series resistance caused by film thinning can mask the activation of one channel. The method for determining the inverted channel was described.

The carrier mobility in ultra-thin SOI MOSFETs can be extracted by adapting the front-gate split C-V method to the back channel. It was found that the mobility in the front channel is smaller than that in the back channel due to Coulomb scattering. The possibility of misevaluation of the carrier mobility, due to direct tunneling from the valence band through very thin gate oxides and related floating-body effects, was pointed out.

In non-planar FinFET-like transistors, additional size and coupling effects are induced by the multiple gates. We showed that the corner effect, i.e., the influence of a gate on the threshold voltage of an adjacent gate, is very small when using low-doped bodies or tall fins. The back-gate influence, which can modify the threshold voltage of the device and activate a back-channel, is screened for narrow fins by the strong coupling between the lateral gates. The drain-to-BOX coupling and the radiation effects are also reduced in narrow devices by the interaction of the lateral gates.

This paper addressed a number of SOI mechanisms that require further modeling, characterization and control. However, the use of SOI technology is not debatable. SOI is the necessary solution for extending the miniaturization of CMOS circuits.

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Akiko Ohata received the M.Sc. degree in theoretical physics and Ph.D. degree in electronics from Tokyo Institute of Technology, Japan. She has engaged in research of Si quantum devices, single electron devices and SOI MOSFETs in Toshiba Corporation, RIKEN Institute, Tokyo Institute of Technology, Gunma University and IMEP.

e-mail: ohata@enserg.fr
IMEP Minatec-INPG
3 Parvis Louis Néel
Grenoble BP257, France

Romain Ritzenthaler was born in Rouen, France, in 1980. He received the M.Sc. degree from the Ecole Nationale Superieure de Physique de Grenoble (ENSPG) in 2003, Grenoble, France. He is currently pursuing his Ph.D. degree with the CEA-Laboratoire d'Electronique et Technologie de l'Information (LETI), Grenoble, France. His work is dedicated to the realization, characterization and simulation of the FinFET devices.

e-mail: ritz_romain@hotmail.com
IMEP Minatec-INPG
3 Parvis Louis Néel
Grenoble BP257, France

CEA-LETI
17 avenue des Martyrs
38054 Grenoble cedex 9, France

Sorin Cristoloveanu received the Ph.D. (1976) and the French Doctorat ès-Sciences (1981) from the National Polytechnic Institute, Grenoble, France. He joined the Centre National de la Recherche Scientifique (CNRS) and became a Director of Research in 1989. He worked at JPL (Pasadena) and at the Universities of Maryland, Florida (Gainesville) and Nashville. He served as Director of the LPCS Laboratory and of the Center for Advanced Projects in Microelectronics (CPMA Grenoble). He is the author or co-author of more than 600 technical journal papers and conference presentations (including 80 invited contributions). He authored or edited 15 books, and

organized 14 international conferences. He is a Fellow of IEEE, a Fellow of the Electrochemical Society, and Editor of "Solid-State Electronics".

e-mail: sorin@enserg.fr
IMEP Minatec-INPG
3 Parvis Louis Néel
Grenoble BP257, France

Olivier Faynot received the M.Sc and Ph.D. degrees from the Institut National Polytechnique de Grenoble, France, in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron fully depleted SOI devices fabricated on ultra-thin SIMOX wafers. He joined LETI (CEA-Grenoble, France) in 1995, working on simulation and modeling of deep submicron fully and partially depleted SOI devices. His main activity was the development of a dedicated partially depleted SOI model, called LETI SOI. From 2000 to 2002, he was involved in the development of a sub 0.1 μm partially depleted technology. Since 2003, he is in charge of the development of advanced single and multiple-gate fully depleted SOI technologies with high k and metal gate. He is author and co-author of more than 70 scientific publications on SOI in journals and international conferences. From 2001 to 2003, Doctor Faynot was on the IEEE International SOI Conference Committee. In 2002 and 2003, he was in the International Electron Device Meeting (IEDM) technical committee. Since 2004, Doctor Faynot joined the Solid State Device and Materials (SSDM) Conference Committee.

e-mail: ofaynot@cea.fr
CEA-LETI
17 avenue des Martyrs
38054 Grenoble cedex 9, France