Paper

SiGe HBT wideband amplifier for millimeter wave applications

Marko Krčmar, Nils Noether, and Georg Boeck

Abstract— A wideband amplifier up to 50 GHz has been implemented in a 0.25 μm, 200 GHz f_t SiGe BiCMOS technology. Die size was 0.7×0.73 mm^2. The two-stage design achieves more than 11 dB gain over the whole 20 to 50 GHz band. Gain maximum was 14.2 dB at 47.5 GHz. Noise figure was lower than 9 dB up to 34 GHz and a current of 30 mA was drawn from a 4 V supply. To the author's best knowledge this is the highest gain bandwidth product of a monolithic SiGe HBT amplifier ever reported.

Keywords— wideband amplifier, HBT, SiGe, millimeter wave, bipolar integrated circuits.

1. Introduction

Up to now compound semiconductors dominate the applications in the millimeter wave range. Rapid technological progress in the field of SiGe HBT technology [1] allows to re-think and to apply silicon technologies also for millimeter wave applications. The SiGe BiCMOS technologies allow integration of analog and digital parts, provide high integration densities and save cost. The main purpose of this work is the demonstration of the millimeter wave capabilities of SiGe BiCMOS technologies. A broadband amplifier has been chosen for this reason. The main goal was a gain greater than 10 dB up to 50 GHz and a bandwidth as high as possible. Compared with narrow band designs, the difficulties grow up significantly because of broadband matching circuits and the lossy silicon substrate decreases the overall performance. Because of these reasons only less comparable work has been published so far. To our knowledge SiGe HBT wideband amplifiers have been published just in [2] (bandwidth = 10 GHz) and [3] (1–15 GHz).

2. Device technology

The circuit was fabricated in a commercially available SiGe BiCMOS technology with $f_t = f_{\max} = 200$ GHz [4, 5].

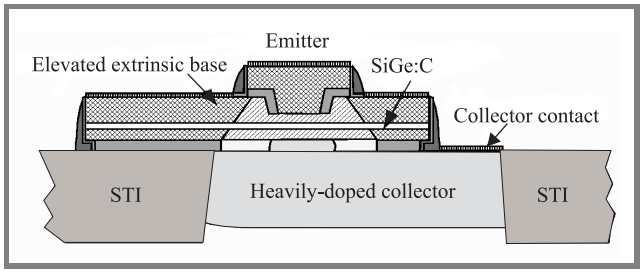

Fig. 1. Schematic cross section of an HBT with elevated extrinsic base.

The HBTs were designed for high performance at low cost. The cross section of the structure is illustrated in Fig. 1. Key features of the device technology are:

- elevated extrinsic base regions self-aligned to the emitter window resulting in low base resistance;
- formation of the whole HBT structure in one active area without shallow trench isolation between emitter and collector contact resulting in low collector resistance and small collector-substrate junction areas;
- device isolation without deep trenches resulting in reduced process complexity and improved heat dissipation.

The HBT module was fabricated in a BiCMOS process after gate patterning and gate spacer formation. During HBT fabrication, CMOS regions are protected with a layer stack that is opened over HBT regions. The HBT fabrication begins with the formation of the collector wells by high-dose ion implantation. The collector wells are laterally confined by shallow trench regions. Next, the active collector region is defined by depositing and patterning on oxide layer. A Si buffer layer, the SiGe:C base layer, and a Si cap layer are grown in one epitaxial step. After epitaxy, a sacrificial layer is deposited, and emitter windows are structured. An additional inside spacer is formed before depositing and structuring the As-doped emitter. Next, spacers are formed at the emitter and the sacrificial layer is removed by wet etching, followed by the self-aligned selective growth of the B-doped extrinsic base. In a reference process without the elevated base, the extrinsic base is formed by ion implantation after emitter structuring as described in [4]. This HBT structure provides low-capacitance isolation from the substrate and low collector resistances.

3. Circuit design

Figure 2 shows the two-stage amplifier, implemented with two cascode stages [6, 7]. Among different architectures this topology has been found to be the best trade-off with respect to gain and bandwidth. The first stage was implemented with the goal of best noise performances. The second one was designed for maximum power gain. Both cascode stages are biased with $V_{CC} = 4$ V and $I_C = 10$ mA and 20 mA, respectively.

Figure 3 shows a photograph of the realized chip. Input/output signal pads are on the left and right side, re-

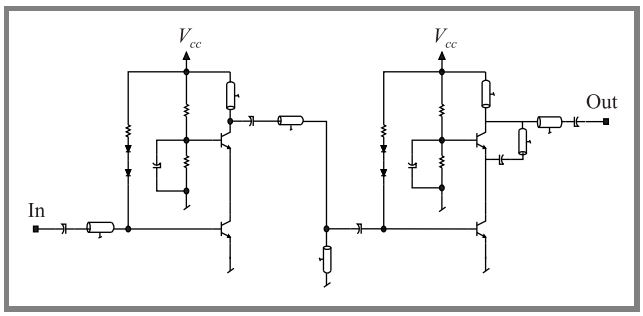

Fig. 2. Simplified schematic of the wideband amplifier.

spectively. The pad structure has been designed for standard GSG on-wafer probing. The three top pads provide the biasing for the whole amplifier in a ground-V_{CC}-ground structure. The identical structure at the bottom side allows the monitoring of the bias voltage. All DC-lines are RF-shorted to ground wherever possible, in order to provide a low ohmic ground for RF-signals. For example, the relatively wide microstrip line in the middle of the chip is a short circuited stub.

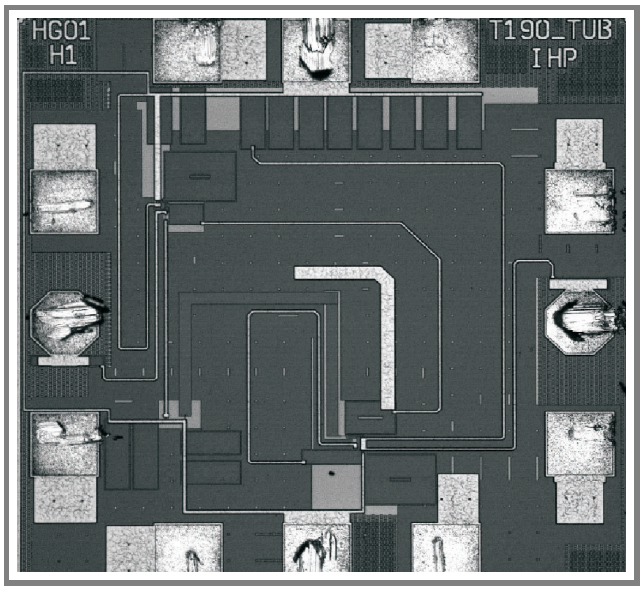

Fig. 3. The photograph of the realized chip.

Because the input impedance of a bipolar transistor shows a dominant real part with week frequency dependence a simple microstrip line was adequate to achieve acceptable 50 Ω-input matching over 20–50 GHz. On the contrary, the output impedance of a bipolar transistor is strongly capacitive and broadband matching is complicated. The solution for this problem was a compensation microstrip line connected in parallel to the output transistor (see Fig. 2). It works as a resonator with a low Q factor and a high bandwidth, neutralizing the parasitic capacitances of the transistor and allowing us to achieve a satisfying 50 Ω-output matching in the 20–50 GHz band. This compensation line not only allows for wideband output matching, but also improves the stability of the amplifier at higher frequencies. A short circuited stub was introduced between the two stages in order to tune the gain flatness, because at the beginning of the design process the gain at the low frequency end of the band was significantly higher. Theoretically this stub is an open circuit for $30 < f < 50$ GHz. Besides of decreasing the gain below 20 GHz we automatically reduced also the risk of instabilities at low frequencies. Once again, microstrip lines were used instead of inductors [8], which were not available, for DC-RF-decoupling. All microstrip lines were realized on the same metal level in order to avoid the coupling between the lines as much as possible [8]. We chose hexagon-shaped signal pads in order to reduce the capacitive coupling between pads and substrate. The die size is 0.7×0.73 mm^2. For the biasing of the cascode transistors a fixed potential provided by a simple voltage divider has been used whereas the common emitter transistors were fed by a diode/resistor combination providing a constant base current. This solution saves chip size and provides at the same time satisfying temperature stability, too.

Wherever possible, the first metal plane, used as ground, was connected with the substrate by p-taps.

Thus, substrate coupling effects are effectively suppressed. This p-taps behave like low ohmic conductors at high frequencies. RF losses are minimized by this way.

4. Results

Seven chips have been characterized from the first wafer run so far with respect to its RF performance. Power supply values and ambient temperature were in all cases 4 V, 30 mA and 25°C, respectively. Figure 4 shows the S_{21} graphs of the ensemble of 7 dies. Besides of one curve we can conclude to a remarkable uniformity and reliability of the semiconductor process technology.

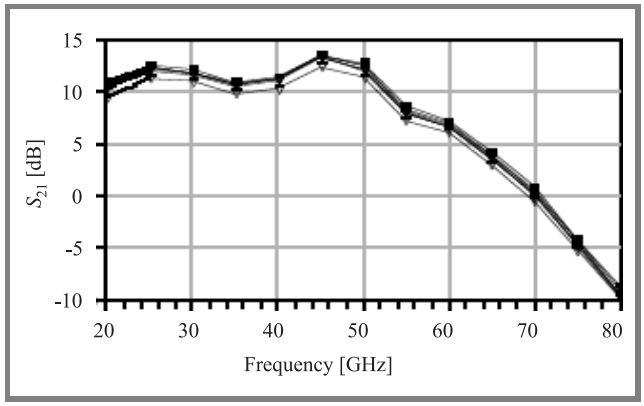

Fig. 4. Measured S_{21} of seven chips ($V_{CC} = 4$ V).

Figures 5a to 5c represent both, measured (squares) and simulated S-parameters. The maximum measured S_{21} achieved is 14.2 dB at 47.5 GHz and more than 11 dB were measured between 20 and 50 GHz (Fig. 5a). Gain flatness

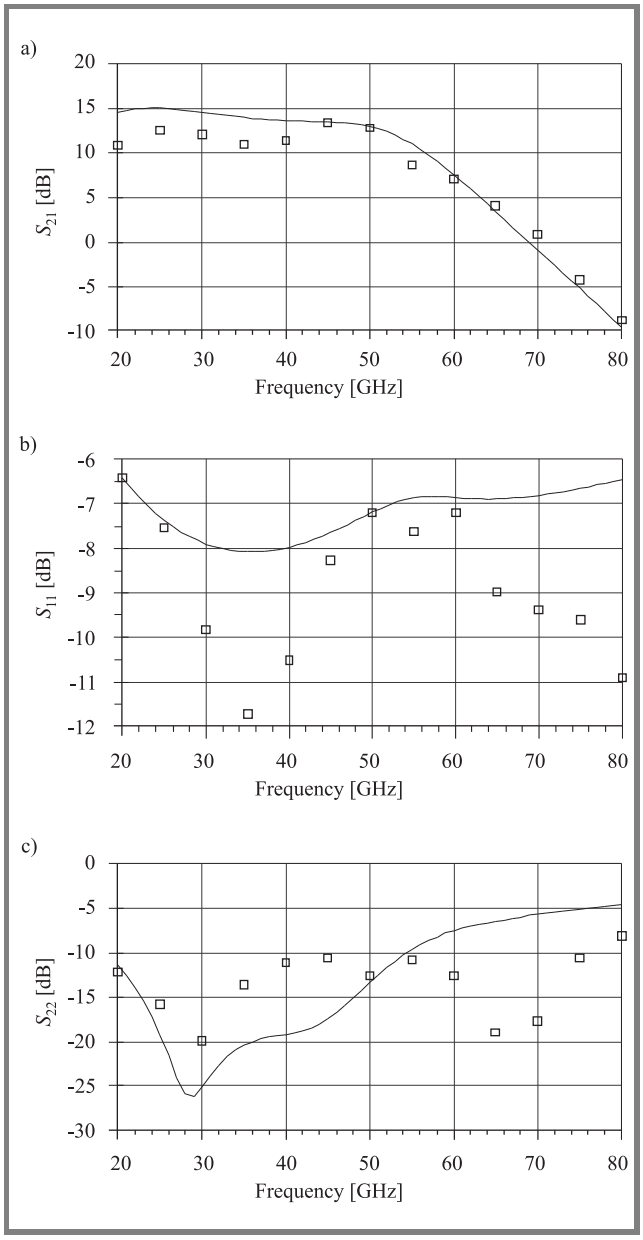

Fig. 5. Simulated and measured: (a) power gain ($V_{CC} = 4$ V); (b) input return loss; (c) output return loss.

within the whole frequency band is about ± 1.6 dB. At the same time, the reverse isolation (not shown) is more than 40 dB from 20–50 GHz. Measured input (Fig. 5b) and output (Fig. 5c) return losses are lower than 6.5 dB and 10 dB, respectively, from 20 to 50 GHz.

4.1. Noise

Noise behavior was measured between 30 and 34 GHz. The band limitation was given by the measurement equipment. Table 1 shows the results. From simulations a *NF* of at least 1 dB lower was expected at these frequencies. According to our simulations best noise values should occur between 40 and 50 GHz in correlation with gain maximum. In that range we expect experimental *NF* values in the order of 7 to 7.5 dB corresponding to simulation results of about 6 dB.

Table 1
Measured noise figure

Frequency [GHz]	*NF* [dB]
30	8.9
31	8.8
33	9.0
34	8.7

4.2. Gain compression

Gain compression was measured and biasing was $V_{CC} = 4$ V and $I_C = 10$ mA and 20 mA, again. The measurements were performed at 47.5 GHz, and an input 1 dB compression point of –10 dBm (Fig. 6) was found corresponding to +3 dBm at the output. This value is slightly higher as predicted by the simulations.

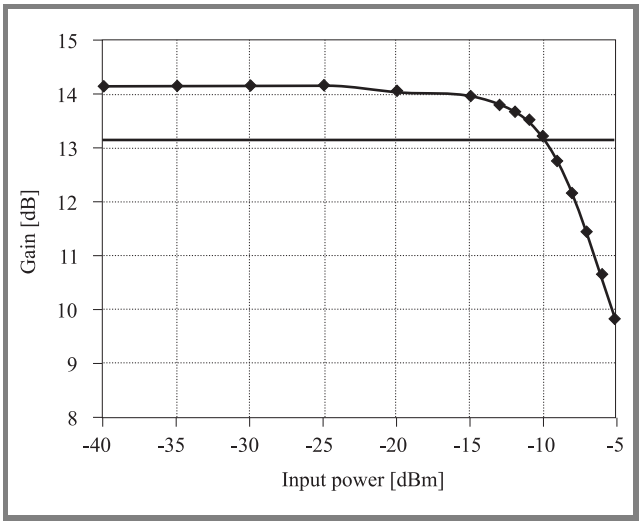

Fig. 6. Gain compression at 47.5 GHz.

The observed discrepancies between measured and simulated results are mainly due to not sufficiently adequate models for the used passive structures in a silicon environment in the millimeter wave region. Verification work at some microstrip discontinuities, transmission lines, vias and substrate coupling effects based on 3D EM simulations showed us considerable discrepancies with circuit simulator based results.
To overcome these problems we are working towards experimental investigation of a passive element library. Based on the characterization of these structures we will establish

a design library containing the models of all passive elements. Using this library we will then re-design the whole amplifier with respect to enhanced performance. Especially with respect to gain, noise and bandwidth we expect considerable improvements.

5. Conclusion

In this work a monolithic wideband amplifier using a SiGe HBT technology has been presented. The chip has been realized on a very low silicon area of 0.7×0.73 mm^2. The main design goals, high bandwidth, more than 10 dB gain within this band and acceptable noise figure and power consumption have been achieved. To the best knowledge of the authors this is the highest gain-bandwidth product ever reported for a monolithic SiGe HBT amplifier. A comparison with state of the art work is given in Table 2.

Table 2
Comparison of state of the art work

Parameter	This work	3–10 GHz LNA [9]
3 dB-frequency range	20–50 GHz	3.1–17.6 GHz
Max. gain	14.2 dB @ 47.5 GHz	22 dB @ 10 GHz
NF	ca. 8 dB	2.7–3.9 dB

Nevertheless, the achieved performance should be improvable if more reliable models for the passive elements are available for the design process. In this case we expect a considerable performance enhancement especially with respect to gain, noise and bandwidth. In case of low power applications the power consumption should be considerably reducible, too.

Acknowledgment

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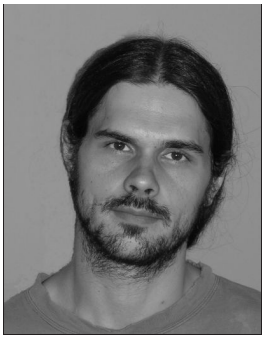

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