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A New Hybrid Topology of D-STATCOM for Power Quality Improvement

N Prazna[1], U Raja Rao[2]

M.Tech Student, Department of EEE, PCET, Anathavaram, India.[1]

Asst. Professor, Department of EEE, PCET, Anathavaram, India.[2]

Abstract— **This work proposes an enhanced new breed conveyance static compensator (D-STATCOM) topology to address some down to earth issues, for example, power rating, filter size, performance of compensation, and power misfortune. A LCL channel has been utilized at the front end of a voltage source inverter (VSI), which gives better exchanging music end while utilizing much littler estimation of an inductor as contrasted and the conventional L channel. A capacitor is utilized as a part of arrangement with a LCL channel to diminish the dc-interface voltage of the D-STATCOM. This thusly diminishes the power rating of the VSI. With decreased dc-connect voltage, the voltage over the shunt capacitor of the LCL channel will be likewise less. It will diminish the power misfortunes in the damping resistor as contrasted and the customary LCL channel with uninvolved damping. Accordingly, the proposed DSTATCOM topology will have lessened weight, cost, rating, and size with enhanced proficiency and current remuneration capacity contrasted and the customary topology. A deliberate system to outline the segments of the uninvolved channel has been displayed. A multilevel fell H-bridge is executed in the VSI operation of a D-STATCOM topology. The viability of the proposed DSTATCOM topology over customary topologies is approved through MATLAB/SIMULINK software.**

Index Terms— **Distribution static compensator (DSTATCOM), multilevel inverter (MLI), cascaded H-bridge, passive filter, power quality (PQ).**

I. INTRODUCTION

Customarily static capacitors and passive filters have been used to enhance power quality (PQ) in a dispersion framework. In any case, these typically have issues, for example, fixed compensation, system-parameter-dependent performance, and possible resonance with line reactance [2]. An appropriation static compensator (DSTATCOM) has been proposed in the writing to beat these disadvantages [3]–[8]. It infuses responsive and sounds segment of load streams to make source ebbs and flows adjusted, sinusoidal, and in stage with the heap voltages. Nonetheless, a conventional DSTATCOM requires a powerful evaluating voltage source inverter (VSI) for load remuneration. The power rating of the DSTATCOM is specifically relative to the current to be remunerated and the dc-connect voltage [10].Generally, the dc-interface voltage is kept up at much higher esteem than the greatest estimation of the stage to-unbiased voltage in a three-stage four-wire framework for palatable pay (in a three-stage three-wire framework, it is higher than the stage to-stage voltage) [2], [10]–[12]. In any case, a higher dc-interface voltage expands the rating of the VSI, makes the VSI substantial, and brings about higher voltage rating of protected door bipolar transistor (IGBT) switches. It prompts to the expansion in the cost, size, weight, and power rating of the VSI. Moreover, customary DSTATCOM topologies utilize a L-sort interfacing channel for forming of the VSI infused streams [13], [14]. The L channel utilizes a substantial inductor, has a low slew rate for following the reference streams, and creates a substantial voltage drop crosswise over it, which, thusly, requires a higher estimation of the dc-connect voltage for legitimate remuneration. Along these lines, the L channel includes cost, size, and power rating. Some half and half topologies have been proposed to consider the previously mentioned restrictions of the customary DSTATCOM, where a diminished rating dynamic channel is utilized with the inactive segments [15]–[21]. In [15] and [16], half and half channels for engine drive applications have been proposed. In [17], creators have accomplished a lessening in the dc-connect voltage for receptive load remuneration. In any case, the lessening in voltage is restricted because of the utilization of a L-sort interfacing channel. This likewise makes the channel greater in size and has a lower slew rate for reference following. A LCL channel has been proposed as the front end of the VSI in the writing to defeat the constraints of a L channel [22]–[25]. It gives better reference following execution while utilizing much lower estimation of uninvolved segments. This likewise decreases the cost, weight, and size of the latent part. Nonetheless, the LCL channel utilizes a comparable dc-interface voltage as that of DSTATCOM utilizing a L channel. Consequently, weaknesses because of high dc-interface voltage are still present when the LCL channel is utilized. Another difficult issue is reverberation damping of the LCL channel, which may push the framework toward insecurity. One arrangement is to utilize dynamic damping. This can be accomplished utilizing either extra sensors or sensor less plans. The sensor less dynamic damping plan is anything but difficult to execute by altering the inverter control structure. It dispenses with the requirement for extra sensors. In any case, higher request computerized channels utilized as a part of these plans may require to be tuned for agreeable execution [26]. Another approach is to go for detached damping. This does not require additional sensor hardware. Be that as it may, inclusion of a damping

resistor in the shunt part of a LCL channel brings about additional power misfortune and diminishes the productivity of the framework [26]. This paper proposes an enhanced half breed DSTATCOM topology where the LCL channel took after by the arrangement capacitor is utilized at the front end of the VSI to address the previously mentioned issues. This topology decreases the extent of the detached segments and the rating of the dc-connect voltage and gives great reference following execution at the same time. Alongside this, a huge lessening in the damping power misfortune is accomplished, which makes this plan reasonable for modern applications. The execution of the proposed topology is approved through the broad reproduction comes about.

II. PROPOSED DSTATCOM TOPOLOGY

A three-phase equivalent circuit diagram of the proposed DSTATCOM topology is shown in Fig. 1. It is realized using

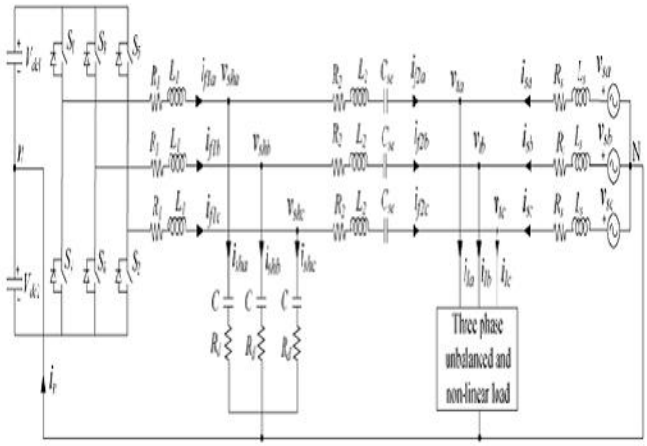

Fig.1. Proposed DSTATCOM topology in the distribution system to compensate unbalanced and nonlinear loads.

a three-stage four-wire two-level nonpartisan point-clasped VSI. The proposed conspire associates a LCL channel at the front end of the VSI, which is trailed by an arrangement capacitor Cse. Presentation of the LCL channel altogether diminishes the span of the detached part and enhances the reference following execution. Expansion of the arrangement capacitor decreases the dc-connect voltage and, subsequently, the power rating of the VSI. Here, R1 and L1 speak to the resistance and inductance, separately, at the VSI side; R2 and L2 speak to the resistance and inductance, individually, at the heap side; and C is the channel capacitance shaping the LCL channel part in every one of the three stages. A damping resistance Rd is utilized as a part of arrangement with C to clammy out reverberation and to give uninvolved damping to the general framework. VSI and channel streams are if1a and if2a, separately, in stage and comparative for different stages. Likewise, voltages crosswise over and streams through the shunt branch of the LCL channel in stage an are given by Vsha and isha, separately, and also for the other two stages. The voltages kept up over the dc-interface capacitors are Vdc1 = Vdc2 = Vdcref . The DSTATCOM, source, and loads are associated with a typical point called the purpose of regular coupling (PCC). Loads utilized here have both straight and nonlinear components, which might be adjusted or lopsided. In the customary DSTATCOM topology considered in this paper, the same VSI is associated with the PCC through an inductor Lf [27]. In the LCL channel based DSTATCOM topology, a LCL channel is associated between the VSI and the PCC [22].

IIa. MULTILEVEL INVERTER TOPOLAGIES

An inverter is an electrical gadget that believers coordinate current (DC) to rotating current (AC); the changed over AC can be at any required voltage and recurrence with the utilization of proper transformers, exchanging, and control circuits. Static inverters have no moving parts and are utilized as a part of an extensive variety of uses, from little exchanging power supplies in PCs, to expansive electric utility high-voltage coordinate current applications that vehicle mass power. Inverters are ordinarily used to supply AC control from DC sources, for example, sun based boards or batteries. The electrical inverter is a high-control electronic oscillator. It is so named in light of the fact that early mechanical AC to DC converters was made to work backward, and therefore were "upset", to change over DC to AC. The inverter plays out the inverse capacity of a rectifier. Sorts in multilevel inverter are talked about underneath. There are three sorts of traditional multilevel inverters to be specific diode clipped, fell H-extension and flying capacitor.

IIb. Cascaded H-Bridges inverter

A solitary stage structure of a m-level fell inverter is shown in fig.2. Every different dc source (SDCS) is associated with a solitary stage full-extension, or H-connect, inverter. Every inverter level can produce three diverse voltage yields, +Vdc, 0, and –Vdc by associating the dc source to the air conditioner yield by various mixes of the four switches, S1, S2, S3, and S4. To get +Vdc, switches S1 and S4 are turned on, while –Vdc can be acquired by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the yield voltage is 0. The air conditioner yields of each of the distinctive full-connect inverter levels are associated in arrangement with the end goal that the incorporated voltage waveform is the aggregate of the inverter yields. The quantity of yield stage voltage levels m in a course inverter is characterized

by m = 2s+1, where s is the quantity of independent dc sources. An illustration stage voltage waveform for a 11-level fell H-connect inverter with 5 SDCSs and 5 full extensions is appeared in figure. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

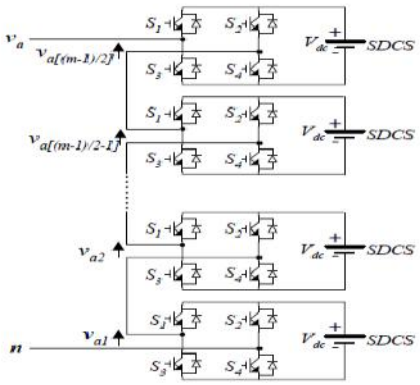

Fig 2 Single-phase structure of a multilevel cascaded H-bridges inverter

III. DSTATCOM CONTROL

The overall control block diagram is shown in Fig. 3. The DSTATCOM is controlled in such a way that the source currents are balanced, sinusoidal, and in phase with the respective terminal voltages. In addition, average load power and losses in the VSI are supplied by the source. Since the source considered. here is non stiff, the direct use of terminal voltages to calculate reference filter currents will not provide satisfactory compensation. Therefore, the fundamental positive sequence components of three-phase voltages are extracted to generate reference filter currents. The equations required for the control of a D –Statcom analyzed through SRF theory with PI controller.(1)

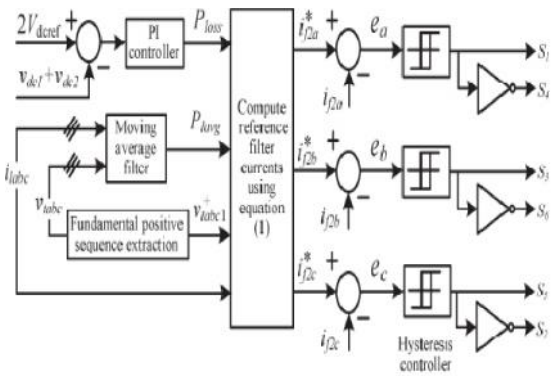

Fig 3 Controller block diagram.

IV.SIMULATION CIRCUITS AND RESULTS

4.1 SIMULATION BLOCK DIAGRAM WITHOUT D-STATCOM/COMPENSATION:

The advantages of the proposed topology are that it uses a lower rating of the VSI, has a smaller value of the filter inductor, reduces the damping power loss, and provides improved current compensation. All these advantages are verified through MATLAB software. System parameters used to validate the performance are given(1). Fig. 3 shows the three phase source currents before compensation which are same as load currents. These currents are unbalanced and distorted due to presence of unbalanced linear and nonlinear loads. Three-phase PCC voltages, as shown in Fig. 4(b), are unbalanced and distorted due to presence of feeder impedance. The performance of the traditional DSTATCOM topology is presented in Fig. 5. The three-phase source currents, which are balanced and sinusoidal, are shown in Fig. 4(a). Fig. 4(b) shows the three-phase PCC voltages. As seen from waveforms, both the source currents and the PCC voltages contain switching frequency components of the VSI. The three-phase filter currents are shown in Fig. 5(c). The waveforms of voltages across upper and lower dc capacitors, as well as the total dc-link voltage, are presented in Fig. 5(d). The voltage across each capacitor is maintained at 520 V, whereas the total dc-link voltage is maintained at 1040 V using the PI controller. The source currents and PCC voltages are balanced and sinusoidal but contain significant switching harmonics ripple. Their percentage total harmonic distortions (THDs) are given (1). To accommodate power losses in the damping resistor, the source currents are slightly increased compared with the traditional topology. Moreover, the total dc-link voltage is maintained at 1040 V (same as the traditional scheme) to achieve load compensation.

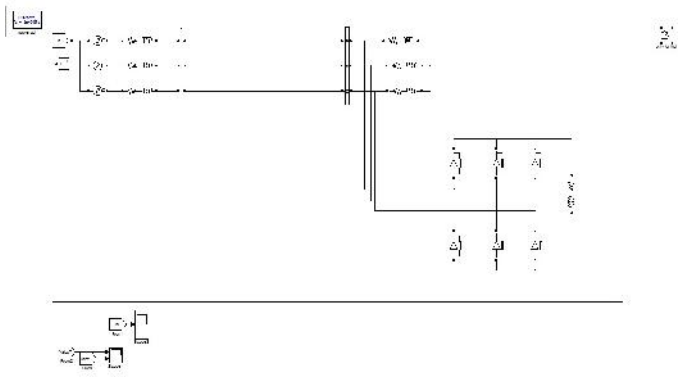

Fig.4.1WITHOUT D-STATCOM/COMPENSATION

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4.2 SIMULATION RESULTS:

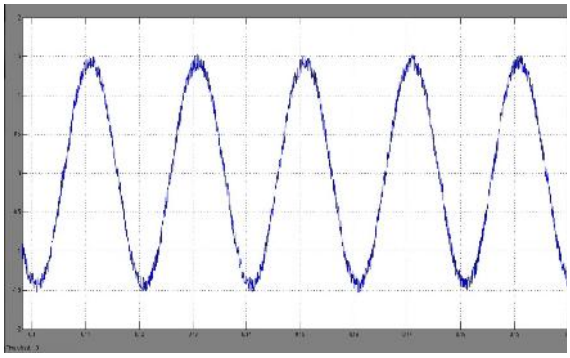


Fig.4.2 (a) wave form for Isa

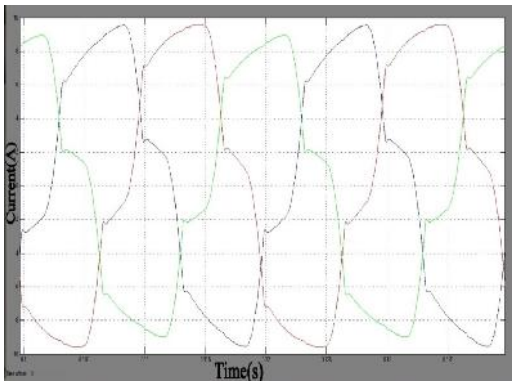


Fig.4.2 (b) Source current:

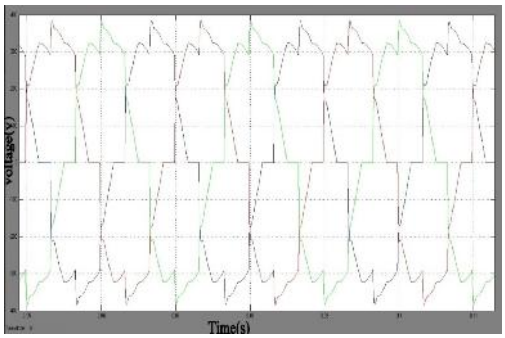
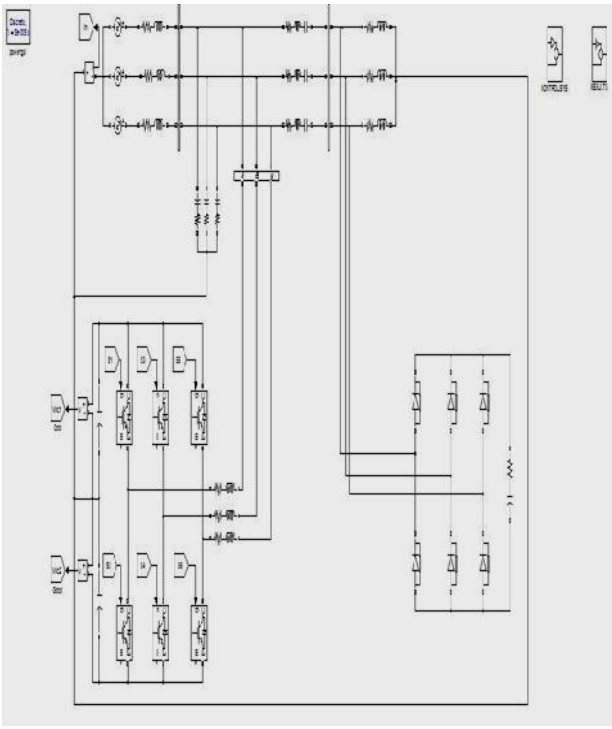


Fig.4.2(C) PCC Voltage

4.3a SIMULATION BLOCK DIAGRAM WITH PROPOSED D-STATCOM:



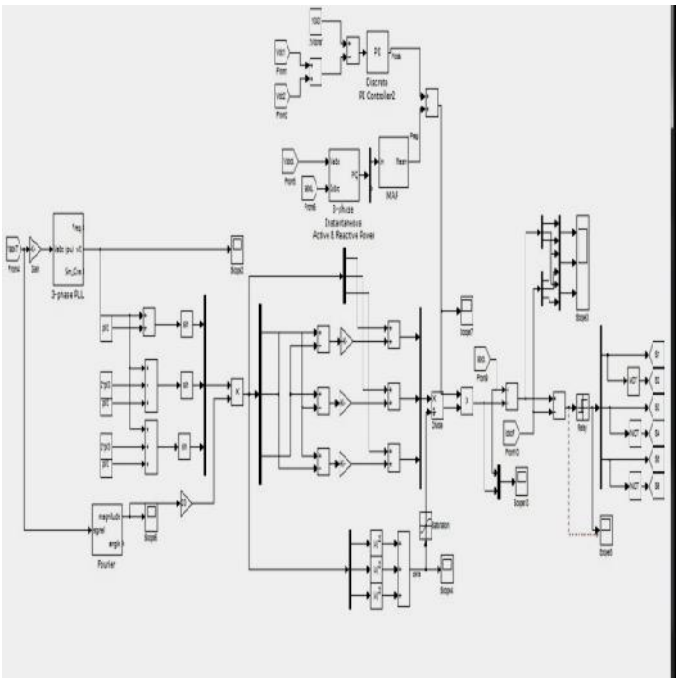


fig 4.3 (b) Control block diagram

4.3.1 SIMULATION RESULTS:

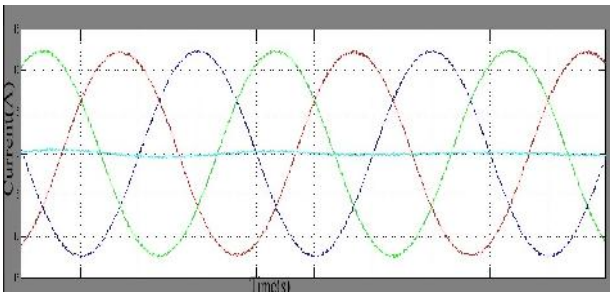


Fig.4.3.1(a)Source currents

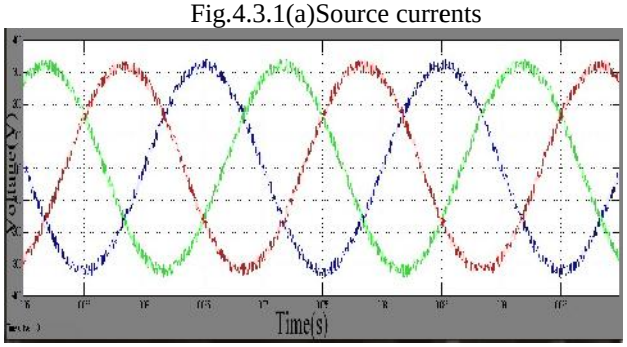


Fig.4.3.1(b) PCC voltages

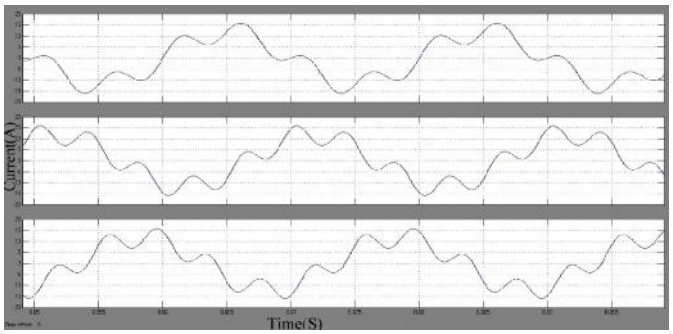


Fig.4.3.1(c) Filter currents

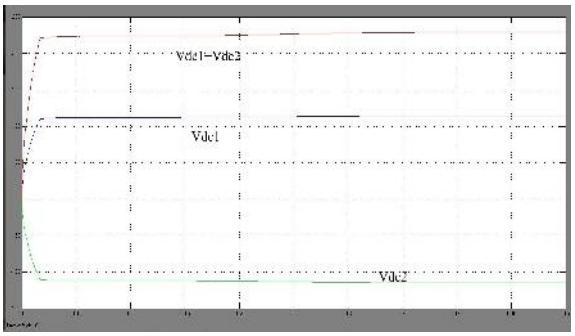


Fig.4.3.1 (d) Voltage across the dc link

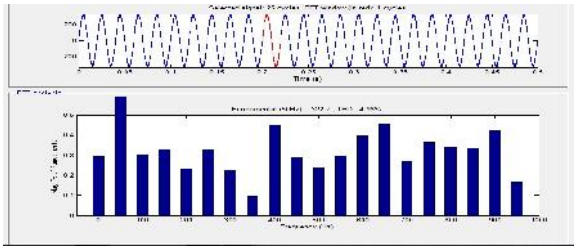
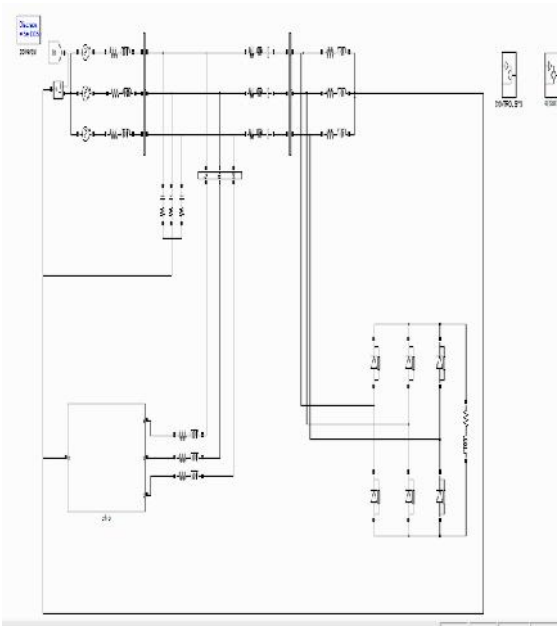
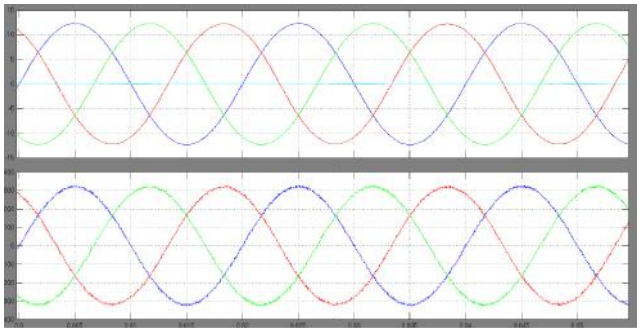


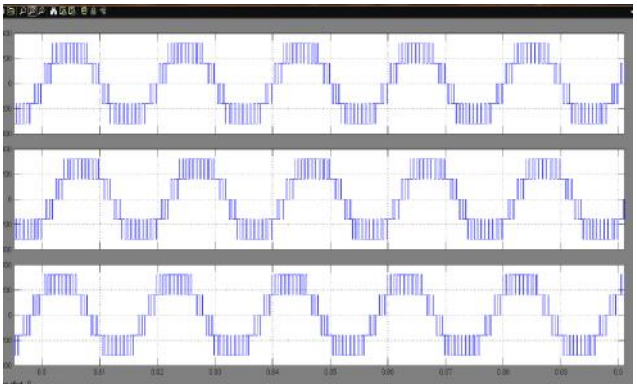
Fig.4.3.1 (e)Reduced Total Harmonic Distortion(4.96%)



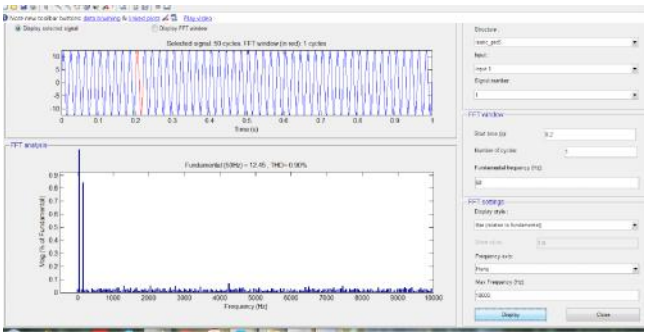
5.1 SIMULINK BLOCK DIAGRAM OF PRAPOSED TOPOLOGY



5.2 Source currents and PCC voltages



5.3 Filter voltages



5.4 Reduced Total Harmonic Distortion(0.9%)

VI.CONCLUSION

In this work, design and operation of an improved hybrid DSTATCOM topology is proposed to compensate reactive and harmonics loads. The hybrid interfacing filter used here consists of an *LCL* filter followed by a series capacitor. This topology provides improved load current compensation capabilities while using reduced dc-link voltage and interfacing filter inductance. Moreover, the current through the shunt capacitor and the damping power losses are significantly reduced compared with the *LCL* filter-based DSTATCOM topology. These contribute significant reduction in cost, weight, size, and power rating of the traditional DSTATCOM topology .A cascaded multilevel inverter D-STATCOM significantly reduces the total harmonic distortion in this project. Effectiveness of the proposed topology has been validated through extensive MATLAB simulation.

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