International Journal of Science Engineering and Advance Technology, IJSEAT, Vol. 4, Issue 5
ISSN 2321-6905
May -2016

International Journal of Science Engineering and Advance Technology

A Comparison between RISC and CISC Microprocessor Architectures

Shahla Gul[1], Noman Aftab[1], Arfa[1], Rani[1]
[1]Department of Computer Science, Abdul Wali Khan University Mardan, KPK, Pakistan
Email: *escallanio@gmail.com

Abstract- In this paper, we have made a comparison between RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer.) RISC and CISC are two different types of microprocessor architectures. RISC is a computer microprocessor that uses simple instructions which can be divided into multiple instructions that performs low level operations within a single clock cycle while CISC is a PC processor which utilizes single direction to execute a few low level operations, for example, stacking from memory, a number juggling operation, and a memory store or are fit for multi-step operations or tending to modes inside single guideline. The principle distinction amongst RISC and CISC is in the quantity of figuring cycles each of their directions take. The distinction in the quantity of cycles depends on the intricacy and the objective of their directions.

I. INTRODUCTION

A reduced instruction set computer (RISC /pronounce as ˈrisk'/) is a computer processor which uses simple instructions that can be divided into multiple instructions which performs low level operations within a single clock cycle, as its name clarify "REDUCED INSTRUCTION SET"RISC (Reduced Instruction Set Computer) is used in portable devices because of its power efficiency Such as Nintendo DS, Apple iPod. RISC is a kind of microchip engineering that utilizations exceptionally upgraded set of directions. RISC decreases the cycles per guideline at the expense of the quantity of directions per program. Pipelining is one of the extraordinary normal for RISC. It is performed by covering the execution of a few guidelines in a pipeline design [1-3]. It has an elite point of interest over the CISC design. The design of a RISC is appeared in Figure 1.

A mind boggling direction set PC (CISC/purport as ˈsisk'/) is a PC processor where single guideline can execute a few low level operations, for example, load from memory, a number-crunching operation and a memory store or are equipped for multi-step operations [4-8] or tending to modes inside single guidelines, as its name clear up "COMPLEX INSTRUCTION SET".

The CISC approach tries to reduce the number of instructions per program, reducing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. As large programs need more storage, so increasing the memory cost and large memory becomes more expensive. To tackle these issues, the quantity of directions per system can be diminished by installing the quantity of operations in a solitary guideline, subsequently making the guidelines more intricate. The engineering of a CISC is appeared in Figure 2.

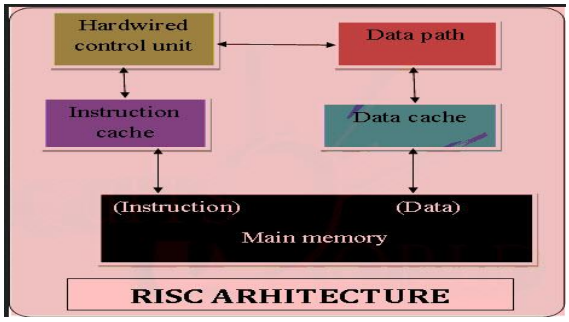

Figure 1: RISC Architecture

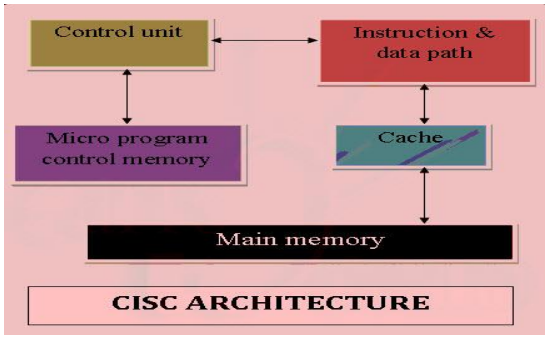

Figure 2: CISC Architecture

II. CHARACTERISTICS of RISC and CISC

RISC architecture uses simple Instructions.RISC supports few simple data types and produces complex data types.RISC permits any register to use in any context.RISC utilizes simple addressing modes and fixed length instructions for pipelining.The amount of work that a computer can perform is reduced by separating load and store instructions.RISC contains a big number of registers to prevent various numbers of interactions with memory.In RISC architecture, Pipelining is easy as the execution of all instructions have to be done in a uniform interval of time i.e. one click.In RISC architecture, more RAM is needed to store assembly level instructions.Reduced instructions need less number of transistors in RISC.Compiler is used for the purpose of to conversion operation means to convert high-level language statement into the code of its form [9-14].

In comparison, CISC has the following characteristics. Instruction decoding is too complex. One instruction is needed to support multiple addressing modes. Less chip space is required enough for general purpose registers for the instructions that are operated directly on memory. Various CISC designs are set up two special registers for the stack pointer, handling interrupts, etc. MUL is referred to as a "complex instruction" and requires the programmer for storing functions [15-17].

III. RISC vs. CISC

RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) are two diverse PC designs that are regularly utilized these days. The primary distinction amongst RISC and CISC is the measure of processing cycles each of their directions thought on playing out a particular capacity [18-26].With CISC, each instruction may use much greater number of cycles before completion than in RISC.The reason behind the difference in number of cycles utilized is the complexity and goal of their instructions. In RISC, each instruction is use to perform a very small task. So if we want some complex task to be done, then we need a lot of these instructions to be combined together. With CISC, each instruction is similar to a high level language code. We only need a few instructions to get what we want as each instruction does a lot.In terms of the list of available instructions, RISC has the longer instructions over CISC. This is because each small step may need a separate instruction [27]unlike in CISC where a single instruction is enough to perform multiple steps. Although CISC may be easier for programmers, it also has its negative aspect [28-36]. Using CISC may not be as proficient as when we use RISC. This is because inefficiencies in the CISC code will then be used again and again, leading to wasted cycles. Using RISC allows the programmer to remove unneeded code and prevent wasting cycles.A simple comparison between these two architecture is shown in Table 1.

CISC	RISC
Emphasizes on hardware	Emphasizes on software
Variable length instruction	Single word instruction
Variable format	Fixed field decoding
Memory Operations	Load and store architecture
Complex Operations	Simple Operations
Includes multi-clock	Single-clock
Complex instructions	Reduced instruction only
Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	Register to register: "LOAD" and "STORE" are independent instructions
High cycles per second, Small code sizes	Low cycles per second, Large code sizes
Transistors used for storing complex instructions	Spends more transistors on memory registers

Table 1: RISC vs. CISC

IV. EXPLANATORY COMPARISON OF CISC AND RISC

A very detailed comparison between RISC and CISC is shown below.

CISC	RISC
1. Very large instruction sets reaching up to and above three hundred separate instructions.	1. Small set of instructions, simplified and reduced instruction set, numbering one hundred instructions or less.
2. Performance was improved by allowing the simplification of program compilers, as the range of more advanced instructions available led to less refinements having to be made at the compilation process. However, the complexity of the processor hardware and architecture that resulted can cause such chips to be difficult to understand and program for, and also means they can be expensive to produce.	2. Because of simple instructions, RISC chips requires less transistors to produce processors. Also the reduced instruction set means that the processor can execute the instructions more quickly, potentially allowing greater speeds. On the other hand only allowing such simple instructions means a greater burden is placed on the software itself. Less instructions in the instruction set means greater emphasis on the efficient writing of software with the instructions that are available.
3. More specialize addressing modes and registers also being implemented, with variable length instruction codes.	3. Addressing modes are simplified back to four or less, and the length of the codes is fixed in order to allow standardization across the instruction set.
4. Instruction pipelining can't be implemented easily.	4. Instruction pipelining can be implemented easily.
5. Many complex instructions can access memory, such as direct addition between data in two memory locations.	5. Only LOAD/STORE instructions can access memory.
6. Mainly used in normal PC's, Workstations and Servers.	6. Mainly used for real time applications.
7. CISC systems shorten execution time by reducing thenumber of instructions per program.	7. RISC systems shorten execution time by reducing the clockcycles per instruction (i.e. simple instructions take lesstimeto interpret).

Table 2: Explanatory Comparison between RISC and CISC

V. Examples Of RISC and CISC

The example of RISC includes but not limited to

- MIPS
- DEC Alpha

- SUN Sparc,
- IBM 801

The example of CISC includes but not limited to

- VAX
- Intel X86
- IBM 360/370

VI. CONCLUSION

We can't differentiate RISC and CISC technology because both are suitable at their specific application. What counts are how fast a chip can execute the instructions it is given and how well it runs existing software. Today, both RISC and CISC producers are doing everything to get an edge on the opposition. To finish up from the above correlation of RISC and CISC (diminished directions set PC and complex guidelines set PC individually.) We understand that RISC is more ideal as far as unpredictability. CISC is excessively mind boggling, making it impossible to comprehend and program which implies they are hard to comprehend and costly to deliver.

REFERENCES

[1]. Khan, F., Bashir, F., & Nakagawa, K. (2012). Dual Head Clustering Scheme in Wireless Sensor Networks. in the IEEE International Conference on Emerging Technologies (pp. 1-8). Islamabad: IEEE Islamabad.

[2]. M. A. Jan, P. Nanda, X. He, Z. Tan and R. P. Liu, "A robust authentication scheme for observing resources in the internet of things environment" in 13th International Conference on Trust, Security and Privacy in Computing and Communications (TrustCom), pp. 205-211, 2014, IEEE.

[3]. Khan, F., & Nakagawa, K. (2012). Performance Improvement in Cognitive Radio Sensor Networks. in the Institute of Electronics, Information and Communication Engineers (IEICE) , 8.

[4]. M. A. Jan, P. Nanda and X. He, "Energy Evaluation Model for an Improved Centralized Clustering Hierarchical Algorithm in WSN," in Wired/Wireless Internet Communication, Lecture Notes in Computer Science, pp. 154–167, Springer, Berlin, Germany, 2013.

[5]. Khan, F., Kamal, S. A., &Arif, F. (2013). Fairness Improvement in long-chain Multi-hop Wireless Adhoc Networks. International Conference on Connected Vehicles & Expo (pp. 1-8). Las Vegas: IEEE Las Vegas, USA.

[6]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "Enhancing lifetime and quality of data in cluster-based hierarchical routing protocol for wireless sensor network", 2013 IEEE International Conference on High Performance Computing and Communications & 2013 IEEE International Conference on Embedded and Ubiquitous Computing (HPCC & EUC), pp. 1400-1407, 2013.

[7]. Q. Jabeen, F. Khan, S. Khan and M.A Jan. (2016). Performance Improvement in Multihop Wireless Mobile Adhoc Networks. *in the Journal Applied, Environmental, and Biological Sciences (JAEBS*), vol. 6(4S), pp. 82-92. Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.

[8]. Khan, F., & Nakagawa, K. (2013). Comparative Study of Spectrum Sensing Techniques in Cognitive Radio Networks. in IEEE World Congress on Communication and Information Technologies (p. 8). Tunisia: IEEE Tunisia.

[9]. Khan, F. (2014). Secure Communication and Routing Architecture in Wireless Sensor Networks. the 3rd Global Conference on Consumer Electronics (GCCE) (p. 4). Tokyo, Japan: IEEE Tokyo.

[10]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "PASCCC: Priority-based application-specific congestion control clustering protocol" Computer Networks, Vol. 74, PP-92-102, 2014.

[11]. Khan, F. (2014, May). Fairness and throughput improvement in multihop wireless ad hoc networks. In *Electrical and Computer Engineering (CCECE), 2014 IEEE 27th Canadian Conference on* (pp. 1-6). IEEE.

[12]. Mian Ahmad Jan and Muhammad Khan, "A Survey of Cluster-based Hierarchical Routing Protocols", in IRACST–International Journal of Computer Networks and Wireless Communications (IJCNWC), Vol.3, April. 2013, pp.138-143.

[13]. Khan, S., Khan, F., & Khan, S.A.(2015). Delay and Throughput Improvement in Wireless Sensor and Actor Networks. 5th National Symposium on Information Technology: Towards New Smart World (NSITNSW) (pp. 1-8). Riyadh: IEEE Riyad Chapter.

[14]. Khan, F., Khan, S., & Khan, S. A. (2015, October). Performance improvement in wireless sensor and actor networks based on actor repositioning. In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 134-139). IEEE.

[15]. Khan, S., Khan, F., Jabeen. Q., Arif. F., & Jan. M. A. (2016). Performance Improvement in Wireless Sensor and Actor Networks. in the Journal Applied, Environmental, and Biological Sciences Print ISSN: 2090-4274 Online ISSN: 2090-4215

[16]. Mian Ahmad Jan and Muhammad Khan, "Denial of Service Attacks and Their Countermeasures in WSN", in IRACST– International Journal of Computer Networks and Wireless Communications (IJCNWC), Vol.3, April. 2013.

[17]. M. A. Jan, P. Nanda, X. He and R. P. Liu, "A Sybil Attack Detection Scheme for a Centralized Clustering-based Hierarchical Network" in Trustcom/BigDataSE/ISPA, Vol.1, PP-318-325, 2015, IEEE.

[18]. Jabeen, Q., Khan, F., Hayat, M.N., Khan, H., Jan., S.R., Ullah, F., (2016) A Survey : Embedded Systems Supporting By Different Operating Systems in the International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.664-673.

[19]. Syed Roohullah Jan, Syed TauhidUllah Shah, Zia UllahJohar, Yasin Shah, Khan, F., " An Innovative Approach to Investigate Various Software Testing Techniques and Strategies", International Journal of Scientific Research in Science, Engineering and Technology(IJSRSET), Print ISSN : 2395-1990, Online ISSN : 2394-4099, Volume 2 Issue 2, pp.682-689, March-April 2016. URL : http://ijsrset.com/IJSRSET1622210.php

[20]. Khan, F., Jan, SR, Tahir, M., & Khan, S., (2015) Applications, Limitations, and Improvements in Visible Light Communication Systems" In *2015 International Conference on Connected Vehicles and Expo (ICCVE)* (pp. 259-262). IEEE.

[21]. Syed Roohullah Jan, Khan, F., Muhammad Tahir, Shahzad Khan,, (2016) "Survey: Dealing Non-Functional Requirements At Architecture Level", VFAST Transactions on Software Engineering, (Accepted 2016)

[22]. M. A. Jan, "Energy-efficient routing and secure communication in wireless sensor networks," Ph.D. dissertation, 2016.

[23]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Lightweight Mutual Authentication Scheme for IoT Objects," *IEEE Transactions on Dependable and Secure Computing (TDSC)*, "Submitted", 2016.

[24]. M. A. Jan, P. Nanda, X. He, and R. P. Liu, "A Sybil Attack Detection Scheme for a Forest Wildfire Monitoring Application," *Elsevier Future Generation Computer Systems (FGCS)*, "Accepted", 2016.

[25]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015, August). DPBSV--An Efficient and Secure Scheme for Big Sensing Data Stream. InTrustcom/BigDataSE/ISPA, 2015 IEEE (Vol. 1, pp. 246-253). IEEE.

[26]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2015). A Dynamic Key Length Based Approach for Real-Time Security Verification of Big Sensing Data Stream. In Web Information Systems Engineering–WISE 2015 (pp. 93-108). Springer International Publishing.

[27]. Puthal, D., Nepal, S., Ranjan, R., & Chen, J. (2016). A dynamic prime number based efficient security mechanism for big sensing data streams.Journal of Computer and System Sciences.

[28]. Puthal, D., &Sahoo, B. (2012). Secure Data Collection & Critical Data Transmission in Mobile Sink WSN: Secure and Energy efficient data collection technique.

[29]. Puthal, D., Sahoo, B., &Sahoo, B. P. S. (2012). Effective Machine to Machine Communications in Smart Grid Networks. ARPN J. Syst. Softw.© 2009-2011 AJSS Journal, 2(1), 18-22.

[30]. M. A. Jan, P. Nanda, M. Usman, and X. He, "PAWN: A Payload-based mutual Authentication scheme for Wireless Sensor Networks*,"* "accepted", 2016.

[31]. M. Usman, M. A. Jan, and X. He, "Cryptography-based Secure Data Storage and Sharing Using HEVC and Public Clouds," *Elsevier Information sciences*, "accepted", 2016.

[32]. Jan, S. R., Khan, F., &Zaman, A. THE PERCEPTION OF STUDENTS ABOUT MOBILE LEARNING AT UNIVERSITY LEVEL. *NO. CONTENTS PAGE NO.*, 97.

[33]. Khan, F., & Nakagawa, K. (2012). B-8-10 Cooperative Spectrum Sensing Techniques in Cognitive Radio Networks. *電子情報通信学会ソサイエティ大会講演論文集*, *2012*(2), 152.

[34]. Safdar, M., Khan, I. A., Ullah, F., Khan, F., & Jan, S. R. Comparative Study of Routing Protocols in Mobile Adhoc Networks.

[35]. Shahzad Khan, Fazlullah Khan, FahimArif, QamarJabeen, M.A Jan and S. A Khan (2016). "Performance Improvement in Wireless Sensor and Actor Networks", Journal of Applied Environmental and Biological Sciences, Vol. 6(4S), pp. 191-200, Print ISSN: 2090-4274 Online ISSN: 2090-4215, TextRoad.

[36]. M. Usman, M. A. Jan, X. He and P. Nanda, "Data Sharing in Secure Multimedia Wireless Sensor Networks," *in 15th IEEE International Conference on Trust, Security and Privacy in Computing and Communications (IEEE TrustCom-16)*, "accepted", 2016.