International Journal of Science Engineering and Advance Technology

Carbon Nanotube based approach on FETs using Ternary Comparator

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Abstract:A Carbon Nanotube Field Effect Transistor (CNFET) is referred to as a FET that utilizes a single Carbon Nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. New approach of ternary magnitude comparator based on the CNFET ternary logic gates. These gates are promising alternative to conventional logic design because of its energy efficiency, it can accomplish by the reduced circuit on ternary logic. Ternary comparator implementation is based on prefix based design and combines ternary and binary logic gates for optimized implementation. A novel approach of a comparator has been implemented and simulated using SPICE. A design response indicates that the 1-bit comparator consumes less power say 0.65µW and has a delay of 21ps. The simulation results for comparators with versatile lengths of operands.

Keywords: Comparator, CNFET, Ternery logic.

I. Introduction

In ternary logic, a three-valued logic is any of several many-valued logic systems in which there are three truth values indicating *true*, *false* and some indeterminate third value. This is contrasted with the more commonly known bivalent logics which provide only for *true* and *false*. Early research on design of ternary logic using CMOS can be found in literature [2] [3]. Carbon nanotube based multilevel voltage mode logic design was presented in [4]. It has been shown that the performance of CMOS technologies can be enhanced by adding MVL blocks to binary ICs [5]. There are two kinds of MVL circuits which are based on MOS technology. One is current mode MVL circuit and the other is voltage mode MVL circuit. Voltage mode MVL is achieved by multi-threshold CMOS design [6]. Multiple threshold values in CMOS can be achieved by using different bias voltages to the bulk terminal of the transistors.
The CNFET is a promising alternative to silicon transistor for achieving low power and high performance [7] [8]. The other advantage of CNFET over CMOS is that the threshold voltage of CNFET is dependent on the device dimensions and specifically to diameter of CNT. Hence design of multi-threshold CNFETS can be accomplished by having CNT with different diameters. A resistive load CNFET based ternary logic design has been proposed in [4]. The disadvantage of this methodology is the need of large off-chip resistances. A more efficient design which avoids the use of resistances is presented in [9]. This methodology relies on the method proposed in [10] & eliminates large resistances by employing active load with p-type CNTFETs in the ternary logic gates. The design of CNFET based ternary arithmetic circuits like 1-bit half adder and 1-bit multiplier is also presented in [9].

II. CNFET

CNFET is a field effect transistor which uses single-wall CNT as the cannel. Owing to a much simpler manufacturing process of CNT, it makes a very promising alternative for the current days MOSFET [7]. The angle of atom arrangement along the tube in a single wall CNT (SWCNT) makes it either conducting or semiconducting. This unique property of the SWCNT is referred to as chirality vector and is represented by the integer pair (*n*,*m*), called the indexes. The nanotube is metallic if *n*=*m* or *n*-*m*=3*i*, where *i*, is integer. If this condition is not met then the nanotube is semiconducting. The diameter of CNT can be calculated by the following equations.

$$D_{CNT} = \left(\frac{\sqrt{3}}{2}\right) a0\sqrt{n2 + m2 + nm} \quad (1)$$

Where, 0.142 nm is the interatomic distance between two carbon atoms. The CNFET also has four terminals as its silicon counterpart. I-V characteristics of MOSFET and those of CNTFET are similar. The voltage required to turn the transistor ON is defined as the threshold voltage. A first order approximation of the threshold voltage of the CNT channel is given by half the bandgap which is an inverse function of the diameter.

$$V_{th} \sim (E_g/2e) = \frac{\sqrt{3}}{3}(aVth/eD_{CNT}) \quad (2)$$

Where a = 2.49 A^0 is the carbon to carbon atomic distance, V_π= 3.033 eV is the carbon π- π bond energy in tight bonding model, e is the electron charge and D_{CNT} is the CNT diameter. From the equation in (2), the threshold voltage of a CNTFET using CNTs with chirality (19, 0), as channels is 0.293V. The DCNT of such a CNT is 1.487 nm, which is obtained from (2). A change in chirality vector changes the threshold voltage of the CNTFET. When the m in the chirality vector is assumed to be always zero, the threshold voltages

ratio of two CNTFETs with different chirality vectors is given by [9].

$$V_{th1}/V_{th2} = D_{CNT2}/ D_{CNT1} = n_2/ n_1 \quad (3)$$

Equation (3) demonstrates that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. Hence the threshold voltage of CNFET can be controlled by changing the chirality vector or the diameter of the CNT [4]. Many advances have been reported in the manufacturing process [14] and synthesis process [15] for fabricating SWCNTs with the desired (n,m) chirality structure. This paper multi-diameter CNFET-based design for ternary logic implementation has been used. The details of the design of CNFET based NTI, STI, PTI, NAND, NOR and ternary decoder are presented in [9].

III. Ternary Logic

Ternary logic is a three valued logic and the functions realized with the three values are called as Ternary logic functions. The values 0, 1 and 2 form the nomenclature to denote the ternary values in this paper. A function *f(X)* is defined as a ternary logic function mapping $\{0,1,2\}^n$ to {0,1,2} where *X* is given by $\{X_1,....X_n\}$.When X_i, X_j = {0,1,2} [9], the basic operations of ternary logic can be defined as follows.

$$X_i+X_j= \max \{X_i, X_j\} \quad (4)$$

$$X_i.X_j = \min \{X_i, X_j\} \quad (5)$$

Where equations (4) and (5) indicate OR and AND operations respectively for ternary logic. The logic symbols for different levels assumed are if voltage level 0, 1/2 Vdd, Vdd then the subsequent Logic value 0, 1, 2. Another important logic gate is an inverter. A general ternary inverter is an operator with one input and three outputs. The Table I shows the ternary inverter truth table where *x* is the input *y0, y1, y2*are outputs. To generate the outputs *y0,y1* and *y2* three inverters are needed namely negative ternary inverter (NTI), standard ternary inverter (STI) and a positive ternary inverter (PTI) respectively.

In ternary logic, the ternary NAND and NOR are multiple entry operators. The truth tables and the definitions of ternary NOR and NAND gates is presented in [9].

Input *x*	NTI (*y0*)	STI (*y1*)	PTI (*y2*)
0	2	2	2
1	0	1	2
2	0	0	0

Table I: Ternary Inverter

IV.Novel GizmoComparator

The proposed design is to generate the $g_j$and e_i signals for each operand bit pairs $A_i$and B_i, where, g_j(greater) indicates $A_i>B_i$ *and* e_i(equal) indicates $A_i=B_i$. The greater and equal signals generated out of each bit positions can be grouped together by grouping logic as presented in [16].

Let $g_i$and e_i indicate the greater and equal signals for i^{th} bit also let $g_j$and e_j indicate the greater and equal signals for $j^{th}$for bit such that $j>i$. Then the grouped greater and equal signals are given by

$$G_{[j:i]} = g_i + e_j . g_i \quad (6)$$

$$E_{[j:i]} = e_j . e_i \quad (7)$$

Where +indicates OR operation and · indicates AND operation. This grouping is done successively until final greater and equal signals indicated by *G [N: 0]* and *E[N: 0]*are obtained. The final greater and equal signals are further used to generatefinal lesser signal *L* using the NOR operation as shown below

$$L_{[N:0]} = G_{[N:0]} + \overline{E_{[N:0]}} \quad (8)$$

***New approach of Ternary comparator*:** In theCNFET based ternary comparator consists of four stages as shown

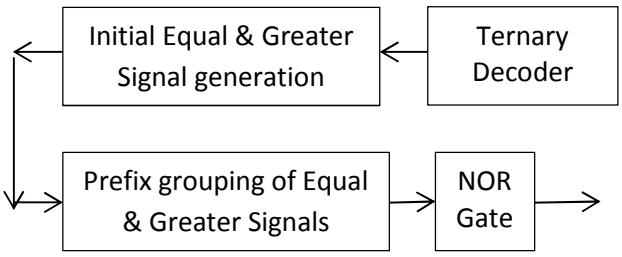

Fig. 1 Ternary Comparator

1) This stage consists of a ternary decoder, whichis a one input 3-output combinational circuit and generatesunary functions for an input x. The response of ternary decoderto the input *x* is given by

$$X_k = \begin{cases} 2, \text{ if } x = k \\ 0, \text{ if } x \neq k \end{cases} \quad (9)$$

Where *k, x* can take logic values of 0, 1, 2. The schematic ofthe ternary decoder is shown in figure 2.The decoder consistsof a PTI gate represented by inverter with '+' sign, two NTIgates, represented by inverters with '-' sign and a NOR gate.

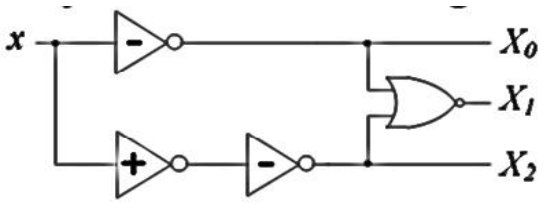

Fig. 2 Ternary Decoder

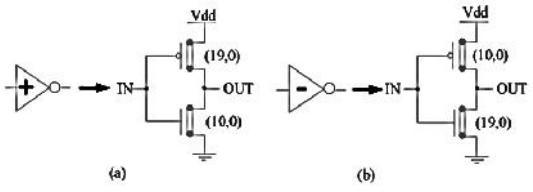

Fig. 3 (a) PTI Gate (b) NTI Gate

ISSN 2321-6905

The design methodology of CNFET PTI and NTI inverter is presented in [9]. The CNFET based PTI schematic diagram is shown in figure 3 (a). The threshold voltage of T1 is 0.557 V and the threshold voltage of T2 is -0.289 V. Therefore, only when the input voltage is higher than 0.6 V, the output voltage is zero. The outputs of NTI and PTI correspond to y0 and y2 of Table I. The CNFET based NTI schematic diagram is shown in figure 3(b). The threshold voltage of T1 is 0.289V, while the threshold voltage of T2 is -0.557V. When the input Voltage is below 0.3V (i.e., logic 0), the output voltage is 0.9 T2 is OFF, and the output voltage will be zero. The NOR gate that is used in the design of decoder is a simple binary logic gate (with logic levels 0 and 2) and can be designed by replacing the MOSFETs in CMOS design with CNFETs.

Ai/Bi	**Eq**	**Gr**	**Eq**	**Gr**	**Eq**	**Gr**
	0	**0**	**1**	**1**	**2**	**2**
0	2					
1		2	2			
2		2		2	2	

Table II KarnaughMap for Equal& Greater signal signal

*2)*This stage consists of a combinational circuit to generate g_i and e_i signals for a 1-bit comparator. The truth table of 1-bit ternary comparator is given in Table III. The karnaugh map of the comparator outputs equal and greater is given in Table II respectively.

A_i	B_i	e_i	g_i
0	0	2	0
0	1	0	0
0	2	0	0
1	0	0	2
1	1	2	0
1	2	0	0
2	0	0	2
2	1	0	2
2	2	2	0

Table III 1-Bit Comparator truth table

The output equations of a 1-bit comparator can be derived from the karnaugh map and are

$$g_i = A_i^1 . B_i^0 + A_i^2 . B_i^0 + A_i^2 . B_i^1 \quad (10)$$

$$e_i = A_i^0 . B_i^0 + A_i^1 . B_i^1 + A_i^2 . B_i^2 \quad (11)$$

Where A_i^k and B_i^k denotes the output of the decoder for theinputs A_i and B_i. This stage uses binary logic gates toimplement (10) and (11). The transistor level implementationof for generation of $g_i$using CNFETs is shown in the figure 4.

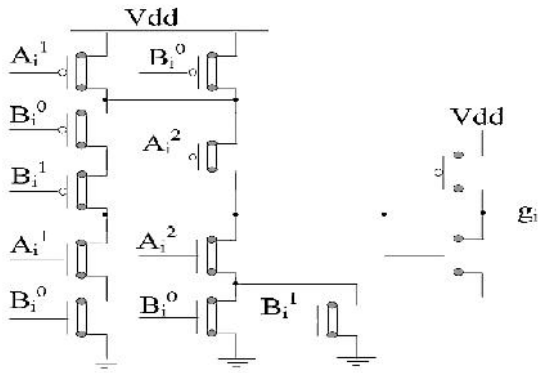

Fig. 4 Greater Signal Generation

All the CNFETs used here will have chirality vector equal to (19, 0). Similarly $e_i$signal is also generated. The equal andgreater signals generated at this stage correspond to the 1-bitcomparison and they act as inputs to the grouping stage.

3) This stage consists of a binary prefix network. At this stage g_i and e_i are grouped according to the equations (6) and (7). As with the previous stage, this stage also uses binary logic gates. For optimized implementation the groupinglogic is designed in such a way that only AOI (AND-OR-INVERT) OrOAI (OR-AND-INVERT) gates are used in the prefix network as shown in the figure 5 for 4-bit comparator.

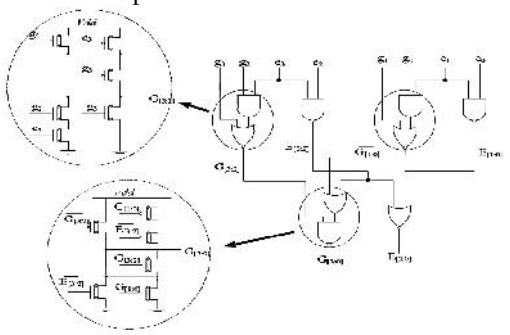

Fig. 5 Prefix grouping stage for 4- Bit Comparator

All the CNFETs used here will have chirality vector equal to (19, 0). This implementation eliminates the need of inverter at the output of each gate. The implementation of OAI and AOI gates is done using CNFETs.

*4)*The final Stage consists of a simple binary NOR gate to generate the lesser signal *L* from the greater and equal signals.

V.Simulation Results

Simulation on all implementations has been performed by HSPICE using the CNTFET model of [11] at 0.9V powersupply and room temperature.

 ISSN 2321-6905

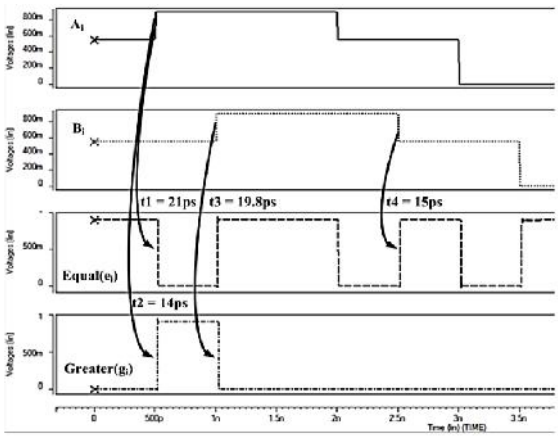

Fig. 6 1-Bit Comparator input & output waveforms

All the CNFETs have used havebeen configured to have three tubes and default pitch valuewhich is equal to 20nm. Figure 5 shows the delay simulationsfor 1-bit comparator Simulation has been performed for 1-bitcomparator stage with greater and equal signals.

The average power consumed by the 1-bit comparator isfound out to be 0.65µW and the power delay product is$13.65x10^{-18}$J.

The table V shows the delay and power results for comparators with different operand lengths.

Operand Length	Delay (ps)	Power (µW)	Power- Delay Product ($x10^{-18}$ J)
2	24.33	1.336	32.5
4	26.76	2.71	72.5
8	29.2	5.45	159.14
16	31.6	10.9	344.44

Table V Comparator result analysis

Conclusion

In this a Novel Gizmo on carbon nanotube FET having a ternary comparator designs. The comparator implementation uses both ternary and binary logic gates. The proposed design is based on prefix structure and is can easily be scaled for any operand length. The proposed ternary comparator design is designed and simulated using SPICE. Simulations results indicate that the proposed 1-bit comparator consumes 0.65µW power and has a delay of 21ps. The result analysis of comparators with different operand lengths is also presented.

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