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Enforce transmission of unnatural power flow of series converter with clamped multi level Neutral point converter

[1]Rangu Seshu Kumar,[2]N.Vijay Kumar
[1]M.Tech(Research Scholar),[2]Assistant Professor,Dept. of EEE in Godavari Institute of Engineering & Technology (GIET),Rajahmundry(A.P),INDIA.
Mail Id: seshumouni@gmail.com

Abstract: In my paper, enforcing of the unnatural power flow in a transmission grid can be controlled by using Unified power flow control (UPFC) to sustain the maximizing power. In the UPFC the direct power is valuable control technique. The direct flow control can be used with any topology of voltage source converter. For series multi level converter non ideal transformers and load. While comparing other controllers we can obtain the better response under balanced and unbalanced conditions. Simulation and experimental results of a full three-phase model with non-ideal transformers, series multilevel converter, and load confirm minimal control delay, no overshoot, no cross coupling. In this paper, the direct power control is demonstrated in detail for a third-level neutral point clamped converter.
Index Terms — Unified power-flow controller (UPFC). Direct power control, multilevel converter, sliding mode control.

I. Introduction

A unified power-flow controller (UPFC) is the most versatile of these flexible AC transmission systems (FACTS) control devices. To enhance the functionality of the ac transmission grid, flexible ac transmission systems (FACTS) support the transmission grid with power electronics. Unless active grid elements are used, the power flow will not follow the path of least impedance, moreover it is uncontrollable. These devices offer a level of control to the transmission system operator.

The major control functions of a UPFC are: (i) active power regulation; (ii) reactive power regulation; and (iii) voltage regulation. The UPFC consists of combined series and shunt devices, and the dc terminals which are connected to a common dc-link capacitor. The series device controls active power flow from the sending to the receiving end by means of adjusting the phase angle of the output voltage. On the other hand, the shunt device performs regulation of the dc-link voltage as well as control of reactive power. The UPFC realizes power flow control, stability improvement; and so on A transmission line equipped with a UPFC can control the balance of the trans-mitted power between parallel lines and, as such, can optimize the use of the transmission grid for all parallel power flows.

A one-wire schematic of a transmission- line system equipped with a UPFC is given in fig A UPFC is connected to the trans-mission line by coupling transformers, both with a shunt and with a series connection. The UPFC consists of two ac/dc converters, the ac sides connected to the shunt and series connection with the transmission line, and the dc sides connected back to back. UPFCs are typically built with voltage -sourced converters, having a capacitor as (limited) dc energy storage.

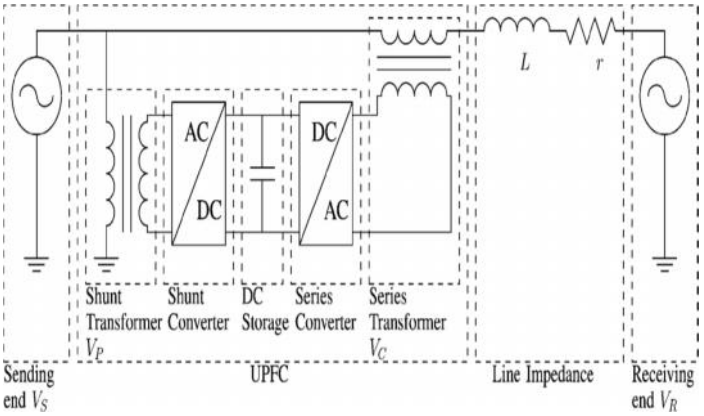

Fig. 1 One-wire schematic of the transmission line with UPFC.

In an overview of the most common control structure for UPFCs is displayed below Fig. 2. An external control describes the set-points of the power system (steady state or dynamic). The internal control describes the actual power electronics and safeties of the UPFC.

The external control is typically divided into a master and middle control. The master control handles targets such as an optimal power system set point, increase of transient stability, or sub synchronous resonance dampening and delivers the middle control set points. Middle control translates these master set points into set points for the series and shunt converter. The internal controller translates these middle-level control set points into switching decisions for the power-electronic components.

Higher level control techniques have primarily focused on optimizing power flow. Later on, the focus shifted to damping sub synchronous resonances of turbine generator shafts and inter area oscillations and transient stability increase. Various methods are used to switch intelligently between higher level control priorities. Recently, a lot of interest into the increase of grid reliability.

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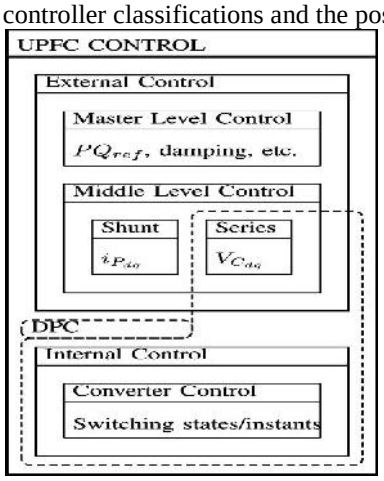
Fig. 2 UPFC controller classifications and the position of the



proposed direct power controller

II. Concepts Of Facts

Power quality:

The term FACTS is used to describe electric power that drives an electrical load and the load's ability to function properly with that electric power.

The electric power industry comprises electricity generation (AC-power), electric power transmission and ultimately electricity distribution to an electricity meter located at the premises of the end user of the electric power. The electricity then moves through the wiring system of the end user until it reaches the load. The complexity of the system to move electric energy from the point of production to the point of consumption combined with variations in weather, generation, demand and other factors provide many opportunities for the quality of supply to be compromised.

Power Quality Issues:

The PQ problems are categorized as follows

1. Transients
(a) Impulsive
(b) Oscillatory
2. Short-duration and Long-duration variations
(a) Interruptions
(b) Sag (dip)
(c) Swell
3. Voltage unbalance
4. Waveform distortion
(a) DC offset
(b) Harmonics
(c) Inter harmonics
(d) Notching
(e) Noise
5. Voltage Flicker
6. Power frequency variations.

Operating Principle Of UPFC:

The basic components of the UPFC are two voltage source inverters (VSIs) sharing a common dc storage capacitor, and connected to the power system through coupling transformers. One VSI is connected to in shunt to the transmission system via a shunt transformer, while the other one is connected in series through a series transformer. The series inverter is controlled to inject a symmetrical three phase voltage system (VSC), of controllable magnitude and phase angle in series with the line to control active and reactive power flows on the transmission line.

A basic UPFC functional scheme is shown in figure below.

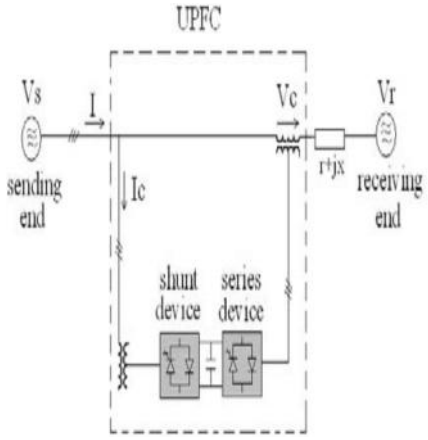


Fig. 3 UPFC functional scheme

So, this inverter will exchange active and reactive power with the line. The reactive power is electronically provided by the series inverter, and the active power is transmitted to the dc terminals. The shunt inverter is operated in such a way as to demand this dc terminal power (positive or negative) from the line keeping the voltage across the storage capacitor V_{dc} constant. So, the net real power absorbed from the line by the UPFC is equal only to the losses of the inverters and their transformers. The remaining capacity of the shunt inverter can be used to exchange reactive power with the line so to provide a voltage regulation at the connection point.

Using the model of Fig.3, differential equations that describe the current i_s in three phases can be formulated.

Voltages $V_{abc} = V_{S_{abc}} + V_{C_{abc}} - V_{R_{abc}}$ are used for notation simplicity.

The differential equations for the UPFC model are given as:

$$L\frac{d}{dt}\begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} = -r \cdot \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} + \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}. \qquad (1)$$

Applying the Clarke and Park transformation results in differential equations in dq space. Voltages

$$V_d = V_{Sd} + V_{Cd} - V_{Rd}$$

and

$$V_q = V_{Sq} + V_{Cq} - V_{Rq}$$

are introduced for notation simplicity. It is assumed that the pulsation ω of the grid is known and varies without discontinuities. Applying the Laplace transformation and with substitution between the two dq space transfer functions (2) is obtained, where current $i_{Sd}(s), i_{Sq}(s)$ are given in function of voltages $V_d(s)$ and $V_q(s)$.

$$\begin{bmatrix} i_{Sd}(s) \\ i_{Sq}(s) \end{bmatrix} = \frac{\frac{1}{L} \cdot \begin{bmatrix} (s+\frac{r}{L}) & \omega \\ -\omega & (s+\frac{r}{L}) \end{bmatrix}}{\left((s+\frac{r}{L})^2+\omega^2\right)} \cdot \begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} \quad (2)$$

The active and reactive power of the power line is determined only by the current over the line and the sending end voltage. Without losing generality of the solution, we synchronize the Park transformation on v_{sa}, resulting in $v_{sq=0}$. Assuming relative voltage stability$V_{sd(s)=}$ v_{sd},$V_{Rdq(S)=}$ V_{Rdq} , . Active and reactive power at the sending end are calculated as

$$p_S(t) = V_{Sd} \cdot i_{Sd}(t) \qquad P_S(s) = V_{Sd} \cdot i_{Sd}(s)$$
$$q_S(t) = -V_{Sd} \cdot i_{Sq}(t) \quad Q_S(s) = -V_{Sd} \cdot i_{Sq}(s). \quad (3)$$

Substituting (2) into (3), we receive the transfer functions, linking $P_{s(S)}$, $Q_{s(S)}$, toV_S ,V_R , and $V_C(S)$. Both active and reactive power consist of an uncontrollable constant part, which is determined by power source voltages, V_S,V_R, and line impedance, L, r and a controllable dynamic part, determined by converter voltage $V_C(S)$, as made explicit in

$$P_S(s) = P_{S0}(V_S, V_R) + \Delta P_S(V_C(s))$$
$$Q_S(s) = Q_{S0}(V_S, V_R) + \Delta Q_S(V_C(s)). \quad (4)$$

Splitting in a constant uncontrollable and a dynamic controllable part results in (5) and (6).For notation simplicity $V_{Cd}(S)$, $V_{Cq}(S)$, are replaced by , $V_{Cd,}$ V_{Cq}

$$P_{S0}(V_S, V_R) = V_{Sd} \cdot \frac{((V_{Sd} \quad V_{Rd}) \cdot r \quad \omega \cdot L \cdot V_{Rq})}{r^2 + (\omega \cdot L)^2}$$
$$Q_{S0}(V_S, V_R) = V_{Sd} \cdot \frac{(V_{Rq} \cdot r + \omega \cdot L \cdot (V_{Sd} - V_{Rd}))}{r^2 + (\omega \cdot L)^2} \quad (5)$$

$$\Delta P_S(V_C(s)) = + V_{Cd}(s) \cdot \frac{V_{Sd} \cdot (L \cdot s + r)}{(L \cdot s + r)^2 + (\omega \cdot L)^2} + V_{Cq}(s) \cdot \frac{V_{Sd} \cdot \omega \cdot L}{(L \cdot s + r)^2 + (\omega \cdot L)^2}$$
$$\Delta Q_S(V_C(s)) = + V_{Cd}(s) \cdot \frac{V_{Sd} \cdot \omega \cdot L}{(L \cdot s + r)^2 + (\omega \cdot L)^2} V_{Cq}(s) \cdot \frac{V_{Sd} \cdot (L \cdot s + r)}{(L \cdot s + r)^2 + (\omega \cdot L)^2}. \quad (6)$$

It is interesting to take a further look at the components of the dynamic part of the active and reactive power $\Delta P_S(s)$, $\Delta Q_S(s)$, especially at the response to steps in series converter injected voltage V_{Cd}/s, V_C/s. Using the initial value theorem on (6), we have It is clear that only $V_{C\,d}(t)$ effects the derivative $d\Delta p_S(t)/dt$ instantaneously, & only $V_C(t)$ effects the derivative $d\Delta q_S(t)/dt$ instantaneously.

$$\lim_{t\to 0+} \frac{d\Delta p_S(t)}{dt} = \lim_{s\to\infty} s \cdot s \cdot \Delta P\left(\frac{V_C}{s}\right) = + \frac{V_{Cd}}{L} \cdot V_{Sd}$$
$$\lim_{t\to 0+} \frac{d\Delta q_S(t)}{dt} = \lim_{s\to\infty} s \cdot s \cdot \Delta Q\left(\frac{V_C}{s}\right) = \frac{V_{Cq}}{L} \cdot V_{Sd}. \quad (7)$$

It is clear that only $V_{C\,d}(t)$ effects the derivative $d\Delta P_S(t)/dt$ instantaneously, & only $V_C(t)$ effects the derivative $d\Delta q_S(t)/dt$ instantaneously.

III Multi level Converter

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits.

Cascaded H-Bridges Inverter:

A single-phase structure of an m-level cascaded inverter is illustrated in Figure Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n \left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right] \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \ldots$$

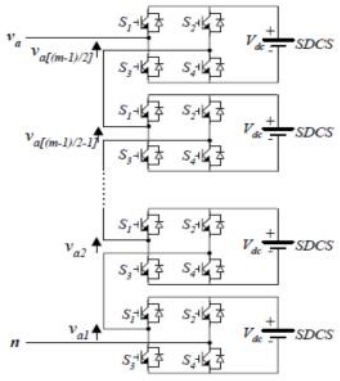


Fig: 4 Single-phase structure of a multilevel cascaded H-bridges inverter

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots$$

Multilevel cascaded inverters have been proposed for such

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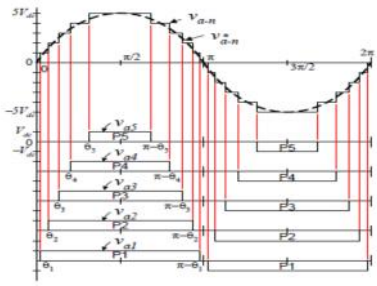


Fig.5 Output phase voltage waveform of an H-level cascade inverter

applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system.

Advantages:

The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).

The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

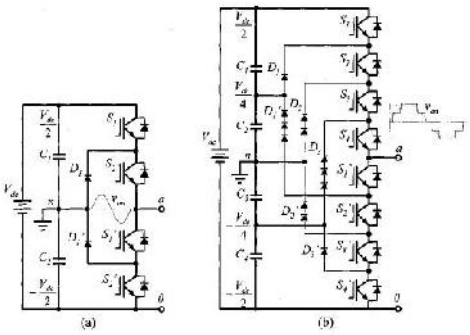
Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

Diode-Clamped Multilevel Inverter:

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static VAR compensation, variable speed motor drives, and high-voltage system interconnections.

The diode clamped multilevel inverter has almost the same structure as the flying capacitor, but instead of capacitors this inverter type uses diodes as clamping devices, creating the desired output voltage. The voltage across each capacitor is defined as $V_{DC}/m-1$, m being the number of levels and $m-1$ the amount of capacitors needed. So, for a two-level inverter the voltage is VDC and for that case one capacitor is used. For a three-level inverter the voltage is VDC/2 and therefore is in need of two capacitors. This specific design makes it possible to increase the number of levels just by increasing the amount of capacitors. In this context the terminology "neutral point clamped" is often used. It describes the neutral point between two capacitors connected across the DC-bus adding an extra level to the system. If m is an even number, the neutral point is not utilized, so then it is usually called a multiple point clamped converter.

Fig. 6 A Diode Clamped converter for a (a) three-level inverter (one phase leg) and for (b) five-level inverter (one phase-leg)



Experience show that higher levels than the three-level converter causes voltage balancing problems, so it is common to use the three-level inverter , but there are studies demonstrating SVPWMs with self balancing systems.

In the fig(b)there are five possible voltage outputs (Van): VDC/2, VDC/4, 0, VDC/4 and VDC/2 and they operate as seen in below Table.

Van	Switches (ON)
VDC/2	S1-S4
VDC/4	S2-S4 and S1'
0	S3,S4,S1',S2'
-VDC/4	S4,S1'-S3'
-VDC/2	S1'-S4'

Table.1 Duty cycle for the switches in one phase leg (five-level inverter)

Reaching higher levels decreases the lower harmonics and the need for filters, but at the same time it magnifies the need for clamping diodes. Advantages with the diode-clamped inverter are the high efficiency. This because all the devices are switched at the fundamental frequency. The diode-clamped inverter also has a easy reactive power control application, but has difficulties controlling the real power for the individual converters.

Three-Level Neutral Point Clamped Converter:

A schematic of a three-level neutral point clamped converter is given in Figure. Each leg of the converter consists of four switching components S_{K1},S_{K2} ,S_{K3} , and two diodes and D_{K1}, andD_{k2} .The diodes D_{K1},$D_{K2\ clamp}$ the voltages of the

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connections between S_{K1},S_{K2} ,andS_{K3} ,S_{K4} , respectively, to the neutral point, between capacitorsC_1 ,C_2 .There are three possible switching combinations for each leg K, thus three voltages U_{mk}. The three levels for voltages U_{mk} produce five different converter phase-output voltages .The upper and lower leg currents I_K,$I_{K'}$ or their respective sum i, i' can be described in function of the output line currents i_K. The system state variables are the line currents i_1 ,i_2 ,i_3 , and the capacitor voltages U_{C1},U_{C2} [32]. is system has the dc-bus current i_0 and the equivalent load source voltages U_{eqk} as inputs. Under the assumption that the converter output voltages U_K are connected to an r_{eq}, L_{eq} system with a sinusoidal voltage source U_{eq} With isolated neutral,

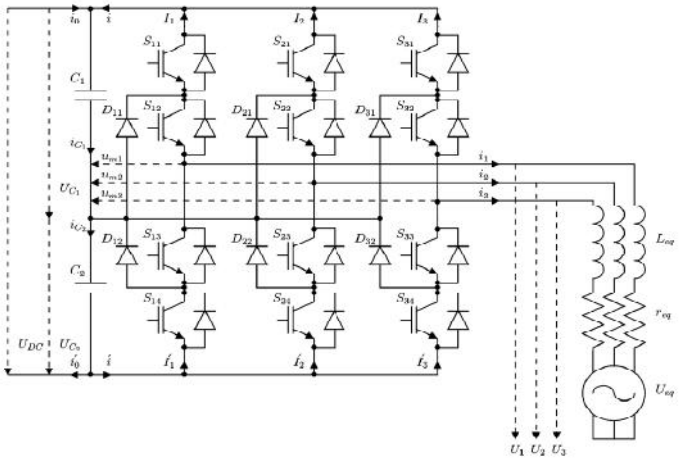

Fig. 7 Three level neutral point clamp converter

As in Fig, we can write the equations for the three-phase currents i_1, i_2,i_3 as in

$$L_{eq} \cdot \frac{di_k}{dt} = U_k - r_{eq} \cdot i_k - U_{eqk} \qquad (8)$$

The capacitor voltages U_{C1},U_{C2} ,are infl0nced by the sum of the upper and lower leg currents i,i' and the input current i_0,$i_{0'}$as in

$$\frac{dU_{C_1}}{dt} = \frac{i_{C_1}}{C_1} = \frac{i_0 + i}{C_1}$$
$$\frac{dU_{C_2}}{dt} = \frac{i_{C_2}}{C_2} = \frac{i_0' + i'}{C_2}. \qquad (9)$$

From the restrictions on the states of the switching devices in each leg of the converter, we can define the ternary variable $\Upsilon_k(t)$, representing the switching state of the entire leg, as

$$\gamma_k(t) = \begin{cases} (S_{k1}, S_{k2} = \text{on}) \wedge (S_{k3}, S_{k4} = \text{off}) & \rightarrow \quad 1 \\ (S_{k2}, S_{k3} = \text{on}) \wedge (S_{k1}, S_{k4} = \text{off}) & \rightarrow \quad 0 \\ (S_{k3}, S_{k4} = \text{on}) \wedge (S_{k1}, S_{k2} = \text{off}) & \rightarrow -1. \end{cases} \qquad (10)$$

To simplify notation, combinations of this variable, Υ_k, Γ and are introduced With this variable $\Upsilon_k(t)$, and the derived variable and straightforward equations can be found for the description of the other variables in the system. Combining the equations of the system dynamics (8) and (9),

$$\Gamma_{1k} = \frac{\gamma_k}{2} \cdot (1 + \gamma_k)$$
$$\Gamma_{2k} = \frac{\gamma_k}{2} \cdot (1 - \gamma_k) \qquad (11)$$
$$\Gamma_1 = [\Gamma_{11} \quad \Gamma_{12} \quad \Gamma_{13}]$$
$$\Gamma_2 = [\Gamma_{21} \quad \Gamma_{22} \quad \Gamma_{23}] \qquad (12)$$
$$\Xi = \frac{1}{3} \cdot \begin{bmatrix} 2\cdot\Gamma_{11} - \Gamma_{12} - \Gamma_{13} & 2\cdot\Gamma_{21} - \Gamma_{22} - \Gamma_{23} \\ -\Gamma_{11} + 2\cdot\Gamma_{12} - \Gamma_{13} & -\Gamma_{21} + 2\cdot\Gamma_{22} - \Gamma_{23} \\ -\Gamma_{11} - \Gamma_{12} + 2\cdot\Gamma_{13} & -\Gamma_{21} - \Gamma_{22} + 2\cdot\Gamma_{23} \end{bmatrix}. \qquad (13)$$

the complete system equation is (14) [32], where Υ_{123} , $\Upsilon_1(\Upsilon_{123})$, $\Upsilon_2(\Upsilon_{123})$, are aiding functions describing the precise dynamics in function of the switching state. It is important to realize that this system equation is not constant, nor continuous.

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ U_{C_1} \\ U_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_{eq}} \cdot I_3 & \frac{\Xi(\gamma_{123})}{L_{eq}} \\ -\frac{\Gamma_1(\gamma_{123})}{C_1} & 0_{1,2} \\ -\frac{\Gamma_2(\gamma_{123})}{C_2} & 0_{1,2} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ U_{C_1} \\ U_{C_2} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L_{eq}} \cdot I_3 & 0_{3,1} \\ 0_{1,3} & \frac{1}{C_1} \\ 0_{1,3} & \frac{1}{C_2} \end{bmatrix} \cdot \begin{bmatrix} U_{eq1} \\ U_{eq2} \\ U_{eq3} \\ i_0 \end{bmatrix}. \qquad (14)$$

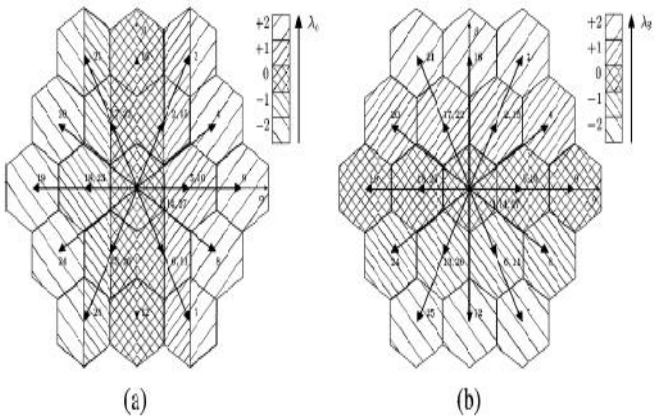

Fig. 8 Vector arrangement in five levels in α,β, for three-level three-phase converter.
(a) Five levels in, α,Υ_α. (b) Five levels in β,Υ_β

Flying Capacitor Multilevel Inverter:

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 . The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Fig.7. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

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The flying capacitor is also known as the capacitor clamped inverter, because of its independent capacitors clamping the voltage to one capacitor voltage level . The structure of the system is formed as a ladder and the voltage of each capacitor is different from the other. When the voltage between two side by side placed capacitors increases, it transmits the size of the voltage steps in the output waveform.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels for the multilevel flying capacitor is static VAR generation. The main advantages and disadvantages of multilevel flying capacitor converters are as follows.

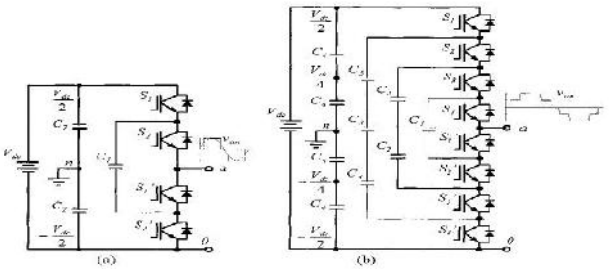

Fig. 9 Circuit of a Flying Capacitor (a) two-level converter for one phase leg (b) three-level converter for one phase leg

Advantages:

Phase redundancies are available for balancing the voltage levels of the capacitors.

Real and reactive power flow can be controlled.

The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages:

Control is complicated to track the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and startup are complex.

Switching utilization and efficiency are poor for real power transmission.

The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

IV Direct Power Control

Direct power control must ensure that the sending end power $P_S(t),q_S(t)$, follows power references $P_{Sref}(t),q_{Sref}(t)$, .Defining the strong relative degree of the controlled output $P_S(t),q_S(t)$, as the minimum i th-order time derivative $d^i(P_S(t))/dt^i$, $d^i(q_S(t))/dt^i$,, that contains a nonzero explicit function of the control vector V_C , a suitable sliding surface is a linear combination of the phase canonical state variable errors.For $P_S(t)$, and $q_S(t)$,i=1,then

$$s_d(t)=K\cdot(p_{Sref}(t)-p_S(t))=K\cdot(\Delta p_{Sref}(t)-\Delta p_S(t))=0$$
$$s_q(t)=K\cdot(q_{Sref}(t)-q_S(t))=K\cdot(\Delta q_{Sref}(t)-\Delta q_S(t))=0. \quad (17)$$

In (17),K is a strictly positive constant; therefore, the only possibility for the system to uphold the surface equations $S_d(t)$,$S_q(t)=0$, is having the real power $P_S(t),q_S(t)$, follow the references, $P_{Sref}(t)$, $q_{Sref}(t)$. A control law that enforces the system to stay on these surfaces, or move toward them at all times.

$$s_d(t)\cdot\dot{s_d}(t)<0$$
$$s_q(t)\cdot\dot{s_q}(t)<0$$

Where $S_d(s)$,$S_q(s)$, are governed by system dynamics involved (6). To uphold (18), the inverter has to appropriately change the sign of the derivatives $S_d(t)$,$S_q(t)$ .Using the results of the initial value theorem on the derivative of the sending end power in (7), the following equation can be developed:

$$\lim_{t\to 0+}\frac{ds_d(t)}{dt}=\lim_{s\to\infty}s\cdot s\cdot S_d(s)=\lim_{s\to\infty}K\cdot s\cdot s\cdot(\Delta P_{Sref}(s))-K\cdot\frac{V_{Cd}}{L}\cdot V_{Sd}$$
$$\lim_{t\to 0+}\frac{ds_q(t)}{dt}=\lim_{s\to\infty}s\cdot s\cdot S_q(s)=\lim_{s\to\infty}K\cdot s\cdot s\cdot(\Delta Q_{Sref}(s))+K\cdot\frac{V_{Cq}}{L}\cdot V_{Sd}. \quad (19)$$

From (19), it can be concluded that to instantaneously influence, $S_d(t),V_{Cd}(t)$ should be used. Similarly, for $S_q(t)$, it is done best by $V_{Cq}(t)$. It is also clear from (19) that impulse or step changes inΔ $P_{Sref}(t)$, $\Delta q_{Sref}(t)$, cannot be followed instantaneously, yet ramps in $\Delta P_{Sref}(t)$, $\Delta q_{Sref}(t)$, can be followed, providing their rate of change is less than (max $(V_{Cd})/L)$, $V_{Sd}(\max(V_{Cq})/L)$, V_{Sd} , and the combination cannot exceed

$$\frac{d\Delta p_{Sref}(t)}{dt}^2+\frac{d\Delta q_{Sref}(t)}{dt}^2<\frac{V_{Cmax}}{L^2}^2\cdot V_{Sd}^2. \quad (20)$$

Considering this conclusion, it is important to determine the conditions to reach the direct power control surfaces using the final value theorem

$$\lim_{t\to\infty}s_d(t)=\lim_{s\to 0}s\cdot S_d(s)=\lim_{s\to 0}K\cdot s\cdot(\Delta P_{Sref}(s))-K\cdot\frac{V_{Sd}}{r^2+\omega^2\cdot L^2}\cdot(V_{Cd}\cdot r+V_{Cq}\cdot\omega\cdot L)$$
$$\lim_{t\to\infty}s_q(t)=\lim_{s\to 0}s\cdot S_q(s)=\lim_{s\to 0}K\cdot s\cdot(\Delta Q_{Sref}(s))-K\cdot\frac{V_{Sd}}{r^2+\omega^2\cdot L^2}\cdot(V_{Cd}\cdot\omega\cdot L-V_{Cq}\cdot r). \quad (21)$$

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From (21), several important conclusions can be drawn. The control can only handle limited steps or ramps of decaying derivative in references, $\Delta P_{Sref}(t)$, $\Delta q_{Sref}(t)$. Also, a clear limit exists to the controllable reference steps, limited by the maximum UPFC series output voltage amplitude, V_{Cmax} as

$$\Delta p_{\mathrm{Sref}}(t)^2 + \Delta q_{\mathrm{Sref}}(t)^2 < {V_{Sd}}^2 \cdot \frac{{V_{\mathrm{Cmax}}}^2}{r^2 + \omega^2 \cdot L^2}. \qquad (22)$$

In the selection *Power to desired change in λ* of Fig., the implementation of 19 exists. To select a physical voltage vector, this decision process is transformed to the αβ domain, remaining with requested changes of the UPFC series output voltage in αβ to the output voltage vector. To limit the switching frequency, the decision is suppressed until the system state crosses a parallel surface at a certain distance from the direct power control surfaces ΔS . Note that this requested change is not expressed in a numeric value of the requested change, but as the direction of change (in this case, a ternary variable, indicating increase +1 , no change 0, decrease -1). Depending on the currently used output vector and the requested change in αβ, an appropriate next vector can be selected. This concludes the converter topology independent part of the controller.

In Fig., in the selection *Desired change in λ to output Voltage*, for a three-level NPC converter, the voltage vector selection is displayed. DPC demands increasing or decreasing the output voltage vector in the α and β direction. Based on the currently applied vector and this demand, the next vector is selected. This is simplified to selection of the voltage vector levels λ_α, λ_β . In the cases that vectors coincide, an extra criterium is needed to unambiguously select a set of switching

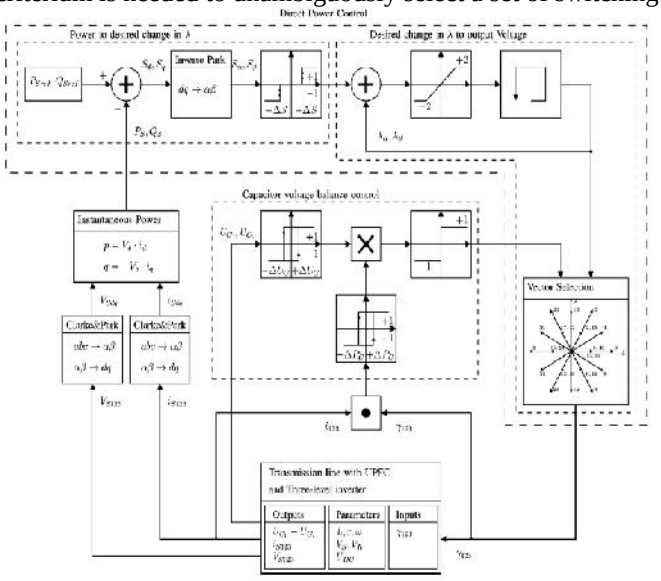

Fig. 10 Overview of control algorithm

$$\mathbb{N}\,\alpha, \beta.\,(\mathrm{a})\,U_{C_1} - U_{C_2} \cdot P > 0.\,(\mathrm{b})\,U_{C_1} - U_{C_2} \cdot P < 0$$

state variables ,$\Upsilon_1, \Upsilon_2, \Upsilon_3$. Even though the voltage vectors may realize the same phase voltages U_1 ,U_2,U_3 ,the precise switching state $\Upsilon_1, \Upsilon_2, \Upsilon_3$, also determines whether energy is drawn or injected from or into capacitors U_{C1} and U_{C2}

$$(U_{C_1} - U_{C_2}) \cdot \frac{d(U_{C_1} - U_{C_2})}{dt} < 0. \qquad (23)$$

To maintain voltage balance U_{C1}-U_{C2}=0, (23) must be upheld at all times. This is displayed in Fig. 6 in selection *Capacitor voltage balance control*. Depending on the sign of the voltage unbalance U_{C1}-U_{C2} and output power P, the voltage vector can be selected so that is upheld. Vector selection, in function of demand for change of the voltage vector in αβ , dimension and capacitor voltage unbalance U_{C1}-U_{C2} is given in Table II(a) and (b). To limit the output frequency, the size of the voltage unbalance has to reach a certain level ΔU_C before it is addressed. In this application, it is enforced by a relay system. The last degree of freedom is within the selection of the null vector 1, 14, 27. They have the same effect on the output voltage U and capacitor voltage imbalance U_{C1}-U_{C2}. To minimize the switching losses, the null vector could be chosen within least switching distance from the previous vector. As such, any order from a higher controller to change the output voltage U in αβ is translated unambiguously into a voltage-output vector. This voltage vector selection method is well covered, including the necessary balancing of the capacitor voltages.

V Simulation Results

The controller is demonstrated in simulation and in experimental results.

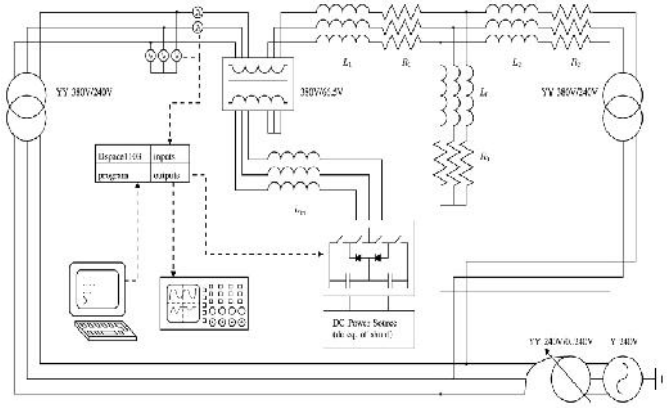

Fig. 11 laboratory setup

Fig. shows the experimental setup. A D Space controller board is used. For controlled startup and ease of use, an autotransformer is used to regulate the mains voltage on the setup. Two isolation transformers are connected to the autotransformer, to represent the sending and receiving end voltages, Iron cored coils are used to represent the load impedance , and transmission-line impedances and. Another step down isolation transformer is used for the series connection of the UPFC inverter to the grid. The values of the separate components are given in Appendix A. Both the simulation and experimental setups use these parameter values so that results can be compared.

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Simulation: The simulation is based on a full three-phase model of the UPFC and the power lines constructed with Matlab Simulink. It is performed on a balanced model of the experimental setup. It contains a model of the converter based on the dynamic equations and control laws. UPFC shunt converter and dc capacitor dynamics are included in the system model.

Mainly The simulation diagram has four stages.(1) sending end (2) UPFC (3) line impedance (4) receiving end.

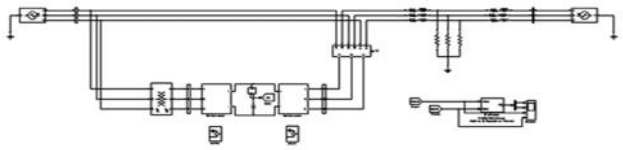

Fig. 12 Simulation Diagram

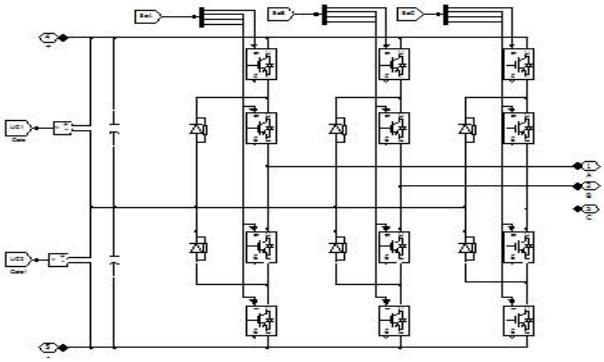

Fig. 13 Simulation diagram for shunt converter:

The shunt converter is set to control the total dc voltage level of the converter dc bus.

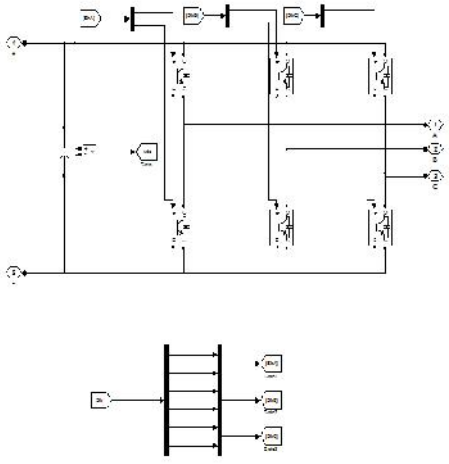

Fig. 14 Simulation diagram for series converter

No reactive power transfer between the shunt converter and the sending end bus is set; the sending and receiving end are simulated as infinite bus.

The transformers are modeled as saturable transformers. In the first set of results, the DPC method is put to demonstrate power-flow control. In a second set, the DPC method is compared in simulation to two other controllers in normal and unbalanced conditions, to demonstrate the superior performance of the DPC method.

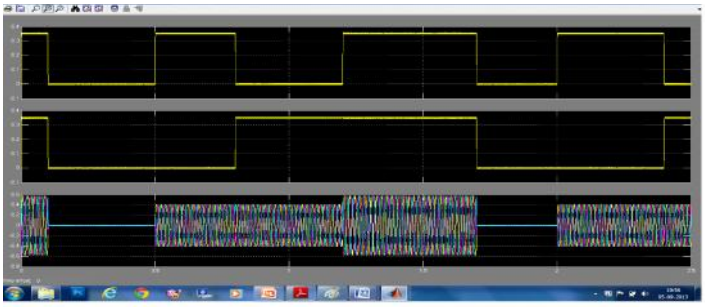

Fig. 15 DPC power-flow control

In simulation P_{Sref},q_{Sref} take values of 0 to 0.316 p.u. and change stepwise. It should be noted that the references, do not represent a realistic reference profile. An overview of 2.5 s of the closed-loop controlled output in Fig. 16 demonstrates that the system can handle any combination of sending end power references P_{Sref}, q_{Sref} and reference changes.

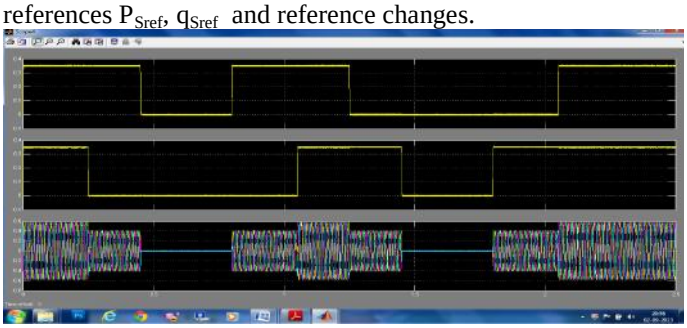

Fig. 16 Closed-loop Controlled Output

UPFC series converter controlling power flow under balanced condition Taking the of P_{sref} ,q_{Sref} Are step wise change, The time is 2.5s the closed-loop controlled output in Fig. demonstrates that the system can handle any combination of sending end power references P_{Sref}, q_{Sref} and reference changes

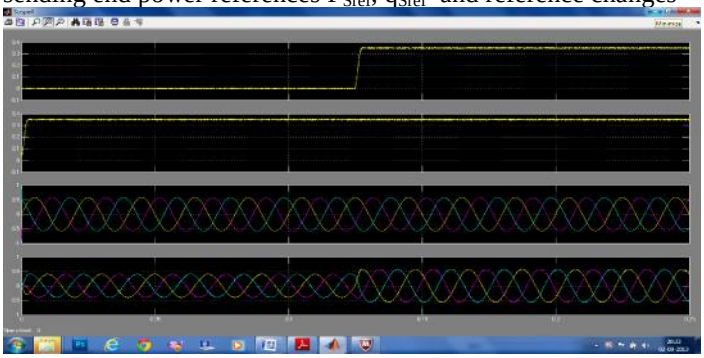

Fig. 17 Stepwise change in active & reactive power flow.

UPFC series converter controlling power flow under balanced condition 250-ms view during stepwise change in active &reactive power flow. Fig. shows that there are no low-frequency phenomena in the currents, and that they are balanced. The direct power controlled system demonstrates no overshoot,

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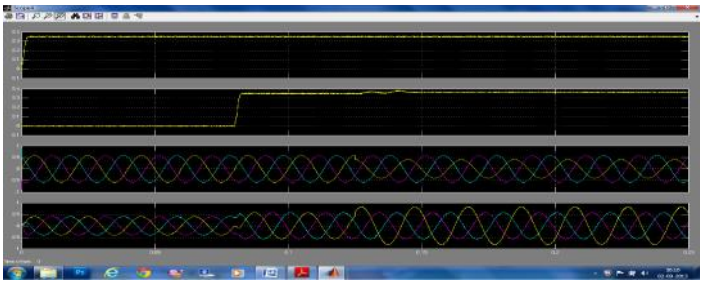
no cross coupling, no steady-state error, and a fast rising and settling time.

UPFC series converter controlling power flow, comparison between DPC-ADC:



.**Fig. 18** UPFC Series converter controlling power flow Comparison of DPC-ADC

DPC Compared to Other Controllers:

The same simulation model is used as in the previous test. The DPC will be compared with two other controllers: advanced dynamic control (ADC) and dynamic inverse control (DIC).Both are middle-level controllers, with a clearly described design methodology. The controllers are designed as specified in their sources, and the parameters can be found in the Appendix. To create fair comparison conditions, the converter control is implemented by a sliding mode controller for the three level converter with the same switching frequency, switching table, and relay widths as the one incorporated in the DPC.

1) Balanced Condition: The three controllers are compared under equal conditions of the previous simulation, which are completely balanced. It can be seen from Fig that the DPC demonstrates the smallest perturbation from the set point in steady-state conditions. ADC demonstrates low-order harmonics and steady-state error, while DIC demonstrates serious low-order harmonics. From Fig which is a zoom of Fig it can be seen that the DIC and ADC have a faster response to a step, but present more overshoot, and have a longer settling time. Overall, the DPC presents better performance under balanced conditions, both in steady state and dynamically.

2) Unbalanced Voltage Sag: The controllers are compared during single line-to-line voltage sag, with 70% of nominal voltage remaining. Fig shows that the DPC is fairly indifferent, whereas DIC and ADC demonstrate an increase in their low-order harmonics. DPC has the best response to unbalanced voltage conditions.

Conclusion

The enforced transmission of unnatural power flow of series converter with clamped multi level Neutral point converter demonstrated the technique has been applied to a three-level NPC converter. The DPC technique was applied to a UPFC to control the power flow on a transmission line. The main advantage of the control techniques are fast dynamic control behavior with no cross coupling or overshoot, with a simple controller, independent of nodal voltage changes. The controller was compared to two other controllers under balanced and unbalanced conditions, and demonstrated better performance, with shorter settling times, no overshoot, and indifference to voltage unbalance. It is readily adaptable to other converter types than the three-level converter demonstrated in this paper. The realization was demonstrated by simulation and experimental results on a scaled model of a transmission line. I conclude that direct power control is an effective method that can be used with UPFC.

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