Designing Of Bidir \oplus cti**Gaav**eDiter For High Power Appli Current Ripple Reduction Technique

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Abstrae f-Ihis paper predses mights to the decision and link capacitor, division dc/dc converter with ltmhreheisb.ciodngfeigsuyratcihorno,nizing operation of two sktWe/ges are only a single bridge is used foam obidwiporecocttoibynpael converter has been designed a bridges are used for electrical isoldætsiogn agnudd fedirneas grahiant eafre derived from t const & rMS cutrare in the source and link capacitor can be improved by capacitoprandaiMiestihoneng and operation of boTthhis stsaigne post angement provides the bettoentrol scheme and eliminat es Explanation befort he Proteprosed Conve circuits roy, the switching frequency cypfanhde effrigien 1 3 as mhobs withe proposed converte system can be obtained. Key WordBridirection onnavlend te*l*rick converter requency automatically forms û boiwlirecti I. INTRODUCTION Fuel cell has a slow dynamic respbansidors o the power supply from the fuel cell cannot cope with the power demand during a transientaleedondbaus, power source is required to compensate the power difference between the fuel cell and the load, and a battery is generally used to supply a transient power. The power flow between the fuel cell and the battery is managed cby a bidirectional dc/d converter. Conventional isolated/bidirectional dc/dc converters for a big lapplications have a voltage ful-biridge (FBF) $B()V$ SFcheme in-volhibeagheigh-HV) side and vario-fue-sol $c(\Omega \cdot F \phi)$ nstcheme-sroilntatghee low (LV) side in geunseeravlothteenoobechbaninfdge (HB) and volfteadgepupsuhl (PP) schemes have disadvantages of high current stress and/or high voltage stress. According of first carrent stress and/of fight voltabig. PSchematic of the proposed bidirectional
The which schemes are used in the LV side, they have several variations suEB as time bucto-HBC FVFFB + C_{H1} and C_{H2} provide resonant current paths t CFFB, and FBYF+ - BP with six or eight turs went to fire popular the HV taggoboou on obsect The These converters suffer from efficien FCV crieferent standation bing the reduces the rms load condition and low e-finicoden or peadaboon of for compensating the discharge c due to switching loss. Also, they reacupisete requubbeentheirCinineetcapeaceixtoprlassizateio such as iavnelanomip circuit to adfetweite \mathfrak{g}_4 perind_{ri} $\mathfrak A$ ave the same value, and the resonant f spikes in the LV side, which increas_{t,}es, t_ehoe_rus wittochtheums.by.effchg.yAlgs.ofre.tophueemscey.cofne one or two as a result. In this paopetswitoage isolated/bifoloje@ickino-cyalsynchronizedûmsithstangoe.oBetohaeu dc/dc converter adopting a current nippele sociantion teshneiques a symmetric is propoTsheed resonant converter with b b \& t b middiges en en langleration, and we w in charge of electrical isolation an_tch _ecoopselaantioQnaionniyanwiithhenoMcaknomM₃oadree. Whe stage with a single bridge. To reduce rm II.PROPOSCEODNVERTER inpuntaveforamsd, its operatiodni**agramod**eare shown in 2.TH ing. resonant conveut the end with according to input ticounts, utared nucleis bidired control is accomplishe₅danuo**s** in MgT hoen I bull Mk. stage is modeled by a pulse current sour

secondary resonant current i_{Lrs} begins to flow through the channel of M_3 , the link capacitor C_b , and the resonant capacitor C_r . After the primary resonant current i_{Lro} crosses zero at t_1 , it flows through the channel of M_1 and the resonant inductor L_r . Because the impedances seen from node A to C_{H1} and C_{H2} are identical, i_{Lrp} is divided into half and each half current flows through the two capacitors. When v_{gs1} is decreased to the Miller plateau voltage $V_{gs, Miller}$

at t_2 , the drain–source voltage of M_{1vds1} is linearly increased, and i_{Lrs} flows through the body diode of M_3 . The discharge current of the drain–source capacitance of M_2C_{dsp}

Fig.2.Operational mode diagram

can be written as $i_{M2} = -C_{\text{dsp}}V_H/T_{\text{off}}$, where T_{off} is the turnoff time of M_1 . Thus, the HV-side current i_{VH} becomes i_{Lrp}/2 $C_{dsp}V_H/T_{off}.$

After M_1 is completely turned off at t_3 , i_{Lrp} starts to flow through the body diode of M_2 , and the ON state of the body diode of M_3 is maintained to provide the current path of i_{Lrs} . When M_2 and M_4 are turned on at t_4 , ZVS of M_2 is accomplished, and i_{Lrs} flows through the channel of M_4 and

 C_r . After t_5 , i_{Lrp} changes its direction, flowing through C_{H1} and C_{H2} similar to mode 2. Thus, i_{VH} also has $i_{Lrp}/2$. Referring to the key waveforms, the current ripple in the HV source is like that of the FB structure, and the charge and discharge currents of *C^b* happen at the same time. The current cancellation helps to reduce the rms current of *C*^b that suffers from the heavy current stress. In steady state, the average discharge current of C_b , which is equal to the average LV-side current I_{VL} , is balanced with the average charge current so that *i*Lrs can be written as

 $i_{\text{Lrs}} = \pi D I_{\text{VL}} \sin(2\pi f_r t)$, where *D* is the duty ratio of M_5 . Because the magnetizing current i_{Lm} is circulated in the primary side, the

effective current supplied from the HV source is equal to half the rectified current i_{Lrs} reflected to the primary side, i.e., $i_{VH} = |n\pi D I_{VL} \sin(2\pi f_r t)/2|$. By averaging this equation, the current gain becomes $I_{VH} = n D I_{VL}$, and it follows that the voltage gain is derived as $V_L = nDV_H$. Thus, the bidirectional power flow is controlled only with *D*.

B. Structural comparisons between the proposed converter and conventional converters

Table1 shows the structural comparisons between the proposed converter and conventional bidirectional converters. The switch block of the proposed converter has a number of advantages over those of basic conventional converters. Considering additional active-clamp circuits to absorb the voltage spikes in conventional converters, the proposed converter has an advantage in the switch block because it does not require any snubber circuitry. The number of magnetic elements in the proposed converter is
equal to or less than those of conventional converters. If the equal to or less than those of conventional converters. However, the proposed converter has drawbacks in capacitor blocks and diode blocks due to the cascaded structure of two converters. Synthesizing the comparisons, the structure of the proposed converter is not inferior to the conventional converters despite the two-stage structure. Table 1

Using (1), the normalized rms current is shown in Fig., and the minimum value can be obtained at $D_{\text{riiple}} = 0.45$. Thus, *n* can be calculated with $I_{VH, max}/D_{\text{right}}I_{VL, max}$. $V_{b, min}$ should be larger than *VL,*max for buck-mode control. In boost-mode control, the second stage should be able to boost $V_{L,\text{min}}$ to $V_{b,\text{max}}$, but the maximum voltage gain *k* between them is not recommended higher than five that is the limit gain in general boost converters. Accordingly, the selection range of *n* becomes

$$
V_{L,\text{max}}/V_{H,\text{min}} < n < kV_{L,\text{min}}/V_{H,\text{max}} \tag{4}
$$
\ne calculated *n* does not meet this condition, some

If the calculated *n* does not meet this condition, some adjustment should be performed.

IV. SIMULATION RESULTS

(a) DC to DC Buck Converter

III. DESIGN STRATEGY

To accomplish the ZVS condition, the peak magnetizing current should be large enough to discharge the drain–source capacitances of MOSFETs during dead time T_{dead} . From this condition, the primary magnetizing inductance L_m to meet ZVS both buck and boost modes can be driven as

$$
buck mode: L_{mF} \le T_{sL} T_{dead} / 16C_{dsp}
$$
 (1)

boost mode :
$$
L_{\text{mR}} \le T_{\text{sL}} T_{\text{dead}} / 16n^2 C_{\text{dss}}
$$
. (2)

Thus, *L^m* can be selected as

$$
L_m = \min(L_{\text{mF}}, L_{\text{mR}}) \tag{3}
$$

where C_{ds} is the drain–source capacitance of M_3 , M_4 . In this inequality, the first term is the maximum L_m for ZVS in buck mode, and the second term is that in boost mode. With the expression of i_{Lrs} and the operational waveforms, the rms current of C_b , $I_{c,rms}$, can be calculated as

$$
I_{c,\text{rms}}/I_{\text{VL}} = [(0.5\pi D)^{2} + D\cos(2\pi D)]^{1/2}, \quad D \le 0.5
$$

$$
I_{c,\text{rms}}/I_{\text{VL}} = [(0.5\pi D)^{2} - D]^{1/2},
$$

$$
D > 0.5
$$

Time (5 micro sec/div.)

(b) DC to DC Boost Converter

Fig.4.Measured waveforms and efficiency

V.CONCLUSIONS

A Designing of bidirectional dc/dc converter with three bridges has been proposed and analyzed. The input-to-output relationships derived through analysis have shown that the converter has a simple bidirectional control scheme. Also, methods to reduce the rms currents in the HV source and link capacitor have been suggested. To verify the

performance, a 2-kW prototype converter with 90-kHz switching frequency has been implemented with design guidelines derived based on rms current reduction. The experimental results show that above 94.1% of efficiency has been obtained irrespective of the power flow direction. Therefore, it may be suitable for isolated/ bidirectional converters with a high voltage gain.

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