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Various Power Dissipation Mechanisms and Leakage Current Reduction Techniques in Deep-Submicron Technology

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Abstract*—Power consumption is a major issue in today's VLSI technology. Earlier power consumption was of secondary concern. In nanometre technology power has become the important issue because increasing transistor count, higher speed of operation, greater leakage currents. Power dissipation is proportional to speed of operation. With shrinking transistor size and technology, reducing power dissipation and over all power management on chip are the key challenges below 100nm. For many designs, reduction of power dissipation is an important issue due to the need to reduce packaging and cooling cost, extended battery life. For power management leakage power also plays an important role in low power VLSI designs. Leakage power increases at a faster rate than dynamic power in technology generation. This paper describes about the various power dissipation methods along with leakage power management techniques for low power VLSI circuits and systems.

Keywords—*VLSI, Dynamic power dissipation, Static power dissipation, CMOS inverter, Variable threshold voltage, Power Gating, MTCMOS, Leakage Control Transistor*.

I. Introduction

Over the last years, low-power design has become a concern in digital VLSI design, especially for portable and high performance systems [1], [3], [4]. In nanometer technology power dissipation has become the most important issue because of Deep-Sub-micrometer Technology. The power size of the transistor and thereby integrated circuits. If this exponential rise in the power density increment continuous, a microprocessor designed a few years later, would have the density increases exponentially, because of the shrinking same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Every 10°c rise in temperature roughly doubles the failure rate.

Another major demand for low power VLSI design packaging and cooling cost depends on power dissipation of the chip. Increasing customer demand for hand-held, battery-operated devices such as cell-phone, PDA, palmtop, laptop, etc.. As these devices are battery operated, battery life is of primary concern [1]. Unfortunately, the battery technology has not kept up with the energy requirement of the portable equipment. Another demand for low power chips and systems comes from the environmental concerns. According to an estimate of the U.S Environmental Protection Agency(EPA), 80% power consumption by office equipment are due to computing equipment and a large part from unused equipment . Power is dissipated in the form of heat and the cooling techniques such as AC, transfers the heat to the environment. To reduce adverse effect on environment power management standards for desktops and laptops has emerged [15].

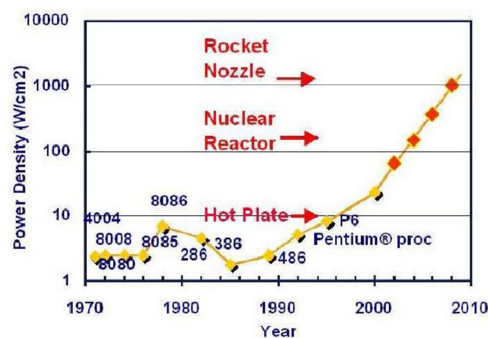

Fig. 1. Increasing power density over the years.

II. SOURCES OF POWER DISSIPATION.

Power consumption is determined by several factors including frequency f, supply voltage V, data activity α, capacitance C, leakage, and short circuit current [2]. Various sources of power dissipations in CMOS circuit is dynamic power, static power [4].

$$P_{total\ power} = P_{dynamic\ power} + P_{static\ power} \quad (1)$$

1. Dynamic power dissipation.

When the circuit is in active or in use the power dissipation due to input change is called dynamic power dissipation [4], it is again classified in to switching power, short circuit power, glitching power dissipation.

$$P_{dynamic} = P_{switching} + P_{short\ circuit} + P_{glitching}. \quad (2)$$

a. Switching power dissipation.

Switching power depends on supply voltage, load capacitance, rate of change of input, switching activity [1], [2].

$$P_{switching\ power} = \alpha\, C V^2_{DD} f. \quad (3)$$

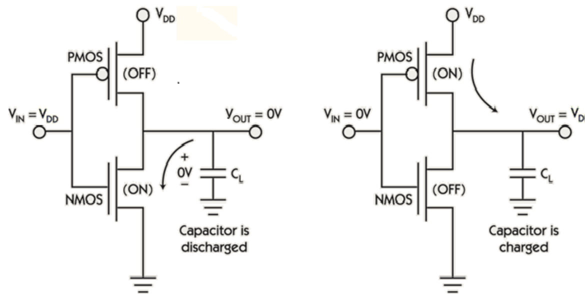

Fig. 2. CMOS inverter switching power analysis.

Switching power dissipation occurs due to charging and discharging of output capacitor. When the input changes from 1 to 0 the pull up transistor is ON and pull down will be OFF and capacitor C charges through pull up transistor. While charging some of power will be dissipated at pull up transistor. Now when again input changes from 0 to 1 the pull down transistor is ON and pull up will be OFF and capacitor C discharges through pull down transistor, and power will be dissipated at pull down transistor [15].

b. Short circuit power dissipation.

Short circuit power dissipation is generated by the short circuit current flowing through both the nMOS and the pMOS transistors during switching. The short circuit current occurs if a logic gate is driven by the input voltage wave forms with the finite rise and fall times. Thus both the nMOS and the pMOS transistors in the circuit conduct simultaneously for a short period of time during the transitions, forming a direct current path between the power supply and ground. This power dissipation takes place even when there is no load or input parasitic capacitor.

$$P_{short\ circuit\ power} = V_{dd}.I_{short\ circuit}\ (\text{i.e } V_{dd}.\ I_{mean})$$

$$\text{i.e. } P_{short\ circuit\ power} = V_{dd}.\ I_{mean}$$
$$= KW/2L.(1-2V_{th}/V_{dd})^3.\tau.f \quad (4)$$

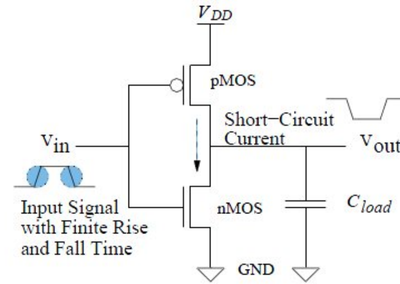

Fig.3. CMOS inverter short circuit power analysis.

Short circuit power dissipation depends on mobility of electrons, channel width& length of transistor, supply and threshold voltage, transition time i.e. rise and fall time of input voltage and frequency of operation.

c. Glitching power dissipation

This glitching power dissipation occurs due to finite delay. This Power dissipated in the intermediate transitions during the evaluation of the logic function of the circuit. In multi-level logic circuits, the propagation delay from one logic block to the next can cause the input signals to the block to change at different times. Thus, a node can exhibit multiple transitions in a single clock cycle before settling to the correct logic level. These intermediate erroneous outputs lead to a power loss in charging and discharging the output load capacitance. This can reduce by using three logic structures instead of chain logic structures.

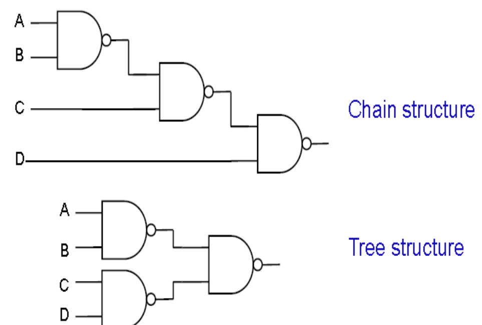

Fig. 4. Glitching Power Analysis.

2. Static power dissipation.

Static power is caused by leakage currents while the gates are idle; that is, no output transitions. Theoretically, CMOS gates should not be consuming any power in this mode. In reality, however, there is always some leakage current passing through the transistors, indicating that the CMOS gates do consume a certain amount of power. Even though the static power consumption, associated with an individual logic gate is extremely small, the total effect becomes significant when tens of millions of gates are utilized in today's integrated circuits (ICs). Furthermore, as transistors shrink in size (as the industry moves from one technology to another), the level of doping has to be increased, thereby causing leakage currents to become larger [15].

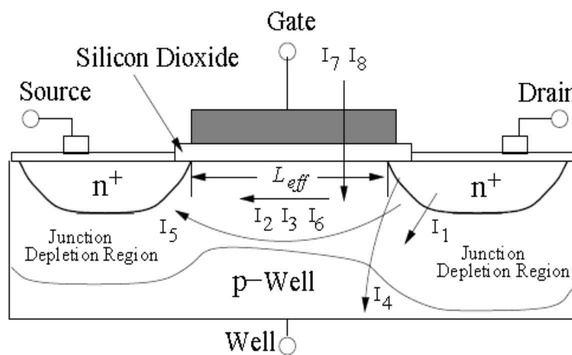

Fig. 5. Leakage currents in short-channel nMOS transistor.

$$P_{static}=P_{diode\ leakage}+P_{sub\ threshold\ leakage}+P_{gate\ leakage}. \quad (5)$$

Reverse Diode Leakage Current (I_1):

The reverse diode leakage occurs when the pn-junction between the drain and the bulk of the transistor is reverse-biased. The reverse-biased drain junction conducts a reverse saturation current which is drawn from the power supply. The reverse leakage current of a pn-junction is expressed as

$$I_{reverse} = A.JS(e^{qvbias/kT} - 1) \quad (6)$$

Where V_{bias} is the reverse bias voltage across the junction, JS is the reverse saturation current density, and A is the junction area. Since the leakage current is proportional to the junction area, it is advisable to minimize the area as much as possible in the layout. The reverse saturation current density is exponentially proportional to the temperature as well so that the JS increases dramatically at higher temperatures

Sub-threshold Leakage Current (I2):

The sub-threshold leakage current (also known as the weak inversion current) occurs when the gate voltage is below the threshold voltage V_{Th}. The sub-threshold leakage current can be approximately formulated as

$$I_{sub\text{-}threshold} = \mu_0.C_{ox}.W/L.V^2.e^{1.8.}e^{(V_{gs}-V_{Th})/\eta V_T} \quad (7)$$

Where μ_0 is the zero bias mobility, Cox is the gate oxide capacitance, and (W=L) represents the width to the length ratio of the leaking MOS device. The variable V_T in equation (7) is the thermal voltage constant, and Vgs represents the gate to the source voltage. The parameter η in equation (7) is the sub-threshold swing co-efficient given by 1 + Cd/Cox with Cd being the depletion layer capacitance of the source/drain junction. One important point about equation (7) is that the sub-threshold leakage current is exponentially proportional to (Vgs-V_{Th}). Traditionally, the threshold voltage V_{Th} has been high enough that with Vgs = 0, the sub-threshold current is very small. However, with today's smaller geometry processes, reduced power supply voltages require the V_{Th} to be reduced also, and thus, the sub-threshold leakage at Vgs = 0 becomes significant. Equation (7) indicates that the sub-threshold leakage can be reduced by increasing the V_{Th} or reducing the Vgs. However, increasing the V_{Th} affects performance, so there is a strong trade off between performance and the power dissipation of a design.

Drain-Induced Barrier-Lowering Effect (I3):

Drain-Induced Barrier Lowering (DIBL) occurs when the depletion region of the drain interacts with the source near the channel surface to lower the source potential barrier [5]. The source then injects carriers into the channel surface without the gate playing a role. As a result, the DIBL is enhanced at a higher drain voltage and shorter L_{eff}. DIBL reduces the V_{Th} for short-channel devices [6].

Gate-Induced Drain Leakage (I4):

The Gate Induced Drain Leakage (GIDL) current arises in the high electric field under the gate/drain overlap region which causes a deep depletion [7]. GIDL occurs at a low VG and high VD bias and generates carriers into the substrate and drain from the surface traps.

Punch-Through (I5):

Punch-Through occurs when the drain and the source depletion region approach each other and electrically touch deep in the channel [8],[13]. Punch-through is a space-charge condition that allows the channel current to exist deep in the sub-gate region, causing the gate to lose control of the sub-gate channel region. Punch-Through is regarded as a subsurface

version of DIBL, and is obviously an undesirable condition and should be prevented in normal circuit operation.

Narrow-Channel Effects (I6):

MOS transistors, which have channel widths W of the same order of magnitude as the maximum depletion region thickness, are defined as narrow-channel devices [9]. The most significant narrow-channel effect is that it increases the actual threshold voltage V_{Th}.

Gate Oxide Tunnelling (I7):

The gate oxide tunnelling current arises due to the finite (non-zero) probability of an electron directly tunnelling through the insulating SiO2 layer. The probability, and thus, the gate tunnelling current itself, is a strong exponential function of the gate oxide layer thickness (tox) and the voltage potential across the gate oxide [10],[13]. For tox ≥2nm, the gate tunnelling current is typically very small, compared to that of the other forms of leakage current [11]. In the most recent generation (i.e. 90nm CMOS technology), the gate oxide thickness is scaled down to a range of 1.2-1.6nm to provide a large current at the reduced voltage supply and to suppress the short-channel effects [12]. This results in the presence of a significant gate tunnelling leakage current, which, in some cases, has caught up to the sub-threshold leakage in magnitude [10].

Hot-Carrier Injection(I8):

Reducing the device dimensions to the DSM regime, accompanied by increasing the substrate doping densities, results in a significant increase of the horizontal and vertical electrical fields in the channel region. However, electrons and holes that gain high kinetic energies in the electric field (hot carriers) can be injected into the gate oxide. This causes permanent changes in the oxide-interface charge distribution, degrading the current-voltage characteristics of the MOSFET. Out of all these leakage currents, the sub-threshold leakage is the dominant source of static power [6]. This thesis focuses on circuit-level techniques to handle the exponentially increased sub-threshold leakage that is caused by technology scaling.

Why leakage power is an issue?

Leakage power increases at faster rate than dynamic power (active power) in technology generation and it becoming a large component of total power dissipation [15]. In standby applications leakage power component becomes a significant % of the total power. Earlier leakage power during standby mode is important to reduce but reduction of runtime leakage power is important in deep submicron technology.

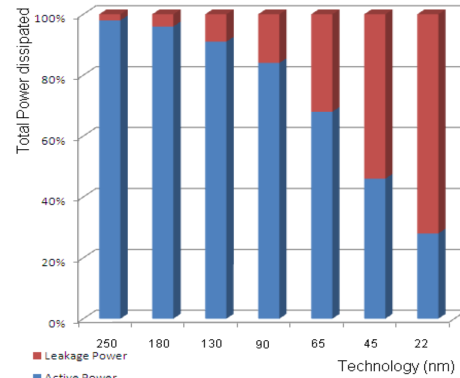

Fig. 6.Technology versus Power dissipation.

III . LEAKAGE REDUCTION APPROACHES.

There are two broad categories approaches,

(1) Standby leakage reduction.

(2) Runtime leakage reduction.

1. Standby leakage reduction

A. Transistor stacking:

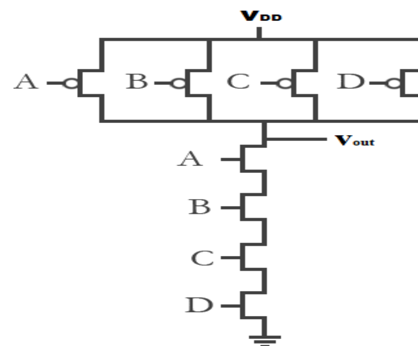

Fig. 7. CMOS four input NAND gate.

When more than one transistor is in series in a CMOS circuit, the leakage current has strong dependence on the number of turned off transistors. This is known as stacking effect [16]. In above circuit gate is connected to 0V and source is connected to higher voltage that is source is negative biased (except lower transistor).

Three input NAND gate leakage power analysis.

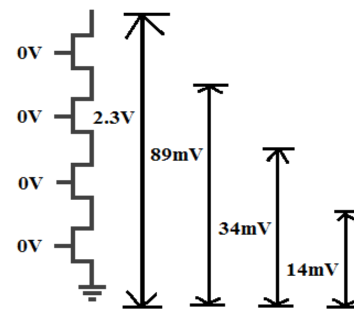

Fig. 8. Transistor stacking analysis.

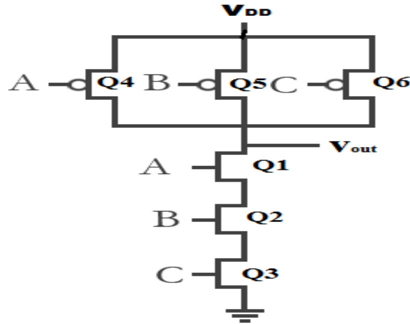

Fig.9:CMOS Three input NAND Gate

Table 1: Three Input NAND Gate Leakage Current analysis

S.No.	StateABC	Leakage Current(nA)	Leaking Transistors
1	000	0.095	Q1Q2Q3
2	001	0.195	Q1Q2
3	010	0.195	Q1Q3
4	011	1.874	Q1
5	100	0.184	Q2Q3
6	101	1.220	Q2
7	110	1.140	Q3
8	111	9.410	Q4Q5Q6

The higher leakage current is 99 times that of the lower leakage current. The leakage current is varying because of three mechanisms.

1. Due to exponential dependence of sub-threshold current on gate-to-source voltage, the leakage current is greatly reduced because of negative gate-to-source voltages.
2. The leakage current is also reduced due to body effect, because the body of all the transistors (except ground transistor) is reverse biased with respect to the source.
3. As the Source-to-Drain voltages for all the transistors are reduced, sub-threshold current due to Drain-Induced-Barrier-Lowering(DIBL) effect also lesser.

From above discussion leakage current depends on input vector. By applying suitable input vector the leakage current can be reduced in standby mode.

B. Variable threshold voltage CMOS (VTCMOS):

Basic principle is to adjust threshold voltage by changing substrate bias. Transistor initially has low threshold voltage (V_{Th}) during normal operation and it is increased by using reverse body bias when the circuit is not in use (standby mode). This substrate bias is altered using substrate bias control circuit. Effective in reducing leakage power dissipation in standby mode [16].

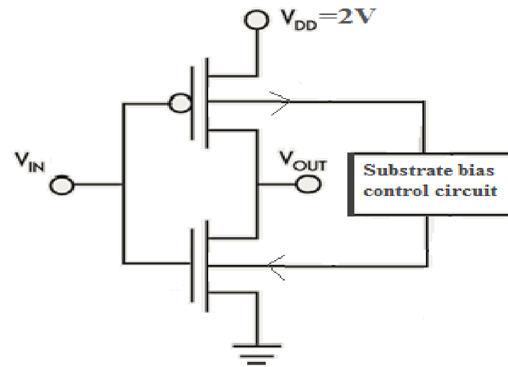

Fig.10. Variable threshold voltage CMOS circuit.

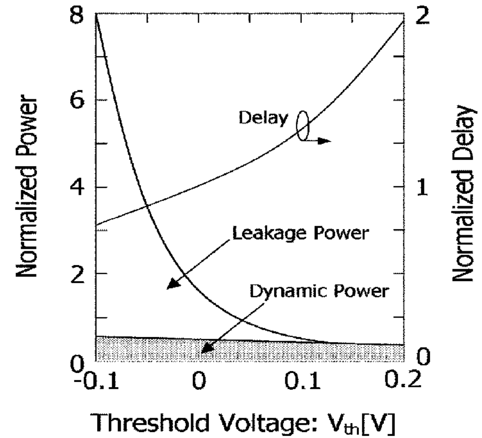

Fig. 11.Power and delay dependence on threshold voltage.

Active mode: V_{BP}=2V, V_{tP}= -0.2V and V_{Bn}=0V, V_{tn}=0.2V.

Standby mode: V_{BP}=4V, V_{tP}= -0.6V and V_{Bn}=-2V, $_{tn}$=0.6V.

For every 100mV increase in threshold voltage, the sub-threshold leakage current reduced by half. But due to substrate bias control circuit area and complexity increases. One has to compromise between leakage current and area.

C. Multi-threshold voltage CMOS (MTCMOS):

Multi threshold voltage CMOS (MTCMOS) reduces the leakage by inserting high-threshold devices in series to low V_{th} circuitry.A sleep control scheme is introduced for efficient power management. In the active mode, SL is set low and sleep control high V_{th} transistors (MP and MN) are turned on. Since their on-resistances are small, the virtual supply voltages (VDDV and VSSV) almost function as real power lines.

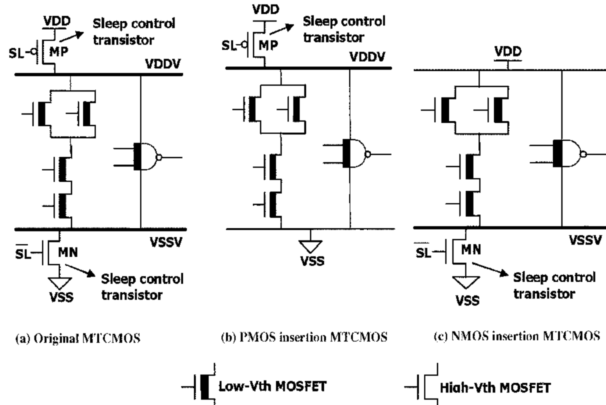

Fig.12.Schematic of MTCMOS circuit.

In the standby mode, SL is set high, MN and MP are turned off, and the leakage current is low. In fact, only one type of high transistor is enough for leakage control [5], [13]. Fig. 11.(b) and (c) shows the PMOS insertion and NMOS insertion schemes, respectively. In above circuit dynamic power is reduced by clock gating i.e. sleep transistor and the leakage power is reduced by power gating circuit which is having high $V_{th.}$ Leakage Power (current) is more for lower V_{th} MOS transistor.

D. Power Gating

Power gating uses high Vth "sleep transistors" (also referred to as power switches) to disconnect power supplies to higher-speed and higher-power logic when that logic is not being actively used. Power can be gated using either header cells (which disconnect the Vdd) or footer cells (which disconnect the Ground).

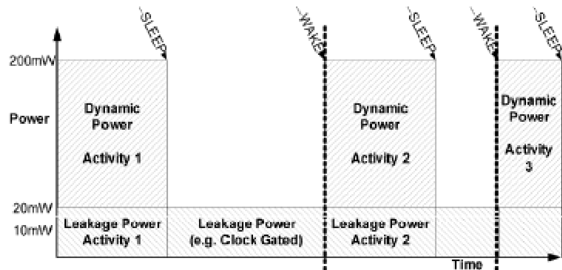

Fig.13. Active profile with clock gating.

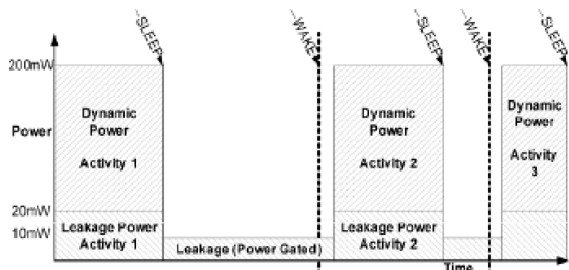

Fig.14. Active profile with clock gating& power gating.

POWER GATING TOPOLOGIES.

1. **Global power gating**.

Global power gating refers to a local topology in which multiple switches are connected to one or more blocks of logic and a single virtual ground is shared in common among all the power gated logic blocks. This topology is effective for large blocks (coarse grained) in which all the logic is power gated. This technique does not apply when there are many different power gated blocks, each controlled by a different sleep enable signal. Significantly lesser area overhead than that of fine grained [13], [16].

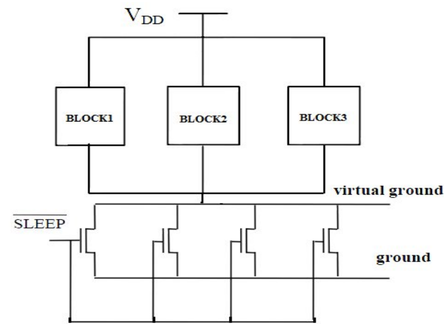

Fig.15. Global power gating topology.

2. **Local power gating**.

Local power gating refers to a logical topology in which each switch singularly gates its own virtual ground connected to its own group of logic. This arrangement results in multiple segment virtual ground for a single sleep control signal. This technology used for fine grained logic [16].

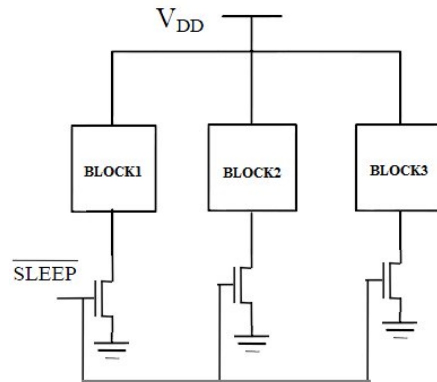

Fig.16. Local power gating topology.

3. **Switch in cell**.

In this topology, each logic cell contains its own switch transistor. Its primary advantage is that delay

calculation is very straight forward. The area overhead is substantial [13], [16].

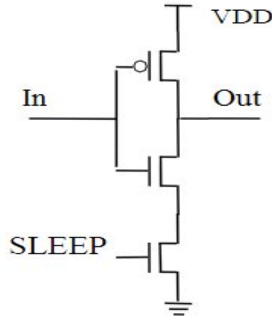

Fig.17. Switch in inverter cell.

4. LECTOR Technique

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from [17], [18], [19] and [20] that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The number of OFF transistors is related to leakage power as shown in Figure 18.

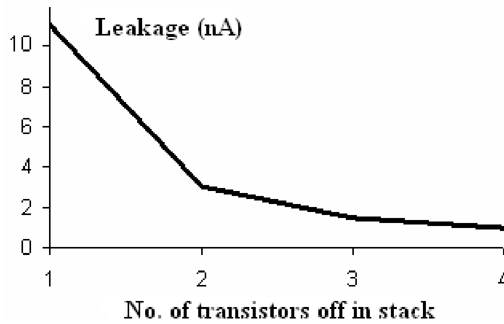

Fig.18. Transistor-stacking Vs Leakage Power.

In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cut off region.

Leakage Control TransistOR (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Figure 18. A PMOS is introduced as LCT1 and a NMOS as LCT2 between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cut off region for any input. Along with the resistance in the path, the propagation delay of the gate also gets increased. The transistors of LCT inverter are sized such that the propagation delay is reduced or equal to its base case.

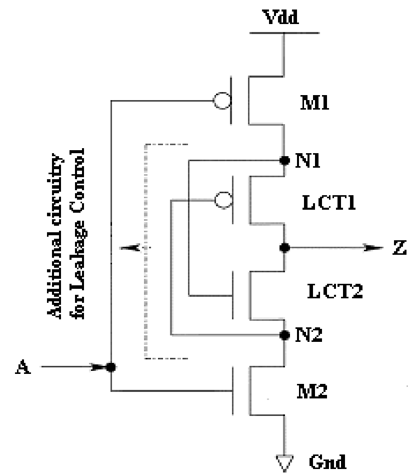

Fig. 19 : LECTOR based CMOS Inverter

Table 2:State Matrix of LCT Inverter

Transistor Reference	Input Vector (A)	
	0	1
M1	ON State	OFF State
M2	OFF State	ON State
LCT1	Near Cut-OFF State	ON State
LCT2	ON State	Near Cut-OFF State

5. LCPMOS

In this technique, a single leakage control transistor (LCT) is controlled by the output of the circuit itself. This leakage control transistor increases the resistance of the path from pull down network to ground thereby increasing the resistance from V_{dd} to ground, leading to significant decrease in leakage currents.

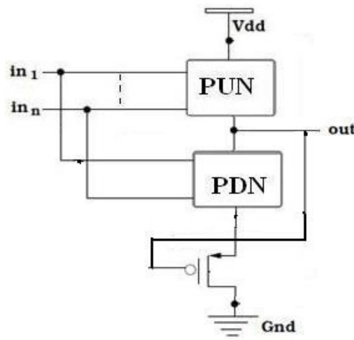

Fig.20. LCPMOSCMOS Gate

The main advantage this technique compared to other techniques is that LCPMOS technique does not require any additional control and monitoring circuitry, so limits the area and the power dissipation in active state [21].

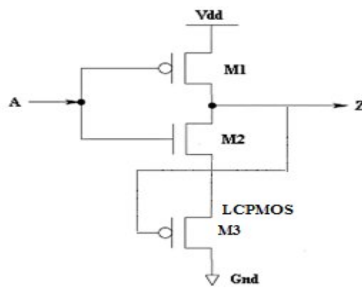

Fig.21. LCPMOS CMOS Inverter.

The CMOS Inverter is shown in Figure.21 with the LCT added between pull-down network and ground. When Vdd=1V, input A=0, the output is high. As the output drives the LCT the LCT goes to OFF state hence provides high resistance path between Vdd and Gnd. When A=1,the output is low; hence LCT will be in ON state hence output is low. LCPMOS inverter for all possible inputs is tabulated in Table.

Table3: State Matrix of LCPMOS Inverter

Transistor Reference	InputVector(A)	
	0	1
M1	ONState	OFFState
M2	OFFState	ONState
LCT	Near Cut-OFF State	ONState

Conclusion

Exceeding Leakage power has become a major concern for the CMOS circuits in deep sub-micron process. As process moves to finer technologies, there is a decrease in the feature sizes and increase in the device density. Lowering the supply voltage leads to lower threshold voltages and oxide thickness. High device density and low threshold voltages result in a significant increase in the leakage power dissipation. In this paper we presented various sources of power dissipation and leakage power reduction approaches in Standby and Runtime modes.

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