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Modulation and Control of Solid-State-Transformer

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"To my mother who is always watching me from the Heaven."

"To my wife and my son who are always by my side."

Abstract

Together with the high penetration of renewable energy into the utility, Solid-State-Transformers (SSTs) have gained more and more attraction in recent years. The exponential demand of electric energy also contributes to the promotion of SSTs in such applications to interconnect grids within a nation or inter-nations to form super-grids. It has also been applied for automotive applications as a substitution for the hybrid energy storage system. As a transformer, SST is an isolation device which can transform the voltage from one level to other levels. Furthermore, SSTs have a lot of distinguished advantages which are not available in the conventional passive transformer such as: improving voltage regulation, load/short-circuit protection, power quality improvement, etc. Especially, the communication capability makes SSTs intelligent devices enabling the concept of the Energy Internet.

However, there are two major issues that restrict the popularity of SSTs: price and efficiency. As for the first issue, it can be solved gradually by mass production and/or by applying cutting edge innovations in the material technology. Nowadays, although SSTs are still costly, their price will be more competitive in the near future.

Let us see from another aspect. Instead of making SSTs cheaper, they can be made worthier with the high price by equipping with advanced functionalities. Functions such as voltage regulation, protection, power management, power quality enhancement, etc. can be accomplished by a correspondent control system.

The efficiency of a SST is not as high as a passive transformer in the same circumstance because it contains a lot of switching devices. Those devices consume power when operating that restricting the overall system performance. However, this issue can also be resolved by improving the modulation strategy. The power dissipation in a SST can be identified and modelized. With an appropriate algorithm, the loss can be significantly reduced. The stress on switching devices is suppressed allowing the usage of lower-rating devices in heavy-duty applications. Besides, the noise caused by the commutation operation is weaken and presents

less effects on other electronic equipments. As a consequence, the whole system will become more reliable.

Motivated by the aforementioned reasons, this dissertation is reserved to deal with modulation and dynamic control of SSTs:

Firstly, a new strategy is proposed to modulate Dual-Active-Bridge (DAB) converters, the core technology of all SST types. The DAB converter is analyzed in the time domain. After that, a closed-form modulation function is derived. The function is then modified to operate when the frequency is restricted. The target is not only to achieve soft-switching in the wide operation range, but also to minimize reactive power in the system.

Secondly, a new observer-based dynamic control system is proposed to improve the voltage regulation as well as the power management capabilities of the converter. The converter is modelized in the frequency domain with high accuracy. Thanks to the decoupled control system, the active and reactive powers can be separated from each other and are individually manageable. Furthermore, by controlling the quadrature component of transferred current to adhere an appropriate reference, reactive power can be handled intentionally. The soft-switching area is expanded to the whole power range. Experiment results confirm that dynamic performance of the converter is much improved.

Finally, all of the above approaches are applied for a Triple-Active-Bridge converter, which is another configuration of SSTs derived from the Dual-Active-Bridge topology, intentionally used for electric vehicle applications. The frequency domain analysis is carried out once again. Each operation modes of the converter will be considered to develop its corresponding soft-switching modulation strategy. The control system is then constructed for only one mode, but the same designed procedures can be applied for other modes.

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Nguyen Duy Dinh

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List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
DAB	Dual-Active-Bridge
DAC	Digital to Analog Converter
DC	Direct Current
DOF	Degree of Freedom
DSP	Digital Signal Processor
DPS	Dual Phase Shift
EMI	Electro-Magnetic Interference
EMS	Energy Management System
EPS	Enhanced Phase Shift
EV	Electric Vehicle
FFT	Fast Fourier Transform
FHA	Fundamental Harmonic Approximation
FPS	Frequency Variation and Phase Shift Modulation
LFT	Low Frequency Transformer
LPF	Low-Pass Filter
LVDC	Low Voltage Direct Current
MFPS	Modified Frequency Variation and Phase Shift Modulation
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
p.u.	per unit
PV	Photo Voltaic

PWM	**P**ulse-**W**idth Modulation
QPS	**Q**uad-**P**hase-**S**hift
RMS	**R**oot-**M**ean-**S**quare
SPS	**S**ingle **P**hase **S**hift
SST	**S**olid-**S**tate-**T**ransformer
TAB	**T**riple-**A**ctive-**B**ridge
TPS	**T**riple **P**hase **S**hift
VFM	**V**ariable **F**requency Modulation
ZCS	**Z**ero **C**urrent **S**witched
ZVS	**Z**ero **V**oltage **S**witched

List of Nomenclatures

δ	Impedance angle of the transmission network
ϵ	Effective skin depth of winding wire
$\boldsymbol{\Gamma}$	Transfer function translated from the state space model
$\boldsymbol{\Gamma}_{diag}$	The diagonal matrix of $\boldsymbol{\Gamma}$
λ	Depth of ZVS, coefficient to tune the phase shift
$\boldsymbol{\Lambda}$	Relative gain matrix
κ	Coefficient for tuning the fundamental peak current
Ω_p	System pole
Ω_s	Nominal angular frequency
ω_s	Angular switching frequency
ϕ	Load angle - the phase difference between primary voltage and primary current
ϕ_1	Load angle seen from the primary side
ϕ_2	Load angle seen from the secondary side
Φ_{min}	The minimum load angle to ensure zero voltage switch
ψ	Phase shift angle between two bridge of DAB converter
ψ_{FPS}	Phase shift generated by the FPS method
ψ_{nl}	Phase shift when the frequency limiter is not used
ψ_{wl}	Phase shift when the frequency limiter is used
θ	Angular variable
θ_{drift}	The drifted amount due to the phase drift phenomenon
Θ_d	The dead-phase, caused by the dead-time, at the nominal switching frequency

ζ	Voltage gain
A_c	Cross section area of magnetic core
$\boldsymbol{A,\ B,\ C,\ D}$	Matrices of the sate space model
B_{max}	The maximum allowable fux density of the transformer
B_{pk}	The peak flux density of the transformer
C_{ds}	Drain-to-Source parasitic capacitor of a MOSFET
C_1	Capacitance of the input capacitor
C_2	Capacitance of the output capacitor
f_s	Switching frequency
F_s	Nominal switching frequency
F_{sample}	Sampling frequency
f_x	Small signal normalized frequency
$F_{x,min}$	Minimum normalized switching frequency
$F_{x,max}$	Maximum normalized switching frequency
$F_{x,nl}$	Normalized frequency when the limiter is not used
$F_{x,wl}$	Normalized frequency when the limiter is used
F_x	Normalized switching frequency
$G_{i2fx}(s)$	Transfer function from f_x to i_2
$G_{ci}(s)$	Terminal current controller
$G_{cid}(s)$	Current controller for i_d
$G_{ciq}(s)$	Current controller for i_q
$G_{if}(s)$	Transfer function from f to i
G_{ii^*}	Transfer function of the closed-current loop
$G_{LPF}(s)$	Transfer function of the low pass filter
$G_{v2i2}(s)$	Transfer function from i_2 to v_2
$G_{ZOH}(s)$	Transfer function of the zero order hold block
K_f	Waveform coefficient
L_s	Leakage inductance of transformer
$\mathcal{L}$	Observer gain
m	Instantaneous voltage ratio
M	Voltage conversion ratio

n	Transformer winding ratio
N_{pri}	Number of turns of primary winding
I_1	Current at terminal 1
I_2	Current at terminal 2
I_2^*	Referent of the terminal current control loop
i_e	Fundamental component of primary current
I_0	First transition current of one switching half cycle
I_ψ	Second transition current of one switching half cycle
I_π	Third transition current of one switching half cycle
$I_{\pi+\psi}$	Forth transition current of one switching half cycle
$I_{\psi,sec}$	The second transition current in a half cycle, referred to secondary side
$i_{2,avg}$	Instantaneous terminal 2 current
$I_{2,avg}$	Average current at terminal 2
I_{2f}	Terminal 2 current after filtered
$i_{abs,avg}$	Average absolute value of the fundamental current
$i_{rec,avg}$	Average rectified transferred current
i_{ds}	The drain-to-source current of a MOSFET
i_d	Direct current of the primary current
i_q	Quadrature current of the primary current
$i_{pri}(t)$	Primary current
$I_{zvs,min}$	The minimum current to completely charge/discharge the body capacitor of MOSFETs
$\boldsymbol{O}$	Observability matrix
P	Average transmission power
P_1	Instantaneous active power at the primary side
P_2	Instantaneous active power at the secondary side
Q	Quality factor of the transmission network
Q_1	Instantaneous reactive power at the primary side
Q_2	Instantaneous reactive power at the secondary side
P_{nl}	Average power when the frequency limiter is not used

P_{wl}	Average power when the frequency limiter is used
r_c	Series resistance of the output capacitor
R_{Load}	Equivalent resistance of the load
R_s	Series resistance of the transmission network
s	Laplace operator
t	Time variable
T_d	Dead-time between two MOSFET in same leg
$\boldsymbol{u}$	Control vector
V_1	DC voltage at port 1
V_2	DC voltage at port 2
V_2^*	Referent of the voltage control loop
v_{1d}	Direct component of the primary voltage
v_{1q}	Quadrature component of the primary voltage
v_{2d}	Direct component of the secondary voltage referred to the primary side
v_{2q}	Quadrature component of the secondary voltage referred to the primary side
v_{1e}	Fundamental component of primary voltage
v'_{2e}	Fundamental component of primary referred secondary voltage
V_{2f}	Terminal 2 voltage after filtered
v_{1m}	Peak of the fundamental primary voltage
v_{2m}	Peak of the fundamental secondary voltage referred to the primary side
$v_{ds}(t)$	Drain-to-source voltage of a MOSFET
v_{gs}	The gate-to-source voltage of a MOSFET
$v_{gs,th}$	The threshold gate-to-souce voltage of a MOSFET
$v_{inv1}(t)$	Voltage across the primary winding of transformer
$v_{inv2}(t)$	Voltage across the secondary winding of transformer
$v'_{inv2}(t)$	Voltage across the secondary winding of transformer referred to primary side

LIST OF NOMENCLATURES

$v_{Ls}(t)$	Voltage across the leakage inductance
$\boldsymbol{W}$	Decoupling matrix
$\tilde{\boldsymbol{x}}$	Observer error
$\boldsymbol{x}$	System state
$\hat{\boldsymbol{x}}$	Observed state
X_L	Reactance of the leakage inductance

Chapter 1

Introduction

1.1   Background

1.1.1   Issues of conventional passive transformer

Since invented by William Stanley in 1885, transformer has become one of the
essential components in many applications such as power transmission and dis-
tribution system, power supply, welding, voltage/current sensor, etc. In the AC
power system, transformers are everywhere to downscale the kV-level voltage to
few hundred volts for house equipments, or to boost the voltage from generators
to join the national utility, or just to perform a galvanic isolation between sides
of the transformer. In such systems, the transformers work at 50 Hz or 60 Hz
frequency. Because of operating at low frequency, transformers usually have low
power-per-volume and low power-per-weight ratios (i.e. low power density).

A transformer can have two or more windings, however, frequency at all windings
must be the same. Transformers used for transmission and distribution usually
have a fixed conversion ratio. That means, the voltage and current at one side are
proportional to the voltage and current at other side with a predictable correla-
tion. Transformer is one of the most robust, long-lasting, reliable and inexpensive
electrical device. Its efficiency is usually more than 95%. At the high power level,
it can be up to 99.5% [1].

However, as the evolution of technology occurs, many applications need more complicated and intelligent functions which cannot be fulfilled by using a transformer standalone. Let us take some examples. In order to asynchronously interconnect between two utilities having different frequencies (such as 50 Hz in the east and 60 Hz in the west sides of Japan), transformers cannot be used directly. Or in the hybrid renewable energy system, the output of the Photo-Voltaic (PV) array as well as the battery is DC; this DC power cannot be injected directly to the utility simply just by using a transformer.

Let us take another example. In a factory, there are many electrical equipments. When they are switched on or off, voltage sags/swells might occur and pass through the transformer to the lines affecting the balance of the grid. Many nonlinear equipments (e.g. rectifiers, switched-mode power supplies, etc.) generate harmonics. Those harmonics, in turns, influence the utility via the transformer causing the current distortion, reducing the power factor and thus, downgrading the power quality. The transformer existing here just duplicates the phase and frequency. The active and reactive powers are entirely transmitted from one side to other sides with no changes. That also means the transformer cannot help improve the power quality.

1.1.2 Solid-State-Transformer

The first prototyped of Solid-State-Transformers (SSTs) was announced in 1970 by McMurray *et. al.* [2]. However, it did not gained a lot of attraction from scientists until recently. The high penetration of renewable energy as well as the demand to interconnect between distinguished grids has promoted the evolution of SSTs. Numerous of outstanding advantages of SSTs [3–6] make them the perfect substitutions for the passive transformers in the conventional applications. Furthermore, in the circumstances where the passive transformers perform inefficiently such as the aforementioned applications, SSTs can take the place.

As a transformer, a SST can interface between two or more isolated sources/sinks bidirectionally. That means each side of a SST can be a source or a sink. For

this reason, from now on, a side of a SST will be so-called a *port* and a SST can be also called a *multi-port converter* (however, a multi-port converter is not necessarily a SST since it can be non-isolated). One SST has at least two ports (or dual-ports). There are unlimited number of ports that a SST can have. The maximum number of ports recorded in the literature was four [7]. However, as the number of ports increases, the difficulty in management and control of power flows between ports becomes exponentially complicated. Therefore, in practice, the most popular configurations are dual-port [8] and triple-port [9] SSTs.

There are various topologies of SSTs to interact an AC (or DC) port with one or more AC (or DC) ports [10]. AC/AC typed SST is the key technology in the asynchronous interconnection application as it can perform the power transmission regardless of the frequency distinction at ports [11]. A DC/AC SST can connect a PV array directly to the AC utility with the maximum power point tracking function installed. It can also be employed to transfer the power bidirectionally between the utility and the battery storage bank in the hybrid energy storage system [12]. In the DC micro grid, DC/DC SSTs play an essential role as they can help reduce the number of converter counts compared to the conventional architecture [13] or they can be used as individual devices to form the grid [14].

SSTs usually operate at high switching frequency ranging from several kHz [15] to 1 MHz [16]. Hence, in terms of size and weight, they are much smaller and lighter than the conventional Low Frequency Transformers (LFTs). This allows SSTs to be very promising choices for applications such as electric vehicles [17–19], where size and weight are high priority. Moreover, SSTs have many advanced features that are not available in case of LFTs, such as harmonics compensation, voltage regulation, overload/short-circuit protection, etc. [5]. Besides, since each SST is controlled by an embedded system, it can *talk* to each others by using some communication protocols. Several individual SSTs can form a *network*, in which each SST plays as an *energy router* [20, 21]. This makes SSTs more *intelligent* than the conventional LFTs and enables the concept of the Energy Internet [22].
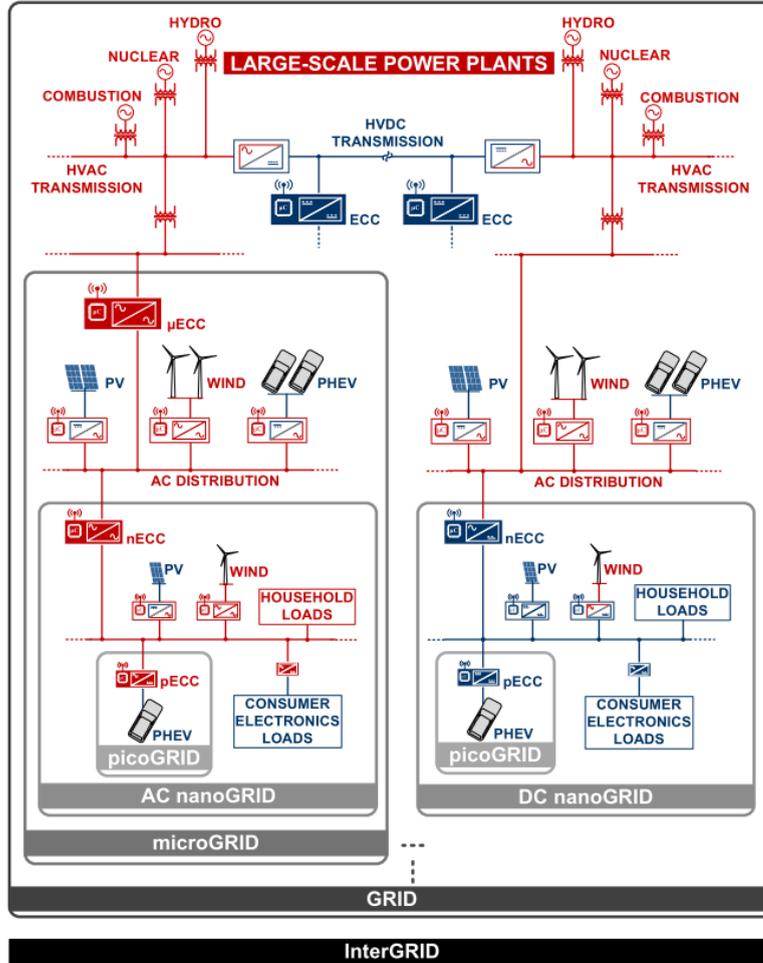
Figure 1.1. Inter-grid concept basing on SSTs for interconnecting AC and DC sub-grids by Boroyevich *et. al.* [24] .

Because of the high potential of SSTs, some smart grid concepts basing on them have been proposed and developed [21–24]. Fig. 1.1 demonstrates a such concept introduced by Boroyevich *et. al.* In this hierarchical structure, SSTs are located everywhere to interconnect between grids and grids, renewable resources and grids, electric vehicles and grids, or between grids and consumer electronic loads. Each of them are equipped with the communication function enabling the possibility for a high-level energy management system (EMS) to control the inter-grid either partially or entirely from remote areas. Recently, the reputation of SSTs has been expanded to locomotive [25], oil and gas processing [26], aircraft [27] applications, etc. In those instances, the SST may be called a intelligent universal transformer [23], a power electronic transformer [25], or a DC transformer [28], etc. Whatever it is named, the bright prospect of SSTs is confirmed more assuredly.

1.1.3   Issues of SST

There are two major issues that dominate the popularity of SSTs. The first one is their price. They are too costly compared to LFTs. It is true because numerous of power electronic devices must be utilized to build up a SST, the production technology is also more difficult, the operation and maintenance require higher-level engineer to accomplish, etc. In spite of the high price, the benefits that a SST can bring make it valuable and worthy. Besides, innovations in the material technology will make the price of power electronic devices cheaper while the performance is better each day. Therefore, in the near future, the price of SSTs will be more competitive allowing them to become the better substitutions for LFTs.

The second issue that affects the proliferation of SSTs is their efficiency. Fig. 1.2 illustrates the efficiency comparison between SST and LFT according to Kolar *et. al.* [5]. Aiming to transfer power between electric sources/sinks having different properties, SSTs might have multiple conversion stages. Due to this reason, the efficiency of a SST is not as high as a LFT when doing the same mission: AC to AC conversion. In the such situation, the maximum efficiency of SSTs recorded in the literature is 98.7%, less than 99.5% of LFTs. It is comprehensible because power electronic devices in SSTs dissipate power when operating that restrict the conversion effectiveness of SST.
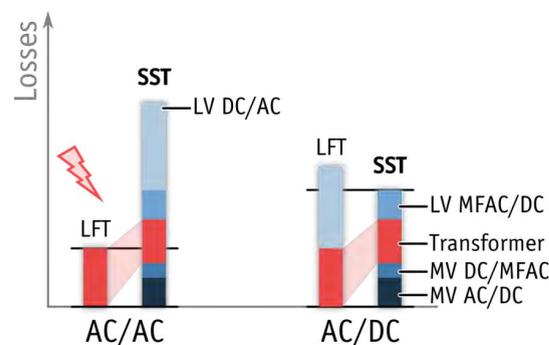
Figure 1.2. Efficiency comparison between LFTs and SSTs [5] .

Nonetheless, in other circumstances such as DC to AC or AC to DC transformations, SST is the superior. For example, the MVAC to LVDC conversion described

in Fig. 1.2 can be accomplished by using a LFT followed by a rectifier. Since located at the low voltage side, the rectifier has to carry high currents causing the system more lossier and bulkier. As for the SST, its rectifier is located at the MVAC side to establish the MVDC bus. After that, a high frequency DC/DC converter is taken place to generate the LVDC bus at the output side. Although the conversion involves more stages, the efficiency of the SST configuration will be higher and the size can be reduced.

1.1.4 Dual-Active-Bridge converter

Among various topologies of SSTs [5], the three-stage type illustrated in Fig. 1.3 is the most flexible. A three-stage SST consists of three main parts: an active rectifier, a grid-tide inverter to synchronize with the utility, and a Dual-Active-Bridge (DAB) DC/DC converter. Among those, the DAB converter is the key component which:

- generates the galvanic isolation between two sides, and

- allows power transmission in bidirectional ways.
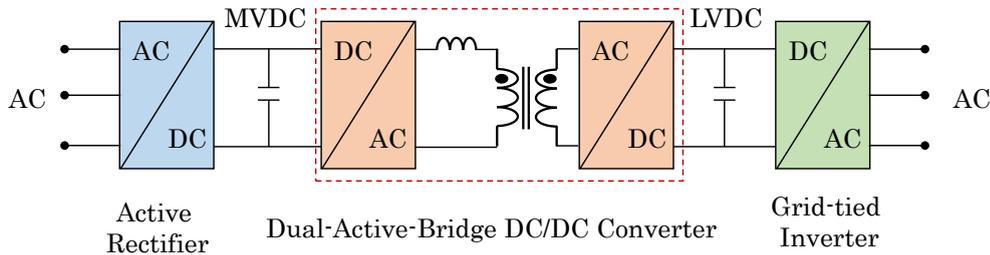
Figure 1.3. Three-stage SST topology.

The DAB converter, which is sometime called DC transformer [29] or power electronic transformer [30], etc., itself is also one SST topology. It was first introduced by De Doncker [31] in 1991. Since then, it has been applied popularly not only in large scale systems [32] but also in small scale one, such as electric vehicles[33], aerospace[34], etc. Compares to other DC/DC converter topologies, DAB-type converters have many advantages:
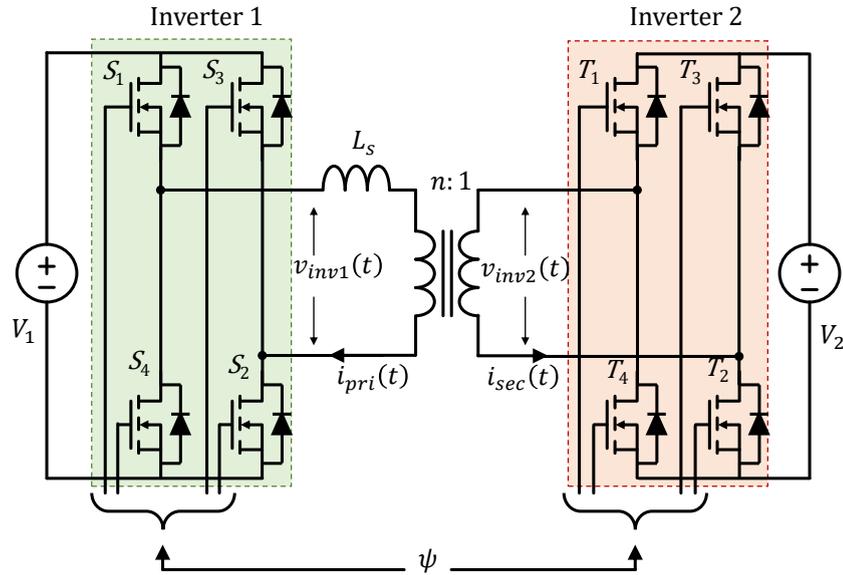
Figure 1.4. DAB converter topology.

- isolated and bidirectional power transmission;

- high voltage ratio can be achieved if a high frequency transformer is used;

- space is saved because the leakage inductance of the transformer can be utilized as the power transmission container;

- inherent soft-switching capability.

DAB converter topology is depicted in Fig. 1.4. There are two H-bridge inverter which link to each other by a two winding transformer. The inductor used for transferring power between two sides is usually integrated inside the transformer as its leakage inductance to save space. For that reason, shell structure, distributed winding technique is employed to make the transformer.

The power flow within the DAB converter is usually manipulated by varying the phase shift between the voltage across the primary and secondary windings of the transformer. The most popular technique is single-phase-shift (SPS) modulation scheme [8, 31, 35–37]. In which, all transistors switch with the duty cycle of 50%. In each inverter, one leg is shifted 180 degrees from each other. Another phase shift angle between two inverters is utilized to handle the power flow. Since the

realization is very simple, the SPS scheme is widely used for DAB converter family. Nevertheless, there are some challenges when operating the converter:

1. When transferring high power, although soft-switching is achieved, the circulating current within inverters is high, especially when the voltage at two terminals are not matched. As a consequence, the reactive power and the conduction loss increase, thus, downgrading the performance of the system.

2. When the voltage of the sender is greater than the receiver, even the phase shift is zero, there still exist unexpected power flowing between two ports. That means the controllable power range is narrower when the voltage ratio is greater than unity.

3. Although the converter has the inherent soft-switching capability, it might be lost at small power range.

4. As the voltage pre-regulator for the grid-tied inverter, the DAB converter should maintain a stable bus voltage. At the same time, it should also eliminate the 300 Hz (or 360 Hz) voltage fluctuation reflected from the AC side.

1.2 Literature review

1.2.1 In term of modulation techniques

Several phase-shift-based techniques have been developed in order to reduce the circulating current and/or to extend the soft-switching region. By adding one or two more degrees of freedom into the modulation, enhanced-phase-shift (EPS), dual-phase-shift (DPS), or triple-phase-shift (TPS) schemes can be formed. The EPS [38–40] scheme uses one more so-called inner phase shift modulation to handle the duty cycle of the voltage across one side of the transformer. Thanks to the inner phase shift, the voltage ratio is controllable. However, this also requires some additional switching states that add more complexity into the analysis and

controller design. The DPS method [41–45] introduces the inner phase shift modulation to both inverters. The voltage ratio is kept constant but the root-mean-square (RMS) voltages are changeable. In TPS strategy [33, 46–51], the inner phase shift angles of the two inverters are different, so that both the voltage ratio and the RMS voltages can be modified. However, since only phase shift modulation is employed in those studies, it is difficult to achieve soft-switching under the light load condition.

The variable frequency modulation (VFM) scheme has been applied popularly in the conventional unidirectional DC/DC resonant converters [52]. Unlike the phase-shift-based modulation methods, VFM can extend the soft-switching region to the light load condition by increasing the switching frequency. Furthermore, frequency variation is also an alternative degree of freedom to help manage the power flow in the converter. For such reasons, VFM has also been applied to DAB converter applications. For example, the target of modulation technique presented in [53] is to turn off the transistors at a specific current of I_{zvs} by varying the switching frequency. At the same time, the terminal current is controlled by phase shift modulation. However, the selection method for the transition current I_{zvs} was not discussed in the dissertation. Besides, there were no results to validate if the experimental I_{zvs} matches the desired one.

In [54], a modulation strategy combining VFM with TPS was introduced. By shaping the transferred current to the triangular waveform, the RMS value of the current is reduced. This technique, however, is only utilized in the light load range since it does not perform as well as the conventional SPS scheme does at the heavy load condition. The strategy introduced in [55] varies the switching frequency basing on the power level condition. When the power is under a certain level, both VFM and EPS are applied to ensure ZVS. This scheme is also employed in the medium and light load conditions. Note that, due to: i) the switching capability of transistor; ii) the need to protect the magnetic devices from saturation; the frequency variable range must be limited. As a consequence, this limitation will affect the coverable power range of the converter. Nevertheless, this problem was not discussed in the aforementioned publications.

Besides, in spite of increasing the degree of freedom of the modulation by adding more control variable(s), most of the methods mentioned above are based on unify function. Thereby, only one or two variables are manipulated, the rest is derived by the function. Nevertheless, how to choose the dominant variable was not discussed in the above studies, especially when the manipulated variable is saturated. Furthermore, the modeling method as well as the operation of the proposed modulation strategy in the transient state was not addressed carefully.

1.2.2   In term of dynamic control

Referring to other publications, discussions on dynamic control for Dual-Active-Bridge (DAB) converter can be found in the literatures. For example, single loop voltage mode for such converter was reported in [44, 56, 57]. In [58], another configuration utilizing feed-forward load current combined with a voltage loop was represented. Two loops current mode topology was introduced in [33, 59]. In term of dynamic control for multi-phase DAB converter, a control strategy in stationary $\alpha\beta$-frame was presented in [60, 61]. In the aforementioned publications, only active power is regulated, none of them manages the circulating (reactive) power within the inverters. Moreover, all of them used terminal current as the feed-back signal. Since the current is DC, a high price transducer (such as the Hall-sensor used in the last chapter) should be employed to sense such quantity.

Analysis and control in the frequency domain with the fundamental harmonic approximation (FHA) method for DAB converter are presented in some recent publications [51, 62]. In which, the inverter voltages and the transferred current are approximated by their fundamental harmonics with high accuracy. Compared to the time-domain analysis, FHA method has some distinguished advantages: 1) active and reactive components of the power flow can be specified; 2) the equations described voltages and currents are independent of operation state of the converter. Based on the FHA analysis, the control method introduced in [62] can maximize the power factor of the converter and enhanced the efficiency about 1% compared to the conventional SPS method. The objective of the strategy addressed in [51]

is to minimize the root-mean-square (rms) current. However, lower rms current or higher power factor may not ensure the better efficiency. Besides, although block diagrams for close loop control in both papers are quite simple which need only the information of voltage ratio, no results about dynamic response were discussed.

Upon the topic of controlling the DAB converter in frequency domain, in [63], a control system based on *dq*-rotation coordinator was addressed. In which, a *dq*-transformation was employed to detach two current components. Actually, that technique is very common for driving low frequency inverter. In which, the instantaneous current will be sampled then transformed by using the Park transformation. However, for high frequency converter, it is very challenge due to the limitation of the sampling speed. Furthermore, this method is only applicable for three phase system.

As for single phase system, the transformation technique cannot be used. Instead, a single phase Phase-Lock-Loop based on the second-order-generalized integrator [64] can be employed. The Adaptive-Notch-Filter [P.3] is another considerable choice as it can also generates the orthogonal signal from the measured signal. Nonetheless, in order to ensure the accuracy of the transformation, the sampling frequency is usually greater than the fundamental frequency at least twenty times. Therefore, when the fundamental frequency is in the range of few tens kHz to few hundreds kHz, such techniques cannot be used due to the low resolution of the sampled signal.

1.3 Objectives

Motivated by the challenges of modulation and control Solid-State-Transformer, specifically DAB converter, as well as by the limitation of the published researches, the main objectives of the dissertation are as follows:

- **Improving the overall efficiency** by achieving ZVS and reducing the circulating current.

- **Extending both the ZVS area and the power range** of DAB converters

- **Developing a control system** to implement the proposed modulation technique in the transient state.

- The control system should have a **good voltage regulation** as well as **noise free** characteristics.

- Operation of the whole system should be verified in several **critical modes such as overload or short-circuit**.

- **Simplicity.** The proposed control algorithms should be simple and feasible to be implemented in the popular digital signal processor platforms and in the real time with low cost.

With the above objectives, the performance of the DAB converter is expected to be improved making the performance of the whole SST system more effective.

1.4 Contributions

The contributions of the dissertation are as follows:

① A new modulation strategy combining frequency and phase shift variation is proposed:

  – to reduce the circulating current (or the reactive power) of DAB converters;

  – ZVS area can be expanded;

  – The reachable power range can be enlarged by 13% when the voltage ratio is 1.5;

  – Overall efficiency can be boosted the overall efficiency by up to 7% compared to the conventional single phase shift method.

② A control system is proposed to realize the new modulation method:

– It can suppress the low frequency voltage fluctuation reflected from AC side;

– It plays as a constant voltage source in the normal operation and as a constant current source when overloading;

– It can regulate the voltage within -16.4% to +11% voltage fluctuation when load is quadrupled;

– The dynamic is fast as the rise time of the voltage is about 22 ms;

– It can detect the short-circuit fault in 1.2 ms and protect the converter by forcing shutdown.

③ An observer-based control system is proposed:

– to estimate the system state in all operation condition, including trapezoidal and triangle current modes;

– The dynamic performance of the system is improved;

– High current overshoot is avoided;

– Voltage overshoot when starting-up under low power condition is reduced;

– Voltage regulation is -14% to +15% as load is quadrupled;

– The constant voltage/current source function is preserved;

– Low frequency harmonics rejection capability is also preserved;

– ZVS capability is preserved;

– The detecting time when short-circuit fault occurs is 2.4 times faster as it is only 500 μs;

④ All proposed control systems are feasible and executable:

– They are all implemented on a very popular digital signal processor platform, TMS320F28335;

– As for the observer-based control system, low cost toroidal current sensor can be employed instead of the expensive Hall transducer;

– All signals necessary for the control system are DC, therefore high sampling frequency is not required.

1.5 Works summary

This dissertation is composed of seven chapters:

Chapter 1 provides the general background of SSTs. By reviewing previous works in the relevant areas, the challenges in term of electrical engineering are addressed. Motivated by those challenges, objectives of this dissertation are presented.

Chapter 2 reports the frequency combined phase shift modulation method in detail. The DAB converter is analyzed in the time domain. After that, a closed-form modulation function is derived. The function is then modified to operate when the frequency is restricted. The experiment validation is conducted in the comparison with another method also based on frequency variation.

Chapter 3 presents the design process of the closed-loop control system to realize the proposed MFPS scheme. The system is then validated in various operation condition, including failure mode.

Chapter 4 describes the analysis of the converter in the frequency domain. Based on that, an observer is developed to estimate system states. Experiment results show that at the vicinity of the linearization point, the observation performance is good. Away from that point, the accuracy of the observer is still acceptable.

Chapter 5 is reserved for designing the observer-based control system. In this chapter, three controllers: two for adjusting direct and quadrature current components and one for regulating terminal 2 voltage. As confirmed by experiment, the dynamic performance is enhanced compared to that of the control system designed in Chapter 3.

In Chapter 6, the approach used in the Chapter 4 is applied to analyze a TAB converter intentionally used for electric vehicle applications. Each operation modes

of the converter will be investigated to develop its corresponding ZVS modulation strategy. Although the evaluation is then undertaken for only one mode, the same designed procedures can be applied for other modes.

The dissertation ends with conclusions and future works in the Chapter 7.

Chapter 2

Frequency Variation Combined Phase Shift Modulation

In this chapter, a new modulation strategy for single phase isolated-dual-active-bridge converters is proposed. The analysis starts with deriving the equations for transition currents and the *load angle* in Section 2 using the well-known approach reported in [31]. After investigating the impact of the dead-time on the transition behavior of transistors, the new ZVS constraint is derived. Based on that, a new modulation method is proposed in Section 3.

The idea is to vary the switching frequency to regulate the load angle to adhere a reference trajectory which is the boundary of the ZVS area. A closed-form modulation function is developed to determine that trajectory. The switching frequency is selected as the dominant control variable, and the phase shift angle is calculated by using the modulation function.

In order to eliminate the impact of the frequency limiter, a modification function is established. Thanks to the function, the proposed modulation can help cover all the power range regardless of how big of the voltage ratio or the frequency limitation. Experiment results show that, by applying the proposed modulation algorithm, the overall efficiency is enhanced up to 7% compared to that when applying the conventional SPS scheme.

2.1 Steady state analysis

2.1.1 Derivation of mathematic equations

The DAB converter is depicted in Fig. 2.1. The voltage at the two ports are V_1 and V_2, respectively. Because of the same role of the two ports, let V_1 be the power transmitter, and V_2 be the receiver. The transformer ratio is $n : 1$. The inductor L_s is utilized as the power deliverer. There are two full-bridge inverters located at the two sides of the transformer. All transistors are switched at the frequency of f_s. Power flow within the converter is manipulated by a bridge shift angle of ψ.

Fig. 2.2 demonstrates one switching cycle of the converter at the steady state under ZVS condition, where $\omega_s = 2\pi f_s$; $v_{inv1}(t)$, $v_{inv2}(t)$ and $i_{pri}(t)$ are the voltages across two sides of the transformer and the transferred current measured at the primary winding, respectively. Let I_0, I_ψ, I_π, and $I_{\pi+\psi}$ be the currents at transition. At the steady state, obviously $I_\pi = -I_0$ and $I_{\pi+\psi} = -I_\psi$.

For simpler analysis, the primary referred diagram illustrated in Fig. 2.3 is utilized. The voltage drop on anti-parallel diodes are assumed to be very small compared to terminal voltages that can be neglected. The resistance of the transmission network is also ignored. Since the switching frequency is usually much faster
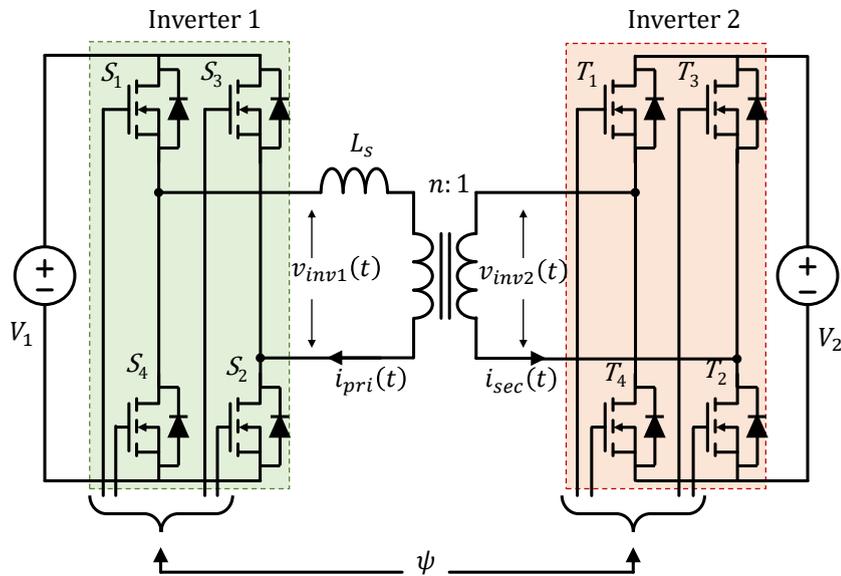
Figure 2.1. DAB converter topology.
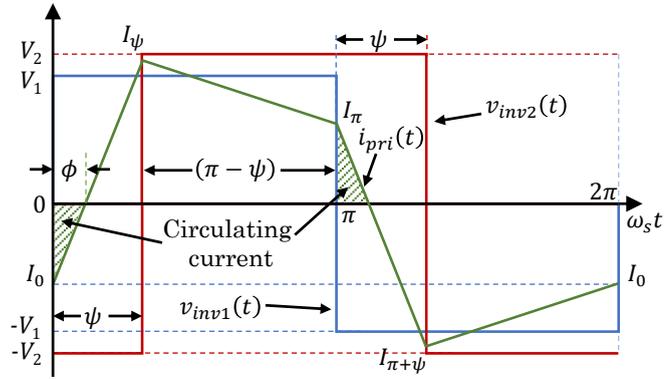
Figure 2.2. Switching waveforms at the steady state.
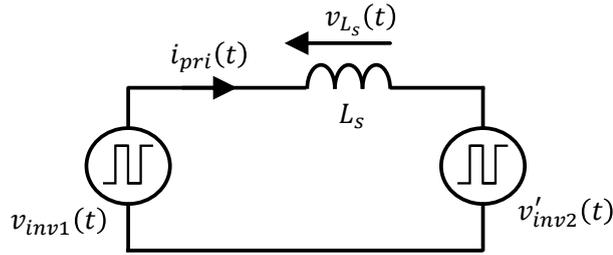
Figure 2.3. Primary referred equivalent circuit.

than the dynamic of capacitors located at the two DC sides, the assumption of constant DC voltage in one switching cycle is made. By applying the analysis method introduced in [31], transition currents I_0 and I_ψ of the inverter 1 and 2, respectively, can be calculated by (2.1):

$$
\begin{cases}
I_0 = & -\dfrac{nV_2}{X_L}\left[\psi - (1 - M)\dfrac{\pi}{2}\right] \\[2mm]
I_\psi = & \dfrac{nV_2}{X_L}\left[M\psi + (1 - M)\dfrac{\pi}{2}\right]
\end{cases}
\tag{2.1}
$$

where M is the voltage ratio, $M = \dfrac{V_1}{nV_2}$ and X_L is the reactance of the transmission network, $X_L = 2\pi f_s L_s$.

Ignoring the resistance of the windings and assuming that the current changes linearly, the load angle ϕ, which is the phase delay between $i_{pri}(t)$ and $v_{inv1}(t)$, can be derived from (2.1) as:

$$
\phi = \frac{1}{1 + M} \times \psi - \frac{1 - M}{1 + M} \times \frac{\pi}{2}
\tag{2.2}
$$

Substituting (2.2) into (2.1), the transition currents are rewritten as:

$$
\begin{cases}
I_0 = & -\dfrac{nV_2}{X_L}\left(1+M\right)\phi \\[3mm]
I_\psi = & \dfrac{nV_2}{X_L}(1+M)\left[M\phi+(1-M)\dfrac{\pi}{2}\right]
\end{cases}
\tag{2.3}
$$

According to [31], ZVS is achieved if (2.4) is fulfilled.

$$
\begin{cases}
I_0 \le 0 \\[2mm]
I_\psi \ge 0
\end{cases}
\tag{2.4}
$$

In term of the load angle, ZVS condition is expressed by (2.5):

$$
\phi \ge \max\left\{0,\ \left(1-\frac{1}{M}\right)\frac{\pi}{2}\right\}
\tag{2.5}
$$

The ZVS constraint (2.5) is derived with the assumption that all MOSFETs transit immediately with no time delay. However, due to the output capacitance C_{ds} of the MOSFET, the drain-source voltage v_{ds} needs some time to drop to zero. Therefore, a dead-time (T_d) is necessary, not only for avoiding shoot-through between switches in one arm, but also for charging/discharging the C_{ds} of the MOSFETs and for achieving ZVS. Discussions on choosing an appropriate dead-time as well as the effect of the dead-time on the converter operation can be found in the literatures [53, 65–68]. In this chapter, the same and fixed amount of dead-time T_d is added to the rising edge of the modulation of all transistors. The next subsection discusses the effect of the dead-time interval on the ZVS condition.

2.1.2 Effect of the dead-time

During the dead-time interval, the output capacitor C_{ds} of MOSFETs are charged (or discharged) by half of the current at the transition causing the drain-source voltage $v_{ds}(t)$ of the corresponding MOSFET to increase (or decrease). If $v_{ds}(t)$ of the next transistor is zero at turn-on, the transition is ZVS; otherwise it is partial ZVS or hard-switching. Due to the charge/discharge time of C_{ds}, both $v_{inv1}(t)$

and $v_{inv2}(t)$ are *drifted* from the theoretical positions (*phase drift phenomenon* [37, 53, 68]). The drifted phase, which is denoted as θ_{drift} in Fig. 2.4, is equal to a half of the phase required for turning-off the transistor. The drift phase θ_{drift} is not constant but depends on terminal voltages, and on the magnitude of the transferred power. Because $v_{inv1}(t)$ is drifted, it is difficult to accurately determine ϕ, which has been defined as the phase difference between $v_{inv1}(t)$ and $i_{pri}(t)$, in the design and analysis stages. Therefore, from now on, the *load angle* ϕ is redefined by the phase measured from the point where the transistor starts turning-off to the zero crossing point of the transferred current. This definition also guarantees the validity of the calculation of ϕ by (2.2).

As for the turn-on action of the switch S_1 of the transmitting inverter, there are two scenarios of switching behavior regarding the relationship between the *dead-phase* θ_d ($\theta_d = \omega_s T_d$) and the load angle ϕ as shown in the simulation waveforms in Fig. 2.4.

- $\phi < \theta_d$: when S_4 turns off, $C_{ds(S_1)}$ is discharged by half of $i_{pri}(t)$; $v_{ds(S_1)}(t)$ drops gradually. If $\phi < \theta_d$, $i_{pri}(t)$ changes its polarity during the dead-time. The capacitor $C_{ds(S_1)}$ is recharged causing $v_{ds(S_1)}(t)$ to increase again. This re-commutation phenomenon leads to current spikes in $i_{ds(S_1)}(t)$ as indicated in Fig. 2.4(a).

- $\phi \geq \theta_d$: when $C_{ds(S_1)}$ is completely discharged, $i_{pri}(t)$ starts flowing through D_1 causing $v_{ds(S_1)}(t)$ to drop to zero. Since $\phi \geq \theta_d$, $i_{pri}(t)$ is negative when S_1 turns on, therefore the transition is completely ZVS as depicted in Fig. 2.4(b). Therefore, the condition for the transistors of inverter 1 to achieve ZVS is:

$$\phi \geq \theta_d \tag{2.6}$$

Substituting (2.6) into (2.3), we have:

$$|I_0| \geq I_{zvs,min} = \frac{nV_2}{X_L}(1 + M)\theta_d = \frac{V_1 + nV_2}{L_s} \times T_d \tag{2.7}$$

(a) $\psi = 29$ degrees, $T_d = 500$ ns; $\phi < \theta_d$, partial ZVS; current spikes may be caused by re-commutation.

(b) $\psi = 30$ degrees, $T_d = 400$ ns; $\phi \geq \theta_d$, the transition is completely ZVS.
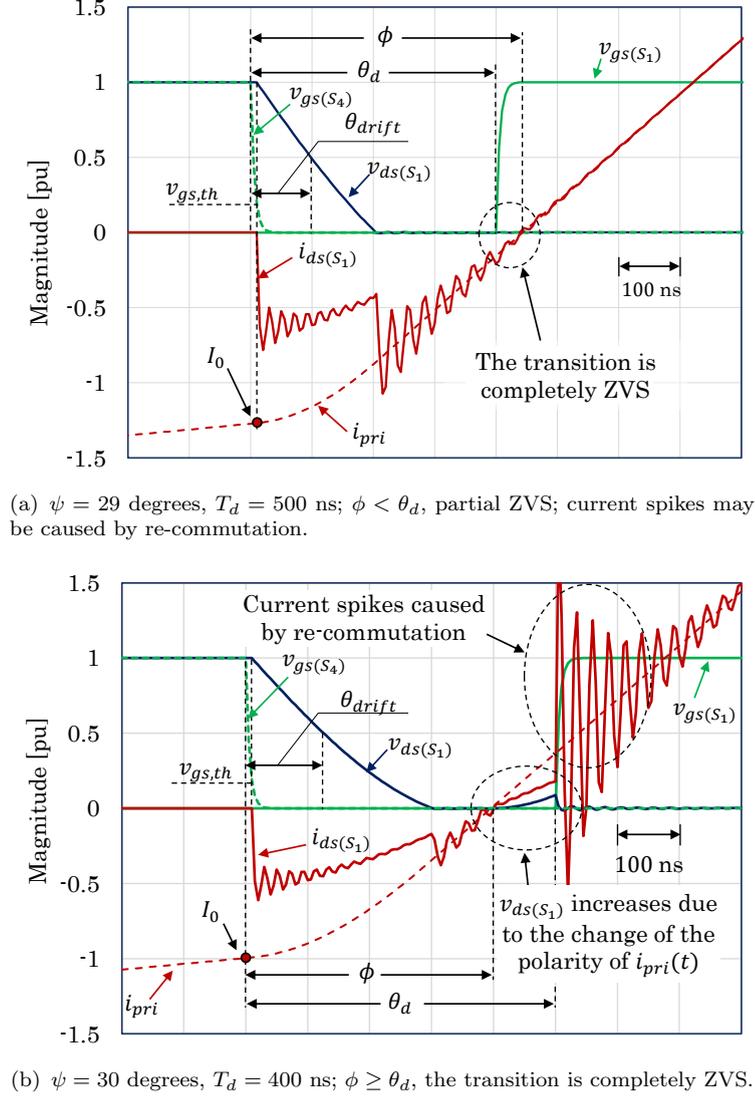
Figure 2.4. Simulation waveform of two switching scenarios of S_1 of inverter 1; $V_1 = 400$ V, $V_2 = 500$ V ($M = 0.8$), $L_s = 100$ μH, and $f_s = 50$ kHz.

where $I_{zvs,min}$ is the minimum transition current to completely charge/discharge the body capacitor during the dead-time interval T_d.

As for the secondary side, the transistors of inverter 2 turn on with the transition current of $I_{\psi,sec} = nM \times I_\psi$ as demonstrated in the simulation waveforms in Fig. 2.5. When $I_{\psi,sec} < I_{zvs,min}$, the discharge process of the output capacitors takes longer time than T_d causing partial ZVS and current spikes on the transistors. This situation is depicted in Fig. 2.5(a). Fig. 2.5(b) describes the switching waveform of T_1 when $I_{\psi,sec} \geq I_{zvs,min}$. In that case, since I_ψ is big enough, $C_{ds(T_1)}$ is completely discharged, and $v_{ds(T_1)}(t)$ is zero at turn-on. Therefore, the condition

for the transistors of inverter 2 to achieve full ZVS is:

$$I_\psi \geq \frac{I_{zvs,min}}{nM} = \frac{V_2}{V_1} \times \frac{V_1 + nV_2}{L_s} \times T_d \tag{2.8}$$

Substituting (2.3) and (2.7) into (2.8), then combining with (2.6), the united ZVS condition is derived as (2.9), where Φ_{min} is the minimum load angle to maintain ZVS.

$$\phi \geq \Phi_{min} = \max\left\{\theta_d, \ \frac{1}{nM^2}\theta_d + \left(1 - \frac{1}{M}\right)\frac{\pi}{2}\right\} \tag{2.9}$$
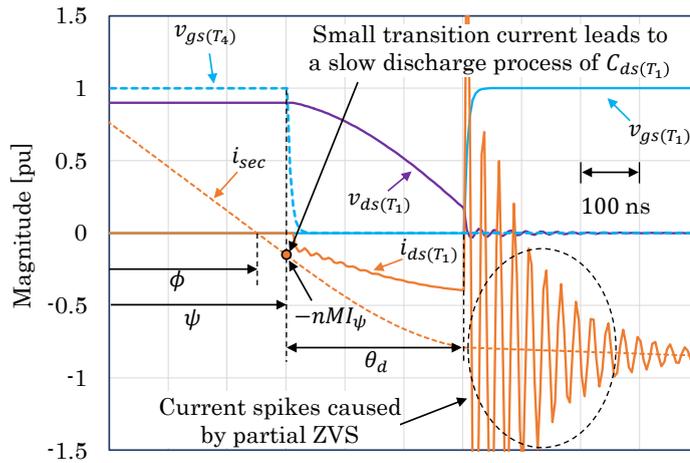
(a) $\psi = 26$ degrees, $T_d = 300$ ns; $I_\psi < I_{zvs,min}$: small transition current leads to a slow discharge process of $C_{ds(T_1)}$; current spikes may be caused by partial ZVS.
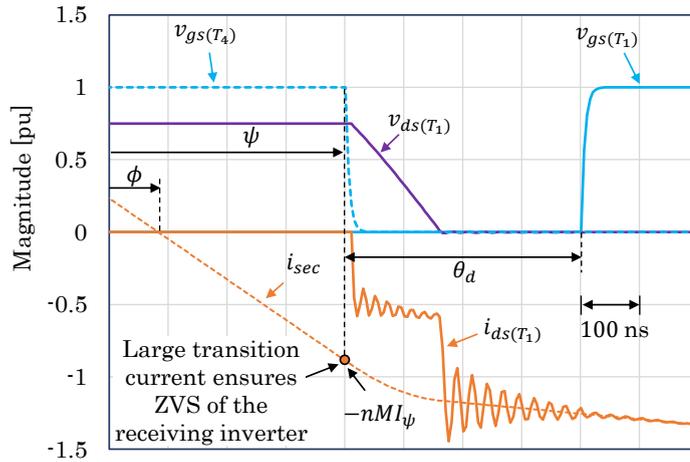
(b) $\psi = 25$ degrees, $T_d = 400$ ns; $I_\psi \geq I_{zvs,min}$: large transition ensures completely ZVS of switches of the receiving inverter.

Figure 2.5. Two ZVS scenarios of T_1 of inverter 2; $V_1 = 400$ V, $V_2 = 300$ V ($M = 1/0.75$), $L_s = 100$ μH, and $f_s = 50$ kHz.

By rearranging (2.2), ψ can be calculated from the load angle ϕ as:

$$\psi = (1 + M) \times \phi + (1 - M) \times \frac{\pi}{2} \tag{2.10}$$

From (2.9) and (2.10), the ZVS condition is rewritten in term of ψ:

$$\psi \geq \begin{cases} (1 + M)\,\theta_d + (1 - M)\,\dfrac{\pi}{2} & , M \leq 1 \\[3mm] \dfrac{1 + M}{nM^2}\theta_d + \left(1 - \dfrac{1}{M}\right)\dfrac{\pi}{2} & , M > 1 \end{cases} \tag{2.11}$$

2.2 Modulation strategy

2.2.1 Modulation function

In order to reduce the reactive power in the system, the load angle should be as small as possible. The united ZVS condition (2.9) suggests that the smallest load angle to ensure ZVS of all switches is Φ_{min}. If ϕ can be regulated at Φ_{min}, the reactive power (and thus, the conduction loss, rms current, current stress, etc.) can be reduced. This can be done by using (2.10).

Equation (2.10) implies that there will always be a phase shift angle to help obtain any given load angle. However, if ψ is used for regulating ϕ, there must be one more modulation variable to handle the magnitude of the power flow which is usually estimated by (2.12):

$$P = \frac{nV_1V_2}{\pi X_L}\psi(\pi - \psi) \tag{2.12}$$

Since P is inversely proportional to the switching frequency f_s, let f_s be the additional control variable. A new modulation strategy combining both frequency variation and phase shifting (FPS) can be established. The target of the proposed modulation method is to minimize the load angle while maintaining ZVS for all transistors by:

– manipulating the bridge shift angle ψ to regulate the load angle ϕ at Φ_{min};
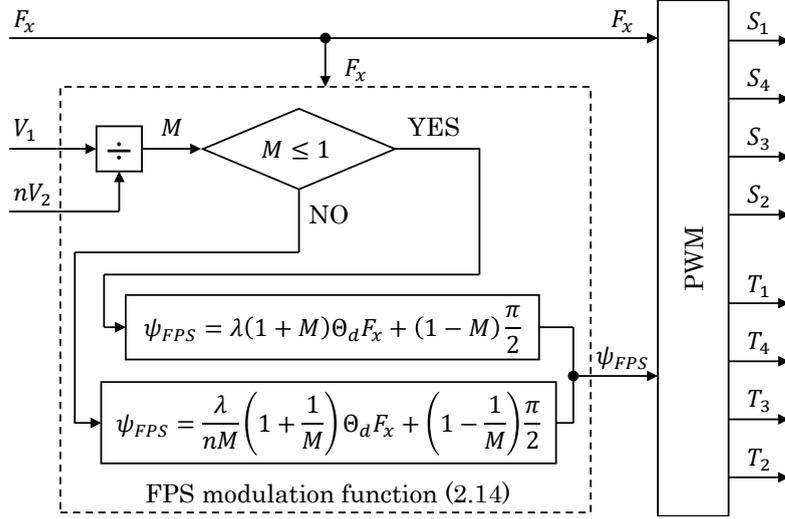
Figure 2.6. FPS function block.

− and at the same time, varying the switching frequency f_s to control the magnitude of the transferred power in the system.

Note that, when f_s varies, the dead-phase caused by the dead-time also changes according to the following equation:

$$\theta_d = 2\pi F_s T_d \times F_x = \Theta_d F_x \tag{2.13}$$

where F_x is the normalized frequency defined by the ratio between the actual switching frequency f_s over the nominal one F_s, $F_x = \frac{f_s}{F_s}$; and Θ_d is the dead-phase at the nominal switching frequency, $\Theta_d = 2\pi F_s T_d$. Substituting (2.13) into (2.11), the modulation function of the proposed FPS method is expressed by (2.14):

$$\psi_{FPS} = \begin{cases} \lambda \left(1 + M\right) \Theta_d F_x + (1 - M)\dfrac{\pi}{2} & , M \leq 1 \\[2mm] \dfrac{\lambda}{nM}\left(1 + \dfrac{1}{M}\right)\Theta_d F_x + \left(1 - \dfrac{1}{M}\right)\dfrac{\pi}{2} & , M > 1 \end{cases} \tag{2.14}$$

The coefficient λ in (2.14) is necessary as it allows a margin for the phase drift phenomenon and for parameters variation. Furthermore, λ can also be utilized to handle the depth of ZVS. A greater value of λ results in the deeper ZVS, and vice versa. For simplify the implementation, in this chapter, λ is set to 1 ($\lambda = 1$).

Function block of the proposed FPS modulation method is demonstrated in Fig. 2.6. The normalized frequency F_x is the dominant control variable. The controller varies F_x to regulate the power flow at the desired state. The phase shift ψ_{FPS} is derived from F_x and the feedback voltage ratio M to keep ϕ at its minimal of Φ_{min}.

Fig. 2.7 illustrates the FPS trajectory and its corresponding power curves in two cases of the voltage ratio. The normalized frequency F_x is varied from 6.0 downward until reaching the maximum power. At the same time, the bridge shift angle ψ_{FPS} is calculated using (2.14). In both cases of M, the calculation results of P are well matched to the simulation ones.

(a) $V_1 = 45\ V$, $nV_2 = 50\ V$ ($M = 0.9$), $L_s = 10.66\ \mu H$, $T_d = 250\ ns$, $\lambda = 1$, $F_s = 50\ kHz$.

(b) $V_1 = 50\ V$, $nV_2 = 40\ V$ ($M = 1.25$), $L_s = 10.66\ \mu H$, $T_d = 250\ ns$, $\lambda = 1$, $F_s = 50\ kHz$.
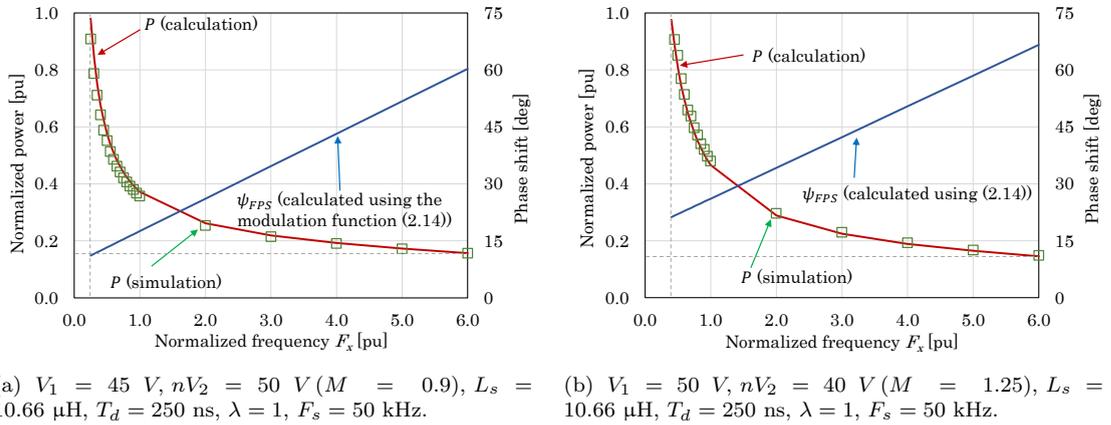
Figure 2.7. FPS trajectories and their corresponding power curves.

2.2.2 Frequency variation limitation

There are some remarks observed from the illustration in Fig. 2.7:

– *Remark 1:* When transferring a small amount of power while maintaining ZVS, the switching frequency is increased to a very high value. In the small power range, although F_x increases dramatically, P decreases slightly, especially when M is close to unity. In fact, there must be a high limitation of $F_{x,max}$ for frequency variation due to the switching capability of switching devices.

The selection of $F_{x,max}$ also depends on the design of the transformer core which is usually designed at a given nominal frequency (F_s). Operating the core at a much higher switching frequency leads to the rise of winding AC resistance due to the skin and proximity effects. Hence, overall performance might be degraded by the unexpected additional copper loss.

– *Remark 2:* Contrarily, large power is transferred at very small F_x. The transmission becomes very sensitive as a small drop in F_x may lead to a big growth in P. Moreover, since the peak flux density is inversely proportional to the switching frequency, when F_x drops too deeply, the transformer might be saturated. Therefore, a low limitation of $F_{x,min}$ should be applied to prevent the transformer from saturating. Because of the low limitation, it is hard to modulate the converter by the original FPS to reach the maximum transmission power.

The reverse of the flux density of the transformer decides the selection of $F_{x,min}$. Let B_{pk} be the peak flux density of the transformer at the nominal frequency F_x (already known when designing the transformer). When the converter operates at $F_{x,min}$, the peak flux density is B_{max}; B_{max} should be equal to 70% ∼ 80% of the saturation flux density (can be found from the datasheet of the magnetic material). According to [69], the number of turns of the primary winding N_{pri} can be calculated by (2.15), where $V_{1,rms}$ is the rms voltage across the primary winding; A_c is the cross section area and $K_f = 4.0$ for square voltage waveform:

$$N_{pri} = \frac{V_{1,rms}}{A_c K_f B_{pk} F_s} = \frac{V_{1,rms}}{A_c K_f B_{max} F_s F_{x,min}} \tag{2.15}$$

From (2.15), $F_{x,min}$ is selected as follows:

$$F_{x,min} = \frac{B_{pk}}{B_{max}} \tag{2.16}$$

When F_x varies within the range of $[F_{x,min}, F_{x,max}]$, the modulation can control the power flow while regulating the load angle at desired value of Φ_{min}. As F_x reaches its limitation, the number of degrees of freedom reduces to only one, which

is the phase shift. At that time, F_x remains at its limitation and, conventionally, ψ starts changing to adjust the power. However, as mentioned above, F_x has been chosen as the dominant control variable while ψ is derived by using the unified function (2.14). The change of the dominant variable from F_x to ψ will add more complexity into the control system. Therefore, the FPS method is being modified to compensate for the frequency limitation.

2.2.3 Modified FPS modulation strategy

Let $F_{x,nl}$ be the frequency without limitation, ψ_{nl} is determined by substituting $F_{x,nl}$ into (2.14). The transmission power obtained by applying the combination $(F_{x,nl}; \psi_{nl})$ is:

$$P_{nl} = \frac{nV_1V_2}{\pi X_L} \times \frac{\psi_{nl}(\pi - \psi_{nl})}{F_{x,nl}} \tag{2.17}$$

When a limiter is applied, the output of the frequency limiter is $F_{x,wl}$. In order to obtain the same amount of transferred power P_{nl}, the required phase shift is ψ_{wl}:

$$P_{nl} = \frac{nV_1V_2}{\pi X_L} \times \frac{\psi_{wl}(\pi - \psi_{wl})}{F_{x,wl}} \tag{2.18}$$

Solving (2.17) and (2.18) for ψ_{wl}, we have the modification function (2.19) to compensate for the limitation of F_x.

$$\psi_{wl} = \frac{\pi}{2} - \sqrt{\frac{F_{x,wl}}{F_{x,nl}}\psi_{nl}(\psi_{nl} - \pi) + \frac{\pi^2}{4}} \tag{2.19}$$

When $F_{x,nl}$ is in the range $[F_{x,min}, \ F_{x,max}]$, $F_{x,nl} = F_{x,wl}$, therefore, from (2.19), $\psi_{wl} = \psi_{nl}$. The modification function (2.19) does not affect the operation of the original FPS method. When $F_{x,nl}$ is out of the limitation, $F_{x,wl}$ is fixed at $F_{x,min}$ or $F_{x,max}$. The phase shift ψ_{wl} calculated by (2.19) is other than ψ_{nl} to help achieve the same amount of power P_{nl}. The function block of the FPS modulation strategy with the addition of the modification function (2.19) is shown in Fig. 2.8. Notes that, since both $F_{x,nl}$ and $F_{x,wl}$ are employed as the input signals of (2.19),
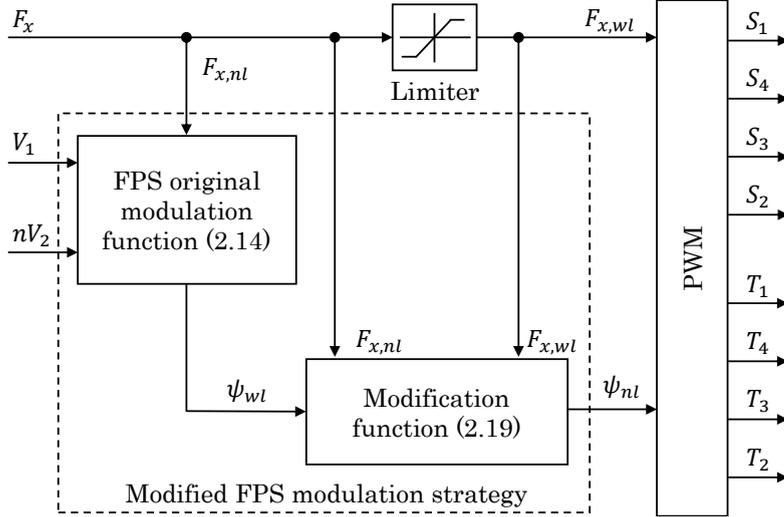
Figure 2.8. Function block of the modified FPS strategy.

the anti-windup function of the controller is not necessary, then realization of the control system can be simpler.

Fig. 2.9(a) presents the differences between the original FPS and the modified FPS (MFPS) modulation trajectories in various cases of the voltage ratio. In the figure, the MFPS trajectories are indicated by the continuous curves whereas, the original ones are graphed by the dashed lines. In the range $[F_{x,min}, F_{x,max}]$, the original FPS and the MFPS trajectories are coincident. And thus, the minimum load angle Φ_{min} can be achieved. As $F_{x,nl} > F_{x,max}$, ψ_{nl} keeps increasing corresponding to the increment of $F_{x,nl}$. Since $F_{x,wl}$ is fixed at $F_{x,max}$, the compensated phase shift
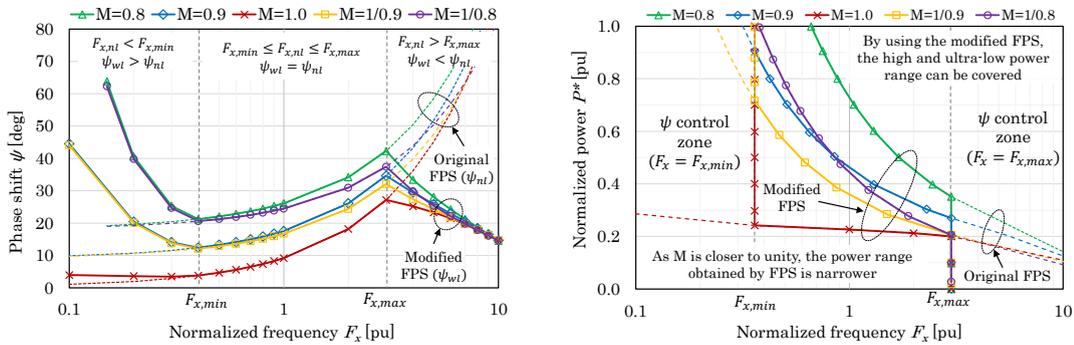
(a) FPS and MFPS modulation trajectories in various cases of M.

(b) Transmission power obtained by FPS and MFPS in various cases of M.

Figure 2.9. The FPS and MFPS trajectories, and their corresponding power curves ($V_1 = 50$ V, $L_s = 10.06$ μH, $T_d = 500$ ns, $\lambda = 1$, $F_s = 50$ kHz, $F_{x,min} = 0.36$, $F_{x,max} = 3.0$, $P^* = 1$ pu $\Leftrightarrow P = 500$ W).

angle ψ_{wl} decreases to reduce the transfered power. As a consequence, the obtained load angle is smaller than the desired one, Φ_{min}. The ZVS constraint (2.9) might be conflicted. However, this is a trade-off between switching loss and conduction loss: ZVS and the AC resistance (conduction loss) will be increased, or partial ZVS (or even hard-switching) and the AC resistance is kept at an acceptable level. Similarly, when $F_{x,nl} < F_{x,min}$, ψ_{wl} rises to allow more power to be transmitted. ZVS is ensured; however, the load angle tends to be greater than its minimal Φ_{min}. Although the dissipation might not be the minimum, the magnetic core is prevented from saturation.

The relation between the switching frequency and the transmission power is described in Fig. 2.9(b). In the figure, the dashed and continuous lines represent the power obtained by applying the original FPS and the modified FPS, respectively. When modulating the converter by the original FPS, the transmission power range is narrower as M is closer to unity. In such a situation, it is very difficult to cover all the power range; otherwise, the switching frequency must be ultra high or ultra-low. When M is other than 1 (e.g. $M = 1.25$), although the original FPS can cover the medium and heavy power range, it cannot expand the transmission to the low power level. That is the common problem of the modulation techniques based only on the frequency variation such as VFM [53]. By applying the MFPS, the whole power range can be covered regardless of how big M is. For example, in order to achieve an ultra-low power transmission, the switching frequency must be very high. Thanks to MFPS, an equivalent combination $(F_{x,wl}, \psi_{wl})$ can be utilized to achieve the desired transfered power without violating the frequency limitation.

2.3 Experiment results

2.3.1 System description

In order to evaluate the proposed modulation strategy, a laboratory-scaled experiment system illustrated in Fig. 2.10 is built. Parameters of the experiment system

are summarized in Table 2.1. A programmable power supply is connected to port 1, whereas a DC electronic load is connected to port 2. The voltage at port 1 is fixed at 50 V, meanwhile port 2 voltage is varied to achieve different voltage ratio M. The port currents are measured by two Hall-effect current transducers, FA-050P. The port voltages are sensed by two Hall-effect voltage sensors, LV25-P. The proposed MFPS method is then implemented in a DSP TMS320F28335 control card.

The transformer used in experiment is shown in Fig. 2.11. In order to achieve high leakage inductance while avoid using an external inductor, shell winding structure (Fig. 2.11(a)) is employed for constructing the transformer. In which, the core height is divided into two halves, each half is filled by a winding. At the designated switching frequency of 50 kHz, the skin depth [70] is:

$$\epsilon = \frac{0.662}{\sqrt{F_s}} \approx 0.3 (\text{mm}) \tag{2.20}$$

Hence, magnet wire sized AWG28 with the bare width of 0.32 mm is employed. Both primary and secondary windings are wound on a ETTD52 ferrite core by Litz wire which is made by twisting 21 strands to reduce the proximity effect as well
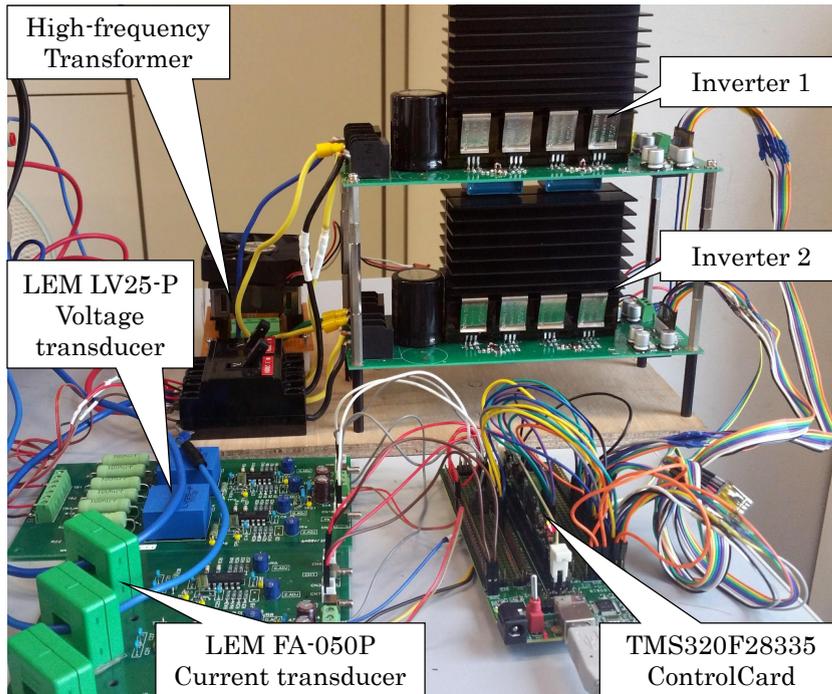
Figure 2.10. Laboratory-scaled 500 W experiment system.

as the winding resistance. The number of turns of both windings are 11, thus the transformer ratio is 1 : 1. The magnetizing and leakage inductance measured at
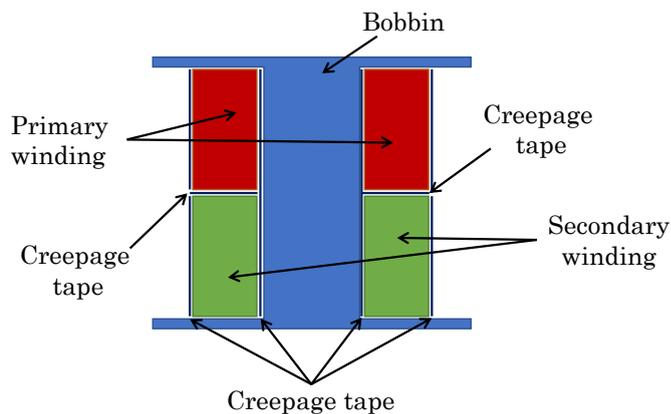
(a) Shell winding topology.
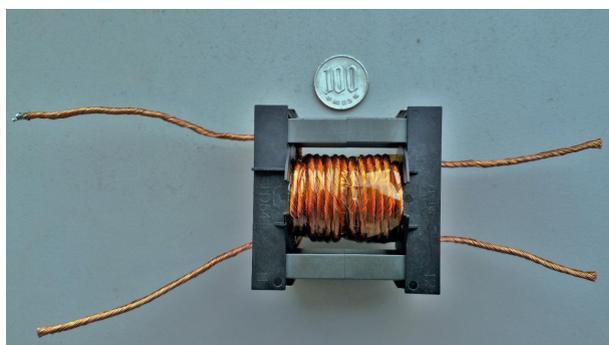
(b) Actual transformer.

Figure 2.11. Transformer used in experiment

TABLE 2.1: List of parameters of the DAB converter.

Parameter	Symbol	Value	Unit/Note
Transformer ratio	n	1:1	
Transformer core		ETD54	EPCOS
Number of turns	N	11	turns
Total inductance	L_s	10.06	µH (@ 50 kHz)
Total resistance	R_s	100	mΩ (@ 50 kHz)
MOSFET	S_{1-4} T_{1-4}	CSD19536KCS	
Terminal 1 voltage	V_1	50	V
DC capacitor	C_1, C_2	6400	µF
Nominal switching frequency	F_s	50	kHz
Dead-time	T_d	500	ns

50 kHz are 530 µH and 10.06 µH, respectively. The designated peak flux density is about 90 mT. The maximum flux density B_{max} is set to 250 mT, thus the low limitation $F_{x,min}$ is 0.36 (i.e. the minimum switching frequency is 18 kHz). The high limitation $F_{x,max}$ of 3.0 is selected (i.e. the maximum switching frequency is 150 kHz). The dead-time is fixed at $T_d = 500$ ns. The coefficient λ is set to 1.0.

Aiming to examine the performance of the proposed MFPS, open-loop evaluations is conducted in comparison with the VFM (which is also based on frequency variation) and the conventional SPS methods. As for the VFM, since there is no specific recommendation for selecting the transition current I_{zvs} in [53], it is examined with $I_{zvs} = I_{zvs,min}$, $I_{zvs} = I_{zvs,min} + 1$ and $I_{zvs} = I_{zvs,min} - 1$ simultaneously. Here, $I_{zvs,min}$ (see (2.7)) is selected as a reference since it is the minimum transition current to completely charge/discharge the drain-source capacitor of MOSFETs within the dead-time as mentioned above. All three modulation methods are investigated under some different conditions of voltage ratio M. The MFPS and VFM modulation trajectories used in the experiments are shown in Fig. 2.12. When $M < 1$ the MFPS trajectory is coincident with the VFM when the transition current of VFM, I_{zvs}, is set to $I_{zvs,min}$ as shown in Fig. 2.12(a) for the case of $M = 0.95$. In contrast, if $M > 1$, the MFPS and VFM ($I_{zvs} = I_{zvs,min}$) trajectories are different from each other (Fig. 2.12(b)).

(a) $M = 0.95$.

(b) $M = 1.15$.
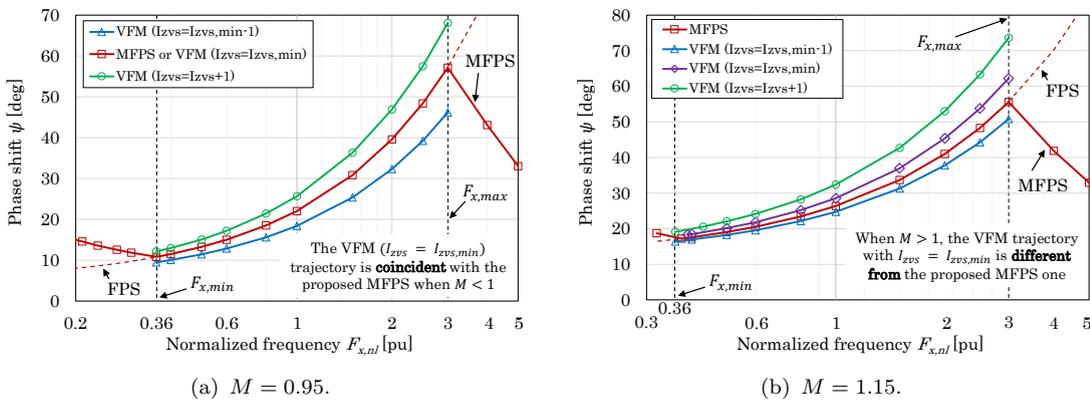
Figure 2.12. Modulation trajectories used in experiment.

2.3.2   Load angle maintenance capability

The load angle comparison is illustrated in Fig. 2.13. In the experiments, the load angle is determined by measuring the time from the point when $v_{ds(S_1)}(t)$ starts falling to the zero crossing point of the transferred current $i_{pri}(t)$. In Fig. 2.13, the trajectory of the minimum load angle Φ_{min} is indicated as the dashed black line. When M is closest to unity (Fig. 2.13(b)), the load angle ϕ_{MFPS} obtained by using MFPS (the square-marked, red curve) is most coincident to Φ_{min} in the frequency variable range. As M gets farther from unity, the phase drift phenomenon has more effect leading to a larger gap between Φ_{min} and ϕ_{MFPS}. The biggest gap of approximately 1.7 degrees is recorded when transferring 500 W at $M = 1.25$ (Fig.2.13(d)). In the scale of 360 degrees, this error is insignificant and ignorable. Hence, it can be concluded that, in all investigated cases of M, the ϕ_{MFPS} is well adhered to Φ_{min}, especially in the high frequency (low power) range. When

(a) $V_1 = 50$ V, $V_2 = 58.82$ V ($M = 0.85$), $I_{zvs,min} = 5.10$ A.

(b) $V_1 = 50$ V, $V_2 = 52.63$ V ($M = 0.95$), $I_{zvs,min} = 4.81$ A.

(c) $V_1 = 50$ V, $V_2 = 43.48$ V ($M = 1.15$), $I_{zvs,min} = 4.43$ A.

(d) $V_1 = 50$ V, $V_2 = 40$ V ($M = 1.25$), $I_{zvs,min} = 4.22$ A.
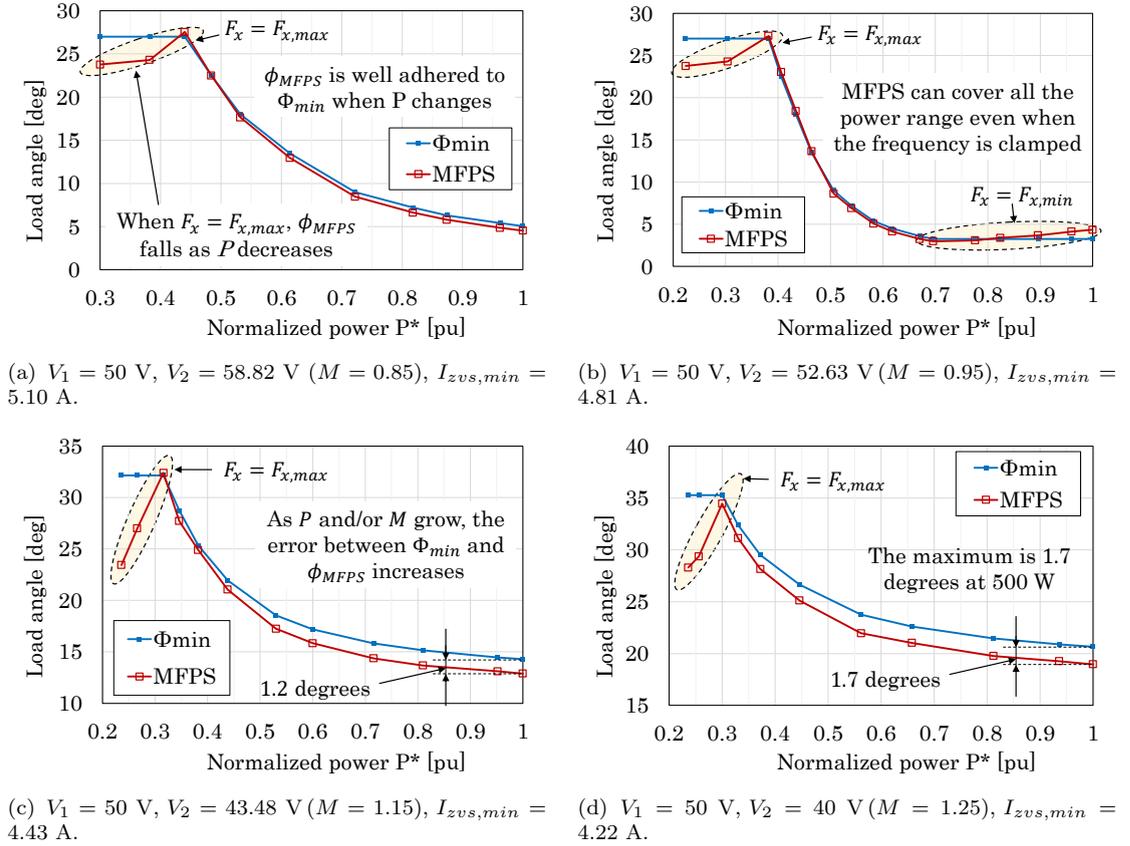
Figure 2.13. Comparison of load angle between MFPS and VFM
($P^* = 1$ pu $\Leftrightarrow P = 500$ W).

the switching frequency reaches its limits, the load angle tends to rise/fall at the heavy/light power transmission, as claimed above.

2.3.3   ZVS achievement capability

Regarding the VFM method, when it is implemented with $I_{zvs} = I_{zvs,min} + 1$, the obtained load angle is greater than Φ_{min}. Contrarily, when I_{zvs} is set to $I_{zvs,min} - 1$, the measured load angle is smaller. Since Φ_{min} is the minimum load angle to overcome the dead-phase θ_d (caused by the dead-time), when the generated load angle is less than Φ_{min}, partial ZVS might occur. One example for this situation is demonstrated in Fig. 2.14. The comparison results are summarized in Table 2.2.

When transferring a 265 W with $M = 0.95$ by employing VFM ($I_{zvs} = I_{zvs,min} - 1$) (VFM 1), the calculated F_x and ψ are 0.36 ($f_s = 18$ kHz) and 9.51, respectively. The measured efficiency is 93.87%, however the peak current is 10.4 A. ZVS is not achieved and current spikes appear as shown in Fig. 2.14(a). The peak voltage stress on the MOSFET is 70.8 V, which is 1.42 times higher than the terminal voltage.

If MFPS is utilized, the power of 265 W is transferred at the switching frequency of 40 kHz ($F_x = 0.8$). As observed from Fig. 2.14(b), the measured load angle is 7.26 degrees which is almost equal to Φ_{min} at 40 kHz (7.2 deg). The peak current is reduced 8 A while ZVS is fully achieved. As a result, the efficiency is boosted by 1.83%.

When using VFM with setting I_{zvs} to be $I_{zvs,min} + 1$ (VFM 2), in order to transfer the same amount of power, modulation parameters of the VFM method are $F_x =$

TABLE 2.2: ZVS capability comparison between VFM and MFPS.

	VFM 1	**MFPS**	**VFM 2**
	$I_{zvs} = I_{zvs,min} - 1$	$I_{zvs} = I_{zvs,min}$	$I_{zvs} = I_{zvs,min} + 1$
$V_{ds,peak}$	**70.8** V	50 V	50 V
$I_{pri,pk}$	10.4 A	8.0 A	**7.8** A
Efficiency	93.87%	**94.25%**	**92.42%**
ZVS	**NO**	YES	YES

1.5 (f_s = 75 kHz) and ψ = 36.29 deg. Although ZVS is achieved and the peak current is reduced to 7.8 A, the conduction loss increases due to the increment
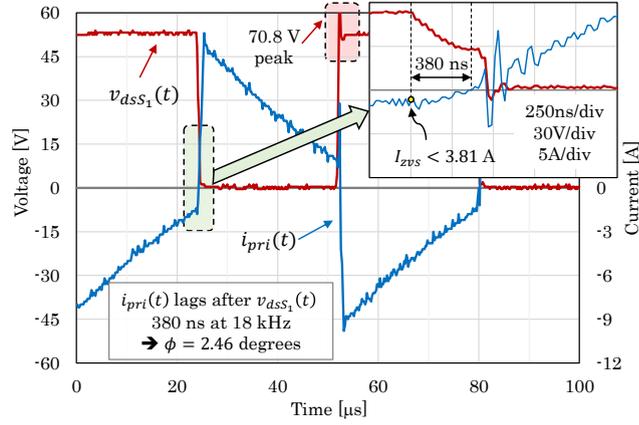
(a) **VFM 1:** $F_x = 0.36$ (f_s = 18 kHz), ψ = 9.51 deg, $I_{zvs} = I_{zvs,min} - 1 = 3.81$ A.
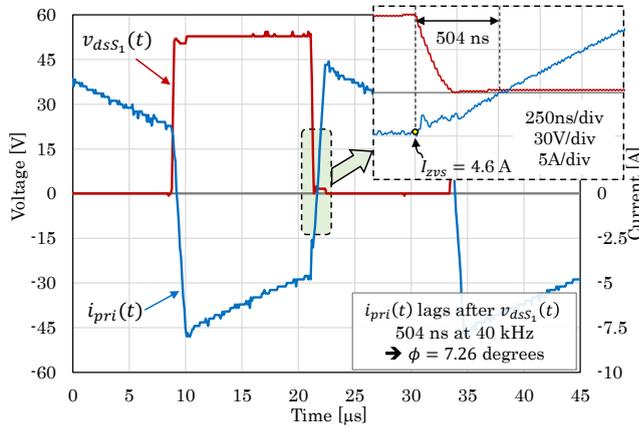
(b) **MFPS:** $F_x = 0.8$ (f_s = 40 kHz), ψ = 18.54 deg.
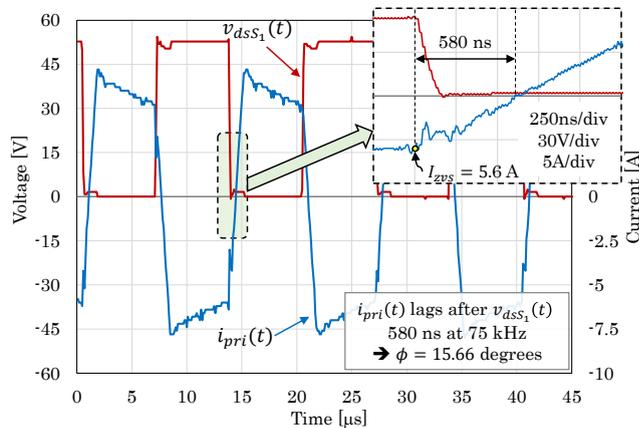
(c) **VFM 2:** $F_x = 1.5$ (f_s = 75 kHz), ψ = 36.29 deg, $I_{zvs} = I_{zvs,min} + 1 = 5.81$ A.

Figure 2.14. The switching behaviors of VFM and MFPS when sending 265 W with $M = 0.95$.

of the circulating power. Consequently, the overall efficiency is slightly decreased to 92.42%. This is due to the increment of the load angle from 2.46 deg in the previous case to 15.66 deg (Fig. 2.14(c)).

2.3.4 Power range expansion

When $M \leq 1$, the voltage at the transmitter side is smaller than the receiver one, thus, the DAB converter operates like a voltage booster. If the phase shift is zero, there will be no power flowing from port 1 to port 2, regardless of the switching frequency.

However, when $M > 1$, the converter undertakes a step down conversion. Under this condition, even when the phase shift is reduced to its minimum at zero, energy is still transferred to the low voltage side due to the potential difference. Hence, there exist a minimum power in the transmission which varies corresponding to the voltage ratio M.

As for the conventional SPS method, it is impossible to expand the power range since the phase shift cannot be smaller than zero or the power flow will be reversed. However, the power range can be significantly expanded by using the proposed MFPS method as reported in Fig. 2.15. In that experiment, the phase shift is kept
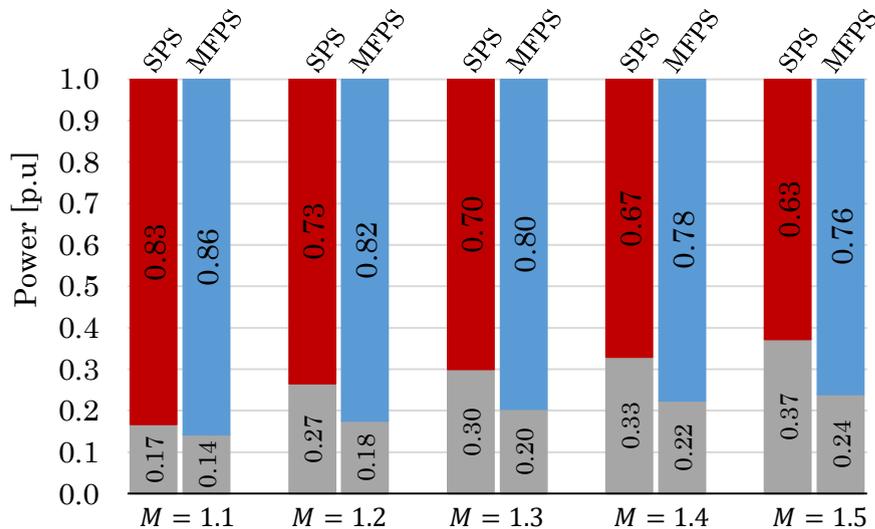
Figure 2.15. Power range comparison between SPS and MFPS methods; shaded areas express the non-coverable range.

at zero, whereas the switching frequency is fixed ($F_x = 1$ for SPS and $F_x = F_{x,max}$ for MFPS); at the same time, the voltage ratio is changed by gradually increasing the terminal 1 voltage.

As the voltage ratio increases, the power range appears to be narrower indicated by the in enlargement of the grayish areas in Fig. 2.15. When SPS method is employed ($F_x = 1$), the effect is very remarkable, especially at high voltage ratio. For example, the size of the non-coverable zone rises from 17% when $M = 1.1$ to 37% when $M = 1.5$ and even more for bigger value of M.

When the proposed MFPS method is used, by setting F_x to 3, the power range is significantly expanded. When $M = 1.1$, the expansion is only 3%. However, it grows gradually as M increases and becomes 12% when $M = 1.5$. That is because the power is inversely propositional to the switching frequency. Hence, the increment of the maximum frequency will result in the decrement of the minimum power.

The maximum switching frequency, which depends on the switching capability of the MOSFET, can be further increased for more expansion of the power range. However, due to the skin and the proximity effects, the AC resistance of the transformer will significantly ascend that lead to the downgrade of the system efficiency. Therefore, compromise should be taken between the efficiency and the coverable power range.

2.3.5 Efficiency comparison

2.3.5.1 MFPS versus SPS

Fig. 2.16 presents the efficiency comparisons among the proposed MFPS, the VFM and the conventional SPS modulation strategies. As for the SPS method, its switching frequency is set to the nominal one ($F_x = 1$) meanwhile the phase shift is increased gradually from ψ_{FPS} until reaching the maximum power of 500 W. In the low power range, the efficiency obtained by SPS method is higher than by methods based on frequency variation. Although hard-switching is occurred, the

switching loss it caused is smaller than the additive conduction loss due to the increment of switching frequency. Nevertheless,as the transferred power increases, the conduction loss caused by SPS method becomes significant resulting in the decrement of efficiency at medium and high power range.

In contrary, the frequency variation based methods like MFPS, can maintain high efficiency at high power because under that condition, both switching frequency and phase shift are smaller than that of the SPS method. Therefore, not only switching loss is eliminated because of soft-switching, conduction loss is also reduced as another consequence. In other words, MFPS method can enhance the efficiency at medium and high power range. For example, when transferring 1 pu of power under the condition: $V_1 = 50$ V and $V_2 = 40$ V ($M = 1.25$), the maximum efficiency enhancement is approximately 7% (Fig. 2.16(d)).

Since SPS can help achieve higher efficiency at low power range whereas MFPS is

(a) $V_1 = 50$ V, $V_2 = 58.82$ V ($M = 0.85$), $I_{zvs,min} = 5.10$ A.

(b) $V_1 = 50$ V, $V_2 = 52.63$ V ($M = 0.95$), $I_{zvs,min} = 4.81$ A.

(c) $V_1 = 50$ V, $V_2 = 43.48$ V ($M = 1.15$), $I_{zvs,min} = 4.43$ A.

(d) $V_1 = 50$ V, $V_2 = 40$ V ($M = 1.25$), $I_{zvs,min} = 4.22$ A.
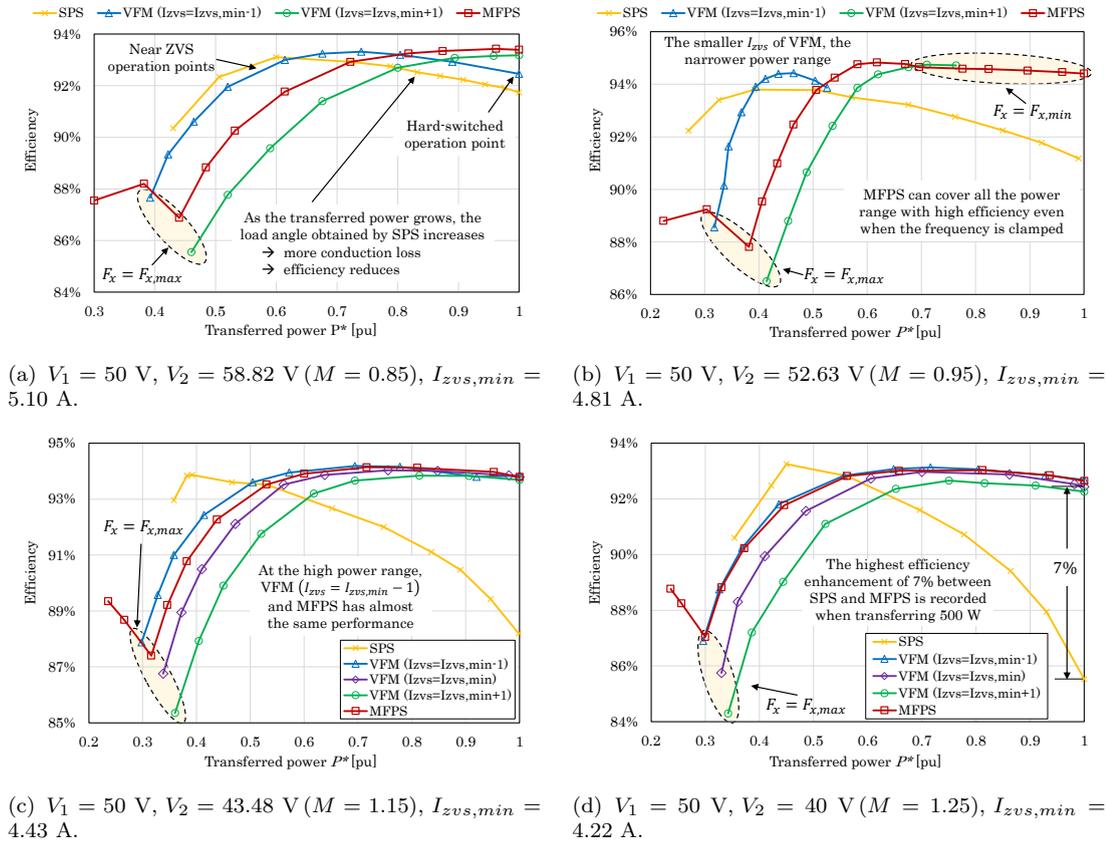
Figure 2.16. Efficiency comparison among MFPS, VFM and SPS
($P^* = 1$ pu $\Leftrightarrow P = 500$ W).

the superior at the medium and high power range, a combination method between SPS and MFPS can be formed by setting the maximum switching frequency to be the nominal one, or $F_{x,max} = 1$. Thereby, high efficiency can be maintained in the whole coverable power range, however, at some prices:

- Since $F_x = 1$, switching frequency is not increased, hence the coverable power range cannot be expanded as claimed before.

- Not only the coverable power range, but also the soft-switching range is not expanded. The converter might suffer from hard-switching at low power range.

2.3.5.2 MFPS versus VFM

Comparison between the MFPS and the VFM is more difficult since performance of the VFM depends on the selection of I_{zvs}. In term of maximum efficiency, a comparison among the three methods is presented in Table 2.3 with data taken from Fig. 2.16. As seen, when the voltage of the transmitting side is less than the receiving one ($M \leq 1$), the proposed MFPS shows the highest performance. However, when $M > 1$, though MFPS can still maintain high efficiency, the maximum efficiency of other methods is a little bit higher.

The MFPS works less efficiently than the VFM with $I_{zvs} = I_{zvs,min} - 1$ in the low and medium power ranges since transistors commutate under near ZVS condition. Among all investigated cases, the biggest gap in efficiency between MFPS and VFM ($I_{zvs} = I_{zvs,min} - 1$) is about -5% when transferring 190 W and $M =$

TABLE 2.3: Maximum efficiency comparison

M	VFM $(I_{zvs} = I_{zvs,min} - 1)$	VFM $(I_{zvs} = I_{zvs,min} + 1)$	VFM $(I_{zvs} = I_{zvs,min})$	SPS	MFPS
0.85	93.32%	93.39%	–	93.11%	**93.43%**
0.95	94.42%	94.75%	–	93.90%	**94.83%**
1.15	**94.18%**	93.84%	93.12 %	93.84%	94.14%
1.25	93.13%	92.66%	93.03 %	**93.25%**	93.03%

0.95 Fig. 2.16(b). As the power increases, the transition condition becomes hard-switching leading to the downgrade of efficiency in the high power level. When increasing the transition current I_{zvs} of the VFM strategy, its performance becomes worse than MFPS, especially in the medium and low power ranges. The maximum difference between MFPS and VFM is about 3% and 4.8% for two cases: $I_{zvs} = I_{zvs,min}$ and $I_{zvs} = I_{zvs,min} + 1$, respectively, when sending 165 W and $M = 1.25$ as depicted in (Fig. 2.16(d)).

Moreover, while the controllable power range covered by VFM depend on the voltage ratio M, MFPS can handle all the coverable power range regardless of how big of M. As observed in Fig. 2.16(b), when F_x is clamped at $F_{x,min}$, the efficiency is still high because ZVS is attained. However, corresponding to the growth of P, the efficiency falls gradually due to the increment of reactive power (load angle). When F_x reaches $F_{x,min}$, however, the efficiency increases at first then decreases. The reason is when ψ is big enough, partial ZVS is achieved leading to the rise of efficiency. Along with the reduction of ψ, the transition condition turns to be hard-switching then the converter works less efficiently. By increasing the high limitation $F_{x,max}$, ZVS operation area can be expanded. However the rise of AC resistance due to the skin effect and proximity effect of transformer winding at high frequency may downgrade the performance of the converter.

2.4 Conclusion

This chapter presented a new modulation strategy, in which frequency variation and phase shift modulation are combined. Some main advantages of this study are as follows:

- The new modulation strategy, MFPS, can control the load angle equally to the phase caused by the dead-time. As a consequence, reactive power was reduced.

− A modification function was proposed to modify the modulation parameters. Thanks to the tool, MFPS can extend the coverable power range compare to the conventional SPS method.

− A formula to estimate the minimum transition current to completely charge/discharge the output capacitor of MOSFET during the dead-time was introduced. It can be used as a reference for other research on the same topic.

− The proposed MFPS can boost the efficiency by approximately 7% compared to the conventional single-phase-shift method.

− By limiting the maximum switching frequency to the nominal one, the proposed MFPS method acts as the conventional one (SPS) under the light load condition then the efficiency will be highest, however, at the prices of hard-switching and narrow power range.

However, there are still also some limitations needing further studies:

− The proposed method can extend but cannot cover the whole power range. This can be conducted by combining not only frequency variation and phase shift, but also the duty cycle modulation. However, this is beyond the scope of this dissertation.

− As experimented, the efficiency when operating the converter under the partial ZVS condition was sometimes even higher than under the completely ZVS one. Since MFPS can handle the load angle, it can also manipulate the converter under the partial ZVS condition. This can be done by reducing the depth of ZVS, or in other words, decreasing the coefficient λ in the modulation function (2.14). However, determining the appropriate value for λ is also out of the scope of this study.

Chapter 3

Dynamic control

In the previous chapter, a new modulation method named MFPS which combines frequency variation and phase shift modulation was proposed. As confirmed by open loop experiment, it perform very well in the medium and high power range. Furthermore, it can help extend the soft-switching area as well as the power range of the converter.

In this chapter, a closed-loop control system is developed to implement the proposed modulation strategy. Intentionally, the control system is designed with one inner current-loop and one outer voltage loop as indicated in Fig. 3.1. The current and the voltage at the port 2 are selected as the controlled variables, whereas the normalized switching frequency is the only control variable.
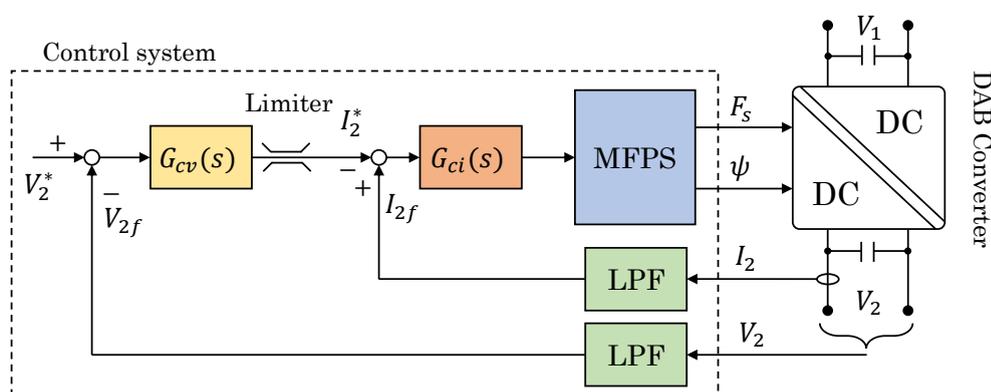
Figure 3.1. Control system diagram.

3.1 Current loop

3.1.1 Modeling

The average current at port 2 in one half cycle, $I_{2,avg}$, is defined by:

$$I_{2,avg} = \frac{1}{\pi} \int_{\psi}^{\pi+\psi} \left(-\frac{i_{pri}(\theta)}{n} \right) d\theta \tag{3.1}$$

where $\theta = \omega_s t$ and:

$$\frac{di_{pri}(\theta)}{d\theta} = \begin{cases} -\dfrac{R_s}{X_L} i_{pri}(\theta) + \dfrac{1}{X_L} \Big(V_1(\theta) - nV_2(\theta) \Big), & \theta \in [\psi, \pi] \\[2mm] -\dfrac{R_s}{X_L} i_{pri}(\theta) - \dfrac{1}{X_L} \Big(V_1(\theta) + nV_2(\theta) \Big), & \theta \in [\pi, \pi + \psi] \end{cases} \tag{3.2}$$

where R_s is the equivalent resistance of the transmission path.

From (3.1) and (3.2), $I_{2,avg}$ can be represented as:

$$\frac{dI_{2,avg}}{dt} = -\frac{R_s}{L_s} I_{2,avg} + \frac{2V_1}{n\pi L_s} \psi - \frac{V_1 - nV_2}{nL_s} \tag{3.3}$$

It is obvious that $I_{2,avg}$ depends on the bridge phase shift angle ψ. Since F_x is selected as the only control variable, the right hand side of (3.3) should be rewritten with regard to F_x. However, when substituting (2.14) and (2.19) into (3.3), two possible models will be obtained depending on the value of the voltage ratio; and both models will become highly nonlinear when $F_{x,nl}$ is out of $[F_{x,min}, F_{x,max}]$. This makes the control system more complicated.

From another aspect, assume that there is no loss in the transmission, the current at the port 2 can be determined from (2.12):

$$I_{2,avg} = \frac{nV_1}{\pi X_L} \psi(\pi - \psi) \times \frac{1}{F_x} \tag{3.4}$$

By linearizing (3.4) around the nominal operation point ($F_x = 1$), the small signal model $i_{2,avg}$ is:

$$i_{2,avg} = -\frac{nV_1}{\pi X_L} \psi(\pi - \psi) \times f_x \tag{3.5}$$

Accordingly, the transfer function from $f_x(s)$ to $i_{2,avg}(s)$ is:

$$G_{i2fx} = \frac{i_{2,avg}(s)}{f_x(s)} = -\frac{nV_1}{\pi X_L}\psi(\pi - \psi) \tag{3.6}$$

3.1.2 Current controller design

The diagram of the current loop is shown in Fig. 3.2. Assumes that, in one sampling cycle, the voltage is constant that the current controller can be designed independently of the influence from the voltage variation. Notes that, since G_{if} is negative, the feedback network is positive whereas the reference current is set negative. It is true because the current is inversely proportional to the switching frequency. According to the diagram, when the feedback current i_{2f} is smaller than the reference, the error is negative then f_x is decreased leading to the decrement of the frequency. Contrarily, when i_{2f} exceeds the reference current, the error becomes positive then f_x is increased yield to the increment of the switching frequency.
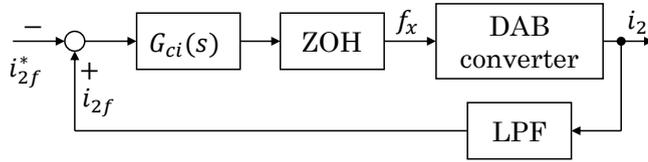
Figure 3.2. Current loop diagram.

The sampling frequency of the current loop is fixed at 50 kHz. Due to the sampling operation, the zero-order-hold (ZOH) is introduced in the control diagram. The transfer function of the ZOH block is approximated by the Pade approximation (3.7). The first order low pass filter LPF is designed with the crossover frequency of one-tenth of the switching frequency (3.8).

$$G_{ZOH}(s) = \frac{1 - \dfrac{s}{4F_{sample}}}{1 + \dfrac{s}{4F_{sample}}} \tag{3.7}$$

$$G_{LPF}(s) = \frac{1}{1 + \dfrac{10s}{\omega_s}} \tag{3.8}$$

where s is the Laplace operator, F_{sample} is the sampling frequency and $\omega_s = 2\pi f_s$.

From (3.6), (3.7) and (3.8), the model of the plant of the current loop is derived as:

$$G_{if} = -\frac{nV_1}{\pi X_L}\psi(\pi - \psi) \times \frac{1 - \dfrac{s}{4F_s}}{(1 + \dfrac{s}{4F_s})(1 + \dfrac{10s}{\omega_s})} \qquad (3.9)$$

Since the switching frequency varies from $F_{x,min}$ to $F_{x,max}$, the crossover frequency of the open-loop is chosen equal to one-tenth of the minimum switching frequency. In order to compensate for the variation of ψ due to the modulation strategy MFPS, the phase margin of the open-loop is set to 75 degrees. Thereby, the PI-modified typed II controller can be designed. Substitutes the parameters listed in Table 2.1 into (3.9) and chose the operation point of: $V_1 = 60$ V; $V_2 = 50$ V ($M = 1.25$), $F_x = 1$ and $\psi = 30$ degrees, we have:

$$G_{ci}(s) = \frac{4798}{s} \times \frac{s + 1.09e4}{s + 2.27e4} \qquad (3.10)$$

The Bode diagram of the open loop system is illustrated in Fig. 3.3. The blue curve represents the characteristics of the plant itself, while the red curve describes the open loop response. As desired, at the chosen crossover frequency, the phase margin of the open loop is 75 degrees. Besides, the gain margin of the open loop
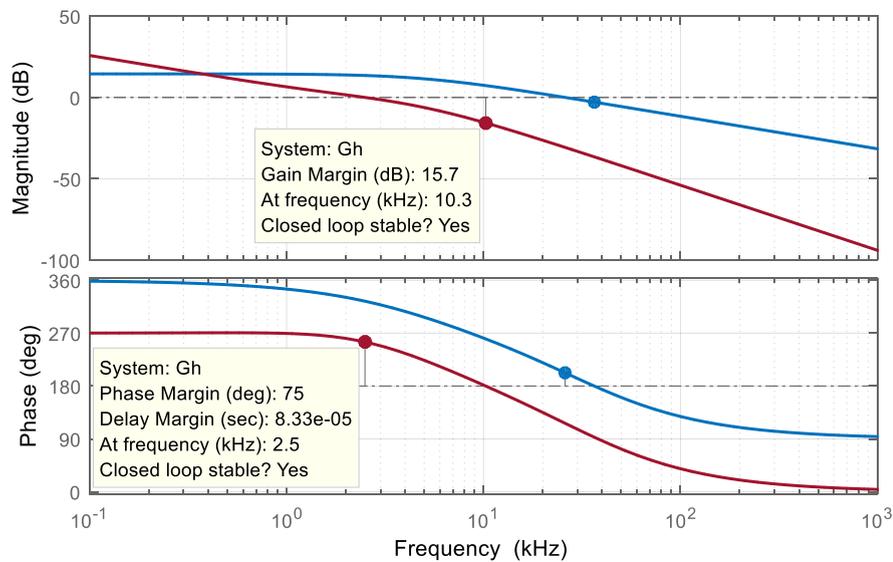
Figure 3.3. Bode diagram of the open current loop.

is 15.7 dB at 10 kHz ensuring all the noise which frequency higher than 10 kHz will be reduced more than 6 times in amplitudes.

3.2 Voltage loop

The diagram of the voltage control loop is described in Fig. 3.4. In order to ensure the assumption that the voltage is constant in one sampling cycle of the current loop, the sampling frequency of the voltage loop is 10 times slower than that of the current loop, thus, the ZOH function block of the voltage loop is approximated by:

$$G_{ZOH,v}(s) = \frac{1 - \dfrac{s}{4F_{sample,v}}}{1 + \dfrac{s}{4F_{sample,v}}} \tag{3.11}$$

where $F_{sample,v} = 500$ Hz.
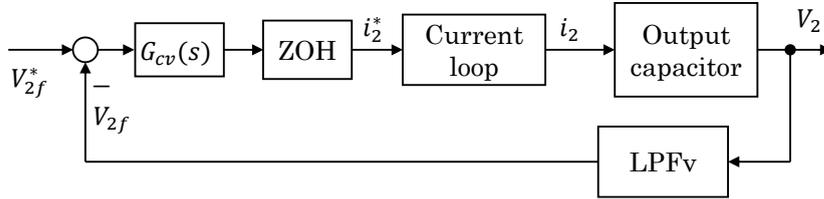
Figure 3.4. Voltage loop diagram.

The transfer function from $i_{2,avg}(s)$ to the terminal voltage $v_2(s)$ can be easily derived as:

$$G_{v_2 i_2}(s) = \frac{v_2(s)}{i_{2,avg}(s)} = \frac{R_{Load}}{1 + s(R_{Load} + r_c)C_2} \tag{3.12}$$

where R_{Load} is the load equivalent resistance; r_c and C_2 are the series resistance and the capacitance of the output capacitor of port 2.

The transfer function of the closed current loop can be also be determined without difficulty as:

$$G_{ii^*}(s) = \frac{i_2(s)}{i_2^*(s)} = \frac{G_{ci}(s)G_{ZOH}(s)G_{i2fx}}{1 + G_{ci}(s)G_{ZOH}(s)G_{i2fx}G_{LPF}(s)} \tag{3.13}$$

The low pass filter LPFv is designed with the crossover frequency of 1 percent of the nominal switching frequency (i.e. 500 Hz):

$$G_{LPFv}(s) = \frac{1}{1 + \dfrac{100s}{\omega_s}} \tag{3.14}$$

Finally, the transfer function of the plant of the voltage loop is yielded:

$$G_{vi} = G_{ZOH,v}(s)G_{ii^*}(s)G_{v_2 i_2}(s)G_{LPF,v}(s) \tag{3.15}$$

Since the DAB converter is intentionally employed as the voltage pre-regulator for the grid-tied inverter within the whole solid-state-transformer (SST), the crossover frequency of the voltage loop is selected as 35 Hz to reduce the influence of the utility frequency. At the same time, the phase margin is set to 75 degrees for ensuring the system robustness against load changes.

Based the above design parameters, the PI-modified typed II controller can be derived. Upon the rated power operation point where

$$R_{Load} = \frac{V_2^2}{P_{2,rated}} = \frac{50^2}{500} = 5 \ (\Omega),$$

substitutes into (3.15) with information in Table 2.1, the controller parameters can be calculated as:

$$G_{ci}(s) = \frac{2186}{s} \times \frac{s + 32.1}{s + 1504} \tag{3.16}$$

Fig. 3.5 shows the Bode diagram of the open voltage loop and the plant as the red and blue curves, respectively. At the crossover frequency of 35 Hz, the phase margin of the open loop is 75 degrees as desired. The gain margin is 21.4 dB at the frequency of 253 Hz tells that all variation faster than 253 Hz will be weaken nearly 12 times. That is meaningful as the DAB serves in the SST operating at utility frequency. In that situation, the 300 Hz (or 360Hz) voltage fluctuation reflecting from the AC side to DC side will be mostly suppressed.
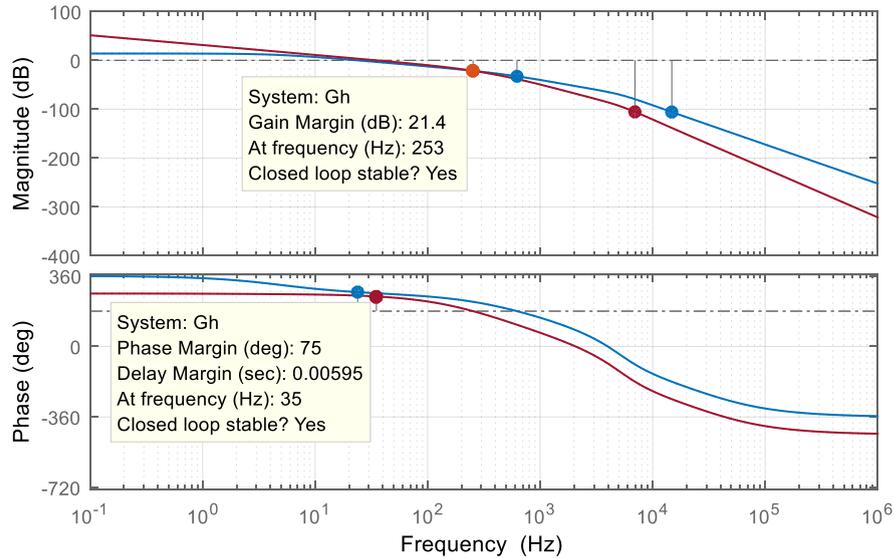
Figure 3.5. Bode diagram of the open voltage loop.

For faster response of the voltage to load change, the crossover frequency can be increased but not too much as that one of the plant is about 100 Hz for the same phase margin. In contrary, the voltage variation suppression effect will be weaken due to the reduction of gain margin.

3.3   Experiment results

The experiment system is the same as depicted in Fig. 2.10 in Chapter 2. All the control system is implemented in the DSP TMS320F28335. The system clock is set at 150 MHz. The sampling time of the current loop is fixed at 50 kHz, while that of the voltage loop is set 10 times slower at 500 Hz. Both DC terminal currents are measured by two ADC channels for both protection and control. As the maximum current is 10 amps, the threshold for shutting down as failure is 20 amperes (twice the rated current). Both port voltages are also measured for calculating the voltage ratio for the MFPS strategy and for regulation.

In all experiments below, the programmable power supply at terminal 1 is configured at the constant voltage mode of 60 V. While the DC electronic load at terminal 2 is set at the constant resistance mode. The desired voltage at terminal 2 is 50 V, thus, the voltage ratio is expected to be $M = 1.2$.

3.3.1 Current loop response

At first, only the current control loop is verified. The referent current is fixed at 8 amperes while the terminal voltages are 60 V and 50 V, respectively ($M = 1.2$). Fig. 3.6 describes the response of the output current as the red curve.
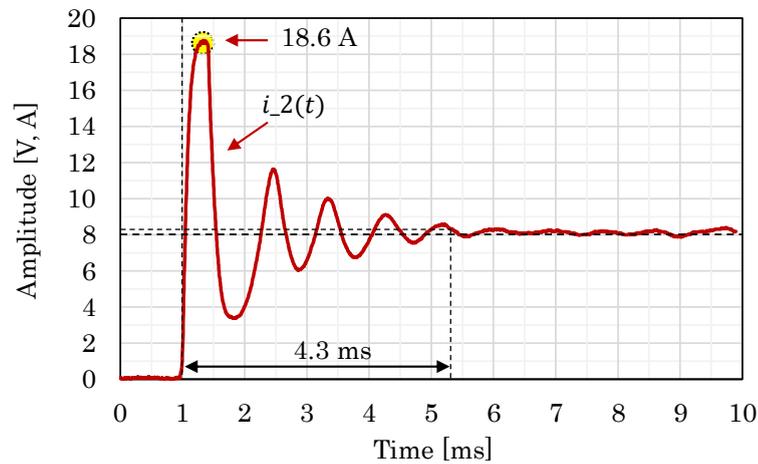
Figure 3.6. Response of the current loop.

The response time of the current is about 40 µs, which is much faster than expected. As the selected crossover frequency is 2.5 kHz, the expected rise time should be 400 µs, which is ten times slower than the measured result. The settling time is, however, much longer at 4.3 ms. Besides, there are high overshoot (18.6 A) and oscillation. That is true because the dynamic of the current was ignored when modeling to avoid nonlinearity and complexity. Nevertheless, since the oscillation frequency is about 740 Hz, it does not affect the terminal voltage as it is far bigger than the crossover frequency of the voltage loop (35 Hz). The high current overshoot, however, may cause unexpected protection as the threshold is only 20 A.

3.3.2 Starting up

In this experiment, the voltage loop performance is confirmed in starting up. The voltage at port 1 is still 60 V and the reference for terminal 2 is 50 V. The test is conducted in two cases: light load and full load start-up. According to Fig. 2.15

about the coverable power range, because the voltage ratio is $M = 1.2$, the load resistance is set at 25 Ω (which is 20% of the rated load (5 Ω)) for the light load start-up.
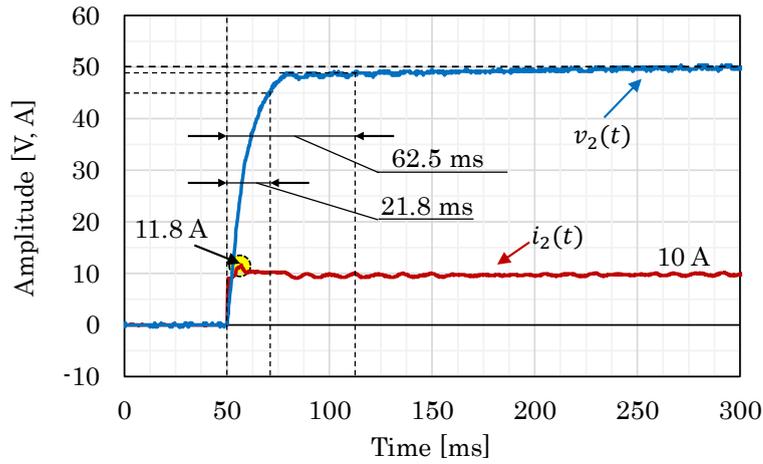
(a) Full load start-up.
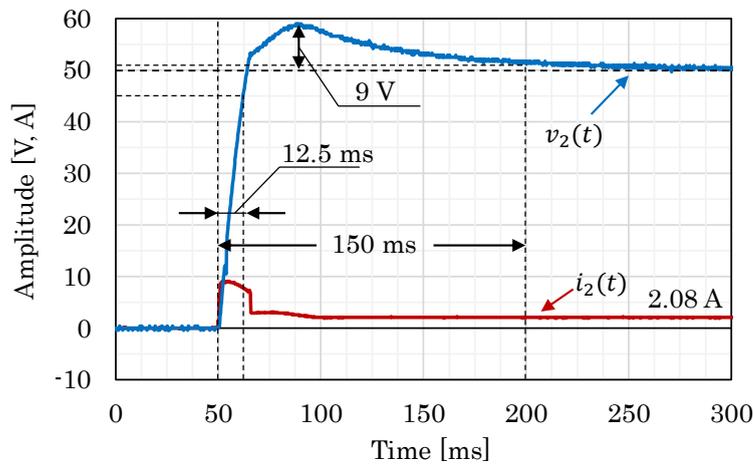
(b) Light load start-up.

Figure 3.7. Start-up response.

Fig. 3.7 illustrates the start-up responses in two mentioned cases. When starting up at the rated condition, the rising time is about 21.8 ms thank to the designed crossover frequency of 35 Hz as shown in Fig. 3.7(a). After the rising time, the voltage is stable without any overshoot or fluctuation. The corresponding current response records an overshoot of 20%, but rapidly vanishes in few mili-seconds.

When stating up with small load, the rising time is even faster at only 12.5 ms (Fig. 3.7(b)) showing that when the load grows, the crossover frequency of the open loop increases. However, as discussed before, the other consequence it led

is the decrement of the robustness as an overshoot of 18% is recorded. Besides, although the rising time is short, the settling time is much longer at approximately 150 ms. The overshoot as well as the settling time can be shorten by designing the voltage controller at the medium power range. However, under high power condition, the rising time might be longer.

3.3.3 Load change

This experiment investigates the robustness of the voltage regulation system when load changes. At first, the load is initialized at 20%, which is the minimum coverable power at $M = 1.2$. At a certain instant, an additional 60% load is suddenly connected to terminal 2 making the total load 80% of the rated. After some time, the added load is shed from terminal 2, then the load once again become 20%. The results are illustrate in Fig. 3.8.

When suddenly adding the load, there is an undershoot of -16.4% in the voltage characteristics as shown in Fig. 3.8(a). At the same time, the current increases dramatically with an overshoot of about 14 amps to compensate for the undershoot. After the response time of about 13 ms, the voltage is restored and becomes stable after 80.5 ms. Because of the maximum current of the programmable power supply is 10 A, the output of the voltage controller was set to 10 A. If it is increased, the voltage can restore faster and thus lessening the voltage undershoot.

On the other hand, when the added load is shed, the voltage is swollen about 11% as described in Fig. 3.8(b). The rising time is short at 8 ms but the settling time is relatively long at 113 ms. After shedding the added load, the remain is the minimum coverable power at the voltage ratio of $M = 1.2$. Under this condition, the switching frequency equals to its maximum, while the phase shift is zero as analyzed in Chapter 2. Since all control variables reach theirs limitation, the voltage decreases gradually due to the discharge operation of the output capacitor on the load resistance without any control effort of the controller.
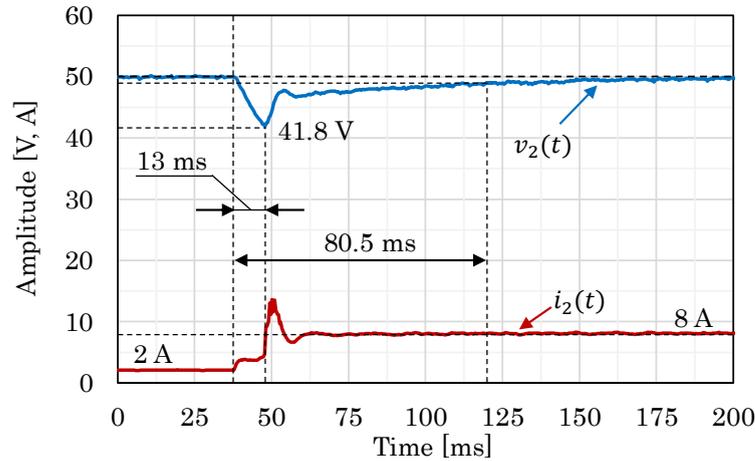
(a) Change from small to heavy load.
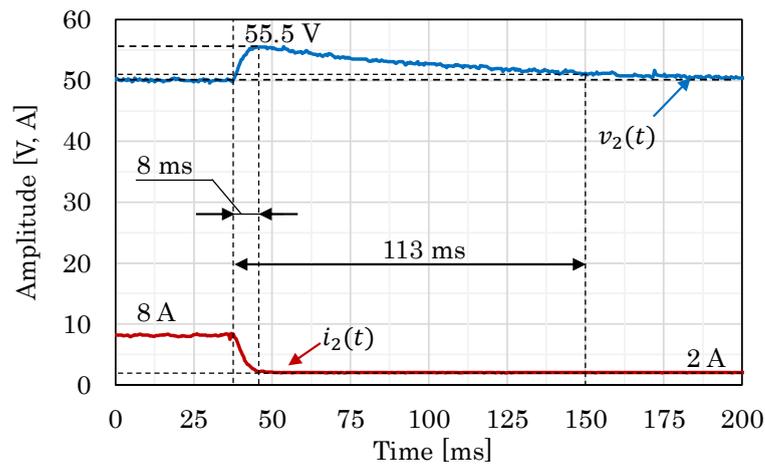
(b) Change from heave to small load.

Figure 3.8. Load change response.

3.3.4 Over loading

This experiment evaluate the protection operation of the control system under the overload condition. The result is presented in Fig. 3.9. Firstly, the system is operating at full load (i.e. $V_2 = 50$ V and $I_2 = 10$ A) and the load equivalent resistance is 5 Ω. At a certain instant, the resistance of the DC electronic load is suddenly reduced to 4.22 Ω. If the terminal voltage is kept stable, the output power will become approximately 600 W, which is 20% overloaded.

Nevertheless, the current limitation is 10 A as stated before. Hence, when the load steps up, after experiencing a 10% overshoot, the output current is regulated
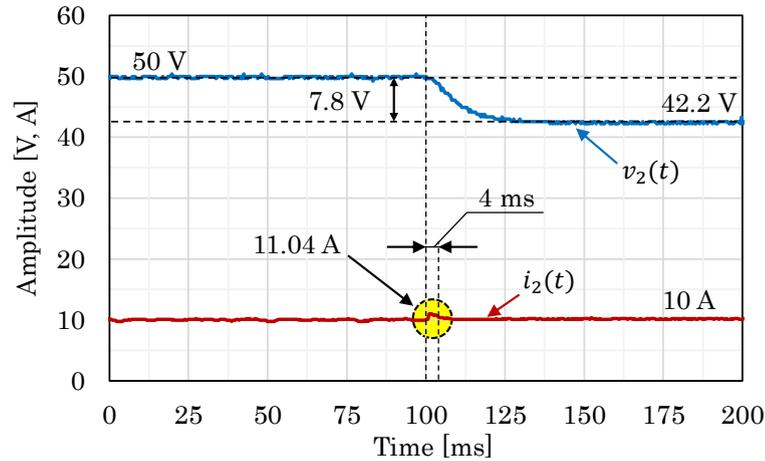
Figure 3.9. System response under the overload condition.

at its maximum value of 10 A in 4 ms. Since then, the converter acts as a current source and the terminal voltage is reduced due to the small resistance of the load.

3.3.5   Short circuit

In this experiment, short circuit fault will be intentionally created to examine the protection capability of the converter. As mentioned above, the current threshold is set at twice the maximum current, i.e. 20 A. It is expected that, when the current exceeds the threshold, the converter should shutdown by turning off all switches. The examination is reported in Fig. 3.10.
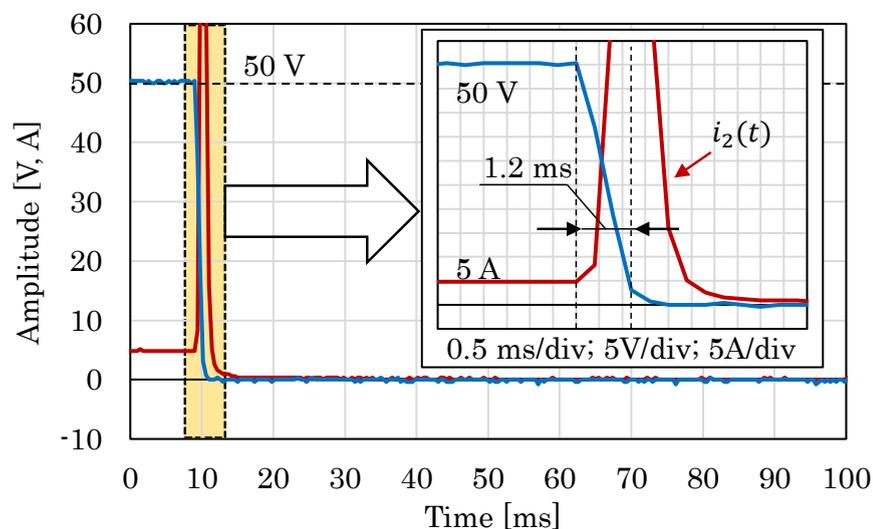
Figure 3.10. Protection action under the short circuit fault.

As shown, when the fault occurs, because the voltage is suddenly dropped, the current is increased to compensate for the reduction. Consequently, the switching frequency, according to the MFPS strategy, should be decreased to its minimum to rise the current. When the current exceeds the threshold, the system protects itself by forcing a shutdown after 1.2 ms since the occurrence of the fault.

As the sampling time is 50 kHz, it means that the shutdown command is given after 60 sampling cycles. Notes that the protection activity operates upon the DC terminal currents. Due to the large output capacitor as well as the delay introduced by the current measurement board, the measured current is slightly lagged from the original one. Besides, the digital low pass filter implemented inside the DSP which crossover frequency is one-tenth of the nominal switching frequency (5 kHz) also contributes 0.2 ms time lag.

3.4   Conclusion

This chapter reported the experimental verification of the MFPS strategy in Chapter 2 in transient state. A dual-loop cascade control system was designed and implemented for undertaking the proposed modulation technique. Some remarkable points of this chapter are as follows:

— The converter can serve as a constant voltage source in normal operation.

— When load changes, the voltage fluctuation was about -16.4% to 11% which are relatively high. They can be decreased by extending the range of the current limiter before feeding to the current control loop.

— The system can help operate like a current source to prevent overloading.

— With the designed control system, the converter can withstand the short-circuit fault in 1.2 ms before shutting down as a protection action.

— The current response was very fast. However, it contained high overshoot that may cause unexpected shutdown due to over current.

Chapter 4

Observer design for estimating system states

In the previous chapters, a modulation method named MFPS and its accompanied control system were proposed. The aim is to transfer the power between two ports of the DAB converter with the load angle minimized. The approach was to estimate and model the angle based on the linearity of the current slope. This is only valid in the trapezoidal current mode. In other modes, such as sinusoidal or triangle current modes, the load angle model changes, thus the modulation function is not unique. That is because the analysis was conducted in the time domain in which mathematic equations depend strongly on the current shape.

The approach of this chapter is to determine the load angle in the frequency domain, where the analysis is independent of switching states. Accordingly, an observer is designed to estimate the two current components from the transferred AC current. Since the angle is the arctangent of the quadrature component over the direct one, the load angle minimization issue becomes optimization of the two current components. Firstly, the design and verification of the observer is presented in this chapter.

4.1 Fundamental harmonic approximation

The DAB converter was depicted in Fig. 2.1 in Chapter 2. For applying the fundamental harmonic approximation method, the primary referred equivalent circuit of the converter expressed in Fig. 4.1 is used. The fundamental component of the voltages across the primary and secondary winding of the transformer are denoted as $v_{1e}(t)$ and $v'_{2e}(t)$, respectively; the fundamental component of the transferred current is $i_e(t)$; R_s and L_s are the equivalent primary referred resistance and inductance of the transmission network.
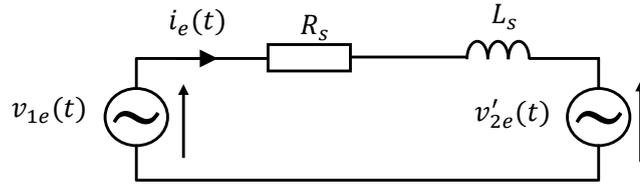
Figure 4.1. Primary referred equivalent circuit.

Since both inverters are modulated with the same switching frequency, the output voltages and the transferred current can be seen as rotation vectors $\vec{v}_{1e}, \vec{v}'_{2e}$, and $\vec{i}_e$ with the same angular speed of ω_s ($\omega_s = 2\pi f_s$). The projections of $\vec{v}_{1e}, \vec{v}'_{2e}$, and $\vec{i}_e$ on d-and q-axis of a dq-frame rotating synchronously with and being aligned along $\vec{v}_{1e}$ are DC components. A vector diagram demonstrating the relation of those vectors is depicted in Fig. 4.2 where δ is the impedance angle, $\delta = \arctan\left(\dfrac{\omega_s L_s}{R_s}\right)$; and two voltage vectors are determined by:

$$\vec{v}_{1e} = \begin{bmatrix} v_{1d}(t) \\ v_{1q}(t) \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} v_1(t) \\ 0 \end{bmatrix} \tag{4.1}$$

$$\vec{v}'_{2e} = \begin{bmatrix} v_{2d}(t) \\ v_{2q}(t) \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} nv_2(t)\cos\psi \\ nv_2(t)\sin\psi \end{bmatrix} \tag{4.2}$$

where $v_{1d}(t)$, $v_{1q}(t)$, $v_{2d}(t)$, and $v_{2q}(t)$ are the d- and q-components of the corresponding quantities.
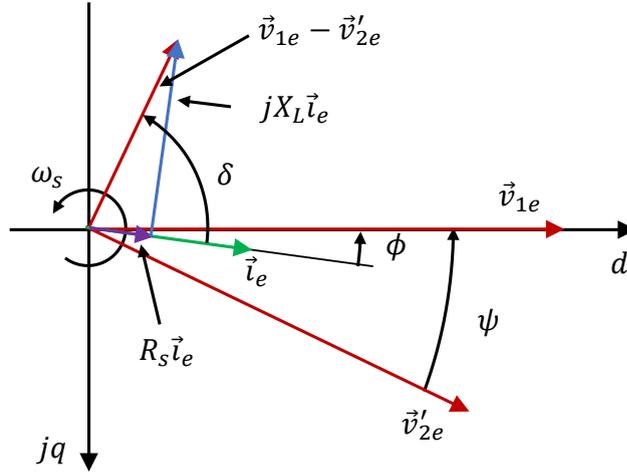
Figure 4.2. Vector diagram.

Let $i_d(t)$ and $i_q(t)$ be the projections of the current vector $\vec{i}_e$ on two axis of the dq-frame. When R_s is neglected, $i_d(t)$ and $i_q(t)$ can be determined by:

$$\vec{i}_e = \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} = \frac{1}{\omega_s L_s} \begin{bmatrix} v_{2q}(t) \\ v_{1d}(t) - v_{2d}(t) \end{bmatrix} \tag{4.3}$$

The instantaneous active and reactive powers seen from the DC side to the AC side of two inverters are defined by (4.4) and (4.5), respectively:

$$\begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{1d}(t)i_d(t) + v_{1q}(t)i_q(t) \\ v_{1d}(t)i_q(t) - v_{1q}(t)i_d(t) \end{bmatrix} \tag{4.4}$$

$$\begin{bmatrix} P_2 \\ Q_2 \end{bmatrix} = -\frac{1}{2} \begin{bmatrix} v_{2d}(t)i_d(t) + v_{2q}(t)i_q(t) \\ v_{2d}(t)i_q(t) - v_{2q}(t)i_d(t) \end{bmatrix} \tag{4.5}$$

Since d-axis of the rotating frame is intentionally aligned to $\vec{v}_{1e}$, the quadrature component of $\vec{v}_{1e}$ is zero, $v_{1q}(t) = 0$. Therefore, (4.4) is rewritten:

$$\begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} = \frac{2v_1(t)}{\pi} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} \tag{4.6}$$

From (4.6), assumed that $v_1(t)$ is constant in one switching cycle, the active power P_1 is proportional to the direct current $i_d(t)$, and the reactive power Q_1 is proportional to $i_q(t)$. Therefore, by regulating two current components, both active and

reactive powers at terminal 1 can be controlled. If the interaction between $i_d(t)$ and $i_q(t)$ can be eliminated, P_1 and Q_1 can be handled separately.

From another aspect, substituting (4.3) into (4.4) and (4.5), we have:

$$\begin{bmatrix} P_1 \\ Q_1 \end{bmatrix} = \frac{1}{2X_L} \begin{bmatrix} v_{1m}(t)v_{2q}(t) \\ v_{1m}(t)\left[v_{md}(t) - v_{2d}(t)\right] \end{bmatrix} \tag{4.7}$$

$$\begin{bmatrix} P_2 \\ Q_2 \end{bmatrix} = \frac{1}{2X_L} \begin{bmatrix} -v_{1m}(t)v_{2q}(t) \\ -v_{1m}(t)v_{2d}(t) + v_{2m}^2(t) \end{bmatrix} \tag{4.8}$$

where $v_{1m}(t) = \dfrac{4}{\pi}v_1(t)$ and $v_{2m}(t) = \dfrac{4}{\pi}v_2(t)$.

The displacement angles ϕ_1 and ϕ_2, which are the phase difference between the current vector and the two voltage vectors, can be determined by:

$$\begin{cases} \tan\phi_1 = \dfrac{Q_1}{P_1} = \dfrac{m - \cos\psi}{\sin\psi} \\ \tan\phi_2 = \dfrac{Q_2}{P_2} = \dfrac{-1 + m\cos\psi}{m\sin\psi} \end{cases} \tag{4.9}$$

where $m = \dfrac{v_1(t)}{nv_2(t)}$.

Equation (4.9) suggests that, ψ_1 and ϕ_2 depend tightly on the bridge shift angle ψ. For a given voltage ratio M, one displacement angle among those two can be regulated by varying ψ.

Note that, ZVS is achieved when ϕ_1 and ϕ_2 are positive and:

$$\begin{cases} \phi_1 \in \left[0; \dfrac{\pi}{2}\right] \text{ and } \phi_2 \in \left[\dfrac{\pi}{2}; \pi\right], & \text{if } P_1 = -P_2 \geq 0 \\ \phi_1 \in \left[\dfrac{\pi}{2}; \pi\right] \text{ and } \phi_2 \in \left[0; \dfrac{\pi}{2}\right], & \text{if } P_1 = -P_2 < 0 \end{cases} \tag{4.10}$$

Combining (4.9) and (4.10), the limitation of the bridge phase shift to ensure ZVS is:

$$\begin{cases} \psi \leq \min\left\{\arccos(m); \ \arccos\left(\dfrac{1}{m}\right)\right\}, & \text{if } P_1 = -P_2 \geq 0 \\ \psi \geq -\max\left\{\arccos(m); \ \arccos\left(\dfrac{1}{m}\right)\right\}, & \text{if } P_1 = -P_2 \leq 0 \end{cases} \tag{4.11}$$

Since ψ is manipulated to maintain soft-switching of the converter, the active power must be handled by another variable. From (4.4) and (4.5), it is obvious that all the power components are inversely proportional to the switching frequency. Thus, frequency variation is employed intending to regulate the active power components.

4.2 Current estimation using state observer

From the primary referred equivalent circuit depicted in Fig. 4.1, the vector diagram expressed in Fig. 4.2 and the Kirchhoff Law, the large signal model of the converter can be obtained:

$$
\begin{cases}
\dfrac{d}{dt}i_d(t) = & -\dfrac{R_s}{L_s}i_d(t) - F_x\Omega_s i_q(t) + \dfrac{4}{\pi L_s}v_1(t) - \dfrac{4n}{\pi L_s}v_2(t)\cos\psi \\
\dfrac{d}{dt}i_q(t) = & F_x\Omega_s i_d(t) - \dfrac{R_s}{L_s}i_q(t) - \dfrac{4n}{\pi L_s}v_2(t)\sin\psi
\end{cases}
\tag{4.12}
$$

where Ω_s is the nominal angular frequency, and F_x is the normalized frequency, $F_x = \dfrac{\omega_s}{\Omega_s}$. At the steady state, the nominal operating point is determined by:

$$
\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \frac{4nV_2}{\pi R_s} \times \frac{1}{1+Q^2} \times \begin{bmatrix} Q\sin\psi + M - \cos\psi \\ Q(M-\cos\psi) - \sin\psi \end{bmatrix}
\tag{4.13}
$$

where Q is the quality factor of the transmission network, $Q = \dfrac{\Omega_s L_s}{R_s}$; $M = \dfrac{V_1}{nV_2}$; V_1 and V_2 are the average terminal voltages at the steady state. In order to determine i_d and i_q, a state observer is developed.

4.2.1 Peak current approximation

Firstly, considering the fundamental current component, its peak, $i_m(t)$, is:

$$
i_m(t) = \sqrt{i_d^2(t) + i_q^2(t)}
\tag{4.14}
$$

The average absolute value of $i_e(t)$ is given by:

$$i_{abs,avg}(t) = \frac{2}{\pi} i_m(t) \qquad (4.15)$$

In practice, both $i_m(t)$ and $i_{abs,avg}(t)$ cannot be measured due to high switching frequency and non-sinusoidal current waveform. However, $i_{abs,avg}$ can be approximated by the average rectified transferred current, $i_{rec,avg}(t)$. In experiment, $i_{rec,avg}(t)$ is detected easily by using a low cost AC current sensor, such as a low-inductance-index toroidal core, to sense the transferred current before rectifying and filtering the obtained signal with rectifier and a low-pass filter, respectively.

The form factor, which is the ratio between $i_{rec,avg}(t)$ and $i_{abs,avg}$, implies the accuracy of the approximation. As named, its value depends on the waveform of the current, thus depends on the voltage ratio and the bridge shift angle as illustrated in Fig. 4.3. Since the current waveform is not affected by the frequency, the form factor is independent from the variation of F_x.

In the simulation results depicted in Fig. 4.3, the form factor is investigated by varying M from 0.5 to 2.0 and ψ from 0 degrees to 90 degrees, whereas the switching frequency is fixed at 50 kHz. As shown, the maximum form factor is about 1.1 pu., and the minimum is 0.95 pu. When ψ gets closer to 90 degrees, the form factor converges to unity since the current waveform is more symmetrical. In all
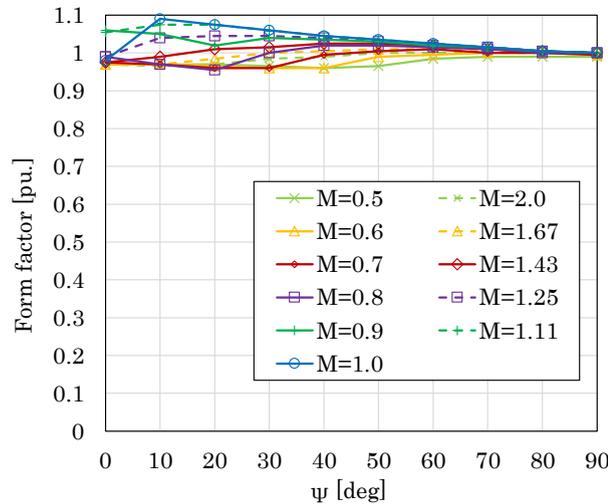
Figure 4.3. Form factor versus ψ and M, simulation condition: $L_s = 10$ µH, $V_1 = 50$ V, $n = 1 : 1$, $F_s = 50$ kHz and $F_x = 1$.

over the investigated cases, the average form factor is 1.0. Therefore, it is reliable to make the following approximation:

$$i_m(t) \approx \frac{\pi}{2} i_{rec,avg}(t) \tag{4.16}$$

The accuracy of the approximation can even be enhanced by adopting an adaptive coefficient, κ, as:

$$i_m(t) = \kappa \frac{\pi}{2} i_{rec,avg}(t) \tag{4.17}$$

In experiment, the coefficient κ might be changed according to the operation condition. For example, κ can be determined by using a lookup table based on the simulation results reported in Fig. 4.3. In this study, for simplicity, κ is intentionally set to 1.0.

4.2.2 Observer design

Let $i_m(t)$ be the output of the converter model, the small signal space state model (4.18) is derived by linearizing the large signal model (4.12) around the nominal operating point (4.13). In the model (4.18), the variation of terminal voltages in one sampling cycle is neglected. The small signal model, in which $i_m(t)$ is the output, is expressed by:

$$\begin{cases} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} \\ i_m &= \boldsymbol{C}\boldsymbol{x} + \boldsymbol{D}\boldsymbol{u} \end{cases} \tag{4.18}$$

where $\boldsymbol{x} = \begin{bmatrix} i_d \\ i_q \end{bmatrix}$, $\boldsymbol{u} = \begin{bmatrix} f_x \\ \psi \end{bmatrix}$, $\boldsymbol{A} = \begin{bmatrix} -\Omega_p & -\Omega_s \\ \Omega_s & -\Omega_p \end{bmatrix}$, $\boldsymbol{B} = \begin{bmatrix} -\Omega_s I_q & \dfrac{4n}{\pi L_s} V_2 \sin\psi \\ \Omega_s I_d & -\dfrac{4n}{\pi L_s} V_2 \cos\psi \end{bmatrix}$,

$\boldsymbol{C} = \begin{bmatrix} \dfrac{I_d}{I_m} & \dfrac{I_q}{I_m} \end{bmatrix}$, $\boldsymbol{D} = \begin{bmatrix} 0 & 0 \end{bmatrix}$; $\Omega_p = \dfrac{R_s}{L_s}$; $I_m = \sqrt{I_d^2 + I_q^2}$; i_d, i_q, f_x and ψ are the small signals of the corresponding quantities.

Considers the observability matrix:

$$\boldsymbol{O} = \begin{bmatrix} \boldsymbol{C} \\ \boldsymbol{C}\boldsymbol{A} \end{bmatrix} = \frac{1}{I_m} \begin{bmatrix} I_d & I_q \\ -\Omega_p I_d + \Omega_s I_q & -\Omega_s I_d - \Omega_p I_q \end{bmatrix} \tag{4.19}$$

Since $rank(\boldsymbol{O})$ is two, the system (4.18) is observable.

The Luenberger-typed state observer to estimate i_d and i_q is expressed by (4.20):

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} = & \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\boldsymbol{u} + \mathcal{L}\left(i_m - \hat{i}_m\right) \\ \hat{i}_m = & \boldsymbol{C}\hat{\boldsymbol{x}} + \boldsymbol{D}\boldsymbol{u} \end{cases} \tag{4.20}$$

where $\mathcal{L}$ is the observer gain matrix, $\mathcal{L} = \begin{bmatrix} l_1 & l_2 \end{bmatrix}^T$; the symbol ˆ above quantities denotes that they are the estimated ones.

Subtracting (4.20) from (4.18), the observer error $\tilde{\boldsymbol{x}}$, $\tilde{\boldsymbol{x}} = \boldsymbol{x} - \hat{\boldsymbol{x}}$, is expressed by:

$$\dot{\tilde{\boldsymbol{x}}} = (\boldsymbol{A} - \mathcal{L}\boldsymbol{C})\tilde{\boldsymbol{x}} \tag{4.21}$$

By assigning values for l_1 and l_2 to make the real part of all eigenvalues of the characteristic matrix $(\boldsymbol{A} - \mathcal{L}\boldsymbol{C})$ negative, the estimation error will vanish in a limited time. According to Ackerman [71], those eigenvalues should be at least two to six times greater than system poles. After selecting the appropriate positions, the pole placement method can be utilized to place the eigenvalues. Consequently, l_1 and l_2 are calculated without difficulty.

4.3 Experiment results

4.3.1 System description

The laboratory-scaled experiment system illustrated in Fig. 4.4 is almost the same as Fig. 2.10 except for the current sensor. In Chapter 2, the control algorithm was based on the terminal current, thus, a Hall-effect current transducer was employed to sense such the DC current. The control strategy proposed in this chapter also
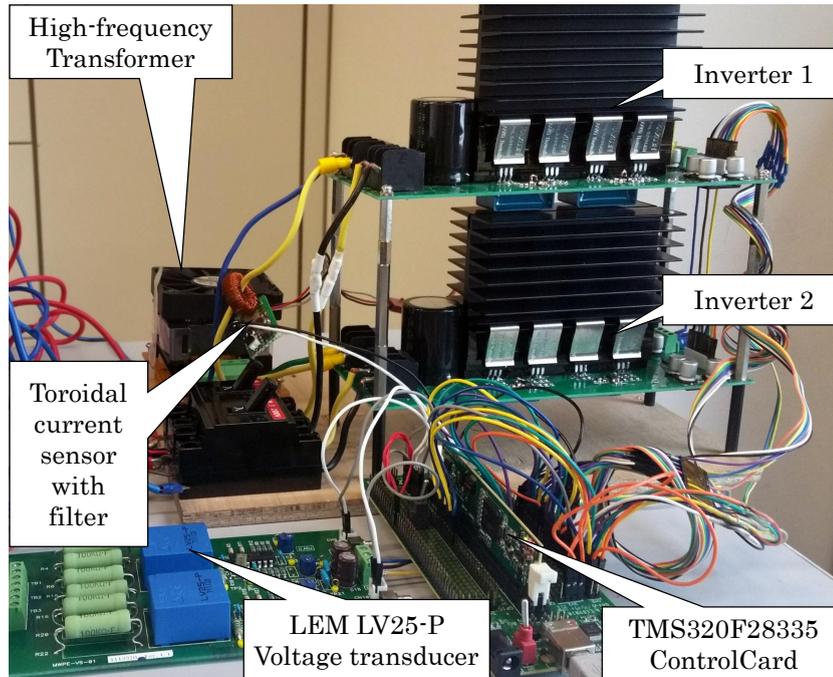
Figure 4.4. Experiment system to verify the observer.

based on a DC signal, however, derived from the AC transferred current which is measured by a low-cost toroidal ferrite core. The crossover frequency of the LC filter used in the measurement circuit is 5 kHz, which is one-tenth of the nominal switching frequency.

Parameters of the experiment system were listed in the Table. 4.1. All the observer as well as the whole control system are implemented in the TMS320F28335 control card. The sampling frequency is still 50 kHz (i.e. the sampling time is $T_z = 20\ \mu s$). The nominal operating point is chosen at $F_x = 1.0$, $\psi = 25$ degrees and $V_1 = 57.5$ V and $V_2 = 50$ V (i.e. $M = 1.15$). The eigenvalues of the observer are placed at two

TABLE 4.1: Additional parameters of DAB converter.

Parameter	Symbol	Value	Unit/Note
Transformer ratio	n	1:1	
Toroidal core		R20/10/7	EPCOS
Number of turns	N_t	100	turns
Sampling frequency	F_{sample}	50	kHz
Nominal switching frequency	F_s	50	kHz
Nominal phase shift	ψ	25	degrees
Nominal voltage ratio	M	1.15	

times of system poles. After discretized, the observer gain is:

$$\mathcal{L} = \begin{bmatrix} 1.5343 \\ -0.0386 \end{bmatrix}$$

An open-loop test is then conducted to verify the validity of the observer. The test is repeated in some cases of voltage ratio and switching frequency. The voltage at port 1 is kept constant at 57.5 V, while that of port 2 varies from 42.5 V to 72 V to obtain various voltage ratios. The nominal voltage ratio used for linearization is $M = 1.15$ (i.e. $V_2 = 50$ V). Accordingly, the minimum voltage ratio of 0.8 (equivalent to +25% overshoot) and the maximum ratio of 1.35 (i.e. -25%) are investigated. Under each condition, ψ is increased gradually with the step of 5 degrees from the boundary of ZVS area until reaching the maximum power. At each step, the observer output $\hat{i}_m$ is recorded and compared to the measured one to confirm the validity of the observer.

Furthermore, the observer states, $\hat{i}_d$ and $\hat{i}_q$ are also stored for comparison with the estimated values which are determined from experiment as follows:

- A current clamp, HIOKI CT9694, is employed to measured the instantaneous AC current, then the Fast Fourier Transform (FFT) function of the digital oscilloscope is applied to detect the peak value of the fundamental current element, I_m.

- The actual load angle ϕ is detected by converting the time difference between the zero crossing points of current and the primary voltage into degrees scale.

- From the peak current and the displacement angle, I_d and I_q can be calculated by: $I_d = I_m \cos\phi$ and $I_q = I_m \sin\phi$.

From $\hat{i}_d$ and $\hat{i}_q$, the observed load angle is then calculated by: $\hat{\phi} = \arctan\dfrac{\hat{i}_q}{\hat{i}_d}$, and compared to the actual one to confirm the validity of load angle detected by the proposed method.

4.3.2 Observer performance

The error characteristic in estimating the peak value of the fundamental current is illustrated in Fig. 4.5. The observer error is defined by subtracting the observed value from the the actual one. In each case of the voltage ratio, it is sketched with respect to the switching frequency and the transmission power.

The error vanishes at the linearization point as expected (Fig. 4.5(c)). At the nominal voltage ratio $M = 1.15$, the error is from -0.5 A to about 0.25 A. As the maximum recorded peak current I_m is about 20 A (when $M = 1.35$, $F_x = 0.5$ and $\psi = 20$ degrees), that error takes only up-to-2.5% of the whole current scale. When the voltage ratio changes, the error also varies slightly and quite symmetrically among different voltage conditions. Nevertheless, the biggest error (Fig. 4.5(f)) does not exceed 1 A. That means, the observer error is less than 5% in all investigated cases.

The variation of the error is stronger upon the changes of switching frequency and phase shift. That is comprehensible since the observer is designed by linearization around one point. Away from that point, the performance will certainly be downgraded. The performance downgrade can also come from another reason.

For example, when $M = 1$ (Fig. 4.5(d)), the error rises from about -0.2 A to 0.5 A when transmitting from 100 W to 260 W at 100 kHz. When doing the same transmission at a lower frequency, the error variation is smaller. The reason is that the sampling frequency is fixed at 50 kHz. If the switching frequency is greater than that, the resolution of the feedback signal is low leading to the performance quality of the observer. On the other hand, when the switching frequency is smaller than 50 kHz, the collected information has relatively better in resolution; and the quality of the observer becomes more stable and less depending on the transmission power.

For that reason, in order to avoid high observer error, the maximum switching frequency is limited to 100 kHz (less than 150 kHz of the previous chapters). The performance can also be improved by increasing the sampling frequency. However,

(a) $M = 1.35$.

(b) $M = 1.25$.

(c) $M = 1.15$.

(d) $M = 1.0$.

(e) $M = 0.9$.

(f) $M = 0.8$.
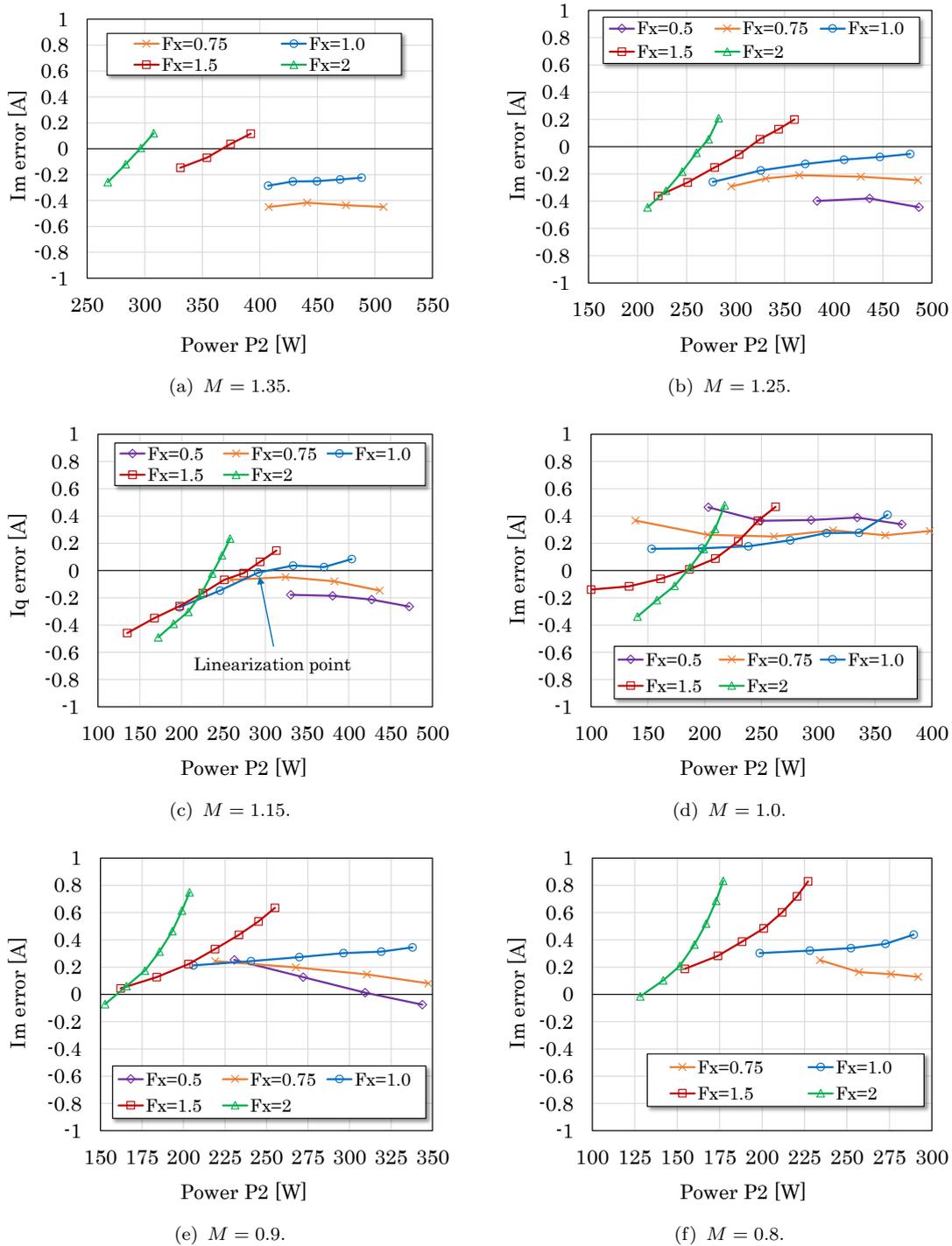
Figure 4.5. Observer error in term of I_m.

it is a challenge. As that frequency is 50 kHz, there is only 20 µs for processing ADC, observer, control system, PWM, etc. By better organizing the program, the processing time can be reduced a little bit but not too much. For further reduction, some functions should be implemented in an external FPGA or DSP.

4.3.3 Direct current error

The error Δi_d between the actual direct current i_d and the observed one $\hat{i}_d$ is shown in Fig. 4.6 for six different cases of voltage ratio. It can be seen from the

(a) $M = 1.35$.

(b) $M = 1.25$.

(c) $M = 1.15$.

(d) $M = 1.0$.

(e) $M = 0.9$.

(f) $M = 0.8$.
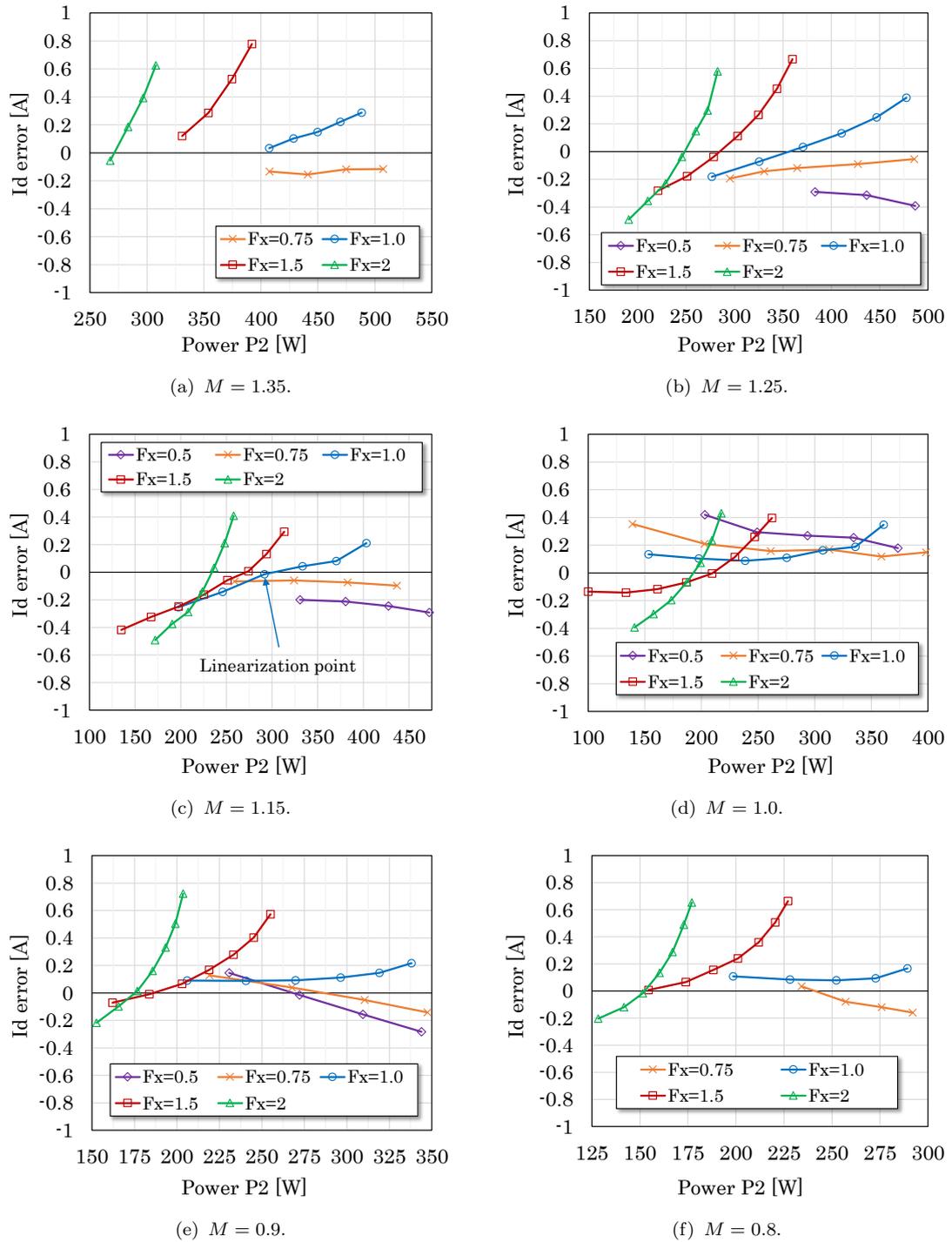
Figure 4.6. Observer error in term of I_d.

figures that the variation of Δi_d with respect to M, F_x and ψ are very similar to that of i_m error which analyzed above.

The error also vanishes at the linearization point. Among all cases, it does not exceed 0.8 A (Fig. 4.6(a)). As for the direct current, the maximum i_d recorded in experiment is about 16 A. Hence, that error is equivalent to about 5%. This point is important because, as claimed before, i_d should be used to handle the active component P_1, which is the real transmission power. The more accuracy in estimating i_d, the more precise in handling P_1, and 5% tolerance is acceptable for such purpose.

Notes that, at the nominal voltage ratio, $M = 1.15$, the tolerance is even lower at 3.13% as the maximum error is about 0.5 A when the switching frequency is 100 kHz (Fig. 4.6(c)). This allows a good regulation as the steady state error of the current loop is less than 5% at any transmission power.

4.3.4 Quadrature current error

Fig. 4.7 demonstrates the error between the actual quadrature current i_q and the estimated value $\hat{i}_q$ with respect to M, F_x and ψ. Unlikes the error characteristics of either i_m or i_d, the quadrature current error is relatively higher.

The error almost disappears at the linearization point, and remains low (from -0.3 A to 0.1 A) through the whole power range when the voltage ratio is at nominal (Fig. 4.7(c)). As the maximum actual quadrature current is about 8 A, the error in percentage is from -3.75% to +1.25% of the scale. The variation of the error with respect to the switching frequency and the phase shift is similar to that of i_m as explained. However, when M varies, the error increases significantly.

For example, when the voltage variation is +13% (Fig. 4.7(d)), the maximum error grows to approximately 0.9 A which is 11.25% of the whole scale. As the fluctuation is +25% (Fig. 4.7(f)), it rises to about 1.3 A (16.25%). Actually, the absolute values of the i_q error is just slightly bigger than that of i_d error of i_m error. However, the smaller scale of i_q makes it seem more sensitive.

(a) $M = 1.35$.

(b) $M = 1.25$.

(c) $M = 1.15$.

(d) $M = 1.0$.

(e) $M = 0.9$.

(f) $M = 0.8$.
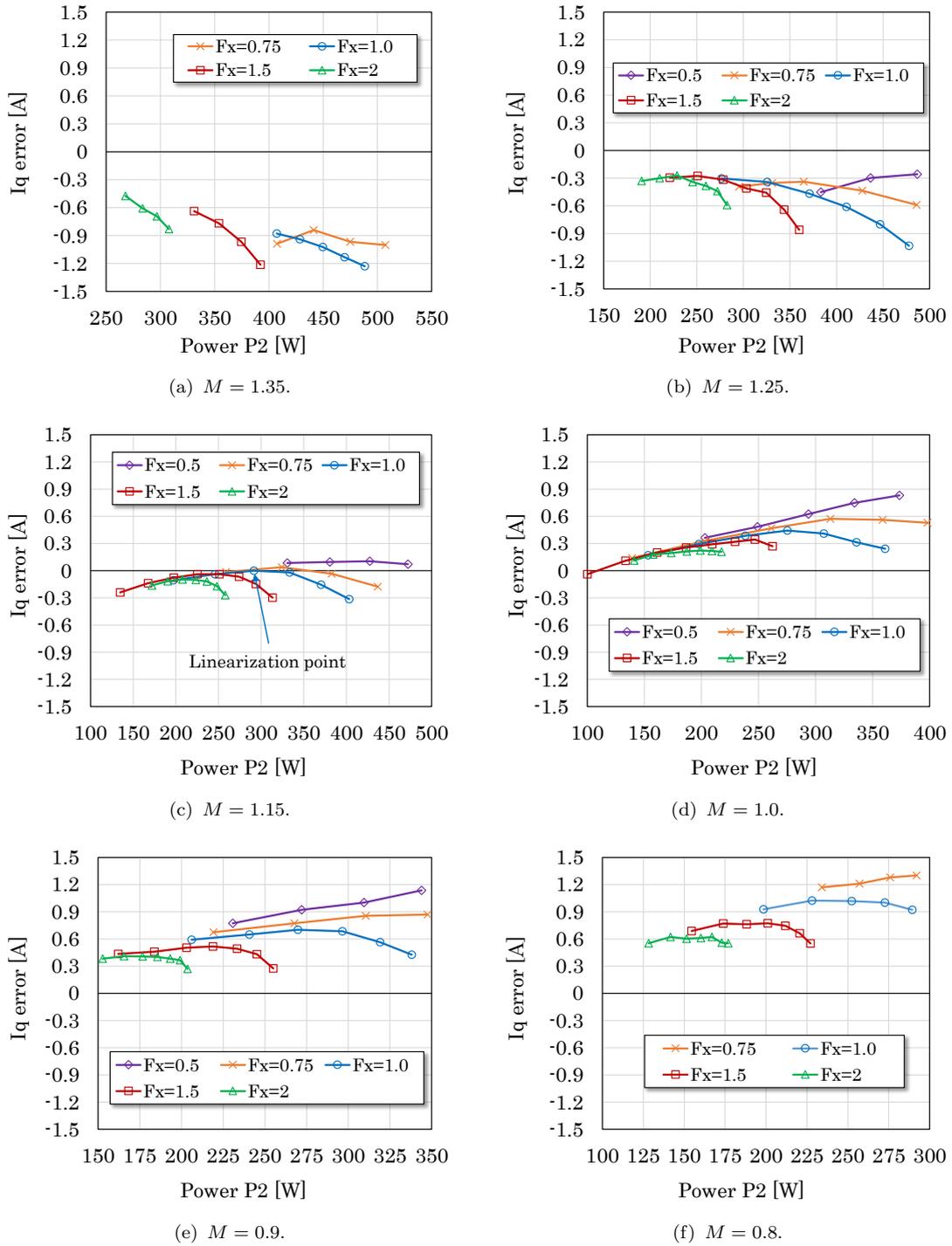
Figure 4.7. Observer error in term of I_q.

Notes that, i_q is proportional to the reactive power Q_1, or in other words, the circulating power. Its value also implies the load angle as defined by (4.9). Therefore, the error in i_q is created not only by the aforementioned reasons (low sampling

frequency, linearization), but also by the distorted and asymmetrical current wave-
form when the voltage ratio and the phase shift change. In order to comprehend
this matter more clearly, let us consider the error in the estimated load angle.

4.3.5 Load angle error

This comparison examines the error between the *"actual"* load angle and the
observed one. The *"actual"* load angle determined in experiment is approximated
by the phase different between the primary voltage and current. Although that
kind of load angle is the optimization target as discussed in Chapter 2, it does not
match exactly with the phase difference between the fundamental components.
Fig. 4.8 demonstrates the drift of the phase due to the distortion by simulation.
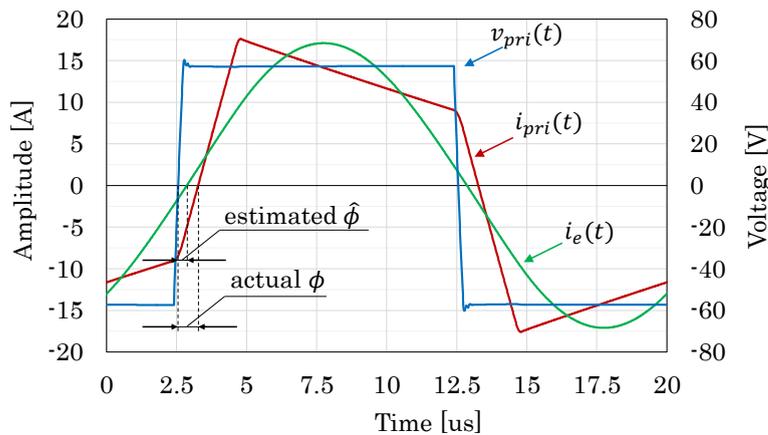
(a) $M = 0.90$.
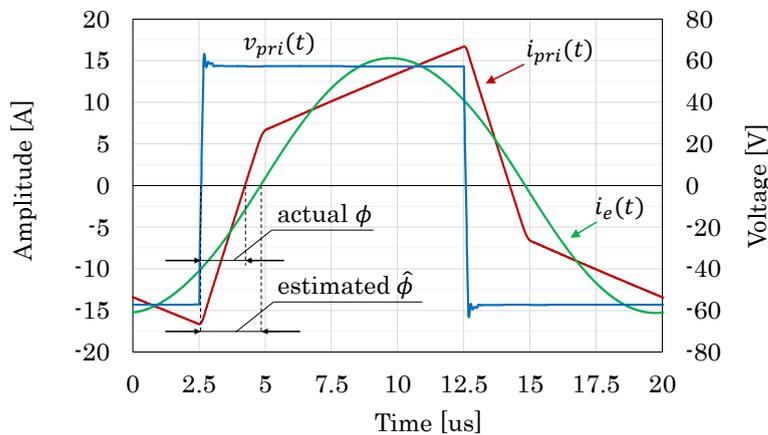
(b) $M = 1.35$.

Figure 4.8. Effect of the current distortion on observer performance.

In both cases, the switching frequency is 50 kHz and the phase shift is 45 degrees. When the conversion ratio is 0.9, the voltage of the sender is smaller than the receiver. As seen in Fig. 4.8(a), the fundamental current appears to be drifted backward making the estimated load angle smaller than the expected one. Contrarily, when transmitting power from the higher voltage port to the lower voltage port as shown in Fig.4.8(b) for the case of $M = 1.35$, the fundamental current is drifted forward. Consequently, the estimated result is greater than desired.

That effect is reflected very well by experiment. Fig. 4.9 describes the error characteristic between the observed and the measured load angles. Because the observer is designed upon one point by linearization, the error vanishes at that point. When the transmission power change by varying switching frequency and phase shift under the nominal voltage ratio, the error varies is from -5 ($F_x = 2$) to 1.5 ($F_x = 0.5$) degrees (Fig. 4.9(c)). At its corresponding frequency, that error is equivalent to -140 ns and $+170$ ns, respectively, which is very small compared to one switching cycle.

The drifting effect becomes more obvious when voltage ratio M changes. As M increases (Fig. 4.9(a) and Fig. 4.9(b)), the error characteristics seems to move downward implying that, the estimated load angle is greater than the measured one. On the other hand, when M gets smaller (Fig. 4.9(d), Fig. 4.9(e) and Fig. 4.9(f)), the curves appear to move upward showing that the observed load angle is less than the measured value.

The maximum load angle error recorded in all investigated cases is about 13 degrees when $M = 0.8$ (+25% voltage overshoot) and $F_x = 0.75$ (Fig. 4.9(f)). At such the frequency, that error is equivalent to approximately 1 μs (3.75% of one switching cycle). Although it is very small compared to the switching cycle, it is two times bigger than the dead-time (which is the desired load angle as discussed in Chapter 2). This, of course, will affect the effort to achieve soft-switching in the transient state as well as the endeavor to optimize the system loss by modulation.

Notes that, the error is insignificant when the voltage ratio is at its nominal. Therefore, if the voltage fluctuation can be kept within 10% (M varies from 0.9 to

(a) $M = 1.35$.

(b) $M = 1.25$.

(c) $M = 1.15$.

(d) $M = 1.0$.

(e) $M = 0.9$.

(f) $M = 0.8$.
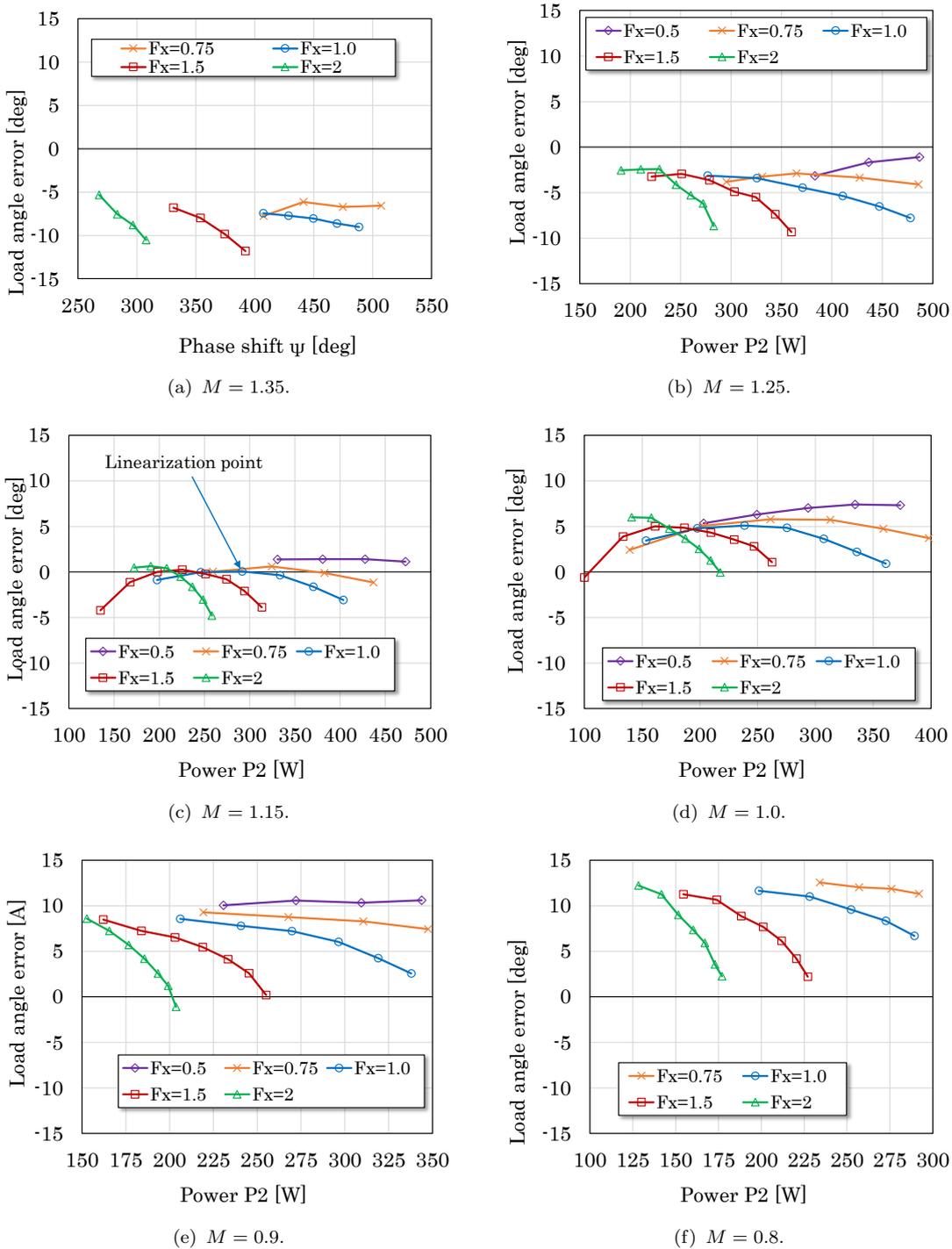
Figure 4.9. Observer error in term of ϕ.

1.35), the error variation will be in the order of ± 9 degrees (from -270 ns to +700 ns at its corresponding frequency). Besides, increasing the sampling frequency is another consideration to reduce the load angle error as explained above.

Another option to improve the observer performance is to employ nonlinear observer as reported in [P.6]. However, it might not eliminate the issue of phase drifting because of current distortion. Compensation for the drift requires further study which is beyond the scope of this dissertation. In the next chapter, an observer-based control system is developed which target is to kept the voltage fluctuation when load changes as low as possible to reduce the error due to distortion.

4.4 Conclusion

In this chapter a linear observer was designed to estimate the direct and the quadrature components of the transmission current. Based on the estimated values, active and reactive powers can be handled directly. Follows are some main point of this chapter:

- The observer used the transfered AC current as the input signal instead of the terminal DC current. The transfered current can be measure easily by using a low-cost toroidal ferrite core. Obviously, the proposed control system is more economical than the others.

- Although using an AC signal for feedback, it was then transformed into a DC signal. Therefore, the sampling frequency was not necessary to be high. Therefore, it is possible to implement the whole control system in the mid-range DSP platforms, such as C2000 series from TI.

- The observer can predict the system state well in the vicinity of the nominal operating point. Away from such point, the accuracy was downgraded as the load angle error was about 13 degrees or 3.75% of a sampling period. As discussed, there are several options to improve the observation performance. They will be the scope of the future study.

- The accuracy of the fundamental harmonic approximation method depends strongly on the voltage ratio and the phase shift angle (on the current waveform) strongly. When the current is asymmetrical, the fundamental current is drifted forward or backward from the original signal. Phase drift compensation should be considered for better prediction of system states.

Chapter 5

Observer-based control system

In Chapter 4, an observer was designed to estimate the direct and the quadrature components of the transferred current. As discussed, the direct current is proportional to the active power, while the quadrature one is proportional to the reactive power. By regulating both current components, the not only transmission power can be handled, the load angle, which implies the circulating current, can also be managed.

This chapter develops a control system based on the estimated data from the designed observer to accomplish the above objectives. Accordingly, the control system consists of three loops: two inner loops are reserved for regulating two current components and one outer loop for adjusting the voltage at terminal 2. The diagram of the control system is depicted in Fig. 5.1.

Figure 5.1. Control system diagram.

5.1 Input-output pairing

Consider the model (5.1) which outputs $\hat{i}_d$ and $\hat{i}_q$:

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} = & \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{y} = & \boldsymbol{C}'\hat{\boldsymbol{x}} + \boldsymbol{D}'\boldsymbol{u} \end{cases} \tag{5.1}$$

where $\hat{\boldsymbol{x}} = \begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix}$, $\boldsymbol{u} = \begin{bmatrix} f_x \\ \psi \end{bmatrix}$, $\boldsymbol{A} = \begin{bmatrix} -\Omega_p & -\Omega_s \\ \Omega_s & -\Omega_p \end{bmatrix}$, $\boldsymbol{B} = \begin{bmatrix} -\Omega_s I_q & \dfrac{4n}{\pi L_s} V_2 \sin\psi \\ \Omega_s I_d & -\dfrac{4n}{\pi L_s} V_2 \cos\psi \end{bmatrix}$,

$\boldsymbol{C}' = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ and $\boldsymbol{D}' = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$.

The model (5.1) is represented in form of a set of transfer functions from inputs to outputs as:

$$\boldsymbol{\Gamma}(s) = \frac{\boldsymbol{Y}(s)}{\boldsymbol{U}(s)} = \boldsymbol{C}'\left(s\boldsymbol{I} - \boldsymbol{A}\right)^{-1}\boldsymbol{B} + \boldsymbol{D}' \tag{5.2}$$

where s is the *Laplace* operator.

Considering the DAB converter with parameters listed in Table 2.1 operating at the nominal point described in Table 4.1, the relative gain array [71] of the system (5.2) is:

$$\boldsymbol{\Lambda} = \boldsymbol{\Gamma}(0) \times \left(\boldsymbol{\Gamma}(0)^{-1}\right)^{T} = \begin{bmatrix} 1.8459 & -0.8459 \\ -0.8459 & 1.8459 \end{bmatrix} \tag{5.3}$$

Since $\boldsymbol{\Lambda}(1,1) = \boldsymbol{\Lambda}(2,2) = 1.8459$, the control action from f_x to i_d and ψ to i_q can be stabilized. Therefore, the pairing strategy is as follows: the normalized frequency f_x is manipulated to regulate i_d, at the same time, the phase shift ψ is used to regulate i_q.

5.2 Decoupler

In order to reduce the interaction between $i_d(t)$ and $i_q(t)$, a decoupled network is designed. Let us split $\boldsymbol{\Gamma}(s)$ into two parts:

$$\boldsymbol{\Gamma} = \tilde{\boldsymbol{\Gamma}}\boldsymbol{\Gamma}_{diag} \tag{5.4}$$

where $\boldsymbol{\Gamma}_{diag}$ is diagonal matrix of $\boldsymbol{\Gamma}(s)$:

$$\boldsymbol{\Gamma}_{diag}(s) = \begin{bmatrix} \Gamma_{11}(s) & 0 \\ 0 & \Gamma_{22}(s) \end{bmatrix}$$

and $\tilde{\boldsymbol{\Gamma}} = \boldsymbol{\Gamma}(\boldsymbol{\Gamma}_{diag})^{-1}$.

By using static matrix $\boldsymbol{W}$, defined by:

$$\boldsymbol{W} = (\tilde{\boldsymbol{\Gamma}})^{-1} = (\boldsymbol{\Gamma}(\boldsymbol{0}))^{-1}\boldsymbol{\Gamma}_{diag}(0), \tag{5.5}$$

the interaction between $i_d(t)$ and $i_q(t)$ at the steady state will be eliminated. Substituting parameters in Table 2.1 and Table 4.1 into (5.5), we have:

$$\boldsymbol{W} = \begin{bmatrix} 1.9547 & 1.5622 \\ 1.1946 & 1.9547 \end{bmatrix}$$

5.3 Current controllers

As the interaction is reduced, two current controllers, $G_{cid}(s)$ and $G_{ciq}(s)$, can be designed individually for two control channels, where $\Gamma_{11}(s)$ and $\Gamma_{22}(s)$ are the transfer functions, respectively. The diagram of each loop is described in Fig. 5.2. Assumes that, in one sampling cycle, the voltage variation is ignorable that the current controller can be designed independently from the voltage loop.

The sampling frequency of current loops is fixed at 50 kHz, therefore, the Zero-Order-Hold blocks in Fig. 3.2 are also the same as described in (3.7). The low pass filters are also configured with the crossover frequency of one-tenth the sampling

(a) Control loop for $\hat{i}_d$.
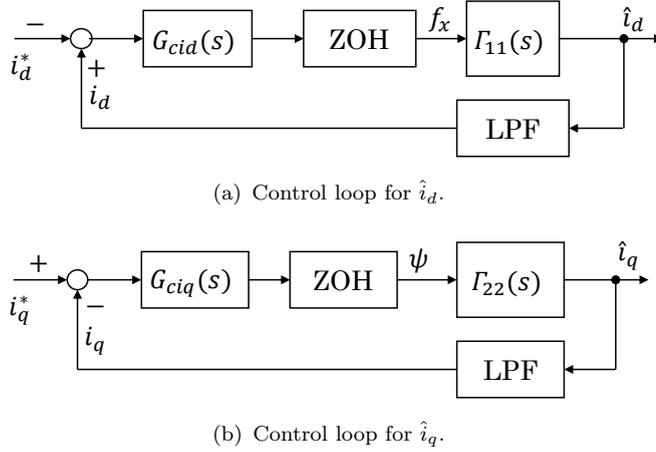

(b) Control loop for $\hat{i}_q$.

Figure 5.2. Current loop diagram.

frequency as (3.8). The plants of two current, thereby, can be derived as:

$$G_{f_x i_d}(s) = G_{ZOH}(s)\Gamma_{11}(s)G_{LPF}(s) \tag{5.6}$$

$$G_{\psi i_q}(s) = G_{ZOH}(s)\Gamma_{22}(s)G_{LPF}(s) \tag{5.7}$$

In order to compare the performance of the observer-based control system in this chapter to which designed in Chapter 3, the same design manner, same criteria as used in Chapter 3 are employed:

- crossover frequency of open loop systems is chosen at 2.5 kHz (10 percent of the minimum switching frequency), and

- phase margin is 75 degrees for ensuring high robustness

Thereby, the two current controller ares:

$$G_{cid}(s) = \frac{6080}{s} \times \frac{s + 6419}{s + 3.84e4} \tag{5.8}$$

$$G_{ciq}(s) = \frac{7325}{s} \times \frac{s + 5774}{s + 4.27e4} \tag{5.9}$$

The Bode diagram of the open loop system is illustrated in Fig. 5.3. The blue curve represents the characteristics of the plant itself, while the red curve describes the open loop response. With the designed controllers, the phase margin of the open
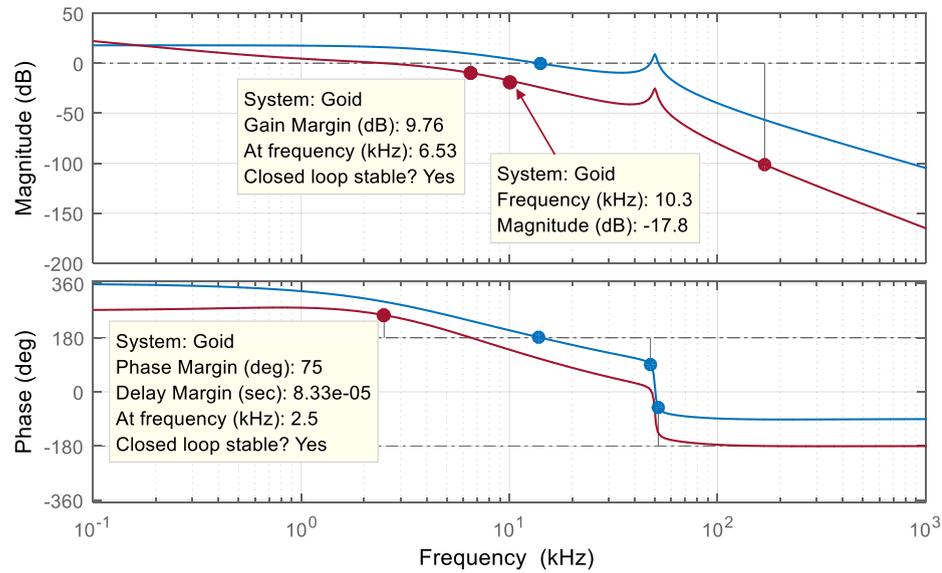
(a) Control loop for $\hat{i}_d$.
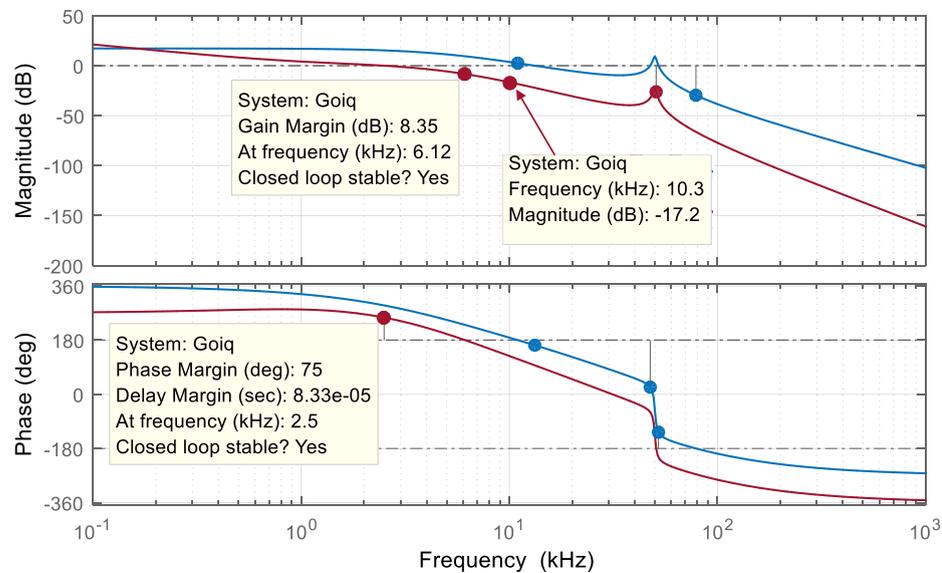
(b) Control loop for $\hat{i}_q$.

Figure 5.3. Bode diagram of the open current loop.

loop are 75 degrees at 2.5 kHz as desired. The gain margin is about 9 dB at 6 kHz and more than 17 dB at 10.3 kHz. It means that the controllers can suppress the noise which frequency higher than 10 kHz about 7.2 times in amplitudes, that is a slightly improvement compared to the robustness of the controller in Chapter 3.

5.4 Voltage controller

As mentioned in the last chapter, the transfer function from the terminal 2 current to the terminal 2 voltage is (3.12):

$$G_{vi_2}(s) = \frac{v_2(s)}{i_{2,avg}(s)} = \frac{R_{Load}}{1 + s(R_{Load} + r_c)C_2}$$

Neglecting the loss in the transmission, we have $P_1 \approx P_2$. Hence, from (4.6), the average terminal 2 current can be approximated by:

$$i_{2,avg}(t) \approx \frac{2v_1(t)}{\pi v_2(t)} i_d(t) \tag{5.10}$$

From (3.12) and (5.10), the transfer function from $i_d(s)$ to $v_2(s)$ is:

$$G_{vi_d}(s) = \frac{v_2(s)}{i_d(s)} = \zeta \times \frac{R_{Load}}{1 + s(R_{Load} + r_c)C_2} \tag{5.11}$$

where $\zeta = \frac{2V_1}{\pi V_2}$.

The diagram of the voltage control loop is described in Fig. 5.4. For comparison purpose, the control system is designed with all stability criteria similar to that reported in Chapter 3. Both the sampling frequency and the crossover frequency of the low pass filter are chosen the same at 500 Hz. The crossover frequency of the voltage loop is also 35 Hz and the phase margin is set to 75 degrees as in in Chapter 3.
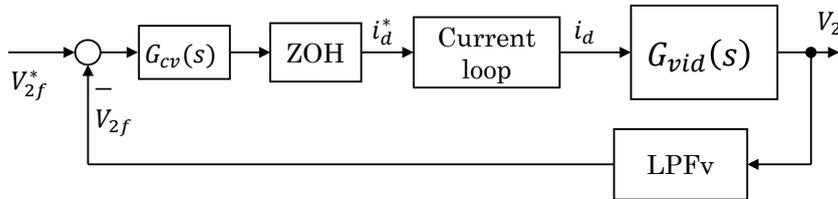

Figure 5.4. Voltage loop diagram.

The PI-modified typed II voltage controller can thus be designed as:

$$G_{cv}(s) = \frac{4200}{s} \times \frac{s + 16}{s + 3000} \tag{5.12}$$
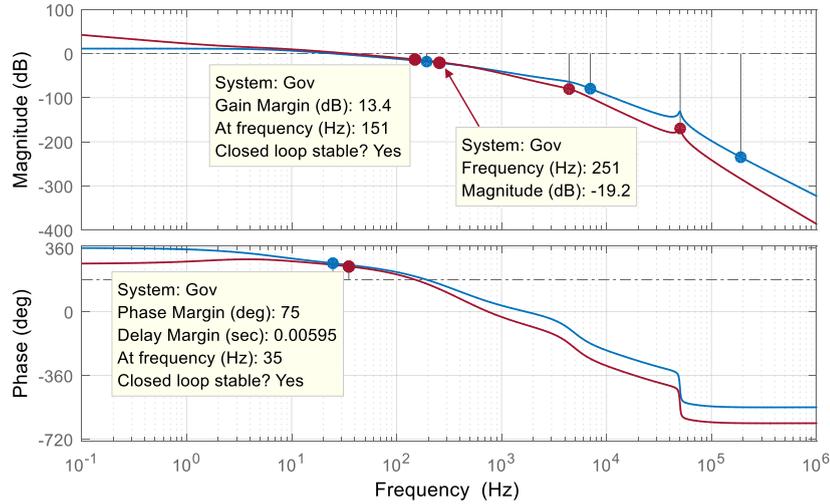
$$\tag{5.13}$$

Figure 5.5. Bode diagram of the open voltage loop.

Fig. 5.5 expresses the Bode diagram of the open voltage loop and the plant as the red and blue curves, respectively. At the crossover frequency of 35 Hz, the phase margin is 75 degrees as expected. The gain margin is 13.4 dB at the frequency of 150 Hz, thus all third order harmonics will be suppressed by 5 times. At 250 Hz, the fifth order harmonics is blocked about 90% by the effect of the controller as the gain margin is 19.2 dB. This, however, slightly less than 21.4 of the voltage controller designed in Chapter 3. Nevertheless, that suppression effect is enough to eliminate almost of the noise reflected from the AC side.

5.5 Generation of I_q^*

As discussed in the Chapter 2, the displacement angle ϕ_1 should satisfy the condition (2.9) to maintain ZVS and to keep the conduction loss small:

$$\phi_1 \geq \Phi_{min} = \max\left\{\theta_d, \ \frac{1}{nM^2}\theta_d + \left(1 - \frac{1}{M}\right)\frac{\pi}{2}\right\} \qquad (\text{with } \theta_d = F_x\Omega_s T_d)$$

Accordingly, the MFPS modulation strategy was proposed intending to regulate the load angle ϕ_1 around Φ_{min}. This intention can also be undertaken by using the control system in this chapter to regulate the quadrature current $i_q(t)$ around a suitable reference.

From (4.6) and (4.9), the quadrature reference current when $\phi_1 = \lambda\Phi_{min}$ is represented by:

$$i_q^*(t) = i_d^*(t)\tan(\lambda\Phi_{min}) \tag{5.14}$$

where λ was defined in the last chapter as the coefficient to handle the Depth of ZVS.

At 50 kHz, Φ_{min} is 9 degrees. If λ is 1 and F_x varies within [0.5; 2], the approximation (5.15) can be utilized to avoid trigonometric function calculation.

$$i_q^*(t) \approx \lambda\Phi_{min}i_d^*(t) \tag{5.15}$$

Equation (5.14) can be utilized to generate commands for the quadrature current loop. However, when the frequency is saturated at its limitation, the phase shift becomes the only control variable. Thus, a modification function was proposed in Chapter 2 to compensate the variation of the frequency into phase shift. Here, the compensation is carried out in a different manner. Fig. 5.6 describes the diagram of the whole voltage loop with the reference calculator for i_q indicated inside the dashed rectangle.

As seen in Fig. 5.6, since both $i_d(t)$ and and $i_q(t)$ are components of the transferred current, they should have the same dynamics. Therefore, same voltage controller $G_{cv}(s)$ is applied for generating $i_q^*(t)$. In order to satisfy (2.9), voltage ratio and switching frequency are feed-forward to derive the minimum load angle Φ_{min}. Two
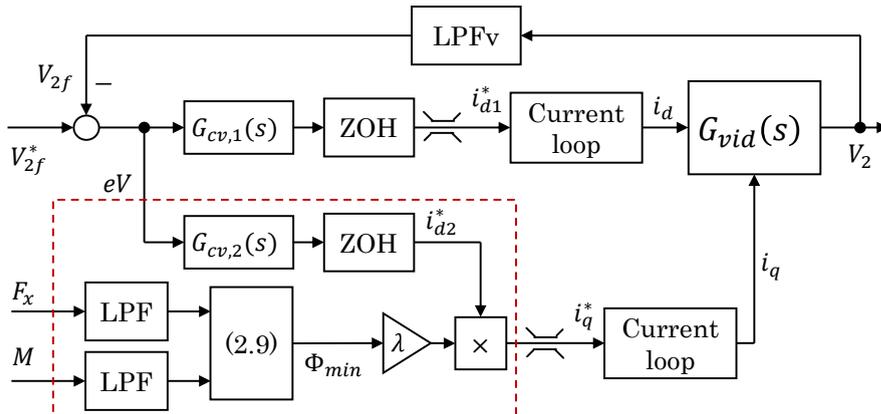

Figure 5.6. Reference calculator.

low-pass filters with bandwidth equal to that of the voltage controller $G_{cv}(s)$ are employed for smoothing the two feed-forward signals. Multiplying them with taking into account the Depth of ZVS coefficient λ results in the optimal reference for the quadrature current loop.

In the normal operation (i.e. F_x is not saturated), two same voltage controller should yield same output $i_{d,1}^* = i_{d,2}^* = i_d^*$, thus i_q^* is calculated by (5.15). When F_x reaches its limitation but V_{2f} does not meet its reference, the voltage error is other than zero causing $i_{d,1}^*$ and $i_{d,2}^*$ continue to increase (or decrease) due to the integral effect of the voltage controllers. As $i_{d,1}^*$ is saturated, $i_{d,2}^*$ keeps on changing making i_q^* independent from i_d^*.

5.6 Experiment results

All experiments in this chapter are implemented in the same system depicted in Fig. 4.4. All setting are the same as reported in Chapter 3. The limitation of the control variables are listed in Table 5.1. As claimed in the last Chapter, $F_{x,max}$ is set to 2 to limit the observation error. The maximum direct current $i_{d,max}$ is 16 A because the maximum current rating of the power supply at Terminal 1 is only 10 A (according to (4.6), $I_d \approx \dfrac{\pi}{2}I_1$). The maximum quadrature current $i_{q,max}$ is 7 A for the load angle of about 23.6 degrees in the transient state. This will ensure the margin of about 3 times for ZVS when $F_x = F_{x,min}$.

TABLE 5.1: Parameters of the observer-based control system.

Parameters	Value	Unit
$i_{d,max}$	16	A
$i_{d,min}$	0	A
$i_{q,max}$	7	A
$i_{q,min}$	0	A
$F_{x,max}$	2	A
$F_{x,min}$	0.5	A
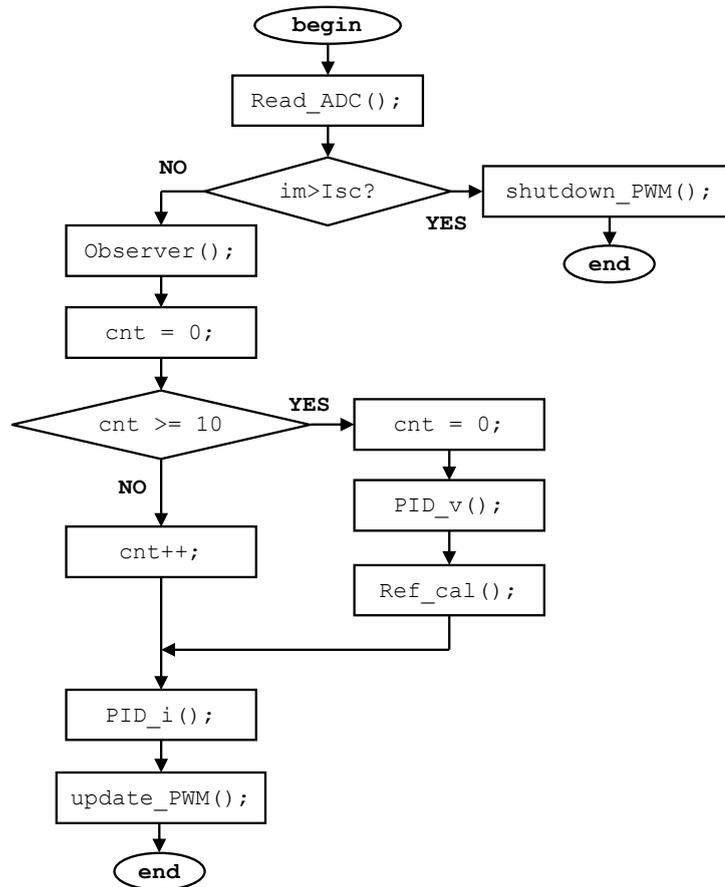
Figure 5.7. Flow chart of the whole control system.

The diagram of the control system is described in Fig. 5.7. Firstly, ADC module of the TMS320F28335 DSP reads the average rectified transfer current and the terminal 2 voltage. If the obtained current is exceed the protection threshold, the flow proceeds to shutdown all PWM signals. Otherwise, the observer procedures are executed. After that, PID functions of the current loops are triggered to calculate the modulation parameters. A counter is employed as a timer to call voltage loop commands after each ten sampling periods. At the end of each counting cycle, the references of current loops are refreshed.

5.6.1   Current loops

Only current control loops are examined in this experiment. Both terminal voltage are kept constant at 60 V and 50 V, respectively by configuring the power supply and the DC electronic load at the constant voltage mode.

5.6.1.1 Step response

The first verification test the step response from 18% to 96% rated load. The result is demonstrated in Fig. 5.8, in which $\hat{i}_d$ and $\hat{i}_q$ are represented by blue and green curves, respectively, whereas the terminal 2 current is sketched as the red curve.
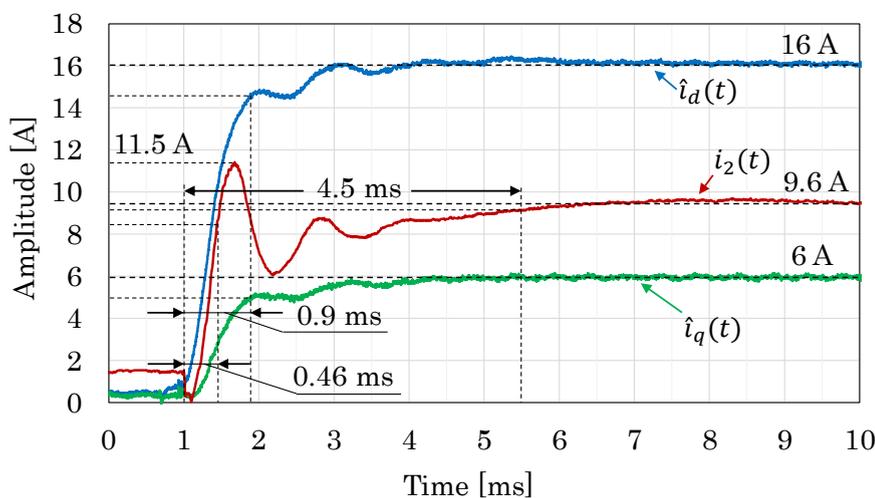
Figure 5.8. Current step response.

At first, both $\hat{i}_d$ and $\hat{i}_q$ are initialized at 0.4 A, accordingly the output power is about 18% which is the minimum controllable power under the testing voltage ratio (Fig. 2.15). At a certain instant, the current commands of both loops suddenly steps up to 16 A and 6 A, respectively. As shown in the figure, both current components are regulated very well at theirs references. There are no fluctuation in the response of the two current component.

As for the terminal current, there is an overshoot of 20% which is much smaller than that of 132% caused by the current controller in Chapter 3. The rising time of the terminal current is 0.46 ms, which is mostly matched with the design parameters as the desired bandwidth is 2.5 kHz. The settling time is almost the same to the previous case as it is about 4.5 ms. The settling time of the two current components are much smaller than that of the terminal current. However, their response time is about 2 times slower, which are the same at 0.9 ms. That is because the dynamic of $i_2(t)$ depends on the load and the output capacitor,

whereas that of $\hat{i}_d$ and $\hat{i}_q$ depend only on the leakage inductance of the transformer and the series resistance of the transmission network. Any mis-determination of such parameters might affect the accuracy of the model.

5.6.1.2   Interaction removal capability

Interaction effect between two control channels is illustrated in Fig. 5.9 and Fig. 5.10. Signals sketched in the figures are obtained by using two PWM pins of the DSP as two DAC channels to convert from the variables to duty cycles then filtering with two low-pass filters. In these experiments, only current loops are examined.

First trial explores the impact of changes in $\hat{i}_d(t)$ on $\hat{i}_q(t)$. At initialization, $\hat{i}_d(t)$ and $\hat{i}_q(t)$ are regulated at 12 A and 6 A, respectively. As shown in Fig. 5.9(a), both current components are handled very well at the desired values. When the reference I_d^* steps up to 16 A, $\hat{i}_d(t)$ starts increasing. After the settling time of about 3 ms, $\hat{i}_d(t)$ becomes stable at exactly 16 A. During the rising time of 1.25 ms, no overshoot or undershoot or oscillation in $\hat{i}_d(t)$ is recorded. In the meantime, there is a -0.8 amps sag in $\hat{i}_q(t)$. As the desired regulation is 6 A, that current sag is about -13% of the steady state value. When suddenly stepping down the reference I_d^* from 16 A back to 12 A (Fig. 5.9(b)), a swell of +0.6 A, in the $\hat{i}_q$ response, which is equivalent to 10% of I_q^*, is recorded. In both cases, as $\hat{i}_d(t)$ reaches to its stable state, $\hat{i}_q(t)$ also restores to its original value.
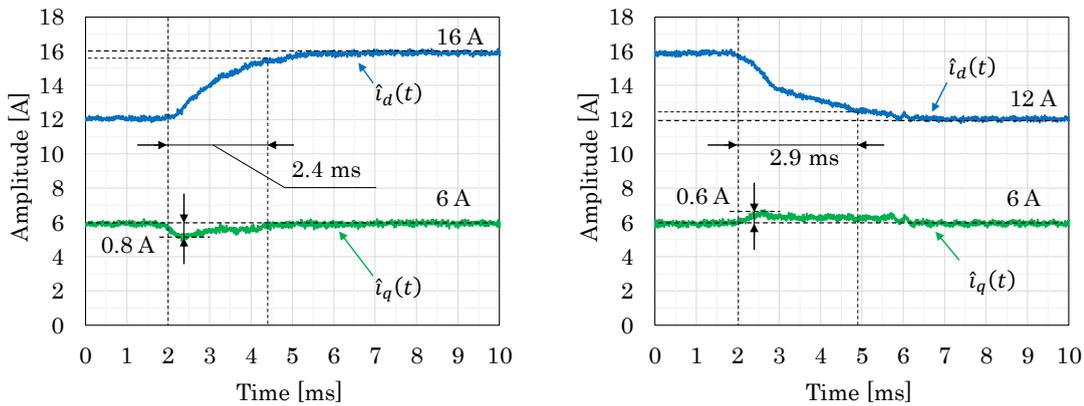
(a) I_d^* steps up from 12 A to 16 A; $I_q^* = 6$ A.   (b) I_d^* steps down from 16 A to 12 A; $I_q^* = 6$ A.
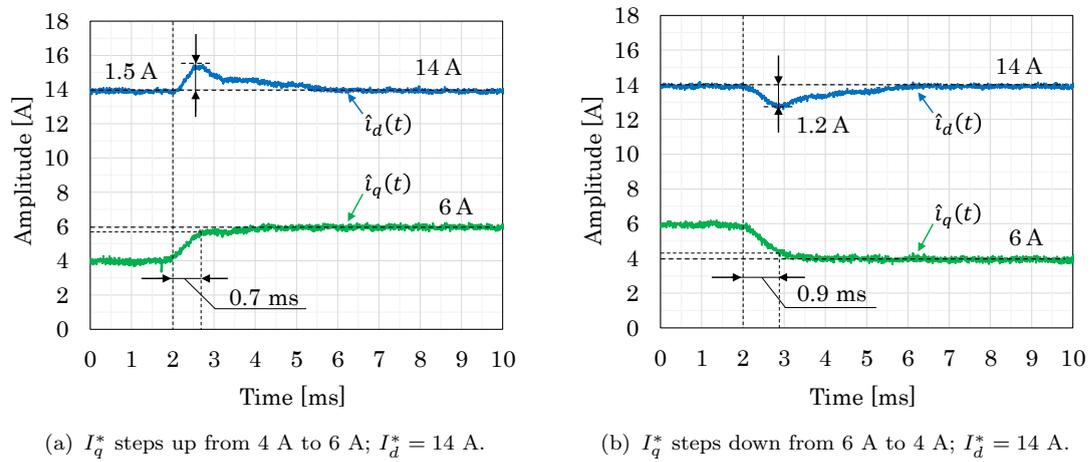
Figure 5.9. Effect of changes in $i_d(t)$ on $i_q(t)$.

(a) I_q^* steps up from 4 A to 6 A; $I_d^* = 14$ A.

(b) I_q^* steps down from 6 A to 4 A; $I_d^* = 14$ A.

Figure 5.10. Effect of changes in $i_q(t)$ on $i_d(t)$.

The changes in $\hat{i}_q(t)$ also cause some fluctuations on $\hat{i}_d(t)$. In the test reported in Fig. 5.10, both components are initialized at 14 A and 6 A, respectively. During the rising time of $\hat{i}_q(t)$ to increase from 4 A to 6 A, an overshoot in $\hat{i}_d(t)$ of 1.5 A is recorded (Fig. 5.10(a)). And when $\hat{i}_q(t)$ falls down from 6 A to 4 A, an undershoot of -1.2 A occurs in $\hat{i}_d(t)$ (Fig. 5.10(b)). Those fluctuation is +10.7% and -8.5% of the preset. When $\hat{i}_q(t)$ settles down at its new values, $\hat{i}_d(t)$ also restores to its original.

As seen, the interaction is not completely eliminated in the transient state. That is because the decoupling technique used here is the static one, which based only on the DC gain of the system model. If dynamic decoupling method is employed, the interaction might be further suppressed.

5.6.2 Voltage loops

5.6.2.1 Start-up

Similar to experiment in Chap 3, start-up tests are conducted to verify the operation of the observer-based control system. There are two cases corresponding to 20% and 100% of the rated load. Results when starting up with 20% load are reported in Fig. 5.11.
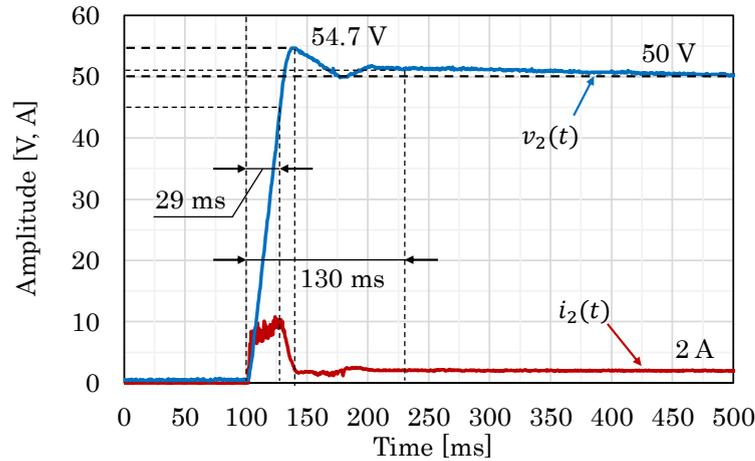
(a) Terminal voltage and current.
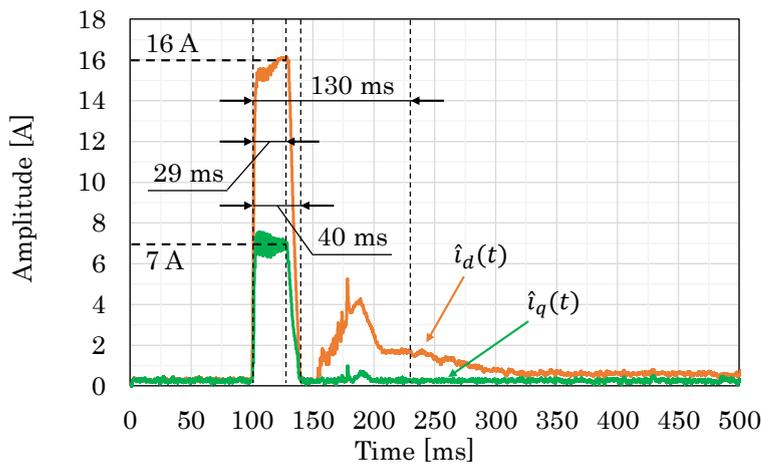
(b) Corresponding $\hat{i}_(d)$ and $\hat{i}_q(t)$.

Figure 5.11. Light load start-up response.

Compares to the small load start-up response in Fig.3.7(b), the voltage response shown in Fig. 5.11(a) is significantly improved. The overshoot is reduced from +18% to +9.4%. The rise time is 29 ms reflecting the desired bandwidth of 35 Hz. The settling time is also slightly shorten from 150 ms to 130 ms. As for $\hat{i}_d(t)$ and $\hat{i}_q(t)$ (Fig. 5.11(b), during the rising time, they are clamped at their maximum values, which are 16 A and 7 A, respectively. This will maintain the load angle in the transient state around 23.6 degrees which is enough to guarantee ZVS in the transient state.

Fig. 5.12 describes system dynamics when stating-up at the rated load. This case, however, have longer rise time and settling time. Unlikes results reported in Fig. 3.7(a), in the transient state shown in Fig. 5.12(a), $i_2(t)$ does not settle down at
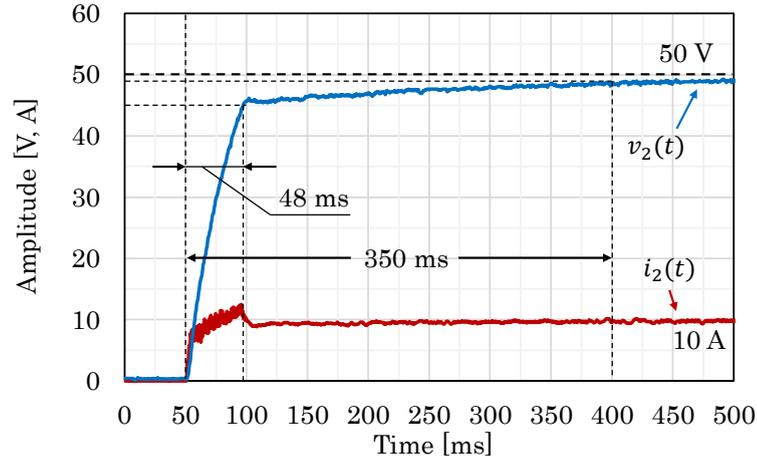
(a) Terminal voltage and current.
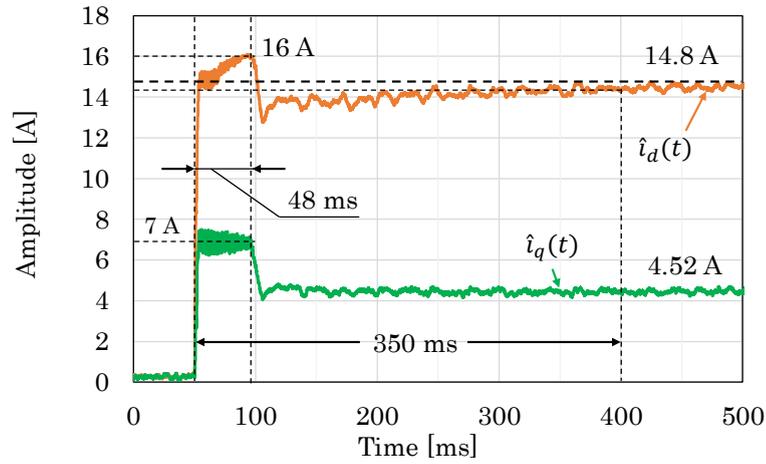
(b) Corresponding $\hat{i}_{(}d)$ and $\hat{i}_q(t)$.

Figure 5.12. Rated load start-up response.

its maximum of 10 amps but increases gradually due to the control behavior of the d-channel controller. Consequently, the rising speed of the terminal voltage is slower. This can be solved with a better designed current controllers. At the steady state, $\hat{i}_d(t)$ and $\hat{i}_q(t)$ are 14.8 A and 4.52 A respectively. That makes the load angle of about 15.8 degrees to ensure ZVS in the steady state.

5.6.2.2 Load change

In this experiment, terminal 1 voltage is set to constant 60 V ($M = 1.2$). At the same time, the DC electronic load operates in the constant resistance mode (25 Ω) which is equivalent to 20% of the rated load. At a certain instant, it is changed
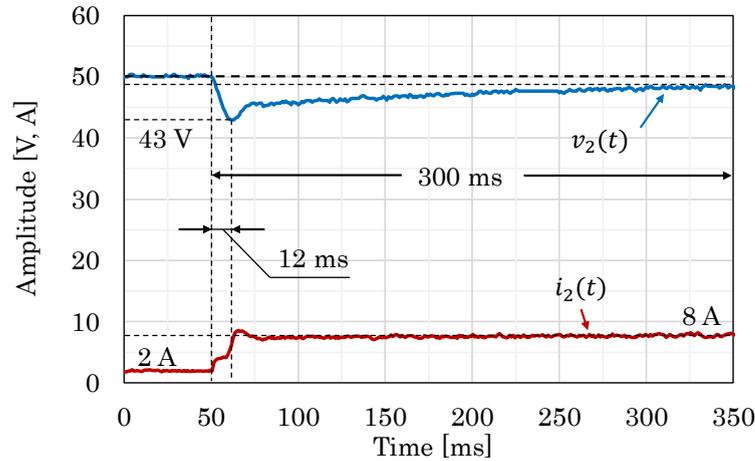
(a) Terminal voltage and current responses.
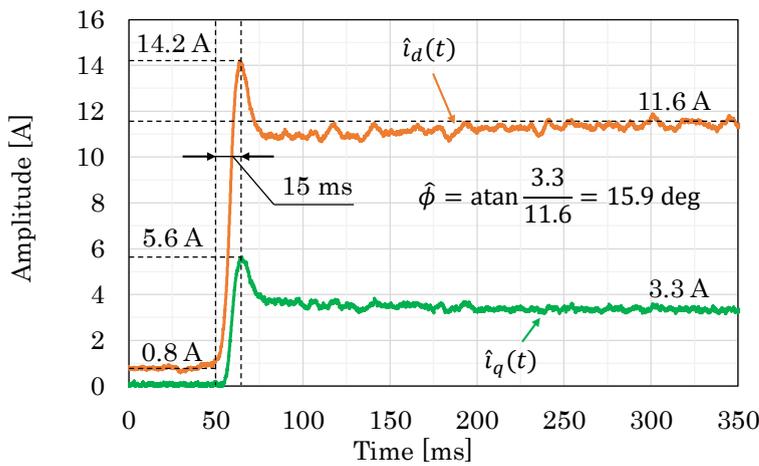
(b) Direct and quadruture current responses.

Figure 5.13. System dynamics when load changes from small to high.

suddenly to 6.25 Ω (80% rated load). After some time, it is instantaneously changed back to 25 Ω. The big of the change is just the same as the experiment conducted in Chapter 3 to verify how difference of the dynamic performance of the two control system. Fig. 5.13 and Fig. 5.14 express the system dynamics when undertaking the experiment.

First, the voltage is regulated at 50 V. When the load suddenly changes, the voltage drops to 43 V before recovering to its stable state at the preset (Fig. 5.13(a)). That undershoot is equivalent to -14%, which is a little bit smaller than -16.4% reported in Chapter 3. In term of current responses (Fig. 5.13(b)), at the instant of load change, both current components rise rapidly to compensate for the voltage drop. The peak currents in the transient state are 14.2 A and 5.6 A, respectively. That
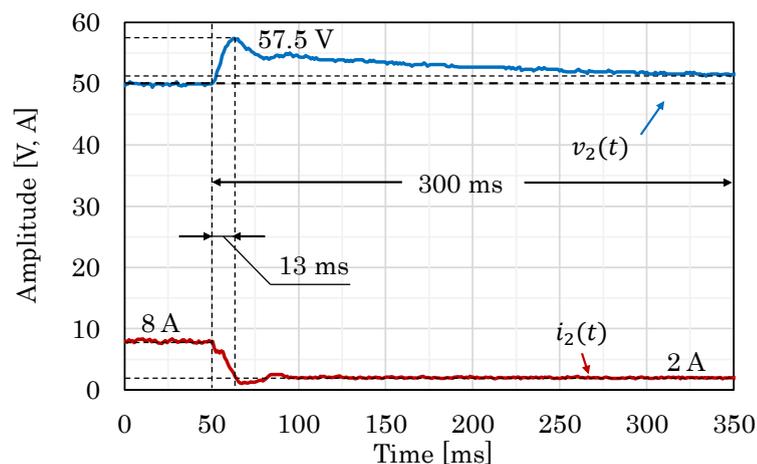
(a) Terminal voltage and current responses.
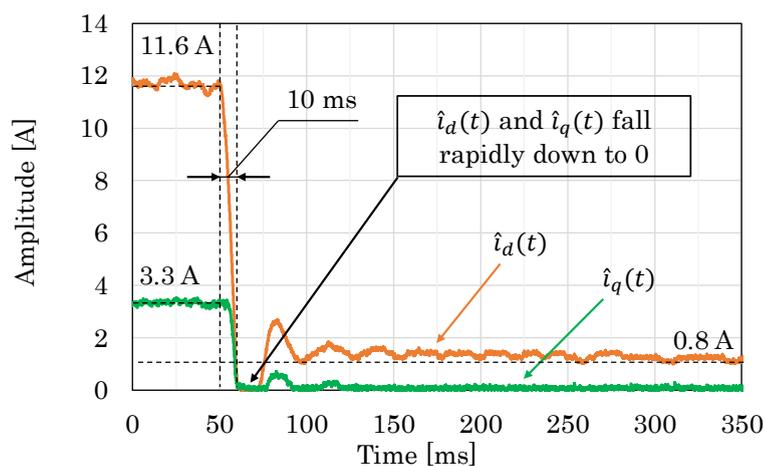
(b) Direct and quadruture current responses.

Figure 5.14. System dynamics when load changes from high to low.

means the load angle is about 21.5 degrees. Notes that, at the peak points, the switching frequency appears to be smaller than at the steady state for steeper current slope. Hence, a big load angle of 21.5 degrees will ensure ZVS of the converter regardless the observation error. At the steady state, the two current components are stable at 11.6 A and 3.3 A, respectively; implying that the load angle is about 15.9 degrees. Experiment to verify the switching behavior and the load angle is presented later.

The terminal voltage and current dynamics when reducing the load are described in Fig. 5.14(a). As shown, a voltage swell of +7.5 V (15% of the steady state value) is recorded. That, however, is slightly bigger than 11% of the performance in Chapter 3. Although, the two observed currents fall rapidly down to zero, the

terminal current slope is not as steep as that observed in Fig. 3.8(b). Consequently, the transient state is relatively longer (13 ms versus 8 ms).

In both experiments above, the dynamic performance are almost the same with that reported in Chapter 3, except the settling times are longer, which are about 300 ms. It can be lessen by optimizing the design of the voltage controller, for example reducing the phase margin and/or widening the bandwidth of the open-loop system.

5.6.2.3 Soft-switching verification

The switching behavior when regulating the terminal voltage at 50 V at 80% rated load is demonstrated in Fig. 5.15. Voltage at Port 1 is 60 V and the load resistance is 6.25 Ω. As described in Fig. 5.13(b), at the steady state, $\hat{i}_d(t)$ and $\hat{i}_q(t)$ are 11.6 and 3.3 A, respectively. Accordingly, the switching frequency is approximately 30 kHz. Under this condition, according to (2.9), the desired load angle is 16.9 degrees.

Because $\hat{i}_d = 11.6$ A and $\hat{i}_q = 3.3$ A, the observed load angle is about 15.9 degrees, which is only 1 degrees different from expectation. The actual load angle, as seen from Fig. 5.15, is 15.12 degrees, that is 0.8 degrees and 1.8 degrees different from the observed value and the expectation. Besides, the waveform shown in Fig. 5.15 also confirms that ZVS is achieved.
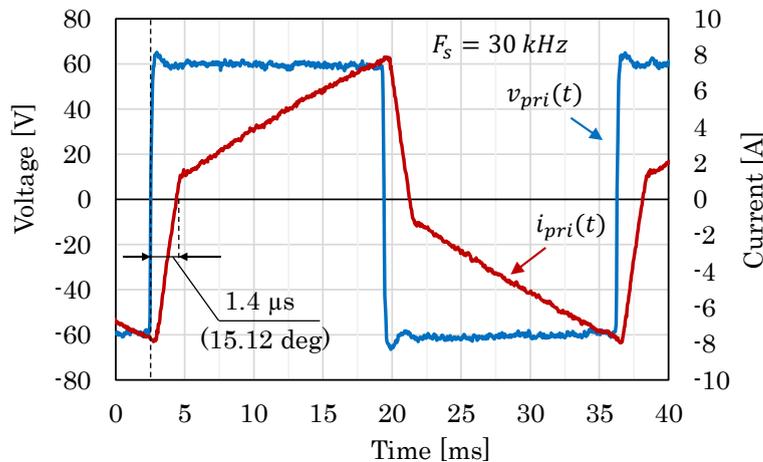
Figure 5.15. Switching behavior when $P_2 = 400$ W and $M = 1.2$.

5.6.3 Overloading

This experiment evaluate the overloading protection capability of the control system. The result is presented in Fig. 5.16. Firstly, the system is operating at 60% of the rated load ($V_2 = 50$ V, $I_2 = 6$ A, the load equivalent resistance is 8.333 Ω and thus, the power at Port 2 is 300 W). As shown in Fig. 5.16(b), $\hat{i}_d(t)$ and $\hat{i}_q(t)$ are 8.9 A and 2.5 A, respectively.
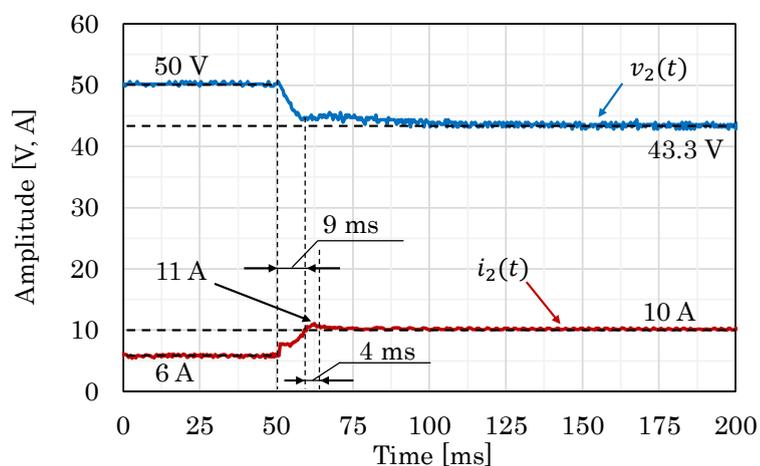
(a) Terminal voltage and current responses.
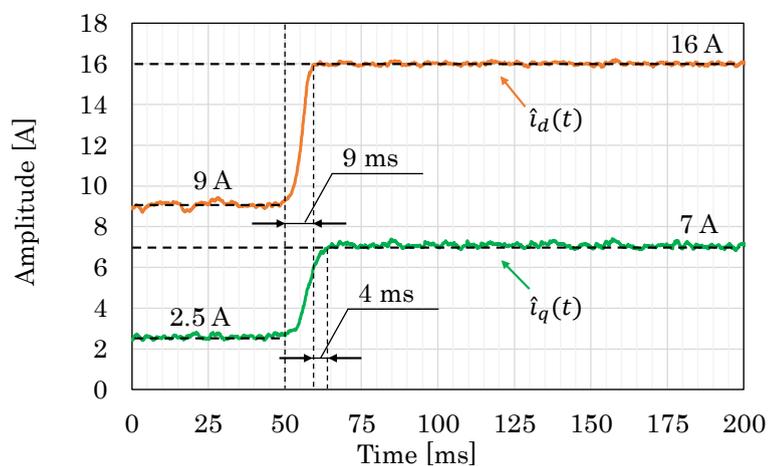
(b) Direct and quadruture current responses.

Figure 5.16. System response under the overload condition, observer-based controller.

At a certain instant, the resistance of the DC electronic load is suddenly reduced to 4.33 Ω that causes about 20% overload fault if the terminal voltage is kept stable. Instantaneously, $\hat{i}_d(t)$ and $\hat{i}_q(t)$ increase rapidly leading to the increment of the terminal current. When that current reaches its limitation of 10 A after a

rise time of 10 ms, $\hat{i}_d(t)$ also saturate at its designated maximum values of 16 A. Nevertheless, as $\hat{i}_q(t)$ continues increasing for an extra 4 ms, the load current has an overshoot of $+1$A.

After that, since there is no more room the two current components to increase, the voltage continue decreasing. Since then, the converter plays as a constant current source which injects a constant current of 10 A into the load. Consequently, the load voltage is stabilized at 43.3 V.

5.6.4 Short circuit

Similar to the test in Chapter 3, short circuit fault is intentionally created to examine how difference in the protection capability of the two control methods. The current threshold is set at the same at 20 A. The voltage and current waveform of the converter through the fault when employing the control system designed in this chapter is reported in Fig. 5.17.

As shown in the figure, the system is operating at the rated condition before the incident. When the fault occurs, the system takes only 0.5 ms to detect the sharp increment of the current and give the protection command. Which is 2.4 times faster than the detection speed of the system in Chapter 3.
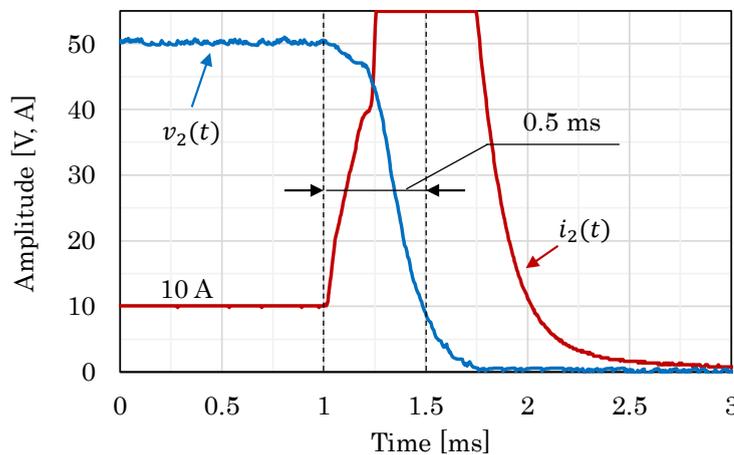
Figure 5.17. Protection behavior of the new control method.

That is because the protection mechanism used in this Chapter is based on the transfer current which dynamics is much faster than that of the terminal current. As the sampling time is 50 kHz, the processor needs only 25 cycles to issue the shutdown command. Since the detection time is reduced, the converter is better protected against risk from short circuit fault.

5.6.5 Efficiency comparison

This section investigate the difference in the overall performance of the two designed control systems. The converter is operated by each strategy while varying the load from 100 W to 500 W when the voltage ratio $M = 1.15$ ($V_1 = 57.5$ V and $V_2 = 50$ V. After that, the transmitted and the received powers are recorded and the efficiency is derived. Fig. 5.18 illustrates the overall efficiency of the converter when controlling by two methods.

As the linearizion point of the observer is 300 W, there, the efficiency obtained by both methods are the same at about 91.5%. When the power increases, due to the observer error, the actual load angle seems to be greater than the observed (and controlled) one (Fig. 4.9(c)). For this reason, the conduction loss is higher than that obtained by the MFPS control system. Consequently, overall efficiency
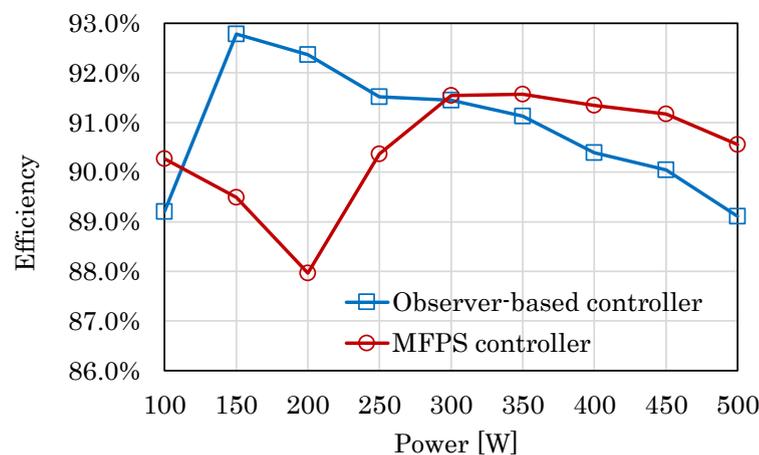
Figure 5.18. Efficiency comparison between the MFPS controller and the observer-based controller.

is slightly reduced as shown in Fig. 5.18. At 500 W, the efficiency reduction is about 1.6%.

In contrary, under the small power condition, the switching frequency is higher. As seen in Fig. 4.9(c), the observation error tends to be bigger downward. Hence, the actual load angle tends to be smaller than expected. The converter operates under the near ZVS condition and the efficiency is higher than that obtained by the MFPS control system. The maximum difference is 4.4% at 200 W.

At 100 W, the error is big enough that cause hard-switching and, as a consequence, the overall is degraded rapidly.

5.7 Conclusion

There are some remarks upon the observer-based control system presented in this chapter:

- Two current components can be regulated well without overshoot or undershoot or oscillation in the response. Interaction was still exist as it is not completely eliminated by the static decoupler. The use of a dynamic decoupler can help further suppressing the interaction.

- The overshoot of the terminal current was only 20% which is much reduced compared to that when control by the controller in Chapter 3.

- The overshoot when starting-up under the light load is reduced by 8.6%.

- Voltage fluctuation when load changes is from -14% to +15%, which is almost the same as the performance reported in Chapter 3.

- Soft-switching can be ensured in both the transient and steady states.

- Similar to the control system designed in Chapter 3, the observer-based control system can also behave as a current source when overloading.

- By using the transferred AC current as the feedback signal, protection capability was enhanced. When the short circuit fault occurs, it took the system only 0.5 ms to detect whereas that of the detection system in Chapter 3 was 1.2 ms.

- The observation error causes some changes in the overall performance: slightly decreasing under the high power condition and relatively increasing in the low power range. The difference is insignificant in the medium power range.

- Moreover, the observer-based control system can control the converter not only in all operation modes: including trapezoidal and triangle current mode.

Chapter 6

Extending the Fundamental Harmonic Analysis Approach for Zero-Voltage-Switch Modulation of Triple-Active-Bridge Converters

6.1 Introduction

In the previous chapters, the Fundamental Harmonic Approximation (FHA) method was applied for modeling and control the Dual-Active-Bridge (DAB) converters. Based on that, an observer was developed to estimate the direct and the quadrature components of the transferred current. And then, a decoupled control system was designed to regulate the two current components. The control system was intentionally applied for frequency-modulated DAB converter. Nevertheless, from the design procedures, we can realize that, the approach is not limit to frequency-modulated converter. Yes, it can also be implemented for converters modulating by other techniques such as phase-shift. This chapter discusses about how to achieve soft-switching for Triple-Active-Bridge (TAB) converters modulating by a so-called Quad-Phase-Shift (QPS) modulation technique using the FHA approach. This study is intended to apply for electric vehicle applications.

In electric vehicles (EVs), there usually have numerous of DC sources and loads, such as source for traction, auxiliary battery, small DC loads, etc. Recently, super capacitor and fuel-cell are also introduced into the EV storage system [72, 73]. In order to interface those sources and loads, a lot of DC/DC converters will be necessary [74]. However, the space inside an EV is very limited. Therefore, the converters must: i) have small size and very high power density; or ii) the quantity of converters should be reduced to save the space for more battery.

From other aspect, 42 V-DC bus has been introduced to the electrical system of EV soon due to some economical benefits [75, 76]. In term of traction drive, the traction motor need a power rail of few hundreds volt to operate. Meanwhile, other equipments, such as horn, wiper, light, etc., requires a low voltage 12 VDC for operation. This motivates to study about a TAB converter which can interface between a 36 V battery bank, a high and a low voltage DC-buses (200 V and 12 V, respectively) for an electric truck.

Due to the bidirectional power transmission capability, TAB converter is very suitable for such application. It can help power both the high voltage DC Link and the DC load in the normal operation as well as charge the regenerative energy into the battery when braking or driving down a slope. Besides, because of high power density, it can promisingly save a lot of space for battery. And its galvanic isolation can satisfy the safety requirement of the EV.

The TAB topology is derived from the DAB configuration discussed in the previous chapters. Unlike DAB type, TAB converter employs a three winding transformer for connecting three inverters. Conventionally, the phase shift technique is usually utilized [17–19, 77–80]. Two bridge shift angles are usually used to handle the power flows within ports [19, 78–80]. However, since the three ports are coupled using a transformer, three power paths ($1 \leftrightarrow 2$, $1 \leftrightarrow 3$, $2 \leftrightarrow 3$) will operate simultaneously. Because there are only two control variables, it is impossible to decouple the three power paths. Some recent researches introduced the so-called inner phase shift angle which shifts the two legs of one inverter from each other [17, 18, 77]. This adds at least one more degrees of freedom making the modulation

more flexible. Hence, the average power at one port can be kept constant or zero (idle mode) while the transmission between the other two ports is still activated.

Furthermore, the introduction of the inner phase shift make soft-switching (which is very difficult to be maintained if there are only two bridge shift angles) easier to be achieved [18, 77]. However, in [18] and [77], the ZVS strategy was developed based on the time domain analysis of the converter. Actually, as for TAB converters, there are numerous of switching states making the analysis complicated. The investigation reported in [17] also employed the FHA method. However, no soft-switching algorithm was presented.

In this chapter, two inner phase angles are added into the modulation of two secondary inverters. Hence, there are totally four phase shift variables. Among those, the two inner phase shifts are used to handle the power flows, whereas the two outer ones are served for achieving ZVS of all transistors. The converter is then analyzed in the frequency domain based on the FHA method. From that, active and reactive power components at all three inverters can be derived. Based on the relation between reactive and active powers (QP-ratio), ZVS condition is defined. After that, a new soft-switching strategy is proposed to help achieve ZVS regardless of the switching states of the converter. Simulation study confirms that the analysis method is reliable. As verified by experiment, ZVS is achieved in all investigated power range and the maximum and average efficiency are 95.58% and 94.66%, respectively.

6.2 Fundamental harmonic analysis

The TAB converter is illustrated in Fig. 6.1. The main battery is connected to port 1, whereas, the DC-bus and load are placed at port 2 and 3, respectively. Since the voltage ratio between any port pairs are quite high, a three winding transformer is used to match the voltage. There are three H-bridge inverters located at the three windings of the transformer to handle the power flow among ports. The inductors L_1, L_2' and L_3', which are the leakage inductances of the
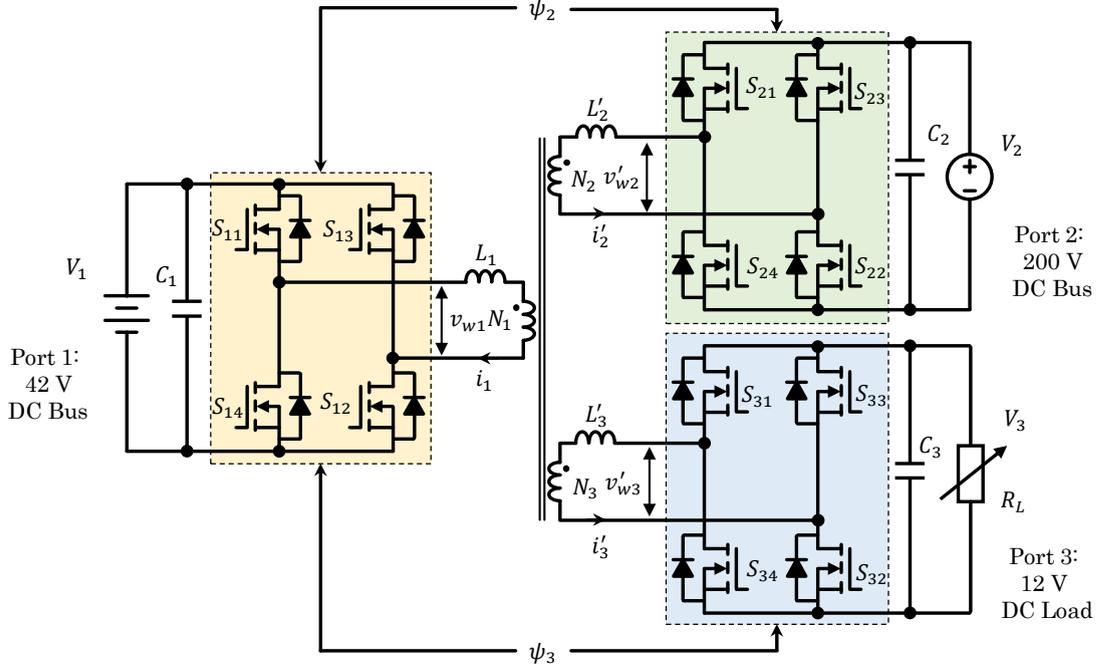
Figure 6.1. Triple-Active-Bridge Converter.
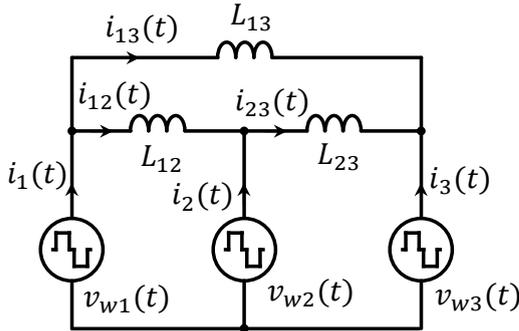
Figure 6.2. Primary-referred equivalent circuit.
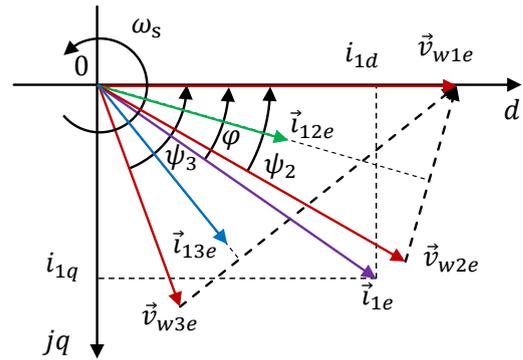
Figure 6.3. Vector diagram.

corresponding winding, are employed as the power containers. The transmission power is usually regulated by varying the phase shift angle ψ_2 and ψ_3 of inverters 2 and 3 with respect to inverter 1. In order to simplify the analysis, the delta-typed primary-referred circuit depicted in Fig. 6.2 is usually used. In which, L_{12}, L_{13} and L_{23} are the equivalent inductance referred to the primary side.

Since all of the quantities: $v_{wx}(t)$, $i_x(t)$ and $i_{xy}(t)$ (the voltage and current at the winding x; and the current flowing from port x to port y, respectively; $x, y \in [1,3]$, $x \neq y$) are AC signals with the same frequency of ω_s, the fundamental component of them can be seen as rotating vectors $\vec{v}_{wxe}$, $\vec{i}_{xe}$ and $\vec{i}_{xye}$. Considering a $dq-$ frame rotating with the speed of ω_s which d-axis is aligned to $\vec{v}_{w1e}$, the projections of all

vectors on $d-$ and $q-$ axis are DC quantities. The vector diagram demonstrating the relation of those vectors is depicted in Fig. 6.3. Accordingly, the three voltage vectors are determined by (6.1), where $n_2 = N_1 : N_2$; $n_3 = N_1 : N_3$; N_x is the number of turns of the winding x, $x \in [1,3]$.

$$
\begin{cases}
\vec{v}_{w1e} = \begin{bmatrix} v_{1d} \\ v_{1q} \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} V_1 \\ 0 \end{bmatrix} \\[2ex]
\vec{v}_{w2e} = \begin{bmatrix} v_{2d} \\ v_{2q} \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} n_2 V_2 \cos \psi_2 \\ n_2 V_2 \sin \psi_2 \end{bmatrix} \\[2ex]
\vec{v}_{w3e} = \begin{bmatrix} v_{3d} \\ v_{3q} \end{bmatrix} = \frac{4}{\pi} \begin{bmatrix} n_3 V_3 \cos \psi_3 \\ n_3 V_3 \sin \psi_3 \end{bmatrix}
\end{cases}
\tag{6.1}
$$

Considers the transmission path from port 1 to port 2. By ignoring the winding resistance, the transferred current $\vec{i}_{12e}$ can be calculated by subtracting $\vec{v}_{w2e}$ from $\vec{v}_{w1e}$ then dividing by the reactance X_{12}, where $X_{12} = \omega_s L_{12}$. Calculations of $\vec{i}_{13e}$ and $\vec{i}_{23e}$ can be done by using the same manner. Hence, the port-to-port currents $\vec{i}_{12e}$, $\vec{i}_{13e}$ and $\vec{i}_{23e}$ are expressed by (6.2). Notes that, since the $d-$axis is intentionally aligned to $\vec{v}_{w1e}$, the quadrature projection $v_{1q} = 0$.

$$
\begin{cases}
\vec{i}_{12e} = \begin{bmatrix} i_{12d} \\ i_{12q} \end{bmatrix} = \frac{1}{X_{12}} \begin{bmatrix} -v_{1q} + v_{2q} \\ v_{1d} - v_{2d} \end{bmatrix} \\[2ex]
\vec{i}_{13e} = \begin{bmatrix} i_{13d} \\ i_{13q} \end{bmatrix} = \frac{1}{X_{13}} \begin{bmatrix} -v_{1q} + v_{3q} \\ v_{1d} - v_{3d} \end{bmatrix} \\[2ex]
\vec{i}_{23e} = \begin{bmatrix} i_{23d} \\ i_{23q} \end{bmatrix} = \frac{1}{X_{23}} \begin{bmatrix} -v_{2q} + v_{3q} \\ v_{2d} - v_{3d} \end{bmatrix}
\end{cases}
\tag{6.2}
$$

Similar to chapter 5, the instantaneous active and reactive power can be calculated by:

$$
\begin{cases}
P = \dfrac{1}{2}(v_d i_d + v_q i_q) \\[2ex]
Q = \dfrac{1}{2}(v_d i_q - v_q i_d)
\end{cases}
\tag{6.3}
$$

Accordingly, the port-to-port active and reactive powers can be easily derived:

$$\begin{bmatrix} P_{xy} \\ Q_{xy} \end{bmatrix} = \frac{1}{2X_{xy}} \begin{bmatrix} v_{xd}v_{yq} - v_{xq}v_{yd} \\ v_{xm}^2 - v_{xd}v_{yd} - v_{xq}v_{yq} \end{bmatrix} \tag{6.4}$$

where $v_{xm}^2 = v_{xd}^2 + v_{xq}^2$; $x, y \in [1,3]$ and $x \neq y$.

From the primary-referred diagram in Fig. 6.2 and the Kirchhoff Law:

$$\begin{cases} \vec{i}_{1e} = [i_{1d} \quad i_{1q}]^T = \vec{i}_{12e} + \vec{i}_{13e} \\ \vec{i}_{2e} = [i_{2d} \quad i_{2q}]^T = -\vec{i}_{12e} + \vec{i}_{23e} \\ \vec{i}_{3e} = [i_{3d} \quad i_{3q}]^T = -\vec{i}_{13e} - \vec{i}_{23e} \end{cases} \tag{6.5}$$

where $\vec{i}_{xe}$, $x \in [1,3]$ is the current flowing in the winding x.

Substitute (6.1) and (6.5) into (6.3), the instantaneous active and reactive power at each winding is defined by:

$$\begin{cases} P_1 = K \left[\dfrac{M_2}{X_{12}} \sin \psi_2 + \dfrac{M_3}{X_{13}} \sin \psi_3 \right] \\[2mm] P_2 = K M_2 \left[-\dfrac{1}{X_{12}} \sin \psi_2 + \dfrac{M_3}{X_{23}} \sin \Delta\psi \right] \\[2mm] P_3 = K M_3 \left[-\dfrac{1}{X_{13}} \sin \psi_3 - \dfrac{M_2}{X_{23}} \sin \Delta\psi \right] \\[2mm] Q_1 = K \left[\dfrac{1}{X_{12}} (1 - M_2 \cos \psi_2) + \dfrac{1}{X_{13}} (1 - M_3 \cos \psi_3) \right] \\[2mm] Q_2 = K M_2 \left[\dfrac{1}{X_{12}} (M_2 - \cos \psi_2) + \dfrac{1}{X_{23}} (M_2 - M_3 \cos \Delta\psi) \right] \\[2mm] Q_3 = K M_3 \left[\dfrac{1}{X_{13}} (M_3 - \cos \psi_3) + \dfrac{1}{X_{23}} (M_3 - M_2 \cos \Delta\psi) \right] \end{cases} \tag{6.6}$$

where $K = \dfrac{8V_1^2}{\pi^2}$; $M_2 = \dfrac{n_2 V_2}{V_1}$; $M_3 = \dfrac{n_3 V_3}{V_1}$; and $\Delta\psi = \psi_3 - \psi_2$. Notes that:

$$\begin{cases} P_{12} = \dfrac{K M_2}{X_{12}} \sin \psi_2 \\[2mm] P_{13} = \dfrac{K M_3}{X_{13}} \sin \psi_3 \\[2mm] P_{23} = \dfrac{K M_2 M_3}{X_{23}} \sin \Delta\psi \end{cases}$$

and that:

$$\begin{cases} P_1 = P_{12} + P_{13} \\ P_2 = -P_{12} + P_{23} \\ P_3 = -P_{13} + P_{23} \end{cases}$$

Obviously, if the power dissipation on inverters is ignored, the active powers P_x ($x \in [1, 3]$) expressed in (6.6) are also the power at the corresponding DC ports. By varying ψ_2 and ψ_3, the active powers can be controlled very well. Furthermore, one port can be kept at the idle state, while the power flow between the other two ports is variable. For example, from (6.6), the phase shift relation to keep $P_3 = 0$ is:

$$\psi_2 = \psi_3 + \arcsin \left(\frac{X_{23}}{M_2 X_{13}} \sin \psi_3 \right) \tag{6.7}$$

Or more generally, the control strategy to keep P_3 constant at the desired value P_3^* is:

$$\psi_2 = \psi_3 + \arcsin \left(\frac{X_{23}}{K M_2 M_3} P_3^* + \frac{X_{23}}{M_2 X_{13}} \sin \psi_3 \right) \tag{6.8}$$

After that, the transmission is modelized as a function of ψ_3 and P_3^*, ψ_2 is then derived from ψ_3 according to (6.7) or (6.8). Equation (6.8) can also be used to decoupled control P_2 and P_3 where ψ_2 takes the charge of P_3 and ψ_3 is responsible for handling P_2. Nevertheless, both (6.7) and (6.8) can control only the active powers.

As discussed before, the reactive power should be put under supervision as well for achieving ZVS and for limiting the conduction loss. In chapter 5, the switching frequency was employed as the additional variable for managing the active power, and the phase shift was charged for the reactive power. That two variables are enough for controlling two power components of a DAB converter. However, as for TAB converters, there are totally six power components must be supervised. With only two phase shift angles, it is impossible to control all active and reactive power components simultaneously. In other words, managing all power components at the same time requires at least one or two more degrees of freedom.

Motivated from this, two inner phase shifts are introduced. An inner phase shift is the added angle to make the phase difference between two legs of one inverter

less than π. Since there are four variables, two inner and two outer phase shifts, can be used in the modulation, this method is named Quad-Phase-Shift (QPS). Next section shows how the QPS scheme changes the mathematic equations and how to achieve ZVS in each operation modes.

6.3 Zero-voltage-switch modulation strategy

6.3.1 Effect of the inner phase shift modulation

By introducing two inner phase shift angles to inverters 2 and 3, the amplitudes of vectors $\vec{v}_{w2e}$ and $\vec{v}_{w3e}$ are modifiable. As a consequence, the fundamental voltage components are also *"drifted"* by a half of the inner phase shift angle as demonstrated in Fig. 6.4 for inverter 2. Let δ_2 and δ_3 be the inner phase shift angles of the corresponding inverter. The three voltage vectors are changed as (6.9):

$$\begin{cases} \vec{v}_{w1e} = \dfrac{4V_1}{\pi} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \\[3mm] \vec{v}_{w2e} = \dfrac{4n_2V_2}{\pi} \cos\dfrac{\delta_2}{2} \begin{bmatrix} \cos\left(\psi_2 + \frac{\delta_2}{2}\right) \\ \sin\left(\psi_2 + \frac{\delta_2}{2}\right) \end{bmatrix} \\[3mm] \vec{v}_{w3e} = \dfrac{4n_3V_3}{\pi} \cos\dfrac{\delta_3}{2} \begin{bmatrix} \cos\left(\psi_3 + \frac{\delta_3}{2}\right) \\ \sin\left(\psi_3 + \frac{\delta_3}{2}\right) \end{bmatrix} \end{cases} \tag{6.9}$$
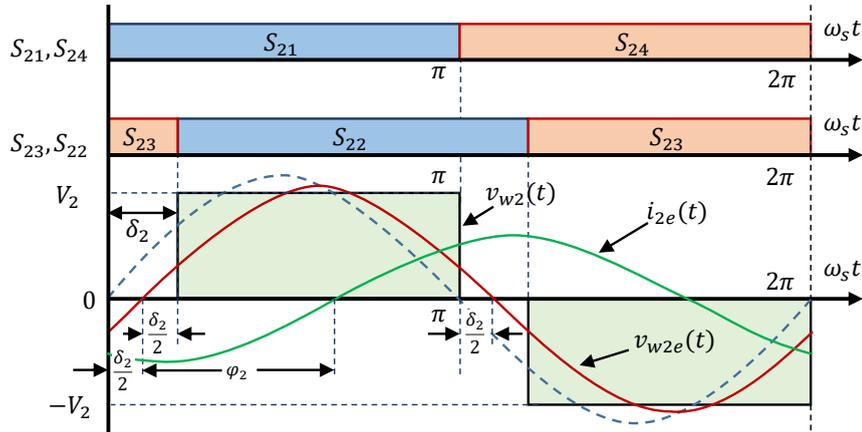

Figure 6.4. Waveforms when employing the inner phase shift modulation.

Recalculating the six power components with regard to the phase drift, we have:

$$
\begin{cases}
P_1 = K \left[\dfrac{m_2}{X_{12}} \sin \psi_{21} + \dfrac{m_3}{X_{13}} \sin \psi_{31} \right] \\[2mm]
P_2 = K m_2 \left[-\dfrac{1}{X_{12}} \sin \psi_{21} + \dfrac{m_3}{X_{23}} \sin \psi_{32} \right] \\[2mm]
P_3 = K m_3 \left[-\dfrac{1}{X_{13}} \sin \psi_{31} - \dfrac{m_2}{X_{23}} \sin \psi_{32} \right] \\[2mm]
Q_1 = K \left[\dfrac{1}{X_{12}} (1 - m_2 \cos \psi_{21}) + \dfrac{1}{X_{13}} (1 - m_3 \cos \psi_{31}) \right] \\[2mm]
Q_2 = K m_2 \left[\dfrac{1}{X_{12}} (m_2 - \cos \psi_{21}) + \dfrac{1}{X_{23}} (m_2 - m_3 \cos \psi_{32}) \right] \\[2mm]
Q_3 = K m_3 \left[\dfrac{1}{X_{13}} (m_3 - \cos \psi_{31}) + \dfrac{1}{X_{23}} (m_3 - m_2 \cos \psi_{32}) \right]
\end{cases}
\tag{6.10}
$$

where $m_x = M_x \cos \dfrac{\delta_x}{2}$, $x \in [2, 3]$; $\psi_{21} = \psi_2 + \dfrac{\delta_2}{2}$, $\psi_{31} = \psi_3 + \dfrac{\delta_3}{2}$ and $\psi_{32} = \psi_{31} - \psi_{21}$. Notes that, ψ_2 and ψ_3 are the actual phase shift angle between bridges; whereas the angles ψ_{21} and ψ_{31} are the *relative* phase shift between the fundamental components of voltages.

The inter-port power flows are also recalculated:

$$
\begin{cases}
P_{12} = \dfrac{K m_2}{X_{12}} \sin \psi_{21} \\[2mm]
P_{13} = \dfrac{K m_3}{X_{13}} \sin \psi_{31} \\[2mm]
P_{23} = \dfrac{K m_2 m_3}{X_{23}} \sin \psi_{32}
\end{cases}
\tag{6.11}
$$

Equations (6.10) and (6.11) suggest that m_2 and m_3 (or the inner phase shift angles δ_2 and δ_3) can be used to regulate the active powers. Furthermore, as observed from Fig. 6.4, in order for all MOSFETs to achieve ZVS, the phase difference φ_x between the current $i_{xe}(t)$ and $v_{xe}(t)$ ($x \in [1,\ 3]$) must satisfy the condition (6.12) of the QP-ratio:

$$
\varphi_x = \arctan \frac{Q_x}{P_x} \in \left[\frac{\delta_x}{2},\ \pi - \frac{\delta_x}{2} \right], \quad \forall x \in [1,\ 3],\ \delta_1 = 0
\tag{6.12}
$$

Condition (6.12) depends on the transmission direction, or in other words, on the sign of the active powers P_x. As described before, the converter system has three

sink/source components: battery (port 1), DC-Bus (port 2) and DC Load (port 3), accordingly, there are three possible transmission modes as follows:

- Mode 1: $P_1 \geq 0, P_2 \leq 0, P_3 \leq 0$

- Mode 2: $P_1 \leq 0, P_2 \geq 0, P_3 \leq 0$

- Mode 3: $P_1 \geq 0, P_2 \geq 0, P_3 \leq 0$

A positive sign implies that the port is sending power, and vice versa, a negative sign means the port is absorbing power. Since port 3 is the passive load (e.g. light, horn, wipers, etc.), it cannot send any power to other ports. Hence, in the three modes listed above, P_3 is always negative.

Among three modes listed above, Mode 3 is insignificantly useful in practice. In this mode, the DC-load is powered by both the battery and the regenerative braking power. However, the rated power of the load is usually very small compared to the dynamic power of the regeneration. Therefore, this mode is excluded from the investigation of this chapter.

Following texts consider the ZVS condition in Mode 1 and Mode 2.

6.3.2 Mode 1: $P_1 \geq 0$, $P_2 \leq 0$ and $P_3 \leq 0$

Depending on the relation between ψ_{21} and ψ_{31}, this mode can be further divided into two submodes: submode 1A and submode 1B.

6.3.2.1 Submode 1A: $\psi_{31} \geq \psi_{21} \geq 0$

Fig. 6.5 describes the directions of power paths in this submode, where P_{xy} implies the power flow between the port pair x and y. Since $P_1 \geq 0$, $P_2 \leq 0$ and $P_3 \leq 0$, the battery discharges energy to power both the DC-Link and the load. And because $\psi_{31} \geq \psi_{21} \geq 0$, energy also flows from the DC link to the DC load. Notes that, although there is one flow in and one flow out at terminal 2, the average
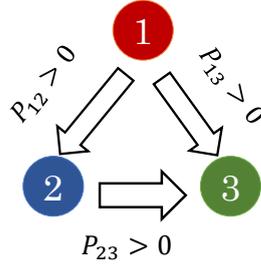
Figure 6.5. Power paths in Mode 1A.

power P_2 is negative. That means, the power portion port 2 passes to the load is less than what it receives from the battery. Therefore, this submode is suitable for operating the converter when the EV is standstill ($P_2 = 0$) or running with a constant low velocity (small P_2).

Substituting (6.10) into (6.12) then rearranging the obtained result, the QP-ratio equations becomes:

$$
\begin{cases}
\dfrac{1}{X_{12}} \times f_1(\delta_2, \psi_{21}) + \dfrac{1}{X_{13}} \times f_2(\delta_3, \psi_{31}) & \geq 0 \\[2ex]
\dfrac{1}{X_{12}} \times g_1(\delta_2, \psi_{21}) + \dfrac{1}{X_{23}} \times g_2(\delta_2, \delta_3, \psi_{32}) & \geq 0 \\[2ex]
\dfrac{1}{X_{13}} \times h_1(\delta_3, \psi_{31}) + \dfrac{1}{X_{23}} \times h_2(\delta_2, \delta_3, \psi_{32}) & \geq 0
\end{cases}
\tag{6.13}
$$

where

$$
\begin{cases}
f_1(\delta_2, \psi_{21}) & = 1 - m_2 \cos \psi_{21} \\[2ex]
f_2(\delta_3, \psi_{31}) & = 1 - m_3 \cos \psi_{31} \\[2ex]
g_1(\delta_2, \psi_{21}) & = \dfrac{m_2^2}{M_2} - \cos\left(\psi_{21} - \dfrac{\delta_2}{2}\right) \\[2ex]
g_2(\delta_2, \delta_3, \psi_{32}) & = \dfrac{m_2^2}{M_2} - m_3 \cos\left(\psi_{32} + \dfrac{\delta_2}{2}\right) \\[2ex]
h_1(\delta_3, \psi_{31}) & = \dfrac{m_3^2}{M_3} - \cos\left(\psi_{31} - \dfrac{\delta_3}{2}\right) \\[2ex]
h_2(\delta_2, \delta_3, \psi_{32}) & = \dfrac{m_3^2}{M_3} - m_2 \cos\left(\psi_{32} - \dfrac{\delta_3}{2}\right)
\end{cases}
$$

Inequalities (6.13) has four variables and highly nonlinear since it contains trigonometric functions. Thus, it is very difficult to solve (6.13) for a global solution which covers all the ZVS region. However, a local solution partially covering the region can be found by letting all the factors, $f_1(\delta_2, \psi_{21})$, $f_2(\delta_3, \psi_{31})$, $g_1(\delta_2, \psi_{21})$,

$g_2(\delta_2, \psi_{32})$, $h_1(\delta_3, \psi_{31})$, and $h_2(\delta_3, \psi_{32})$, be greater than or equal to 0:

$$\begin{cases} f_1(\delta_2, \psi_{21}) & \geq 0 \\ f_2(\delta_3, \psi_{31}) & \geq 0 \\ g_1(\delta_2, \psi_{21}) & \geq 0 \\ g_2(\delta_2, \delta_3, \psi_{32}) & \geq 0 \\ h_1(\delta_3, \psi_{31}) & \geq 0 \\ h_2(\delta_2, \delta_3, \psi_{32}) & \geq 0 \end{cases} \tag{6.14}$$

Although a set $(\delta_2, \delta_3, \psi_{21}, \psi_{31})$ satisfying (6.13) might not make (6.14) appropriate, a combination fulfills (6.14) will always gratify (6.13). That is the reason why the such combination is so-called a *local solution*.

Assuming that δ_2 and δ_3 are known then solving (6.14) for ψ_{21}, ψ_{31} and ψ_{32} with the assumption:

$$\psi_{31} \geq \psi_{21} \geq 0,$$

we have:

$$\begin{cases} \psi_{21} \geq \Psi_{21,min} = \max \begin{cases} \arccos\left(\min\left\{\dfrac{1}{m_2},\ 1\right\}\right) \\ \arccos\left(\min\left\{\dfrac{m_2^2}{M_2},\ 1\right\}\right) + \dfrac{\delta_2}{2} \end{cases} \\[4em] \psi_{31} \geq \Psi_{31,min} = \max \begin{cases} \arccos\left(\min\left\{\dfrac{1}{m_3},\ 1\right\}\right) \\ \arccos\left(\min\left\{\dfrac{m_3^2}{M_3},\ 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases} \\[4em] \psi_{32} \geq \Psi_{32,min} = \max \begin{cases} \arccos\left(\min\left\{\dfrac{m_2^2}{M_2 m_3},\ 1\right\}\right) - \dfrac{\delta_2}{2} \\ \arccos\left(\min\left\{\dfrac{m_3^2}{M_3 m_2},\ 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases} \end{cases} \tag{6.15}$$

As mentioned, the solution (6.15) may not cover all the ZVS area of this transmission mode; however, it can guarantee ZVS for all transistors. Fig. 6.6 demonstrates the ZVS area according to (6.15) when $M_2 = M_3 = 1$. Since (6.15) is a local solution, the shaded area might consist some ZVS operation points. However, the non-shaded areas in the figure are surely the soft-switching zones. The boundaries of the ZVS area are $\Psi_{21,min}$ and $\Psi_{31,min}$. In order to reduce the conduction loss, the displacement angle φ_x defined in (6.12) should be minimized. Therefore, in
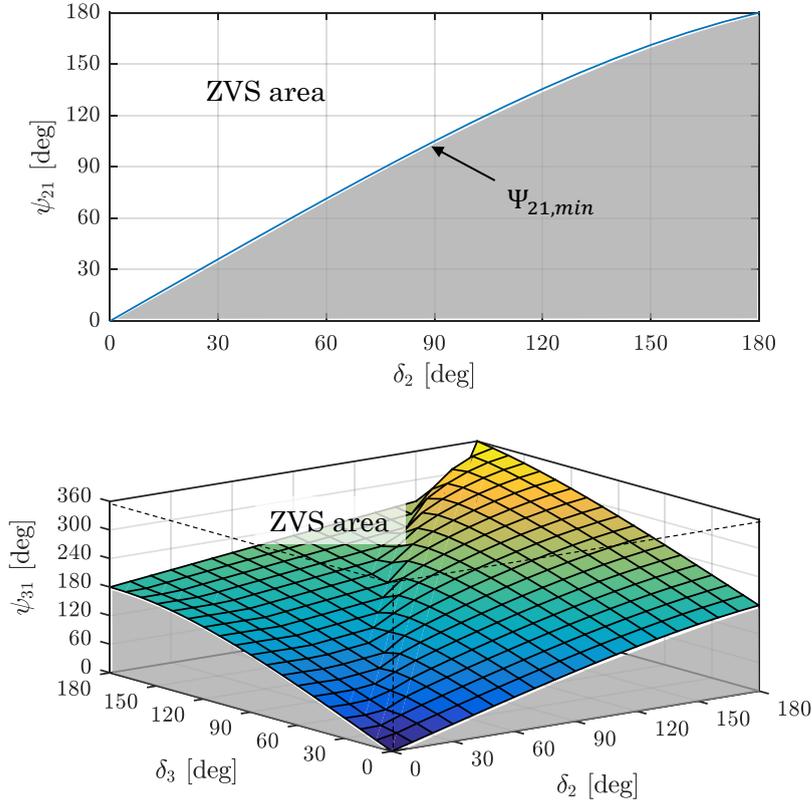
Figure 6.6. ZVS area in Mode 1A, $M_2 = M_3 = 1$.

this study, the relative bridge shift angles are intentionally assigned to the smallest ones (the lower boundary of the ZVS area) as (6.16). At the same time, δ_2 and δ_3 are used to regulate the active power components.

$$
\begin{cases}
\psi_{21} = \Psi_{21,min} \\
\psi_{31} = \max \left\{ \Psi_{31,min}, \ \Psi_{21,min} + \Psi_{32,min} \right\}
\end{cases}
\tag{6.16}
$$

The actual bridge shift angles ψ_2 and ψ_3 can then be calculated from ψ_{21}, ψ_{31}, δ_2 and δ_3 as (6.17):

$$
\begin{cases}
\psi_2 = \psi_{21} - \dfrac{\delta_2}{2} \\[2mm]
\psi_3 = \psi_{31} - \dfrac{\delta_3}{2}
\end{cases}
\tag{6.17}
$$

Actually, the ZVS function described in (6.15) is quite complicated since it contains trigonometric and inverse trigonometric functions. Hence, in practice, it can be implemented by using lookup table to boost the calculation speed.

6.3.2.2   Submode 1B: $\psi_{21} \geq \psi_{31} \geq 0$

The directions of power paths in this mode is illustrated in Fig. 6.7. Since $\psi_{21} \geq \psi_{31} \geq 0$, there is energy flows from the load back to the DC Link. To ensure the average power P_3 negative, the power portion port 2 takes from port 3 must be smaller than the portion port 3 obtains from the battery. This submode is thus suitable for the acceleration process of the EV or running in the normal traffic condition (horn, wiper, light, etc. are not used).
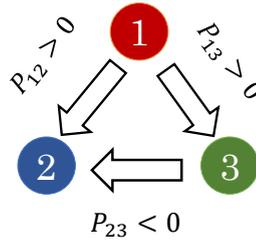
Figure 6.7. Power paths in Mode 1B.

Using the assumption $\psi_{21} \geq \psi_{31} \geq 0$ to solve (6.14) for ψ_{21} and ψ_{31}, we have:

$$
\begin{aligned}
\psi_{21} \geq \Psi_{21,min} &= \max \begin{cases} \arccos\left(\min\left\{\dfrac{1}{m_2}, 1\right\}\right) \\ \arccos\left(\min\left\{\dfrac{m_2^2}{M_2}, 1\right\}\right) + \dfrac{\delta_2}{2} \end{cases} \\
\psi_{31} \geq \Psi_{31,min} &= \max \begin{cases} \arccos\left(\min\left\{\dfrac{1}{m_3}, 1\right\}\right) \\ \arccos\left(\min\left\{\dfrac{m_3^2}{M_3}, 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases} \\
\psi_{32} \leq \Psi_{32,max} &= \min \begin{cases} -\arccos\left(\min\left\{\dfrac{m_2^2}{M_2 m_3}, 1\right\}\right) - \dfrac{\delta_2}{2} \\ -\arccos\left(\min\left\{\dfrac{m_3^2}{M_3 m_2}, 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases}
\end{aligned} \tag{6.18}
$$

Fig. 6.8 illustrates the ZVS area in this mode according to (6.18). Actually, Fig. 6.8 and Fig. 6.6 are quite similar except the roles of ψ_{21} and ψ_{31} have been swapped. That is because in the local solutions (6.15) and (6.18) solved from (6.14), ports 2 and 3 are treated equally as no impedance (X_{xy}) exists in the equations.
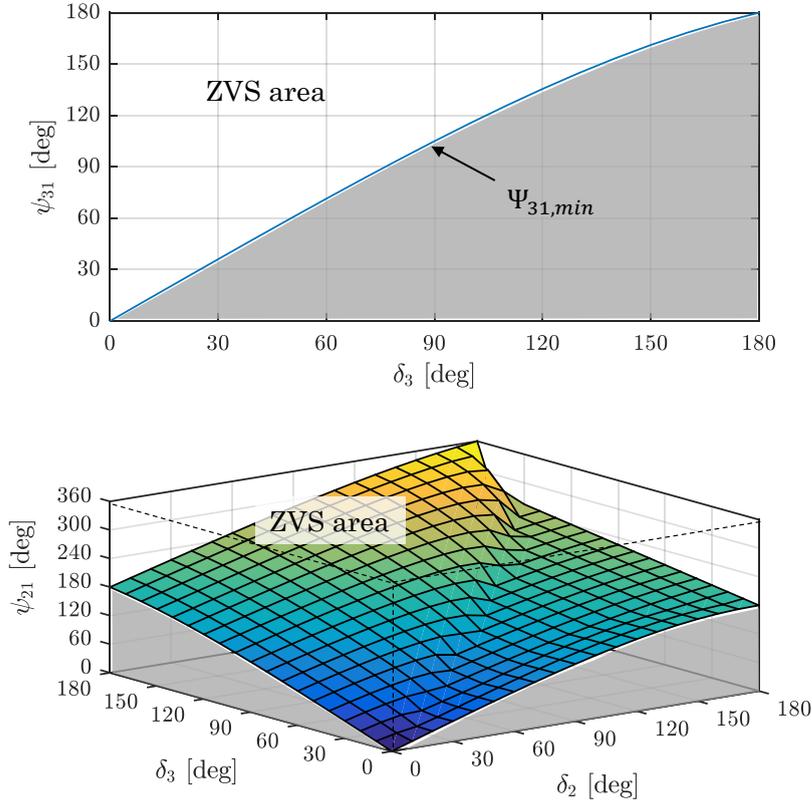
Figure 6.8. ZVS area in Mode 1B, $M_2 = M_3 = 1$.

Alike Mode 1A, the low boundary of the ZVS area is selected as the ZVS trajectory in this mode:

$$
\begin{cases}
\psi_{21} = \max \left\{ \Psi_{21,min}, \ \Psi_{31,min} - \Psi_{32,max} \right\} \\
\psi_{31} = \Psi_{31,min}
\end{cases}
\tag{6.19}
$$

And finally, (6.17) is employed to derive the actual phase shift angles for the modulation.

6.3.3 Mode 2: $P_1 \leq 0$, $P_2 \geq 0$ and $P_3 \leq 0$

In this mode, the DC-bus absorbs the power from the regenerative braking process ($P_2 > 0$) to charge the battery ($P_1 < 0$) and to feed the DC-load ($P_3 < 0$). Depending on the relation between ψ_{21} and ψ_{31}, this mode is also divided into two submodes.

6.3.3.1 Submode 2A: $\psi_{21} \leq \psi_{31} \leq 0$

Fig. 6.9 describes the power direction in submode 2A. As mentioned, port 3 is powered by the regenerative energy. Since $\psi_{21} \leq \psi_{31} \leq 0$, there is a power flow passes through the load to charge the battery ($P_{13} < 0$). This mode is useful when we want to save most of the regenerative energy into the battery.

Figure 6.9. Power paths in Mode 2A.

Figure 6.10. ZVS area in Mode 2A, $M_2 = M_3 = 1$.

By using the same manner of analysis, the ZVS condition of this mode is:

$$
\begin{cases}
\psi_{21} \leq \Psi_{21,max} = \min
\begin{cases}
-\arccos\left(\min\left\{\dfrac{1}{m_2},\, 1\right\}\right) \\[2ex]
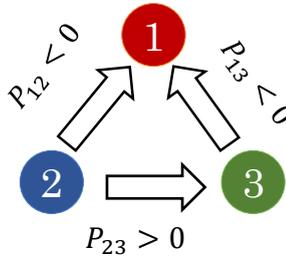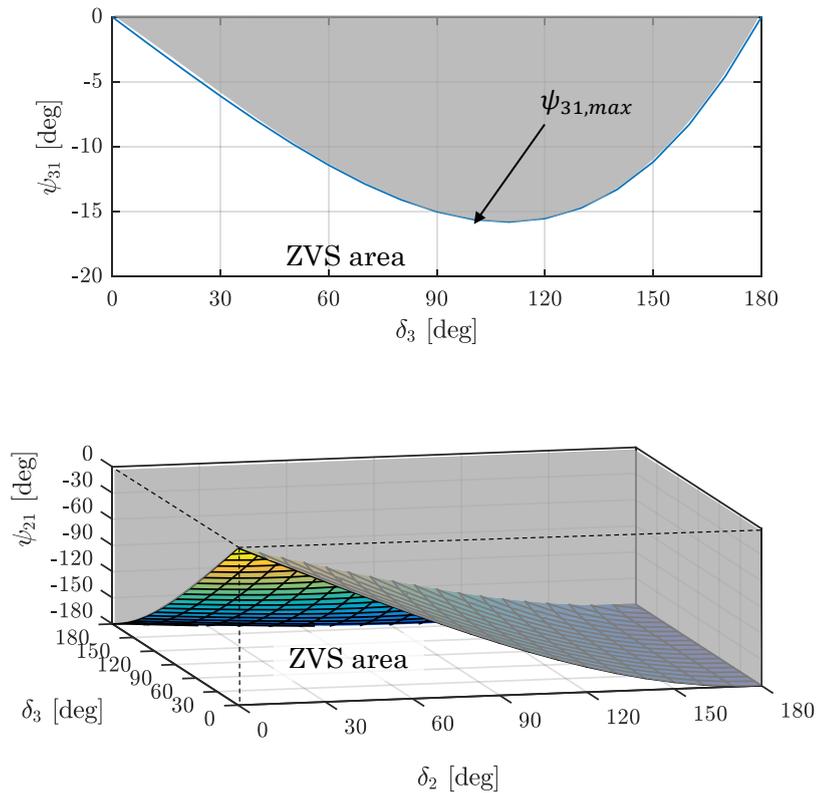-\arccos\left(\min\left\{\dfrac{m_2^2}{M_2},\, 1\right\}\right) - \dfrac{\delta_2}{2}
\end{cases} \\[6ex]
\psi_{31} \leq \Psi_{31,max} = \min
\begin{cases}
-\arccos\left(\min\left\{\dfrac{1}{m_3},\, 1\right\}\right) \\[2ex]
-\arccos\left(\min\left\{\dfrac{m_3^2}{M_3},\, 1\right\}\right) + \dfrac{\delta_3}{2}
\end{cases} \\[6ex]
\psi_{32} \geq \Psi_{32,min} = \max
\begin{cases}
\arccos\left(\min\left\{\dfrac{m_2^2}{M_2 m_3},\, 1\right\}\right) + \dfrac{\delta_2}{2} \\[2ex]
\arccos\left(\min\left\{\dfrac{m_3^2}{M_3 m_2},\, 1\right\}\right) + \dfrac{\delta_3}{2}
\end{cases}
\end{cases}
\tag{6.20}
$$

In this situation, both ψ_{21} and ψ_{31} are negative. Therefore, the highest boundaries are selected as the modulation trajectory. The modulation strategy of this mode is (6.21) and is demonstrated in Fig. 6.10.

$$
\begin{cases}
\psi_{21} = \min\left\{\Psi_{21,max},\ \Psi_{31,max} - \Psi_{32,min}\right\} \\[2ex]
\psi_{31} = \Psi_{31,max}
\end{cases}
\tag{6.21}
$$

6.3.3.2 Submode 2B: $\psi_{21} \leq 0 \leq \psi_{31}$

Fig. 6.11 describes the power direction in submode 2B. Since $\psi_{21} \leq 0 \leq \psi_{31}$, the load receives power from both the battery and the regenerative process. This mode can be used when the battery is almost full, however, attention should be paid on the power rating of the DC load.
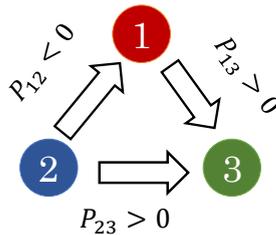
Figure 6.11. Power paths in Mode 2B.

The ZVS condition of this mode is:

$$\psi_{21} \leq \Psi_{21,max} = \min \begin{cases} -\arccos\left(\min\left\{\dfrac{1}{m_2},\ 1\right\}\right) \\[2mm] -\arccos\left(\min\left\{\dfrac{m_2^2}{M_2},\ 1\right\}\right) - \dfrac{\delta_2}{2} \end{cases}$$

$$\psi_{31} \geq \Psi_{31,min} = \max \begin{cases} \arccos\left(\min\left\{\dfrac{1}{m_3},\ 1\right\}\right) \\[2mm] \arccos\left(\min\left\{\dfrac{m_3^2}{M_3},\ 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases} \quad (6.22)$$

$$\psi_{32} \geq \Psi_{32,min} = \max \begin{cases} \arccos\left(\min\left\{\dfrac{m_2^2}{M_2 m_3},\ 1\right\}\right) + \dfrac{\delta_2}{2} \\[2mm] \arccos\left(\min\left\{\dfrac{m_3^2}{M_3 m_2},\ 1\right\}\right) + \dfrac{\delta_3}{2} \end{cases}$$

Fig. 6.12 describes the ZVS area of this mode. Since $\psi_{21} \leq 0 \leq \psi_{31}$, the highest boundary $\Psi_{21,max}$ is assigned for ψ_{21}, whereas the lowest boundary $\Psi_{31,min}$ is chosen
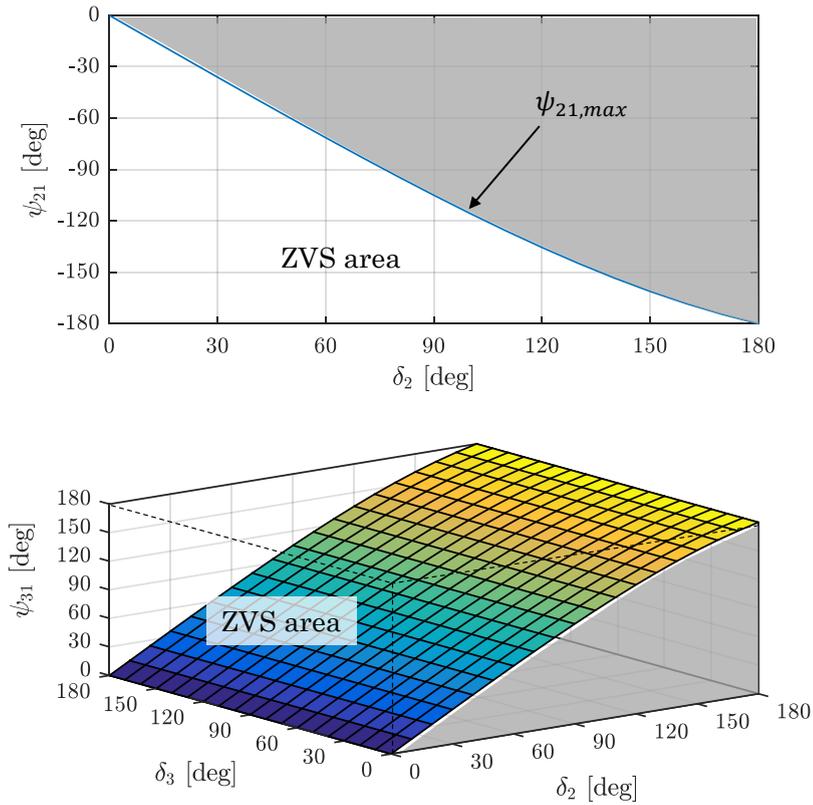
Figure 6.12. ZVS area in Mode 2B, $M_2 = M_3 = 1$.

for ψ_{31}. The modulation strategy of this mode is (6.23):

$$\begin{cases} \psi_{21} = \min \left\{ \Psi_{21,max}, \ \Psi_{31,max} - \Psi_{32,min} \right\} \\ \psi_{31} = \Psi_{31,max} \end{cases} \tag{6.23}$$

6.4   Closed-loop control consideration

The whole system diagram is illustrated in Fig. 6.13. A decoupled network is employed to detach the two control channels to individually manage the power flowing to port 2 and port 3. Two current controllers $G_{c2}(s)$ and $G_{c3}(s)$ are utilized to regulate the flows of power. Discussion on designing $G_{c2}(s)$, $G_{c3}(s)$ and the decoupled network are out of the scope of this chapter. They will be readdress in the future study.
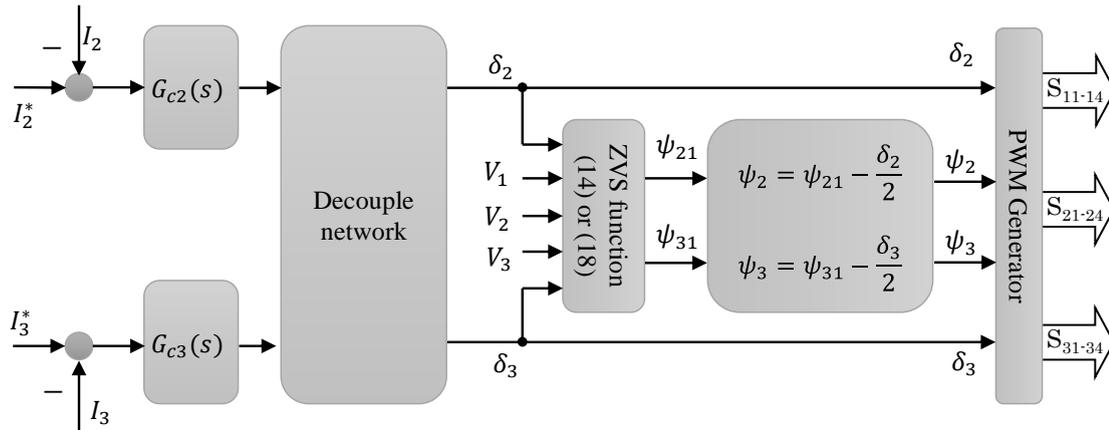
Figure 6.13. The proposed control system.

6.5   Simulation and experiment results

6.5.1   System description

Fig. 6.14(a) indicates the diagram of the prototype system. A picture of the system is shown in Fig. 6.14(b). Port 1 is connected to a programmable power supply set at constant voltage mode. Port 2 and 3 are connected to two DC electronic loads which are configured to operate under the constant voltage mode.
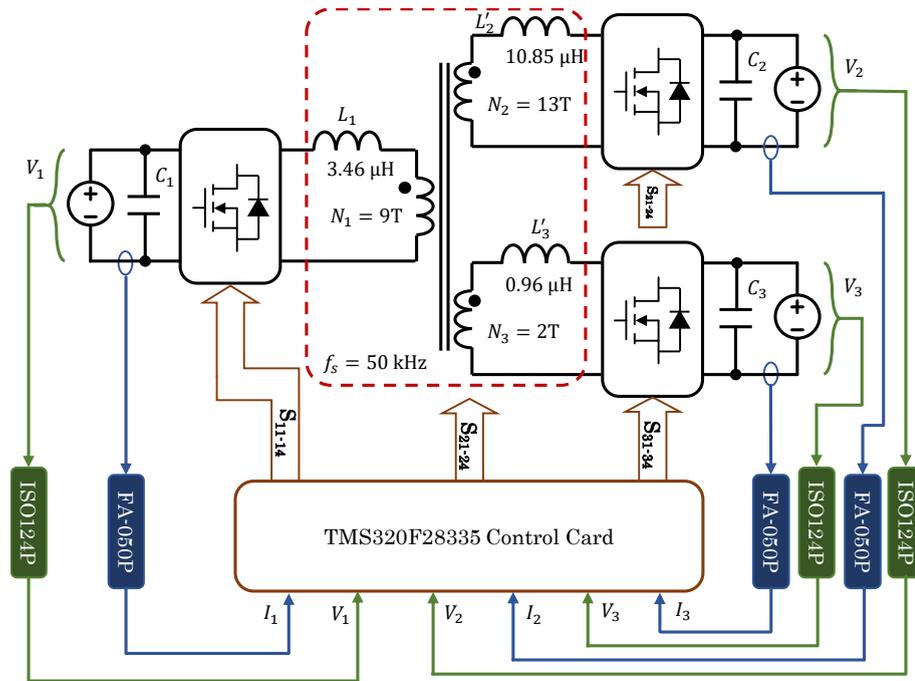
(a) Experiment system diagram.
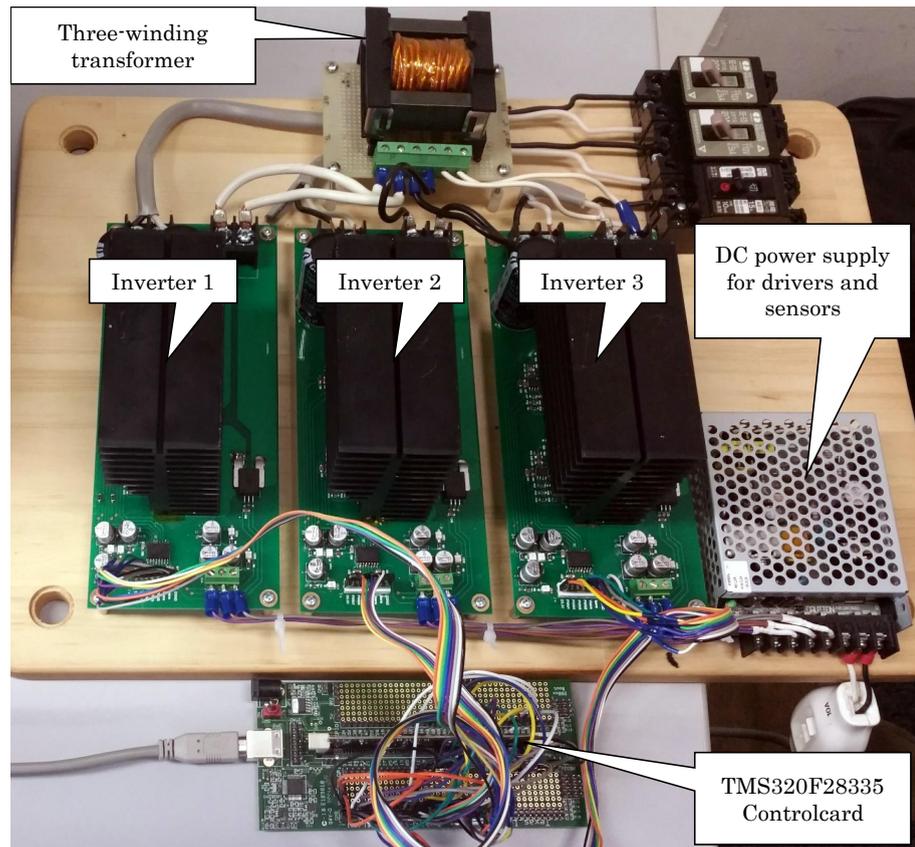
(b) Real system.

Figure 6.14. Laboratory-scaled experiment system.

TABLE 6.1: List of parameters of the TAB converter.

Parameter	Symbol	Value	Unit/Note
Pri. number of turns	N_1	9	Turns
Sec. 1 number of turns	N_2	13	Turns
Sec. 2 number of turns	N_3	2	Turns
Transformer core		ETD54	EPCOS
Pri. inductance	L_1	3.46	µH (@ 50 kHz)
Sec. 1 inductance	L_2'	10.85	µH (@ 50 kHz)
Sec. 2 inductance	L_3'	0.96	µH (@ 50 kHz)
MOSFETs	S_{11-14}	CSD19536KCS	Texas Instrument
	S_{21-24}	FCP104N60	Fairchild
	S_{31-34}	CSD19536KCS	Texas Instrument
Terminal 1 voltage	V_1	42	V
Terminal 2 voltage	V_2	60	V
Terminal 3 voltage	V_3	12	V
DC capacitor	C_1, C_2, C_3	2000	µF
Switching frequency	F_s	50	kHz
Dead-time	T_d	500	ns
Sampling frequency	F_z	50	kHz

Terminal voltages are detected by three on-board voltage sensors, ISO124P. A three-winding transformer is used to interface between all inverters. Number of turns of the primary and two secondary windings are 9T, 13T and 2T, respectively. All windings are wound by numerous of twisted AWG28 strands. The leakage inductance of each winding measured at 50 kHz are 3.46 µH, 10.85 µH and 0.96 µH, respectively. Referred to the primary side, the delta inductance are:

$$L_{12} = 9.5 \text{ µH}$$

$$L_{13} = 35.8 \text{ µH}$$

$$L_{23} = 53.3 \text{ µH}$$

Summary of the system parameters is given in the Table 6.1.

PWM signals are generated from a floating point DSP TMS320F28335 control card. The switching frequency and the sampling frequency are the same at 50 kHz. The dead-time between two MOSFETs in one leg is fixed at 500 ns for all inverters.

Because of the similarity of modes, only Mode 1B is examined in this section. The same verification procedures can be applied for other modes.

6.5.2 Simulation verification

In order to evaluate the accuracy of the analysis, a simulation study is carried out. Port voltages are set to 42 V, 60 V and 12 V, respectively. Consequently, the voltage ratio M_2 and M_3 are 1.0 and 1.3. The inner phase shift δ_3 is kept constant at 60 degrees. This will theoretically initialize an inter-port transmission between port 1 and 3 with $P_{13} \approx 100.8$ W according to (6.11). The other inner phase shift, δ_2, is then gradually increased with a step of 10 degrees until one port power changes its polarity. At each point, the bridge shift angles ψ_2 and ψ_3 are calculated based on (6.19) and (6.17). All other parameters are taken from Table 6.1. Simulation results are illustrated in Fig. 6.15.

Fig. 6.15(a) shows the active power characterization in Mode 1B. The continuous curves imply the calculated values whereas the dashed curves express the simulated ones. Different markers describe different port powers. Equations (6.10) were utilized for calculation. As shown, the calculated and the simulation curve pairs are close to each other in the whole investigated power range. The maximum error of about 43.6 W is recorded in the power characteristics of port 2. This is equivalent to 7.27% of the whole scale (600 W). The errors are insignificant between the calculated and the simulated powers of ports 1 and 3.

The accuracy of reactive powers estimation is evaluated by comparing the actual load angles and the calculated ones. The comparison is illustrated in Fig. 6.15(b). In simulation, the load angle is determined by measuring the lagged times of the winding currents with respect to the primary voltage $v_{w1}(t)$ then converting into phases. As shown, all load angles are well predicted by calculation as the simulated and the calculated values are asymptotic to each other. The maximum distinction is only 10.3 degrees. Over the scale of 360 degrees for one switching cycle, the gap is equivalent to 2.78%. From the two comparisons above, it can be concluded that the active and reactive powers estimated by (6.10) is reliable.
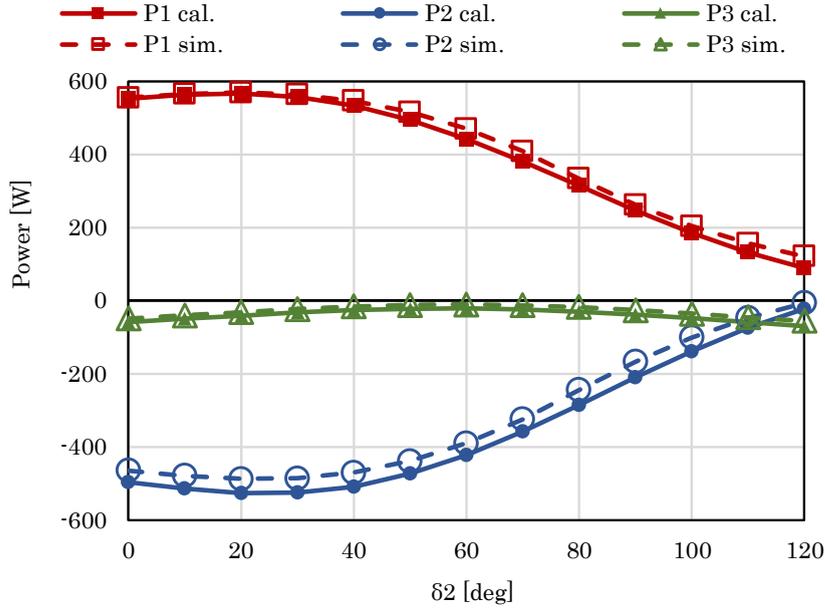
(a) Active power characterization.
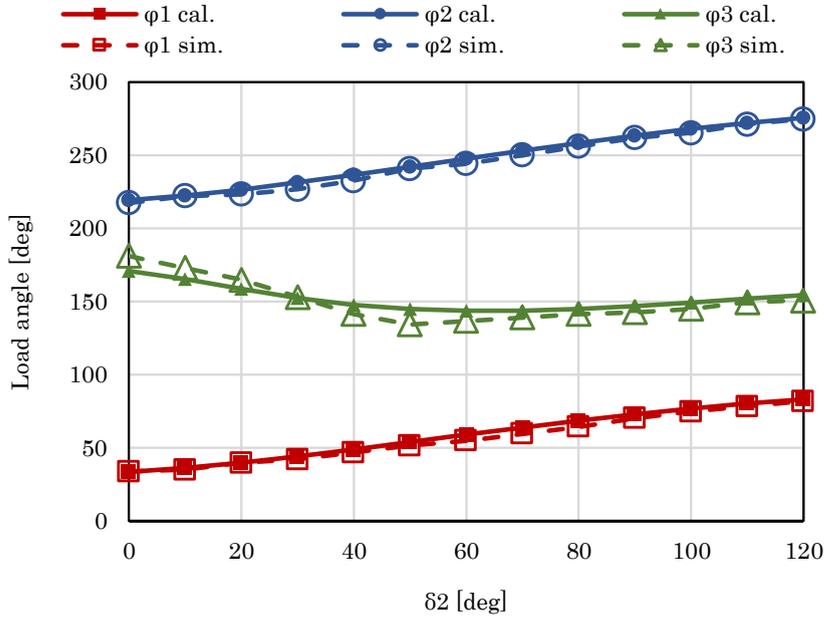
(b) Load angles characterization.

Figure 6.15. Simulation results in Mode 1B; $\delta_3 = 60$ deg; $\delta_2 = 0 \sim 120$ deg; ψ_2 and ψ_3 are derived by (6.19) and (6.17); $V_1 = 42$ V, $V_2 = 60$ V and $V_3 = 12$ V.

In term of ZVS behavior, obviously, φ_1 is positive, thus inverter 1 is ZVS. As for inverters 2 and 3, the corresponding load angles are put in the correlation with the ZVS limitation according to the condition (6.12) as presented in Fig. 6.16. The ZVS boundaries sketched in Fig. 6.16(a) and Fig. 6.16(b) are shifted by the relative bridge shift angles to match with the load angles obtained above. In those

(a) ZVS area of inverter 2.

(b) ZVS area of inverter 3.
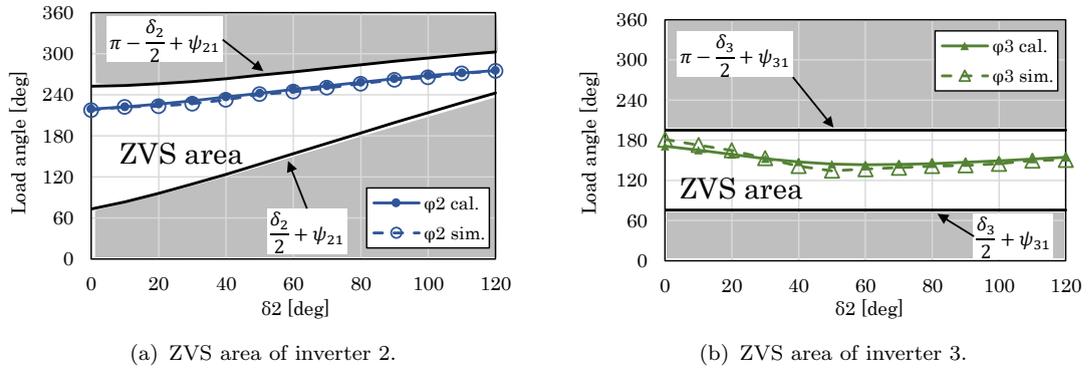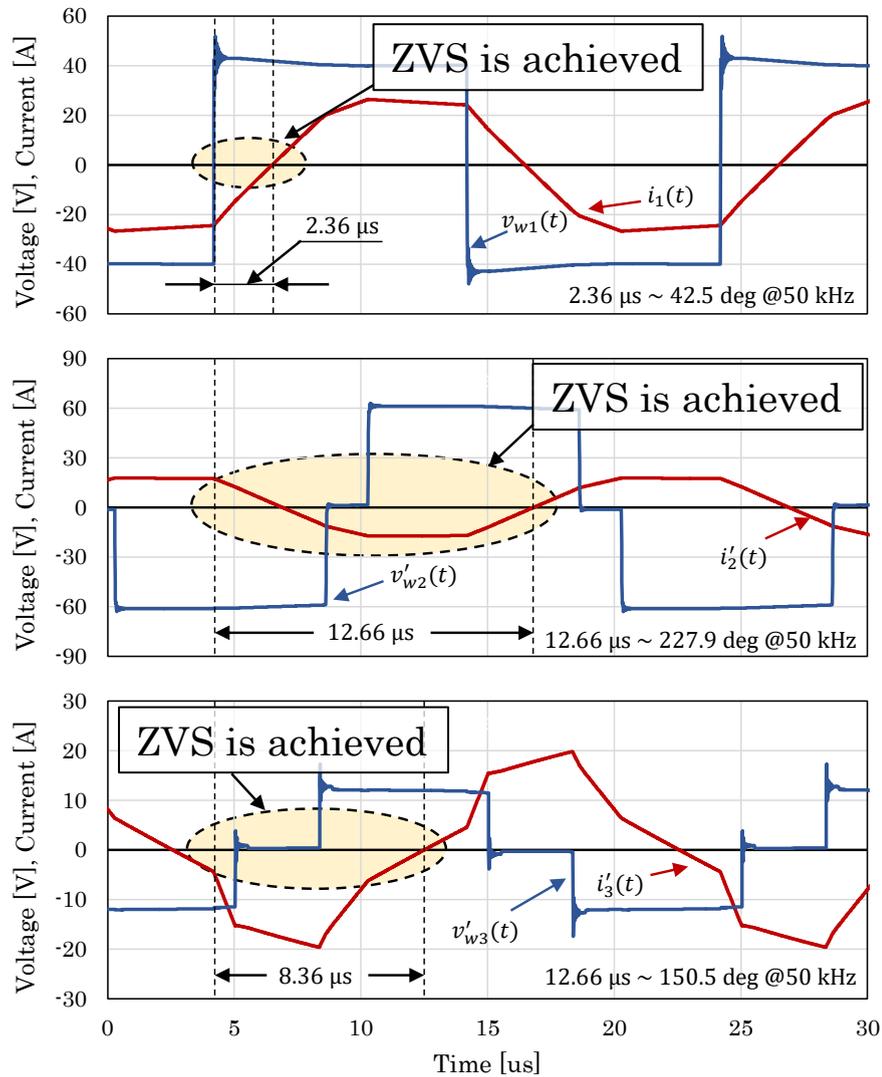
Figure 6.16. ZVS area in Mode 1B.

Figure 6.17. Simulation waveform in Mode 1B; $\delta_2 = 30$ deg, $\delta_3 = 60$ deg, $\psi_2 = 79.7$ deg, $\psi_3 = 15.35$ deg, $V_1 = 42$ V, $V_2 = 60$ V and $V_3 = 12$ V.

figures, the non-shaded areas indicate the ZVS regions of the respective inverters. As shown, the φ_2 and φ_3 trajectories are located inside the ZVS areas. Therefore, ZVS achievement of all inverters in Mode 1B is confirmed.

Fig. 6.17 describes the voltage and current waveforms when $\delta_2 = 30$ degrees and $\delta_3 = 60$ degrees. Using (6.19) and (6.17), ψ_2 and ψ_3 are derived as 79.7 and 15.35 degrees, respectively. The lagged times of winding currents with respect to $v_{w1}(t)$ are 2.36 μs, 12.66 μs and 8.36 μs. At 50 kHz, those lagged times are equivalent to 42.5, 227.9 and 150.5 degrees, respectively. Under the same condition, the predicted angles obtained from calculation are 44.2, 231.3 and 152.5, respectively. Once again, the accuracy in the estimation as well as the ZVS attainment is validated.

6.5.3   Experiment verification

Fig. 6.18 demonstrates the experimental switching characteristic of the converter when using the proposed modulation strategy to send a 150 W active power from port 1. The winding currents are indicated as red curves, meanwhile the drain-to-source voltages of the low side transistor (S_{14}, S_{24} and S_{34}) are shown as blue curves. Notes that, the drain-to-source voltage $v_{ds(S_{14})}(t)$ is also the positive portion of the AC winding voltage $v_{w1}(t)$. The terminal voltages are: 50 V, 72.8 V and 11.15 V, respectively. Thus, the voltage ratio M_2 and M_3 are equal to unity. The inner phase shifts δ_2 and δ_3 are 0 and 7.5 degrees, respectively. The outer phase shift ψ_2 is 10.6 degrees and ψ_3 is 5.3 degrees. Expectingly, the load angles are 2.3, 182.3 and 182.3 degrees, respectively.

The lagged times measured in the experiment are 0.306 μs, 10.25 μs and 10.25 μs for the corresponding winding currents with respect to the rising edge of $v_{ds(S_{14})}(t)$. At 50 kHz, correspondingly, they are equivalent to 5.51 degrees, 184.5 degrees and 184.5 degrees. Comparing with the theoretical values, the errors are 3.21, 2.2 and 2.2 degrees, respectively. Since the errors are insignificant, the precision of the estimation method is verified.
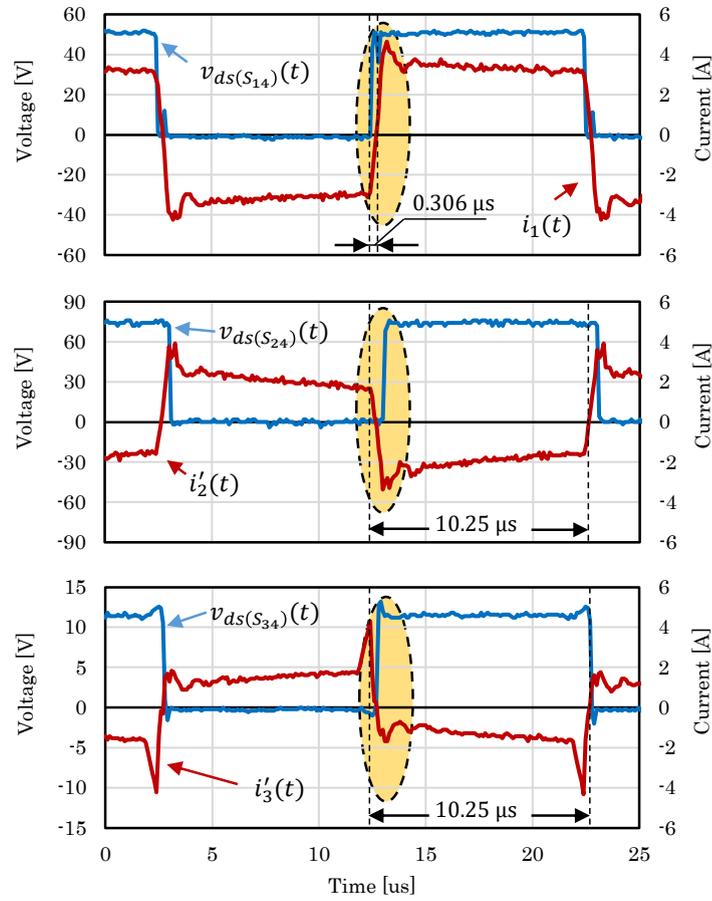
Figure 6.18. Voltage and current waveforms when sending 150 W from port 1; $V_1 = 50$ V, $V_2 = 72.8$ V, $V_3 = 11.15$ V, $\delta_2 = 0$ deg, $\delta_3 = 7.5$ deg; by using (6.18) and (6.17), the bridge shift angles can be calculated as $\psi_2 = 10.6$ deg and $\psi_3 = 5.3$ deg; the measured efficiency is 95.02%.
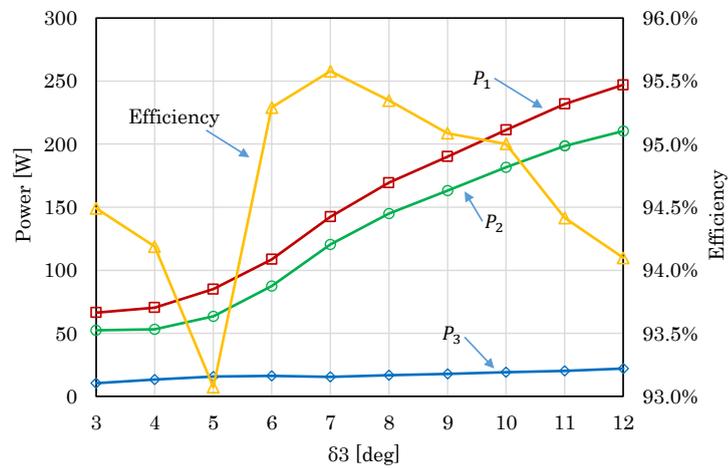
Figure 6.19. Experimental power characterization and efficiency; $\delta_2 = 0$ degrees; $V_1 = 50$ V, $V_2 = 72.8$ V and $V_3 = 11.15$ V; the maximum efficiency is 95.58%; the minimum efficiency is 93.07%; the average efficiency is 94.66%.

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The turn-on activity of transistor is highlighted in the shaded areas. Because the transition currents are negative in all instances, ZVS is achieved for all transistors. Moreover, as $\delta_2 = 0$ degrees, $\delta_3 = 7.5$ degrees, $\psi_2 = 10.6$ and $\psi_3 = 5.3$ degrees ($\psi_{21} = 10.6$ and $\psi_{31} = 9.05$); φ_1 must be positive, φ_2 must be in [10.6, 190.6], and φ_3 must be in [12.8, 185.3] for ZVS of all inverters. Since $\varphi_1 = 5.51$ degrees, $\varphi_2 = \varphi_3 = 184.5$ degrees, the condition is satisfied. Besides, it can be observed that the values of φ_1, φ_2 and φ_3 are very close to their corresponding ZVS limitation. That means, the depth of ZVS is small. Consequently, the overall efficiency in this circumstance is 95.02%.

Fig. 6.19 shows the experimental power characterization and the overall efficiency (i.e. the ratio between the sum of P_2 and P_3 over P_1) when $M_2 = M_3 = 1$ and $\delta_2 = 0$ degrees. The inner phase shift δ_3 is increased with the step of 1 degree. Consequently, P_1, P_2 and P_3 rise gradually. The maximum efficiency of 95.58% is recorded when $\delta_3 = 7$ degrees, $P_1 = 142.3$ W, $P_2 = 120.5$ W and $P_3 = 15.6$ W. In the investigated power range, the average efficiency is 94.66%.

6.6 Conclusion

This chapter proposed a new soft-switching technique for three-port bidirectional DC/DC converter. Unlikes other published modulation method for such converter, the bridge shift angles in this chapter were used for achieving ZVS. Two inner phase shift angles are introduced to manipulate the transmission power. The analysis was based on the fundamental harmonic approximation, therefore, the difficulty due to numerous of switching states was avoided.

Simulation study has confirmed that the analysis method was reasonable as it can ensure the maximum estimation error of 7.27% between the calculated and the simulated active power over the scale of 600 W. Consequently, the ZVS behavior was well predicted and achieved by the proposed modulation strategy for operating in Mode 1B.

As confirmed by the experiment results, by using the proposed modulation strategy, ZVS can be achieved for all transistors regardless of the switching state. The depth of ZVS was small as the load angles are closed to the soft-switching boundaries. As a result, the maximum efficiency of 95.58% was recorded. Furthermore, in the examined power range, the proposed modulation method can ensure the average efficiency of 94.66%.

However, though having totally four operation modes, only one Mode 1B was validated in this chapter. Nevertheless, the same analysis method can be applied for other transmission modes. Besides, a closed-loop control system to realize the proposed modulation method was not designed in this chapter. It will be readdressed in the future studies.

Chapter 7

Conclusion and Future Work

7.1   Conclusions

This dissertation presented about modulation and dynamic control for Dual-Active-Bridge (DAB) and Triple-Active-Bridge (TAB) bidirectional DC/DC converters which are classified as DC-to-DC typed Solid-State-Transformers. Five topics have been discussed: modulation and control for a DAB converter in the time and frequency domains; and applying the proposed approaches to analyze a TAB converter in the frequency domain then control it in the time domain.

Major contributions of this dissertation include:

(1) A new strategy named MFPS was proposed in Chapter 2 for modulating DAB converters:

   – Soft-switching area as well as the coverable power range were extended,

   – Efficiency was improved in the medium and high power range

   – Maximum efficiency improvement was 7%

   – By choosing an appropriate high limitation for the switching frequency, high efficiency can be maintained in wide range, even in the low power condition.

② A control system to realized the proposed MFPS was designed in Chapter 3:

- Terminal 2 voltage was well regulated as the fluctuation was from -15.6% to 11%

- Low frequency harmonics reflected from AC side can be suppressed

- When overloading, the converter can operate like a constant current source

- The control system can detect the short-circuit fault in 1.2 ms then protect the system by forcing a shutdown

③ A linear observer was designed in Chapter 4 to estimate the direct and the quadrature components of the transmission current:

- A toroidal core current sensor was used instead of the expensive Hall-effect transducer to measure the current, thus, the cost can be reduced.

- In spite of feeding-back an AC signal, the sampling speed was just comparable to the switching frequency. That allows to use mid-range popular DSP in such application.

- At the designated voltage ratio, the observer worked well as the observation error was less than 5 degrees (1.4% of a switching cycle).

- The maximum observer error was 13 degrees, equivalent to 3.6% of a switching cycle. If sampling frequency can be increased, the error can be even lower.

④ An observer-based control system was developed in Chapter 5:

- The current modeling was more accurate as high overshoot and oscillation were nearly eliminated in the current response.

- Dynamic performance of the current loop was much improved as the current overshoot was suppressed from 96% to only 20%. Therefore, wrong protection due to current overshooting is avoided.

– The load angle minimization objective was accomplished by reference assignment of the two current loops.

– A load regulation of -14% to 15% was achieved by the control system, which is almost the same as obtained by the control system in Chapter 3. Further improvement can be attained by carefully tuning the parameters of the controllers.

– Similar to the control system designed in Chapter 3, the observer-based control system can also behave as a current source when overloading.

– The short-circuit fault detection time was 2.4 times shorten for better protection of the converter.

⑤ A new modulation technique named QPS was proposed for TAB converters in automotive applications in Chapter 6:

– Soft-switching was achievable in all transmission modes

– Modulation functions are independent from the switching states

– The maximum efficiency recorded in experiments was 95.58%

– The average efficiency in the examined power range is 94.66%

7.2 Future works

There are still some issues that need further studies to accomplish, such as:

① Although the proposed MFPS in Chapter 2 can extend the soft-switching area to the light load range, it cannot perform the same characteristic in the ultra-low or no load conditions due to the limitation in the switching capability of transistors. This issue can be solved by combining the MFPS method with, for example, the burst mode modulation scheme [55].

② In the MFPS method, the depth of soft-switching was set equally to the dead-time. However, the transition time of transistor is usually less than

the dead-time. Hence, if adaptive dead-time can be considered to further minimized the soft-switching depth.

③ The observer model was obtained by linearizing around one operating point. Therefore, away from such point, the accuracy of the estimation was downgraded. This can be solved by employing nonlinear observer as reported in [P.6]. Reduced-order configuration can also be considered to lessen the calculation amount as presented in [P.5].

④ The performance of the observer also depended on the current waveform. As it is more asymmetric (small phase shift, terminal voltage are not matched), the phase drift between the fundamental and the actual current becomes more significant. Hence, the observation error appeared to increase. However, the phase drift effect was not compensated in this study.

⑤ The interaction between the direct and the quadrature currents was not completely eliminated and might lead to the lost of soft-switching in the transient state. There are two possible methods to solve this issue:

– Increasing the depth of soft-switching to reserve for the observer error, the fluctuation in the response and for the interaction between control channels.

– The decoupled technique used in this dissertation was the static type. Hence, employing an advanced scheme such as dynamic decoupled method might help improve the decoupling performance.

⑥ The soft-switching proposed in Chapter 6 was not the optimal. The soft-switching condition equations were not completely solved due to their complexity. Consequently, the depth of soft-switching was not completely manageable.

⑦ Although the same evaluation procedures can be applied for other operation modes, only one mode was examined. Besides, mode selection mechanism was also not discussed in Chapter 6.

⑧ The design of the control system to realize the proposed QPS modulation strategy was not discussed in 6. Since the QPS scheme was based on FHA method, the same observer-based control algorithm as presented in Chapter 5 can be applied. If the simplicity of implementation is higher priority, the control structure based on steady state relations as introduced in Chapter 2 is also a considerable choice.

References

[1] T. Kubo, H. Sachs, and S. Nadel, "Opportunities for new appliance and equipment efficiency standards: Energy and economic savings beyond current standards programs," in *New Appliance and Equipment Efficiency Standards, ACEEE*. American Council for an Energy-Efficient Economy, 2001.

[2] M. William, "Power converter circuits having a high frequency link," Jun. 23 1970, uS Patent 3,517,300.

[3] X. She, R. Burgos, G. Wang, F. Wang, and A. Q. Huang, "Review of solid state transformer in the distribution system: From components to field application," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*. IEEE, 2012, pp. 4077–4084.

[4] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[5] J. Kolar and J. Huber, "Solid-state transformers-key design challenges applicability and future concepts," in *8th Int. Power Electron. and Motion Control Conf., Hefei, China*, 2016.

[6] G. T. Heydt, "The next generation of power distribution systems," *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 225–235, 2010.

[7] Z. Qian, O. Abdel-Rahman, and I. Batarseh, "An integrated four-port dc/dc converter for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1877–1887, 2010.

REFERENCES

[8] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system," *IEEE Trans. Power. Electron.*, vol. 29, no. 8, pp. 4091–4106, 2014.

[9] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. Hendrix, "Family of multiport bidirectional dc–dc converters," *IEE Proceedings-Electric Power Applications*, vol. 153, no. 3, pp. 451–458, 2006.

[10] J. W. Kolar and G. Ortiz, "Solid-state-transformers: key components of future traction and smart grid systems," in *Proceedings of the International Power Electronics Conference-ECCE Asia (IPEC 2014)*, 2014, pp. 18–21.

[11] H. Fan and H. Li, "High-frequency transformer isolated bidirectional dc–dc converter modules with high efficiency over wide load range for 20 kva solid-state transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3599–3608, 2011.

[12] X. She, A. Q. Huang, S. Lukic, and M. E. Baran, "On integration of solid-state transformer with zonal dc microgrid," *IEEE Trans. on Smart Grid*, vol. 3, no. 2, pp. 975–985, 2012.

[13] W. Jiang and B. Fahimi, "Multiport power electronic interface-concept, modeling, and design," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1890–1900, 2011.

[14] X. Yu, X. She, X. Zhou, and A. Q. Huang, "Power management for dc microgrid enabled by solid-state transformer," *IEEE Trans. on Smart Grid*, vol. 5, no. 2, pp. 954–965, 2014.

[15] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, 2015.

[16] D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic, "Gan-fet based dual active bridge dc-dc converter," in *Applied Power Electronics Conference and*

Exposition (APEC), 2011 Twenty-Sixth Annual IEEE. IEEE, 2011, pp. 1425–1432.

[17] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional dc-dc converter with decoupled power flow management," *IEEE Trans. Power. Electron.*, vol. 23, no. 5, pp. 2443–2453, 2008.

[18] H. Tao, J. L. Duarte, and M. A. Hendrix, "Three-port triple-half-bridge bidirectional converter with zero-voltage switching," *IEEE Trans. Power. Electron.*, vol. 23, no. 2, pp. 782–792, 2008.

[19] J. L. Duarte, M. Hendrix, and M. G. Simões, "Three-port bidirectional converter for hybrid fuel cell systems," *IEEE Trans. Power. Electron.*, vol. 22, no. 2, pp. 480–487, 2007.

[20] Y. Xu, J. Zhang, W. Wang, A. Juneja, and S. Bhattacharya, "Energy router: Architectures and functionalities toward energy internet," in *Smart Grid Communications (SmartGridComm), 2011 IEEE International Conference on.* IEEE, 2011, pp. 31–36.

[21] J. Zhang, W. Wang, and S. Bhattacharya, "Architecture of solid state transformer-based energy router and models of energy traffic," in *Innovative Smart Grid Technologies (ISGT), 2012 IEEE PES.* IEEE, 2012, pp. 1–8.

[22] A. Q. Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, "The future renewable electric energy delivery and management (freedm) system: the energy internet," *Proceedings of the IEEE*, vol. 99, no. 1, pp. 133–148, 2011.

[23] A. Maitra, A. Sundaram, M. Gandhi, S. Bird, and S. Doss, "Intelligent universal transformer design and applications," in *Electricity Distribution-Part 1, 2009. CIRED 2009. 20th International Conference and Exhibition on.* IET, 2009, pp. 1–7.

[24] D. Boroyevich, I. Cvetković, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems a contemplative view," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on.* IEEE, 2010, pp. 1369–1380.

[25] D. Dujic, F. Kieferndorf, F. Canales, and U. Drofenik, "Power electronic traction transformer technology," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 1. IEEE, 2012, pp. 636–642.

[26] P. Lundberg, M. Callavik, M. Bahrman, and P. Sandeberg, "Platforms for change: High-voltage dc converters and cable technologies for offshore renewable integration and dc grid expansions," *IEEE Power and Energy Magazine*, vol. 10, no. 6, pp. 30–38, 2012.

[27] H. D. Kim, J. L. Felder, M. T. Tong, and M. Armstrong, "Revolutionary aeropropulsion concept for sustainable aviation: turbo-electric distributed propulsion," 2013.

[28] D. Jovcic, "Bidirectional, high-power dc transformer," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 2276–2283, 2009.

[29] B. Zhao, Q. Song, J. Li, X. Xu, and W. Liu, "Comparative analysis of multilevel-high-frequency-link and multilevel-dc-link dc-dc transformers based on mmc and dual-active-bridge for mvdc application," *IEEE Transactions on Power Electronics*, 2017.

[30] N. Hugo, P. Stefanutti, M. Pellerin, and A. Akdag, "Power electronics traction transformer," in *Power Electronics and Applications, 2007 European Conference on.* IEEE, 2007, pp. 1–10.

[31] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, 1991.

[32] M. Bragard, N. Soltau, S. Thomas, and R. W. De Doncker, "The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems," *IEEE Trans. Power. Electron.*, vol. 25, no. 12, pp. 3049–3056, 2010.

[33] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge," *IEEE Trans. Power. Electron.*, vol. 24, no. 12, pp. 2756–2768, 2009.

[34] R. Naayagi, A. J. Forsyth, and R. Shuttleworth, "High-power bidirectional dc–dc converter for aerospace applications," *IEEE Trans. Power. Electron.*, vol. 27, no. 11, pp. 4366–4379, 2012.

[35] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Trans. Power. Electron.*, vol. 28, no. 8, pp. 3931–3940, 2013.

[36] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual h-bridge-based isolated bidirectional dc–dc converter," *IET Power Electron.*, vol. 1, no. 4, pp. 507–517, 2008.

[37] S. Inoue and H. Akagi, "A bidirectional dc–dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power. Electron.*, vol. 22, no. 6, pp. 2299–2306, 2007.

[38] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power. Electron.*, vol. 24, no. 7, pp. 1826–1838, 2009.

[39] G. G. Oggier, R. Ledhold, G. O. García, A. R. Oliva, J. C. Balda, and F. Barlow, "Extending the zvs operating range of dual active bridge high-power dc-dc converters," in *Power Electronics Specialists Conference*, 2006, pp. 1–7.

[40] G. Oggier, G. O. García, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc–dc converter under soft switching in the whole operating range," *IEEE Trans. Power. Electron.*, vol. 26, no. 4, pp. 1228–1236, 2011.

[41] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc–dc converters using novel dual-phase-shift control," *IEEE Trans. Power. Electron.*, vol. 23, no. 6, pp. 2905–2914, 2008.

[42] H. Bai, Z. Nie, and C. C. Mi, "Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional dc–dc converters," *IEEE Trans. Power. Electron.*, vol. 25, no. 6, pp. 1444–1449, 2010.

[43] B. Zhao, Q. Song, and W. Liu, "Power characterization of isolated bidirectional dual-active-bridge dc–dc converter with dual-phase-shift control," *IEEE Trans. Power. Electron.*, vol. 27, no. 9, pp. 4172–4176, 2012.

[44] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional dc–dc converter with dual-phase-shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, 2013.

[45] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional dc–dc converter based on dual-phase-shift control for dc distribution application," *IEEE Trans. Power. Electron.*, vol. 28, no. 4, pp. 1711–1727, 2013.

[46] F. Krismer and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, 2012.

[47] ——, "Closed form solution for minimum conduction loss modulation of dab converters," *IEEE Trans. Power. Electron.*, vol. 27, no. 1, pp. 174–188, 2012.

[48] K. Wu, C. W. de Silva, and W. G. Dunford, "Stability analysis of isolated bidirectional dual active full-bridge dc–dc converter with triple phase-shift control," *IEEE Trans. Power. Electron.*, vol. 27, no. 4, pp. 2007–2017, 2012.

[49] A. K. Jain and R. Ayyanar, "Pwm control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power. Electron.*, vol. 26, no. 4, pp. 1215–1227, 2011.

[50] L. Corradini, D. Seltzer, D. Bloomquist, R. Zane, D. Maksimović, and B. Jacobson, "Minimum current operation of bidirectional dual-bridge series resonant dc/dc converters," *IEEE Trans. Power. Electron.*, vol. 27, no. 7, pp. 3266–3276, 2012.

[51] W. Choi, K.-M. Rho, and B.-H. Cho, "Fundamental duty modulation of dual-active-bridge converter for wide-range operation," *IEEE Trans. Power. Electron.*, vol. 31, no. 6, pp. 4048–4064, 2016.

[52] M. K. Kazimierczuk and D. Czarkowski, *Resonant power converters.* John Wiley & Sons, 2012.

[53] J. Hiltunen, V. Väisänen, R. Juntunen, and P. Silventoinen, "Variable-frequency phase shift modulation of a dual active bridge converter," *IEEE Trans. Power. Electron.*, vol. 30, no. 12, pp. 7138–7148, 2015.

[54] X.-F. He, Z. Zhang, Y.-Y. Cai, and Y.-F. Liu, "A variable switching frequency hybrid control for zvs dual active bridge converters to achieve high efficiency in wide load range," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE.* IEEE, 2014, pp. 1095–1099.

[55] G. G. Oggier and M. Ordonez, "High-efficiency dab converter using switching sequences and burst mode," *IEEE Trans. Power. Electron.*, vol. 31, no. 3, pp. 2069–2082, 2016.

[56] H. Qin and J. W. Kimball, "Closed-loop control of dc–dc dual-active-bridge converters driving single-phase inverters," *IEEE Trans. Power. Electron.*, vol. 29, no. 2, pp. 1006–1017, 2014.

REFERENCES

[57] D. Segaran, B. McGrath, and D. Holmes, "Adaptive dynamic control of a bi-directional dc-dc converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE.* IEEE, 2010, pp. 1442–1449.

[58] D. Segaran, D. G. Holmes, and B. P. McGrath, "Enhanced load step response for a bidirectional dc–dc converter," *IEEE Trans. Power. Electron.*, vol. 28, no. 1, pp. 371–379, 2013.

[59] S. Dutta, S. Hazra, and S. Bhattacharya, "A digital predictive current-mode controller for a single-phase high-frequency transformer-isolated dual-active bridge dc-to-dc converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5943–5952, 2016.

[60] S. P. Engel, N. Soltau, H. Stagge, and R. W. De Doncker, "Dynamic and balanced control of three-phase high-power dual-active bridge dc–dc converters in dc-grid applications," *IEEE Trans. Power. Electron.*, vol. 28, no. 4, pp. 1880–1889, 2013.

[61] ——, "Improved instantaneous current control for high-power three-phase dual-active bridge dc–dc converters," *IEEE Trans. Power. Electron.*, vol. 29, no. 8, pp. 4067–4077, 2014.

[62] B. Zhao, Q. Song, W. Liu, G. Liu, and Y. Zhao, "Universal high-frequency-link characterization and practical fundamental-optimal strategy for dual-active-bridge dc-dc converter under pwm plus phase-shift control," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6488–6494, 2015.

[63] A. K. Tripathi, K. Mainali, D. C. Patel, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Design considerations of a 15-kv sic igbt-based medium-voltage high-frequency isolated dc–dc converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3284–3294, 2015.

[64] M. Ciobotaru, R. Teodorescu, F. Blaabjerg *et al.*, "A new single-phase pll structure based on second order generalized integrator," in *Power Electronics Specialists Conference*, 2006, pp. 1–6.

[65] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high-frequency isolated bidirectional full-bridge dc–dc converter: Comprehensive theoretical analysis and experimental verification," *IEEE Trans. Power. Electron.*, vol. 29, no. 4, pp. 1667–1680, 2014.

[66] D. Costinett, R. Zane, and D. Maksimovic, "Automatic voltage and dead time control for efficiency optimization in a dual active bridge converter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*. IEEE, 2012, pp. 1104–1111.

[67] J. Li, Z. Chen, Z. Shen, P. Mattavelli, J. Liu, and D. Boroyevich, "An adaptive dead-time control scheme for high-switching-frequency dual-active-bridge converter," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012, pp. 1355–1361.

[68] Y. Xie, J. Sun, and J. S. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power dc/dc converter over a wide operating range," *IEEE Trans. Power. Electron.*, vol. 25, no. 1, pp. 54–66, 2010.

[69] M. K. Kazimierczuk, *High-frequency magnetic components*. John Wiley & Sons, 2009.

[70] C. W. T. McLyman, *Transformer and inductor design handbook*. CRC press, 2016.

[71] G. F. Franklin, J. D. Powell, and M. L. Workman, *Digital control of dynamic systems*. Addison-wesley Menlo Park, 1998, vol. 3.

[72] A. F. Burke, "Batteries and ultracapacitors for electric, hybrid, and fuel cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp. 806–820, 2007.

[73] J. Bauman and M. Kazerani, "A comparative study of fuel-cell–battery, fuel-cell–ultracapacitor, and fuel-cell–battery–ultracapacitor vehicles," *IEEE Trans. Veh. Technol.*, vol. 57, no. 2, pp. 760–769, 2008.

REFERENCES

[74] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: State of the art," *IEEE Trans. Veh. Technol.*, vol. 59, no. 6, pp. 2806–2814, 2010.

[75] J. Neubert, "Powering up," *IEE Review*, vol. 46, no. 5, pp. 21–25, 2000.

[76] K. Rajashekara, "42 v architecture for automobiles," in *Electrical Insulation Conference and Electrical Manufacturing & Coil Winding Technology Conference, 2003. Proceedings.* IEEE, 2003, pp. 431–434.

[77] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. Hendrix, "Transformer-coupled multiport zvs bidirectional dc–dc converter with wide input range," *IEEE Trans. Power. Electron.*, vol. 23, no. 2, pp. 771–781, 2008.

[78] A. Ajami and P. A. Shayan, "Soft switching method for multiport dc/dc converters applicable in grid connected clean energy sources," *IET Power Electron.*, vol. 8, no. 7, pp. 1246–1254, 2015.

[79] S. Y. Kim, H.-S. Song, and K. Nam, "Idling port isolation control of three-port bidirectional converter for evs," *IEEE Trans. Power. Electron.*, vol. 27, no. 5, pp. 2495–2506, 2012.

[80] M. Phattanasak, R. Gavagsaz-Ghoachani, J.-P. Martin, B. Nahid-Mobarakeh, S. Pierfederici, and B. Davat, "Control of a hybrid energy source comprising a fuel cell and two storage devices using isolated three-port bidirectional dc–dc converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 491–497, 2015.

List of Publications

Accepted journals:

[P.1] N.D. Dinh, N.D. Tuyen, and G. Fujita, "New modulation strategy combining phase shift and frequency variation for Dual-Active-Bridge converters," *IEEJ Journal on Industry Application*, Vol. 6, No. 2, pp. 140-150, 2017.

[P.2] N.D. Dinh, N.D. Tuyen, and G. Fujita, "An observer-based digital control system for individually management of active and reactive power of Dual-Active-Bridge converter," *Journal of International Council on Electrical Engineering (JICEE)*, Vol. 7, No. 1, pp. 234-241, 2017.

[P.3] N.D. Dinh, N.D. Tuyen, G. Fujita, and T. Funabashi, "Adaptive notch filter solution under unbalanced and/or distorted point of common coupling voltage for three-phase four-wire shunt active power filter with sinusoidal utility current strategy," *IET Gener. Transm. Distrib.*, Vol. 9, No. 13, pp. 1580-1596, Jan. 2015.

International conferences (first author):

[P.4] N.D. Dinh, G. Fujita, and M.C. Ta, "A new soft-switching strategy for three-port converter to be applied in EV application," *International Future Energy Electronics Conference 2017 (IFEEC-ECCE Asia)*, Kaohsiung, Taiwan, Jun. 2017.

[P.5] N.D. Dinh, G. Fujita, Q. Bui-Dang and M.C Ta, "A reduced-order observer-based control system designed in the frequency domain for Dual-Active-Bridge converter," *2016 4th IEEE International Conference on Sustainable Energy Technologies (ICSET)*, Hanoi, Vietnam, Nov. 2016.

[P.6] N.D. Dinh, N.M. Linh, N.D Tuyen, and G. Fujita, "Observer-based nonlinear control for frequency modulated Dual-Active-Bridge converter," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, United States, Sep. 2016.

[P.7] N.D. Dinh, G. Fujita, and N.D. Tuyen "An observer-based digital control system for individually management of active and reactive power of Dual-Active-Bridge converter," *2016 International Conference on Electrical Engineering (ICEE)*, Okinawa, Japan, Jul. 2016.

[P.8] N.D. Dinh, and G. Fujita, "Observer-based decoupling power control for frequency modulated Dual-Active-Bridge converter," *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, China, pp. 754-760, May 2016.

[P.9] N.D. Dinh, and G. Fujita, "Direct power control for Dual-Active-Bridge converter," *2016 10th South East ASIAN Technical University Consortium Symposium (SEATUC)*, Tokyo, Japan, Feb. 2016.

[P.10] N.D. Dinh, G. Fujita, and M.C. Ta "New Enhanced-Phase-Shift modulation strategy of semi Dual-Active-Bridge Converter for EV application," *2015 3rd Vietnam Conference on Control and Automation (VCCA)*, Thai Nguyen, Vietnam, Nov. 2015.

[P.11] N.D. Dinh, N.D Tuyen, G. Fujita, and T. Funabashi "Dual-active-bridge series resonant converter: A new control strategy using phase-shifting combined frequency modulation," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, pp. 1215-1222, Sep. 2015.

[P.12] N.D. Dinh, N.D Tuyen, G. Fujita, M.N.B. Muhtazaruddin, "Investigation of ZVS condition for dual-active-bridge converter using dual-phase-shift modulation," *2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Hong Kong, China, Dec. 2014.

[P.13] N.D. Dinh, and M.C. Ta, "New direct torque control scheme for BLDC motor drives suitable for EV applications," *2014 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Coimbra, Portugal, Oct. 2014.

International conferences (co-author):

[P.14] Y. Nishiya, N.D. Dinh, and G. Fujita, "Comparison of two level PWM and three level PWM in Dual Active Bridge converter," *2016 4th IEEE International Conference on Sustainable Energy Technologies (ICSET)*, Hanoi, Vietnam, Nov. 2016.

[P.15] K.P. Nguyen, N.D. Dinh, and G. Fujita "Multi-area economic dispatch using Hybrid Cuckoo search algorithm," *2015 50th International Universities Power Engineering Conference (UPEC)*, United Kingdom, Sep. 2015.

[P.16] N.D Tuyen, N.D. Dinh, G. Fujita, and T. Funabashi "Applying adaptive notch filter in -coordinate to improve 3-phase 4-wire shunt APF performance under non-ideal PCC voltage," *2015 IEEE Power and Energy Society General Meeting (PESGM)*, Denver, United States, pp. 323-328, Jul. 2015.