13.56 MHz high power and high efficiency inverter for dynamic EV charging systems

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To my Family:

My parents: Nguyen Huu On and Nguyen Thi Nga

My wife: Duong Thi Thanh

My sons:Nguyen Minh Chau and Nguyen Minh Khanh.

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Nguyen Kien Trung

Abstract

Recently, Electric Vehicles (EVs) are a promising solution for reducing CO_2 emission and air pollution in the big cities. However, until now, the EVs have been not so attractive to consumers due to the short running distance, long charging time and high battery cost. The dynamic charging solution has been proposed to reduce the energy dependence and battery cost of EVs. As the demand of that systems, a 13.56 MHz high power inverter with the efficiency of over 95% is required. With the previous researches, there are three major research challenges have been recorded. At very high switching frequency such as 13.56 MHz, the influence of the parasitic elements in the circuit is the first challenge because it strongly affect both of power and drive circuit of the inverter. Consequently, the inverter may be damaged or unstable. Secondly, the switching and gate drive power loss in the inverter are also the challenge when it proportionally increase with the switching frequency. At 13.56 MHz, it is difficult to obtain the extremely high efficiency such as 95%. Finally, the high output power required is another challenge due to the low rate-parameters and the challenges in the parallel connecting of the high speed switching devices. To overcome these challenges, a number of the analyses and proposed design are presented in this dissertation.

Firstly, the effect of the parasitic elements in the high switching frequency half-bridge inverter is analyzed and evaluated in detail based on the perspective of the ringing loop in the circuit. Based on these, an optimized PCB design is proposed to minimize the parasitic inductance in the ringing loop of the inverter. With the improved

PCB, the experiment results show that, the peak voltage and the amplitude of the ringing current in the circuit is reduced. However, the ZVS condition and the stability of the inverter at high input voltage condition are not achieved due to the high frequency ringing in the circuit. Therefore, a ringing damping circuit is proposed. The high stability and the low power loss on the proposed damping circuit is the advantage to obtain high efficiency of the inverter. In the experiment results, the ringing current in the circuit is damped. A 1.2 kW output power is obtained with the efficiency of 93.1%. This is an improvement in the 13.56 MHz inverter. However, it does not meet the required efficiency of the inverter for the dynamic EV charging systems due to limited switching speed of the silicon-MOSFET.

Secondly, to improve the efficiency of the inverter, the GaN HEMT device is used. In an experiment, the inverter using GaN HEMT obtains the efficiency of 97.5% which shows the potential to meet the required efficiency of the inverter for the dynamic EV charging systems. However, the output power of the inverter is limited due to the low rate current of the GaN HEMT. And the parallel connection of GaN HEMT devices at 13.56 MHz is very difficult because of the strong unbalance dynamic current distribution. Therefore, a design using multiphase resonant inverter is proposed. The proposed module design, the proposed power loss analysis method to obtain highest efficiency and the proposed drive circuit design have been addressed in detail. In experiment, a 3 kW inverter with the efficiency of 96.1% is achieved that significantly improves the efficiency of 13.56 MHz inverter. A 10 kW inverter with the efficiency of over 95% will be developed by following this proposed design in near future.

Finally, the 13.56 MHz high power inverter with the efficiency of over 95% can be realizable. However, the Class DE operation mode which is used in multiphase resonant inverter requires exact parameter of load, resonant circuit and several turning in the experiment process. Therefore, it is still difficult to apply in the dynamic charging systems

where the parameters of the coupling system will always change in the operation. The inverter behavior analysis and the further researches to keep the soft switching condition in the operation with the dynamic coupling system are necessary in the future work.

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List of Abbreviations

Greek Symbols

π $\simeq 3.14\ldots$

Acronyms

BW Bandwidth

EM Electromagnetic

ESR Equivalent Series Resistance

EV Electric Vehicle

$HEMT$ High-Electron-Mobility Transistor

ISM Industrial, Science and Medical radio band

PCB Printed Circuit Board

SAE Society of Automotive Engineers

SOA Safe Operating Area

WPT Wireless Power Transfer

ZCS Zero Current Switching

$ZdVS$ Zero Voltage slope Switching

ZVS Zero Voltage Switching

Chapter 1

Introduction

1.1 Wireless power transfer and EV dynamic charging systems

Recently, Electric Vehicles (EVs) are a promising solution for reducing CO_2 emission and air pollution in the big cities. However until now, the EVs have been not so attractive to the consumers due to the short running distance, long charging time and high battery cost. Hence, the dynamic wireless charging solution has been proposed to reduce the energy dependence and battery cost of EVs [1-4].

The wireless power transfer (WPT) technology had been researching to apply in EVs charging from several years ago. In the late of 1970s, a 20 kW WPT system was conducted for a running EV [1]. The wireless transfer distance was 2.5cm. Huge couplers were used because of the using only 180 Hz frequency power source. By the development of power electronic, the frequency has been increasing to reduce the couplers size while increase the transfer distance and obtain high efficiency. In the recent technology, as shown in Fig. 1.1, the EV WPT systems are almost using frequency in range from 20 to 150 kHz [2-9]. A few hundred millimeters transfer distance with over 90% efficiency was achieved at kilowatt power level [2-9]. In MHz frequency range, the size and weight of the coupling coils are much reduced. The transfer distance can expand to more than

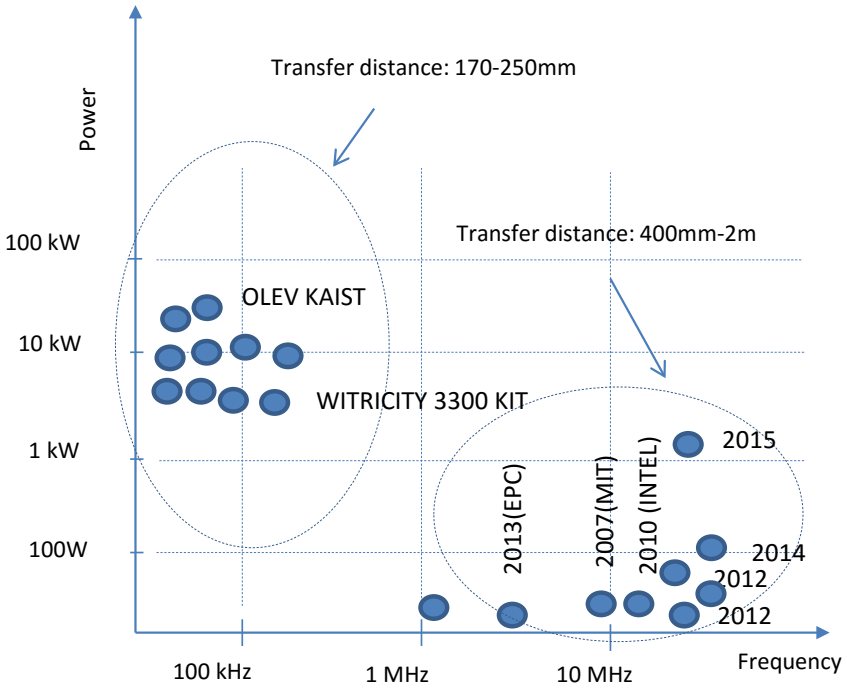


Figure 1.1: Transfer power versus operating frequency of WPT in recent researches [2].

1 meter with transfer efficiency over 90% [10]. These features promise a great performance for EV dynamic charging systems. In this project, we arm to build a WPT system for EV dynamic charging applications with the transfer distance is up to 1 meter. Therefore, the operation frequency of 13.56 MHz in ISM band is chosen. However, the MHz operation frequency is still hard to apply in EV charging system because it is difficult to convert several kilowatts power at MHz frequency with high efficiency [2].

Fig. 1.2 shows the structure of a dynamic EV charging system including the transmitting side in the ground and the receiving side in the vehicle. In the transmitting side, the electrical energy from the utility power source will be converted to the DC power source by using a rectifier. Then a high frequency inverter is used to generate the 13.56 MHz current in the transmitting coil from the DC power source. In the receiving side, the 13.56 MHz frequency current

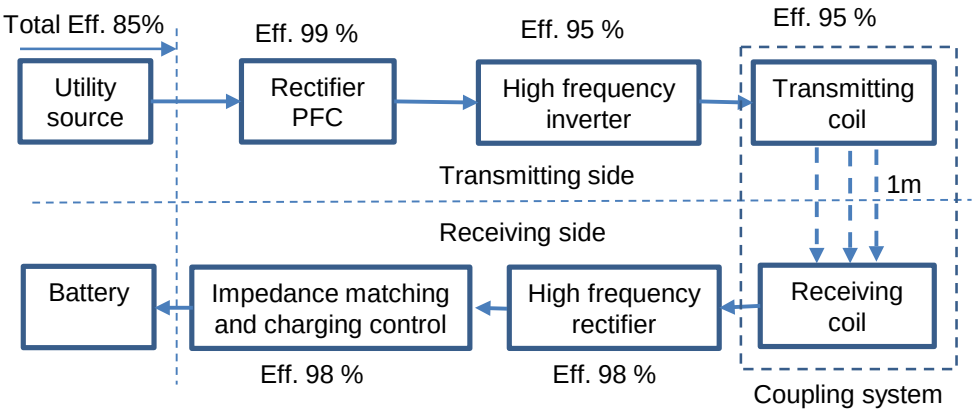


Figure 1.2: Structure of a dynamic EV charging system.

received from the receiving coil will be rectified to DC power source again by a high frequency rectifier. The DC source will be used to charge the batteries on the vehicle through an impedance matching and charging control circuit. With recent technology, the efficiency of such dynamic EV charging system mainly depends on the efficiency of the 13.56 MHz inverter in the transmitting side and the transfer efficiency between the coupling coils.

There are standards about power levels and efficiency of EV WPT which is recommended in the developing SAE J2954 standard [11]. The efficiency of over 85% for whole systems is recommended [11]. To satisfy such efficiency, the efficiency of each part in the dynamic EV charging system is shown in Fig. 1.2. The efficiency of over 95% for 13.56MHz high power inverter is required.

1.2 High power and high frequency inverter for EV dynamic charging systems

At high operation frequency, the class E and class Φ2 inverters can achieve high efficiency due to realizing the zero voltage switching (ZVS) and the zero voltage slope switching(ZdVS) condition [12-16]. Furthermore, the simple gate drive circuit is required for these inverter because they use only one switch referenced

to ground . Therefore, the class E and class Φ2 inverters are the most suitable topology for the high switching frequency applications. In 2006, a 13.4 W class E inverter operating at 13.56 MHz switching frequency with the efficiency of 91% was presented in [13]. In May 2015, a 13.56 MHz 1.3 kW class Φ2 inverter with GaN FET for Wireless Power Transfer which obtained efficiency of 94.6% was presented in [16]. However, these types of inverters are difficult to apply at high power level because the topology of these inverters use only one power switch [12-16] and the stress voltage on the power switch is very high in the comparison with the input DC voltage [12-16].

Half-bridge class D inverters have been used for a long time. The stress voltage on the power switches equals to the input DC voltage that is the most advantage of this topology to apply in high power applications. The theoretical efficiency of a Class-D amplifier is 100% with the ideal switches. However, in practical inverter, the limited switching speed of the switching devices causes the switching power loss which increases with the increasing of the switching frequency. At 13.56 MHz, the general class D inverter obtains the efficiency of about 70-80% [17]. The switching power loss on the class D inverter can be eliminated by the applying of the soft-switching conditions. In 2012, a 13.56 MHz 1.7 KW class D inverter with the efficiency of 87% is obtained by the realizing the ZVS condition [17].

Class DE inverters have the same structure as the half-bridge Class D with the addition of shunt capacitance across both switches. With the optimizing the parameters, class DE inverters can achieve the soft-switching condition as the same with class E inverter while the stress voltage is the same with Class D inverters [18]. Vries et al. shows that the Class DE inverter is capable of efficient operation for frequencies up to 5 MHz with power levels up to 1 kW [18]. However, the authors also observed the practical challenges associated with Class DE in MHz frequency operation including PCB layout, the high side gate drive, and synchronization of high and low side gate drive pulses [18].

In order to design the high power inverter, the half-bridge inverter topology is chosen in the design which is presented in this dissertation. The final design target is 10 kW inverter operating at 13.56 MHZ with the efficiency of over 95%. The

design is divided in three design steps. The first step, a 1 kW inverter is designed with the consideration about the influent of the parasitic elements at 13.56 MHz switching frequency. Then, 3 kW and 10 kW inverter is designed in step 2 and step 3 respectively with the consideration on the efficiency improvement and the increasing of the output power. In this dissertation, the first and second steps are presented.

1.3 Research challenges and objectives

1.3.1 Research challenges

Based on the review results, Three major research challenges are recognized in this project as following:

- Firstly, as the analysis in the previous research [18-25], the influences of the parasitic elements have been recorded as one of the first research challenges at high switching frequency applications. At very high switching frequency such as 13.56 MHz, the parasitic elements will affect both of the power circuit and gate drive circuit of the inverter. Consequently, the inverter may be damaged or unstable.
- Secondly, the extremely high efficiency required (over 95%) is also the research challenge because the switching power loss and the drive power loss are very high at 13.56 MHz.
- Thirdly, the high output power required at very high switching frequency is another challenge due to the low rate-parameters and the challenges in the parallel connecting of the high speed switching devices.

1.3.2 Research objectives

Motivated by the challenges mentioned above, the main objects of the research in this dissertation are as follows:

- Attenuate the influence of the parasitic elements at 13.56 MHz switching frequency.
- Improve the efficiency of the inverter to over 95%.
- Expand the output power of the inverter up to 3 kW based on the low rate power switching devices.

1.4 Contribution of this dissertation

Based on the research achievements, the contribution of this dissertation can be listed as following:

- Completed the analysis and evaluation of the influence of the parasitic elements in the 13.56 MHz inverter based on the point view of the high frequency ringing in the circuit.
- Proposed a PCB design method to minimize the parasitic inductances in the circuit and improve the stability of the inverter: the overall parasitic inductance reduces 23.4% and the stability of the inverter is improved by avoid the several anti- resonances at low frequencies.
- Proposed a ringing damping circuit to damp the ringing in the circuit by using the parasitic inductance of the trace lines: the ringing is damped with the very low power loss on the damping circuit at 13.56 MHz inverter. The stability of the inverter is much improved. Finally, the inverter using silicon MOSFET obtains the efficiency of 93.1% at the output power of 1.2 kW.
- Evaluated the first generation of the high voltage cascode GaN HEMT in 13.56 MHz inverter. The results show that the cascode GaN HEMT is more suitable than the silicon MOSFETs at 13.56 MHz inverter. The efficiency of over 97% is obtained in the inverter using the cascode GaN HEMTs.

- Proposed a design of a high power and high efficiency inverter using the cascode GaN HEMT based on the multiphase resonant inverter. The proposal includes the proposed module design solution, the proposed design method based on the power loss analysis to obtain the highest efficiency, and the proposed of the drive circuit design. Finally, a 3kW inverter with the efficiency of 96.1% is achieved in the experiment.

1.5 Dissertation outline

This dissertation includes of seven chapters. Chapter 1 introduces about the motivations, requirements, challenges, objectives, and the contributions of the research which is presented in this dissertation. The analysis and evaluation of the influence of the parasitic elements is presents in chapter 2. The equations to estimate the ringing frequency and the parasitic inductance of the ringing loop also are provided in this chapter. Chapter 3 presents a proposed PCB design to minimize the parasitic inductance of the ringing loop including proposed design, EM simulation, and experiment. A proposed ringing damping circuit is presented in chapter 4. The proposed circuit, the design method, simulation method and experiment are presented in detail. Chapter 5 presents the evaluation of the applying cascode GaN HEMT in 13.56 MHz. The drive design for the cascode GaN HEMT at 13.56 MHz is addressed in this chapter. Based on these, a proposed design the high power and high efficiency inverter using the cascode GaN HETM is presented in chapter 6. The optimum design method is proposed. Finally, the conclusion and the future work are given in chapter 7.

Chapter 2

Effect of parasitic elements

2.1 Introduction

At high frequency, the inverter is strongly affected by parasitic elements. The effects of parasitic elements on MOSFET switching characteristics are widely investigated as shown in [20-25]. All of previous studies showed that the switching performance of MOSFET will be worse at high frequency due to the influence of parasitic elements. As the switching power loss increases, the voltage stress and voltage slew rate also increase. Furthermore, the circuit might be unstable due to the oscillation in the gate driver circuit [20]. Even though the effects of parasitic elements are carefully investigated but the investigating frequency is around 1 MHz [20]. Since the ringing frequency is much higher than the switching frequency, the ringing in power loop will be damped before the next switching period, so the inverter is stable.

At 13.56 MHz, the ringing frequency is near to switching frequency, the inverter will be more unstable because the ringing in power loop is very difficult to damp. Furthermore at high frequency and high power condition, since the current and voltage are high and ringing, the effect of parasitic elements will be much heavier. The power switches can be easily destroyed due to very high peak voltage, very high slew rate voltage dv/dt or very high slew rate current di/dt. Therefore, this chapter analyzes and evaluates the effect of the parasitic elements

based on the high frequency ringing in the circuit. The equations to calculate the ringing frequency in the circuit and estimate the parasitic of the ringing loop are build. Finally, a experiment result about the effect of ringing at 13.56 MHz switching frequency is shown.

2.2 Parasitic model of half-bridge inverter

The circuit diagram of an inverter included of parasitic elements is shown in Fig. 2.1. Two MOSFETs V_1 and V_2 are connected in a half-bridge topology. The considered parasitic elements of the MOSFETs include gate-source capacitance $C_{gs1,2}$, gate-drain capacitance $C_{gd1,2}$, drain-source capacitance $C_{ds1,2}$, common source inductance $L_{s1,2}$, and drain inductance $L_{d1,3}$. The internal gate drive resistance (which is usually around 1 ohm for high-frequency power MOSFETs) and inductance are merged into the external gate drive resistance $R_{g1,2}$ and inductance $L_{g1,2}$ as they are connected in series and play the same role in the circuit. The parasitic capacitances of the MOSFETs depend on its physical parameters. The parasitic inductances of the MOSFETs depend on the packing type of the MOSFETs. Hence, at high operation frequency, the special RF MOSFET module which is packed to the minimized the parasitic inductance is better than the discrete one. In the first step of this research, the RF MOSFET module DRF1400 is used including two MOSFETs in the half-bridge topology as show in Fig. 2.1.

All stray inductances in the power loop and external to the MOSFET are lumped and represented by $L_{d2}, L_{d4}, L_{d5}, L_{d6}$ and L_{d7}. L_{d6} and L_{d7} are stray inductances of connection wire from DC source to the MOSFETs of inverter. L_{d2} and L_{d3} are stray inductances of connection wires among two MOSFETs. To remove effects of parasitic inductance L_{d6} and L_{d7}, input capacitors C_{in} and input inductor filter Lin are added. These capacitors and inductor act as an input filter which provide a path for high-frequency oscillations bypassing and prevent the high frequency current comeback to the DC source.

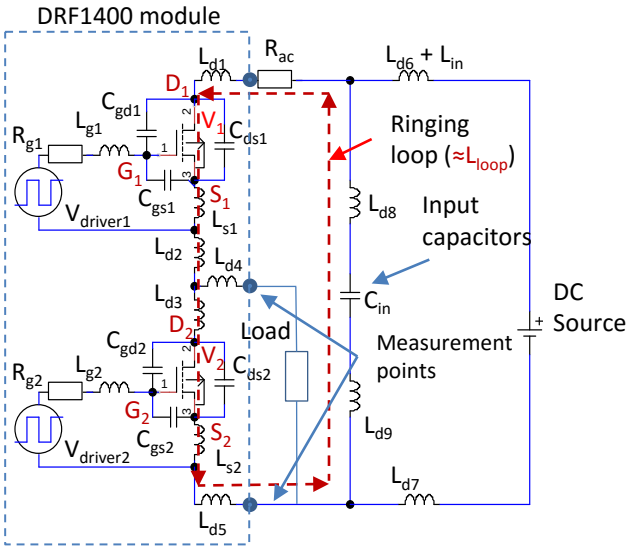


Figure 2.1: Parasitic model of a half-bridge inverter.

2.3 Ringing loop in half-bridge inverter

When the inverter operates at 13.56 MHz, the switching power loss on the power switch is much higher than the conduction power loss. Zero voltage switching (ZVS) condition is the key technique to obtain high efficiency. Fig. 2.2 shows the simple equivalent circuit of a half-bridge including two MOSFETs accompany with parasitic output capacitors and the charging process of output capacitor when the high-side MOSFET turning off. The output current is defined as indicated in (2.1). The relationship between voltage across C_{s1} and C_{s2} is shown in equation (2.2).

$$i_L(t) = I_L \sin(\omega t + \varphi) \tag{2.1}$$

$$v_{dc} = v_{C_{s1}}(t) + v_{C_{s2}}(t) \tag{2.2}$$

It can be assumed that C_{s1} and C_{s2} are charged and discharged by all of output current. According (2.3), the condition that Drain-Source voltage of bottom MOSFET reaches zero before the load current inverses is shown in (2.4). In fact, the time needs to be greater than the value expressed in (2.4) because a part of

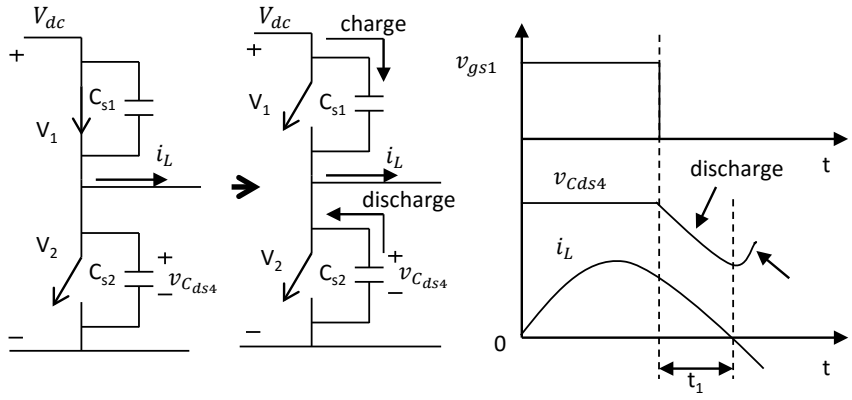


Figure 2.2: Charging process of output capacitor

load current flows through the conduct channel of MOSFET.

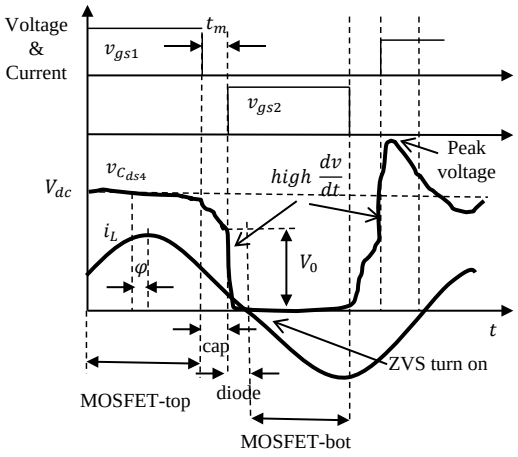
$$\begin{aligned} i_L(t) &= C_{s1}\frac{dv_{C_{s1}}(t)}{dt} - C_{s2}\frac{dv_{C_{s2}}(t)}{dt} \\ &= (C_{s1} + C_{s2})\frac{dv_{C_{s1}}(t)}{dt} \end{aligned} \tag{2.3}$$

$$\cos(\omega t_1) > \frac{V_{dc}}{I_L}\omega(C_{s1} + C_{s2}) - 1 \tag{2.4}$$

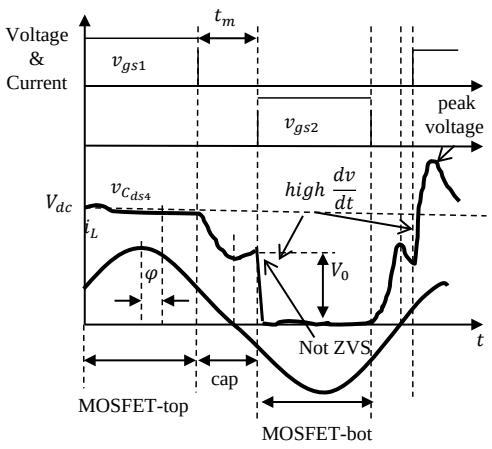
Fig. 2.3 shows three possible switching conditions when the inverter operates above resonance frequency. Case shown in fig. 2.3(c) shows the situation when no charging and discharging losses are present at turn on because the drain-source voltage of bottom MOSFET reaches to zero before the load current reverses. The ZVS condition is also achieved. When the dead time is turned exactly, the voltage of drain-source capacitor can reach to zero in time when the load current reverses. This case typically is called class DE operation. This is the perfect switching condition which is the most suitable for high frequency inverter where the switching power loss is minimized and the ringing is not observed in the circuit. However, at 13.56 MHz, the charging and discharging time are comparable with switching period. Therefore, in this case, the phase lag φ is large which leads to low power corresponding at output of inverter. The device utilization is low. Furthermore, from (4) the condition to obtain ZVS as shown in Fig. 2.3(c) depend on vary parameters such as resonant frequency of load, load

current and the dead time. In dynamic charging system, the distance between transmitting coil and receiving coil changes lead to the resonant frequency of coupling systems and load current changes [17]. Therefore the situation shown in Fig. 2.3(c) does not often obtain.

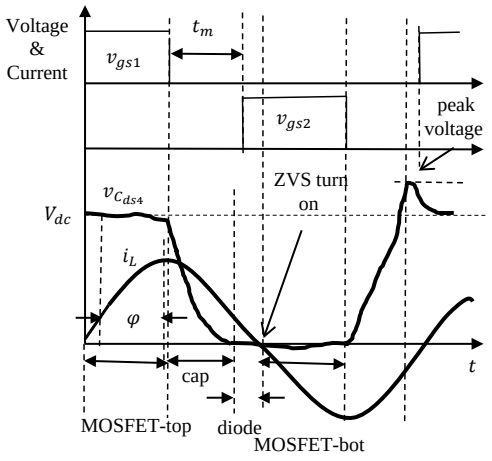
Cases shown in Fig. 2.3 (a) and Fig. 2.3(b) are situations when the drain-



(a) Class D and ZVS



(b) Class D and Not ZVS



(c) ZVS and ZdVS

Figure 2.3: The possible switching condition above resonance

source voltage of bottom MOSFET does not reach to zero before the load current reverses. The difference between cases (a) and (b) is the dead time. In case (a),

the dead time is very short. The bottom MOSFET is turned on before the load current inverses. The load current will pass through the body diode of bottom MOSFET before it reverses. The ZVS condition is achieved. In case (b), the dead time is longer. The bottom MOSFET is turned on after the load current reverses. In this case, the ZVS condition is not achieved.

In these cases, when the bottom MOSFET is turned on the parallel capacitor C_{s2} will be shorted and C_{s1} will be full charged which causes of high dv/dt, high di/dt and high spike current on the MOSFETs. The forced charge/discharge current of output capacitor of MOSFETs with high di/dt makes high peak voltage on the MOSFET when it passes through the parasitic inductances in the circuit. The ringing current and the ringing voltage in the circuit are generated in this situation due to the charge/discharge process among output capacitor of MOSFETs and parasitic inductance in the loop which is called as the ringing loop in Fig. 2.1.

In this research, we use an integrated MOSFET module DRF1400. This module includes two power MOSFETs in a half bridge topology as shown in Fig. 2.1. The total equivalent parasitic inductance of ringing loop is given as

$$L_{loop} = L_{mod} + L_{lin} \tag{2.5}$$

where

$$L_{mod} = L_{d1} + L_{s1} + L_{d2} + L_{d3} + L_{s2} + L_{d5} \tag{2.6}$$

$$L_{lin} = L_{d8} + L_{d9} \tag{2.7}$$

are the parasitic inductances of the MOSFET module and the trace lines, respectively.

Fig. 2.4(a) and Fig.2.4(b) show two equivalent circuits of ringing loop in operating. The power loop is represented by the continuous line and the ringing loop is represented by the dash line. In both of case, the ringing loop is created by self-oscillation of parasitic inductance of ringing loop L_{loop} and output capacitor of MOSFET C_{oss} as shown in Fig. 2.4(c). The voltage across the high-side MOSFET when the low-side MOSFET turned on is calculated in (2.8). The

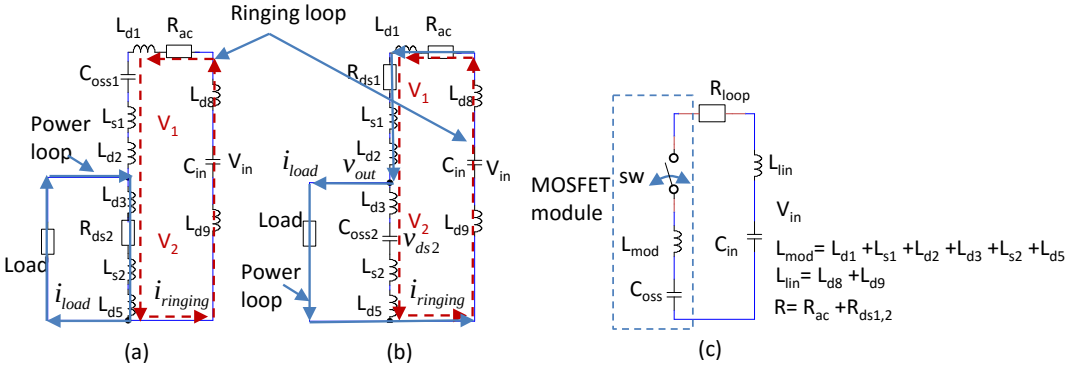


Figure 2.4: Equivalent circuit of ringing loop in operating
(a) V_1:OFF and V_2:ON, (b) V_1:ON and V_2:OFF, (c) Final equivalent circuit

spike current on the low-side MOSFET when it turned on can be calculated by equation (2.9). The charging and discharging losses which can be calculated as shown in (2.10) are added to typical switching loss of MOSFET.

$$V_0 = V_{dc} - \frac{I_L}{\omega(C_{s1}+C_{s2})}[\cos(\omega(t_1 - t_m)) + 1] \tag{2.8}$$

$$i_{spike} = V_0/R_{ds(on)} \tag{2.9}$$

$$P_{cd(loss)} = 2f_s(\frac{1}{2}C_{s1}V_0^2 + \frac{1}{2}C_{s2}V_0^2) \tag{2.10}$$

Where f_s is switching frequency; $R_{ds(on)}$ is the drain-source resistance of MOSFET when it is in on state. Based on the equivalent circuit in Fig. 2.4(c), the drain-source voltage of low-side MOSFET when it turns off is derived as:

$$\begin{aligned} v_{ds}(t) &= V_{in} + \frac{V_0}{\sin\varphi_1} e^{-t/t_d}\sin(\omega_r t - \varphi_1) \\ &= V_{in} + v_{ringing} \end{aligned} \tag{2.11}$$

where

$$\begin{aligned} t_d &= 2L_{loop}/R_{loop} \\ \omega_r &= [1/L_{loop}C_{oss} - (R_{loop}/2L_{loop})^2]^1/2 \\ R_{loop} &= R_{ac} + R_{DS} \\ v_{ringing} &= V_r e^{-t/t_d}\sin(\omega_r t + \varphi) \end{aligned} \tag{2.12}$$

V_{in} is the input voltage across input capacitor C_{in}. R_{ac} represents the ac and dc resistance of trace line in ringing loop. The ac resistance increases as the ringing frequency increases. R_{DS} is the resistance of MOSFET when it is in ON state.

From (2.9), (2.10) and (2.11) the voltage V_0 directly affect to the charge/discharge power loss, spice current, the peak voltage on the MOSFET and the amplitude of ringing voltage in the circuit. Therefore, no snubber circuit which is connected in parallel with MOSFETs can be added in this case because it will reduce the charging and discharging time of output capacitor of MOSFET lead to the high value of voltage V_0.

The amplitude of ringing part reduces base on exponential function with the time constant t_d. Table 2.1 shows the amplitude of ringing part at the end of switching period with 1 MHz and 13.56 MHz switching frequency.

Table 2.1: Amplitude of ringing at the end of switching period

Parameter	$V_r e^{-t/t_d}$	
Switching frequency	1 MHz	13.56 MHz
Damping time t	500 ns	36.87 ns
R_{loop}	0.24Ω	0.26Ω
L_{loop}=5 nH	$0.000006V_r$	$0.38V_r$
L_{loop}=10 nH	$0.0025V_r$	$0.62V_r$
L_{loop}=15 nH	$0.018V_r$	$0.73V_r$
L_{loop}=20 nH	$0.05V_r$	$0.79V_r$

The results in Table 2.1 show that at 1 MHz switching frequency, almost ringing will be damped at the end of the switching period by nature way. However at 13.56 MHz, the ringing can not be damped by the nature way at the end of switching period. It is note that the (2.8) is correct only when the ringing is zero at the transition time of the MOSFETs. In the case of non-damped ringing, the initial conditions always change, therefore (2.8) is incorrect and it is difficult to calculate the voltage and current in the circuit. It is mean that the calculation results in Table 2.1 are not accurate at 13.56 MHz. However, it still shows the phenomenon of the parasitic inductance effect when the switching

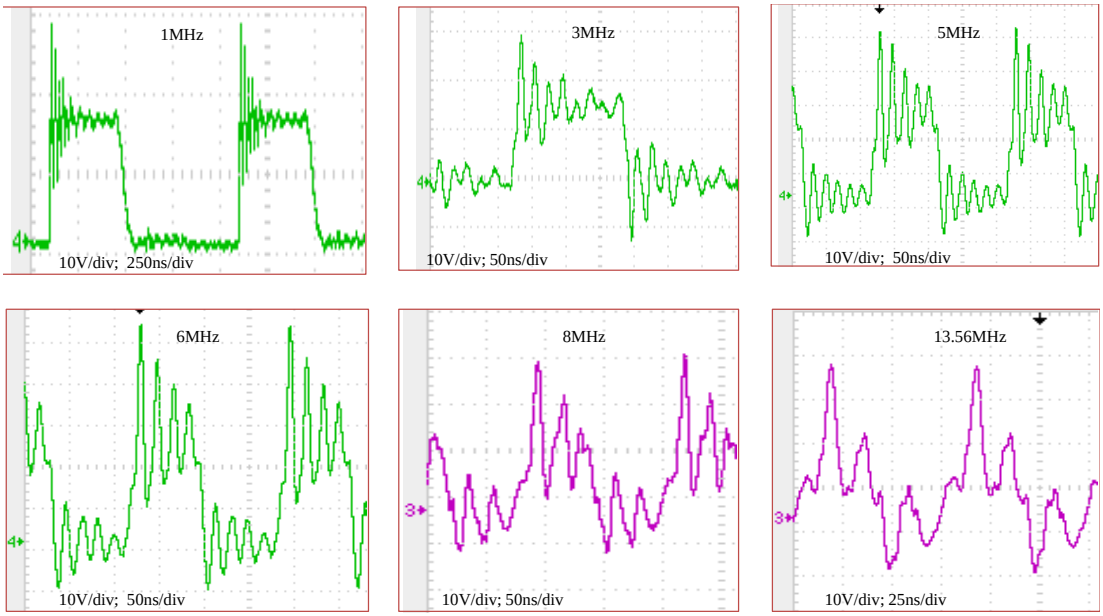


Figure 2.5: Output voltage waveform when switching frequency change from 1 MHz to 13.56 MHz (Conventional PCB design, V_{dc} =15 V, I_{load}=1 A)

frequency increases. And the amplitude of ringing part at the end of switching period when the MOSFET change the state depends on the parasitic inductance value of the ringing loop. In this analysis, if the parasitic inductance of ringing loop is over 10 nH, the ringing is still very high when the MOSFETs change the state. As the result, the voltage across the MOSFET will be changed based on the ringing waveform. If the ringing frequency is low, the switching power loss will be very high and the output voltage waveform will excite harmonics. The very high switching power loss may damage the power MOSFETs immediately. Furthermore, the very high frequency oscillation is fed to the transmitting coil. The conduction loss in the transmitting coil will be very high due to skin effect. The ringing current is added to the drain current of conducting MOSFET which causes increasing conduction loss and peak current on the MOSFET[20].

Furthermore, the ringing current in the power circuit also make the EMI noise which will effect to the driver circuit. The driver pulse waveform will be affected by noise and the switching performance of MOSFET will be reduced[21].

Fig. 2.5 shows the output voltage waveform of class D inverter when switching frequency changes from 1 MHz to 13.56 MHz. These experimental results are taken in the conventional PCB design. The result shows the effect of parasitic inductances to the performance of inverter. The ringing frequency in the output voltage is almost constant at 58 MHz when the switching frequency changes. When the switching frequency increases, the amplitude of ringing part at the end of switching period is larger. From 3 MHz, the ringing cannot be damped. And from 8 MHz, the output voltage begins excised harmonics. At 13.56 MHz, the output voltage waveform is almost ringing. The switching power loss on the MOSFETs is very high. The MOSFETs may broken. The experiment results show the same phenomenon of the parasitic inductance effect when the switching frequency increases with the calculation results in table 2.1.

2.4 Discussion

Base on the analysis in this chapter, we can conclude that the forced charge/discharge of output capacitor of MOSFET and the parasitic inductances in the ringing loop are the root cause of the peak voltage and ringing in the circuit. At 13.56 MHz, the ringing in the circuit is un-damp able by nature way. Therefore, in addition the effects which have been mentioned in previous research, the effects of parasitic inductance may damage the power switch due to very high switching power loss and unstable due to the effects of ringing current to gate-source voltage of MOSFET. Therefore, minimizing the parasitic inductance in the ringing loop and ringing damping design are the key points to improve the performance of inverter at 13.56 MHz.

Chapter 3

PCB design

3.1 Introduction

At high frequency, PCB layout design is always very critical. The effect of parasitic elements can be minimized by optimizing the PCB layout design. Several techniques and studies have been already discussing about this problem [26-27]. However almost of them design the PCB layout at low power level with very small device and the operating frequency is around 1 MHz. When using high power device, PCB design is difficult to minimize parasitic inductance due to the size of device and the heat sink of device. Furthermore, at 13.56 MHz, the mutual effect is stronger. Therefore the direction of current in the circuit is critical in PCB design to reduce parasitic inductance.

In this chapter, a PCB layout design is proposed to obtain low parasitic inductance. All of PCB layout designs are simulated and analyzed by a full-wave electro-magnetic (EM) simulations using Sonnet em software. In the simulation and experiment results, the ringing frequencies and parasitic inductance are compared to the conventional design. The proposed PCB layout can provide a 23.4% decrease in parasitic inductance over the conventional one.

3.2 Parasitic inductance

As presented in [32], the parasitic inductance of trace line and via in designed PCB can be calculated as following equation:
Parasitic inductance of trace line

$$L = 0.002l\left[ln\left(\frac{2l}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{l}\right)\right](H) \tag{3.1}$$

Where l, t and w is length, thickness and width of the line, respectively which are given in centimeter. Parasitic inductance of via

$$L = \frac{\mu_0}{2\pi}h\left[ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right) + \frac{3}{2}\left(r - \sqrt{r^2+h^2}\right)\right](H) \tag{3.2}$$

where h is high and r is radius of via.

To reduce the value of parasitic inductance, the PCB trace line length should be designed as short as possible and the trace line width should be designed as lager as possible. The parasitic inductance of via depends on board thickness.

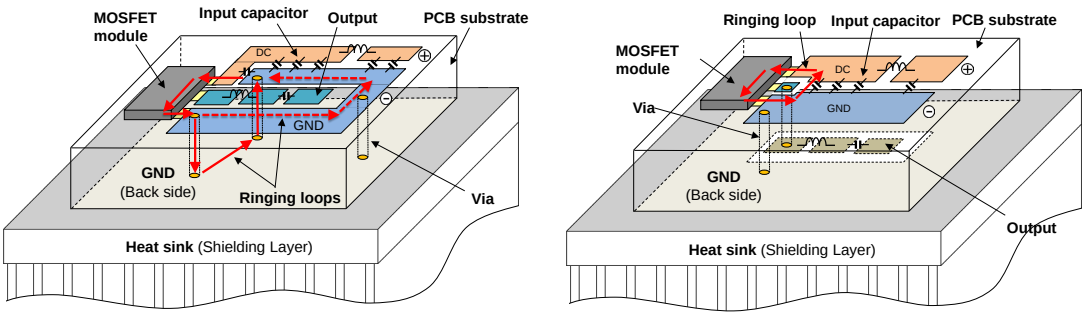
3.3 Conventional PCB design

Generally, the laminate structure is applied in DC side of inverter to realize the low parasitic inductance by using field self-cancellation effect. However, that method can not be applied for DRF1400 MOSFET module due to its physical packing shape. Furthermore, at high frequency almost device is packed in surface mount type. The connections among layers of PCB have to use vias. Therefore, when the field self-cancellation effect can not be applied, using laminate structure is not optimized design as following analysis.

The conventional PCB layout is presented in Fig. 3.1(a) [28]. The input capacitors are placed on the top layout of PCB board with MOSFET module and in close proximity with Drain pin of MOSFET module. In the bottom layout, the

ground plane is connected to the top layout by vias. In this design, the ringing loop travels through two physical loops. The lateral loop is on the top layout shown in Fig. 3.1(a) with dash arrows. The vertical loop traveling perpendicular to the ground plane with via connections is shown in Fig. 3.1(a) with solid arrows. The parasitic inductance on the vertical loop mainly influences the parasitic inductance of ringing loop because the trace length of vertical loop is shorter than that of lateral loop. The parasitic inductance on vertical loop includes of parasitic inductance of trace line on the top layout, trace line on the bottom layout and vias through the board. In practical design, the parasitic inductances of vias depend on vias design and board thickness. The board thickness must be minimized to minimize the parasitic inductance of vias. For the conventional PCB layout, the loop parasitic inductance mainly depends on the board thickness and vias when the ringing loop is on both top and bottom layout of the PCB.

Furthermore, the ringing current travels in two layers of PCB and in the large area will generate several parasitic ringing and EMI noise which will affect to the performance and the stable of inverter.



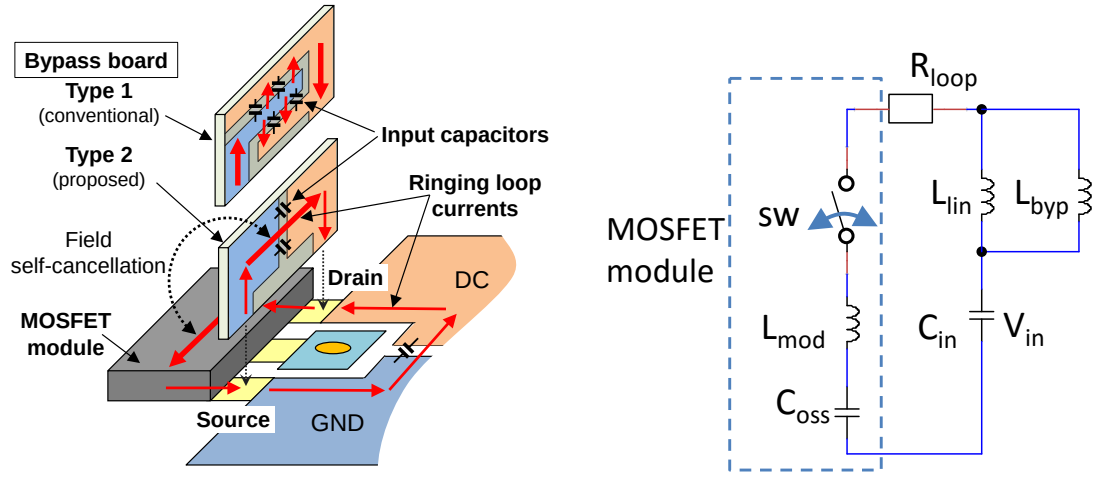
(a) Conventional design (layout 1)

(b) Proposed design (layout 2)

Figure 3.1: PCB layout design

3.4 Proposed PCB design

The proposed PCB layout design is shown in Fig. 3.1(b). The input capacitors and MOSFET are still placed on the top layout of the PCB. However, in this



(a) PCB design (b) Equivalent circuit

Figure 3.2: Inverter design using bypass board

design, the output port is placed on the bottom layout. Consequently, the input capacitors can be placed in the middle area between the drain and source of the MOSFET module to minimize the physical trace length of the ringing loop. The trace lines are designed as large as possible to minimize parasitic inductance. In this design, the ringing loop only travels in the TOP layout of circuit board as shown in Fig. 3.1(b).

The proposed PCB layout provides four advantages comparing to the conventional PCB layout design:

- Minimizing parasitic inductances of ringing loop.
- Parasitic inductance of ringing loop is independent of board thickness.
- The traveling area of ringing current is minimized to reduce the radiation EMI noise.
- The trace length is shorter and the trace width is larger. Therefore the AC resistance due to skin effect is smaller. As a result, the conducting power loss on the circuit will be reduced [32].

While minimizing the physical size of the ringing loop is important to reduce parasitic inductance, the field self- cancellation method can also reduce parasitic inductances. In this design, a metal heat sink is designed to cover not only the bottom of MOSFET module but also the area of PCB where contains the power loop. Heat sink will act as a "shield layer". The power loop generates a magnetic field that induces a current, opposite in direction of current in the power loop, inside a shield layer. In turn, the current in shield layer generates a magnetic field to cancel the original magnetic field of power loop [26]. As a result, the parasitic inductances will be reduced.

A bypass board, which is vertical with respect to the PCB, is designed and placed in close proximity to the MOSFET module, as shown in Fig. 3.2. The ringing loop inductance after the bypass board is added to the PCB can be expressed as

$$L_{loop} = \frac{L_{lin}L_{byp}}{L_{lin} + L_{byp}} + L_{mod} - \Delta L \tag{3.3}$$

where L_{byp} is the parasitic inductance of the bypass board, ΔL is the amount of reduction in L_{loop} as a result of the field self-cancellation effect. Note that the bypass board reduces L_{loop} in two ways: (1) through providing a current path in parallel with the main trace line (see Fig. 3.2) [28], and (2) through providing a ringing current flowing in the opposite direction with regard to the current in the MOSFET module. The latter field self-cancellation effect becomes mostly effective when the dominant current flow direction in the bypass board becomes anti-parallel with respect to the current direction in the MOSFET module. Since the current in the conventional bypass board [28], which we refer to as Type 1 (Fig. 3.2), mostly flows in vertical direction with respect to the current in the MOSFET module, we propose a bypass board of Type 2 with improved layout enabling the dominant current flowing in the desired direction. Summarizing techniques of the proposed layout to reduce the parasitic inductances is as follows,

- Design the ringing loop only on the top layout.
- Place the arranged bypass board by using self-cancellation of magnetic field.

- Using the heat sink as a shield layer.

Next, the effect of the proposed layout is analyzed by EM simulation.

3.5 Simulation

To verify the effectiveness of proposed PCB design, full-wave electro-magnetic (EM) simulations are performed using Sonnet em. Different inverter configurations using various design options, such as different PCB layouts, the heat sink (acting as a shield layer) and the bypass board, are analyzed.

3.5.1 Simulation method

The EM simulation model of PCB is shown in Fig. 3.3(a), including of two metal layers, vias, and input capacitors . The major parameters used in the simulation are listed in Table 3.1. The shielding effect of the heat sink is taken into account by placing additional metal layer underneath the bottom layout of the PCB. The thickness of the air (Air2 in Fig. 3.3a) defining the separation between the PCB bottom layer and the shield layer was set as 0.1 mm. In order to extract the

Table 3.1: Summary of major parameters used in simulation

Material parameter	Dielectric constant	4.1
	Loss tangent	0.02
	Metal Conductivity (cu)	5.8e7 S/m
Layer thickness	Air1	30 mm
	Air2	0.1 mm
	Air3	30 mm
	PCB substrate	1.6 mm

parasitic inductance of the trace line of (2.7), the ringing loop in the PCB is disconnected at the interface of the MOSFET module, leaving a two-port circuit consisting solely of the trace lines and the input capacitors. The ports to excite

the circuit are placed at the wall of the analysis box using port extension lines which are de-embedded so as not to effect the simulation results. The equivalent circuit of the two-port circuit is an inductor (L_{lin}) and a capacitor (C_{in}) connected in series, so it should behave effectively as an inductor with inductance L_{lin} at sufficiently high frequency. The inductance L_{lin} is estimated using the following steps:

- Step 1: Convert the simulated S-parameters of the two-port circuit to Y-parameters to compute the effective inductance seen between ports 1 and 2 by using following equation,

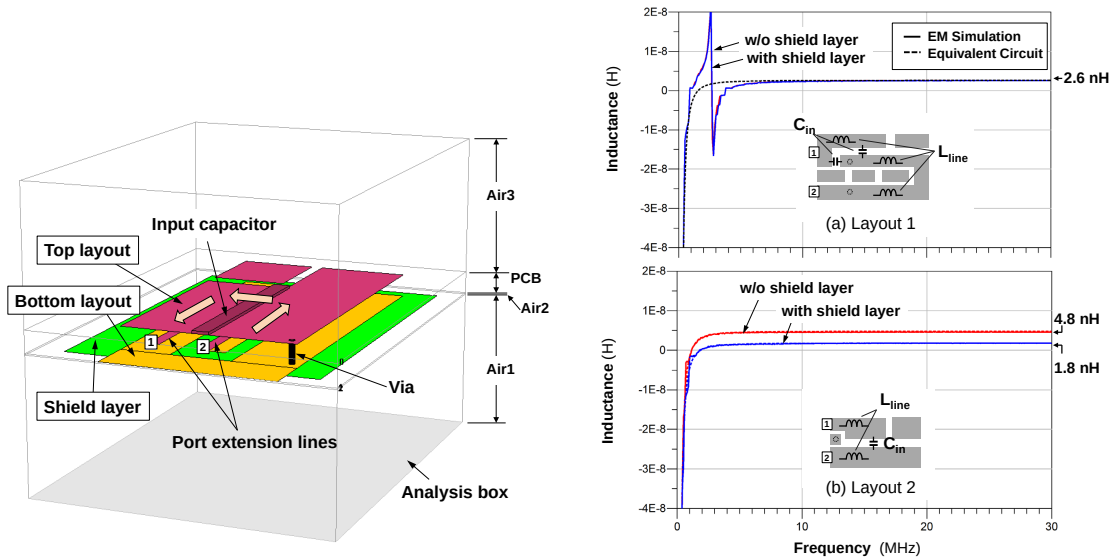
$$L_{eff}(\omega) = \frac{1}{\omega} Im\left(\frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y12^2}\right) \tag{3.4}$$

  This formula can be applied when the inductor is used in differential configuration [31]. Fig. 3.3(b) shows the EM-simulated $L_{eff}(\omega)$ as a function of frequency (solid lines). It can be seen that as the frequency becomes higher $L_{eff}(\omega)$ turns from negative to positive value at the frequency of series LC resonance and converges to the constant as the frequency is increased.

- Step 2: Assume an equivalent circuit of simple series-connected L_{lin} and C_{in}. Then compute $L_{eff}(\omega)$ for the equivalent circuit and optimize L_{lin} so that the overall frequency variation fit the EM-simulated $L_{eff}(\omega)$ obtained in step 1.

3.5.2 Effect of PCB layout and shield layer

Fig. 3.3(b) summarizes the simulated $L_{eff}(\omega)$ frequency dependence for Layout 1 and 2. It can be seen that with the optimum L_{lin} value (with C_{in} fixed at 4000 nF) the equivalent circuit result fits the EM-simulation result. The validity of the obtained L_{lin} values can be confirmed by observing that the $L_{eff}(\omega)$ curves for both EM simulation and equivalent circuit cross zero at the same series-LC resonant frequencies and both have the same converging levels determined by the L_{lin} value. Thus, the L_{lin} value for Layout 1 is obtained as 2.6 nH, regardless



(a) EM Simulation model for analyzing PCB

(b) Frequency dependence of effective inductance)

Figure 3.3: PCB layout EM simulation

of using the shield layer (heat sink) because the PCB itself is already shielded by the GND metal pattern on the back side. On the other hand, in the case of Layout 2, the optimum L_{lin} value is 1.8 nH with the shield layer whereas it is 4.3 nH without the shield layer.

While the overall $L_{eff}(\omega)$ frequency response obtained by the EM simulation can be reproduced by using a series LC circuit, there are some other sub-resonating behaviors that cannot be explained by such simple equivalent circuit. This is particularly evident in Layout 1, in which case the complicated layout leads to distributed L, C elements causing additional parallel LC resonances (see inset of Fig. 3.3(b)). The proposed PCB of Layout 2 has thus additional advantage of preventing unpredictable sub-resonances that could lead to malfunctioning of the inverter.

3.5.3 Effect of Bypass board

In order to confirm the field self-cancellation effect of the bypass board, we compare the ringing loop inductances for the inverter with and without the bypass board. Fig. 3.4 shows EM simulation models used for this particular purpose. Since the simulator uses a planar solver, horizontal dummy metal pads are used to represent the current paths through the MOSFET module and the overlying bypass board, although the latter is intended to be vertical in the real design (Fig. 3.2).

The proximity effect of the bypass board and the MOSFET module can be studied by varying the distance (d) between the two opposite current paths. This can be done by varying the thickness of the air between the top layout and the bottom layout, as shown in Fig. 3.4. Fig. 3.5 is a schematic illustration of how the total inductance components vary with the inverter design. If the PCB layout is fixed, L_{loop} obtained by the afore-mentioned method should decrease as the bypass board becomes close to the MOSFET module, as illustrated in Fig.

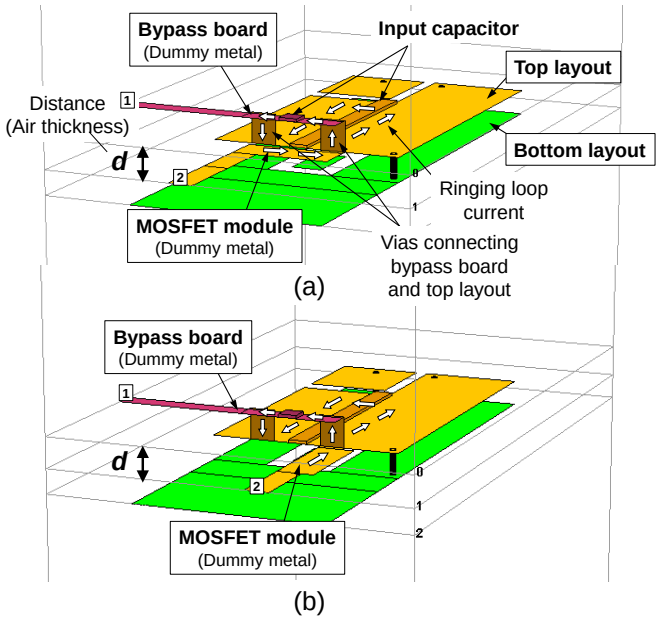


Figure 3.4: EM simulation models used to evaluate the effect of the bypass board (without shield layer)

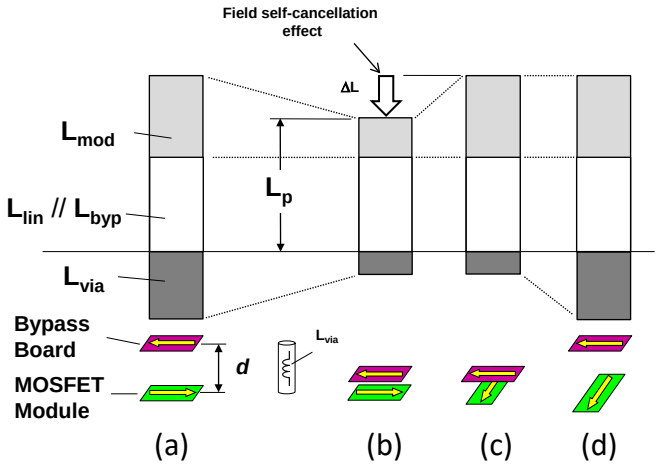


Figure 3.5: Schematic illustration of the parasitic inductance components.

3.5(a) and (b). Now, however, this method overestimates the proximity effect of the bypass board, because it includes the effect of the reduction in the via inductance (L_{via}).

In order to avoid this problem, the following method is used. Since the field self-cancellation effect is not in effect when the two current paths become perpendicular to each other, the dummy metal as the MOSFET module in Fig. 3.4(a) is rotated by 90 degree, as shown in Fig. 3.4(b). Since Lvia is not changed in this modification, by taking the difference between the total inductance for the two cases (Figs 3.5(b) and (c)), only the desired inductance difference ΔL due to the field self-cancellation effect is obtained. This method is based on the assumption that the inductance of the MOSFET module is not changed by the 90 degree rotation. To confirm this, the total inductances for Figs. 3.5(a) and 3.5(d), in which cases the two current paths are sufficiently distant (d = 16.0 mm) and thus the field self-cancellation effect should be negligible anyway, are computed and found to be identical.

The values of ΔL for bypass board of Type 1 and Type 2 estimated this way are 0.4 nH and 1.2 nH, respectively, clearly showing the advantage of the Type 2 bypass board. The L_{loop} values for various PCB designs, obtained by taking the sum of the inductance elements in (3.4), are summarized in Table 3.2. Here, L_{byp}

is obtained by EM-simulation for an isolated bypass board, Lmod is estimated using the data sheet from the manufacturer of the MOSFET module [29]. The results indicate that the optimal layout for the PCB and the bypass board as well as the shield layer significantly reduce the ringing loop inductance.

Table 3.2: Summary of simulation results

Design options			Inductance (nH)				
PCB layout	Bypass board	Shield layer	L_{lin}	L_{byp}	L_{mod}	ΔL	L_{loop}
Layout 1	-	Yes	2.6	-	5.8	0	8.4
Layout 1	Type 1	Yes	2.6	15.0	5.8	0.4	7.6
Layout 1	Type 2	Yes	2.6	8.4	5.8	1.2	6.5
Layout 2	No	No	4.8	-	5.8	0	10.6
Layout 2	No	Yes	1.8	-	5.8	0	7.6
Layout 2	Type 2	Yes	1.8	8.4	5.8	1.2	6.1

3.6 Experiment results

3.6.1 Parasitic inductance estimation method

At high frequency, the measurement technique is very important to properly measure the ringing transient. The ringing waveform measurements have been performed with Tektronix MSO3014 which the bandwidth and sample rate are 100 MHz and 2.5GS/s respectively. The voltage probe is Tektronix P6139B. The parameters of probe are shown in Table 3.3. The probe is directly soldered on the

Table 3.3: The parameters of probe

Name	BW (-3dB)	R_{in}/C_{in}	CM range
Tecktronix P6139B	500 MHz	10 MΩ /8 pF	300 V_{RMS}

output pin of MOSFET module. The ground wire of probe is as short as possible. The rising time and falling time of signal which we obtain in the measurement

result is affected by parameters of probe and oscilloscope as shown in Fig. 3.6. The Parasitic inductance of the ringing loop is estimated based on the measuring

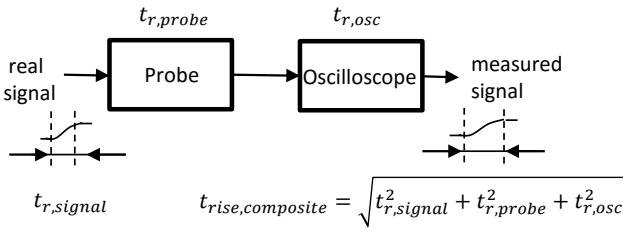


Figure 3.6: Composite rise time of the series connection of voltage probe and oscilloscope.

of the ringing frequency in the voltage across the low-side MOSFET as show in Fig 3.7. Measurement point is shown in Fig. 2.1. Then the L_{loop} is estimated from equation (2.12). The parameter of circuit is shown in Table 3.4. DRF1400 MOSFET module includes two ARF300 RF power MOSFETs connecting in half-bridge topology [29]. In this case the output capacitor of MOSFET at 15 V is estimated from characteristic curve in datasheet of ARF300 RF power MOSFET [30].

Table 3.4: Circuit parameter

Parameter	Value
MOSFET	DRF1400
Output capacitor C_{oss} (at 15 V)	700 pF
$R_{DS(on}$	0.24Ω
R_{ac}	0.014Ω

3.6.2 Experiment results

To compare the performance of the proposed PCB design with conventional design, two separate boards are created:

- Layout 1: Conventional PCB layout

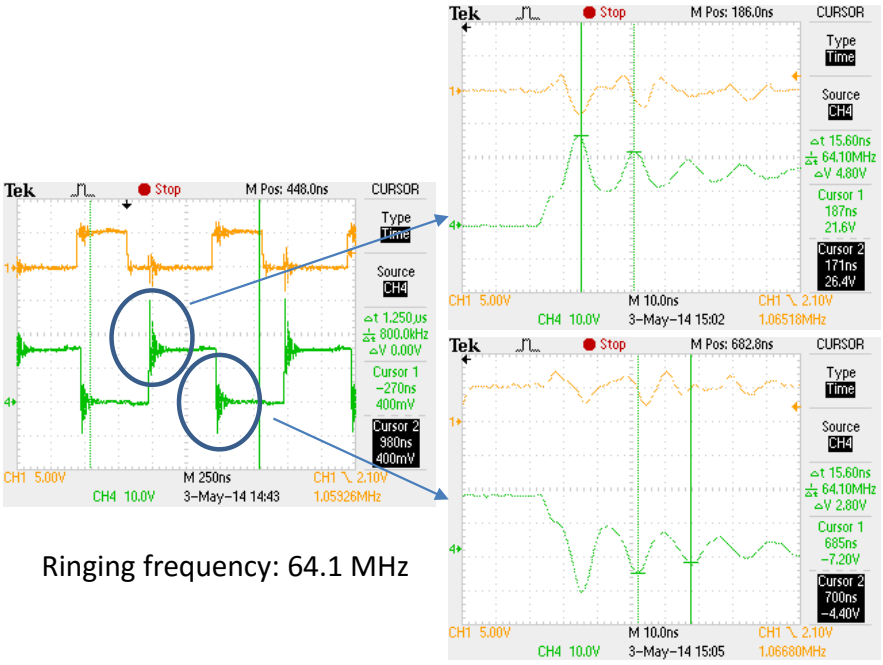


Figure 3.7: Ringing frequency estimation method

- Layout 2: Proposed optimal PCB layout

All of boards are made from the same type of copper board and all of devices using on each board are also the same. The parameter of PCB board is shown in table 3.1 which is used to simulate the PCB designs. The prototype of the proposed PCB design is shown in Fig. 3.8

The measurement and estimation results are shown in Table 3.5 and Fig. 3.9. The design in case 2 is the conventional PCB design and the design in case 5 is proposed PCB design.

Fig. 3.9 shows that the experiment results and simulation results have the same trend in parasitic inductance reduction. The difference between experiment results and simulation results is acceptable. There are reasons which make that difference. In simulation, we did not simulate the effect of shield layer to the parasitic inductance of MOSFET module. In the experiment result the output capacitor of MOSFET which is used to estimate parasitic inductance of ringing loop is estimation value. This value makes error in the experiment result. The

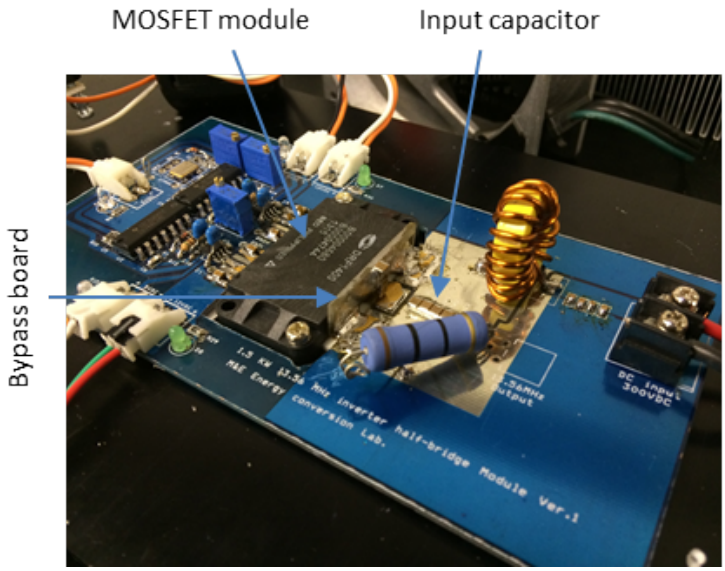


Figure 3.8: Prototype of the proposed PCB design

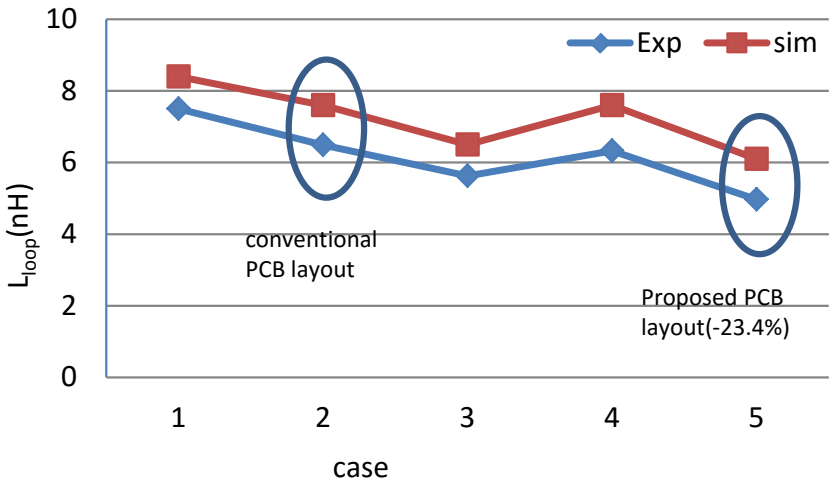


Figure 3.9: Experiment and simulation results of loop inductance

parasitic inductance of probe also makes the error in the measurement result. However we use the same method with both of proposed PCB design and conventional PCB design. Therefore the error does not effect to the comparison relationship between proposed design and conventional design.

Table 3.5: Measurement and estimation results

Case	Design	Ringing Freq. (MHz)	L_{loop}(nH)	
			Exp	Sim
1	Layout 1	58.14	10.7	8.4
2	Layout 1 + Bypass board 1	62.5	9.27	7.6
3	Layout 1 + Bypass board 2	67.13	8.04	6.5
4	Layout 2	63.3	9.04	7.6
5	Layout 2 + Bypass board 2	71.43	7.1	6.1

The results in case 2 and case 3 show that the proposed bypass board can reduce parasitic inductance of layout 1 from 9.27 nH to 8.04 nH. These results verify the effectiveness of field self-cancellation effect which was simulated in previous section.

The results in case 1 and case 4 verify the effectiveness of proposed main PCB board. The parasitic inductance of PCB board without bypass board reduces from 10.7 nH to 9.04 nH. If we assume that the parasitic inductance of MOSFET module is 5.8 nH [29], the parasitic inductance of trace line outside MOSEFT in ringing loop will reduce from 4.9 nH to 3.24 nH. In other word, the proposed main PCB board can reduce 33.9% parasitic inductance of PCB trace line. And the parasitic inductance of ringing loop is independent of board thickness.

The experiment results in case 2 and case 5 show that the proposed design can provide overall 23.4% reduction in parasitic inductance in ringing loop compared to the conventional design, which agree reasonably well with the simulation. With proposed design, the parasitic inductance of PCB trace line is significantly reduced and independent of boar thickness. The parasitic inductance inside MOSFET module also is reduced by applying field self-cancellation effect.

3.7 Discussion

This chapter presented an analysis and PCB design for a class D inverter operating at 13.56MHz using MOSFET DRF1400. At high frequency, the parasitic

inductance becomes a major factor effects on the performance and stability of inverters. PCB design is a key solution to minimize parasitic elements in the circuit.

An optimal PCB design was proposed to achieve the better performance than that of conventional design. The ringing frequency increased 14.3%, the parasitic inductance reduced 23.4% . The stability of inverter also increased. In ringing loop, the trace length was minimized and the trace width also was maximized. Therefore the conduction loss of trace line was minimized. The switching performance of MOSFET was significantly improved and the switching power loss might reduce.

Chapter 4

Ringing damping design

4.1 Introduction

When the inverter operates at 13.56 MHz, the influence of parasitic elements becomes a major factor which effects to the performance and efficiency of inverter. Event with the optimization PCB layout design, the parasitic ringing always exists in the power loop of the inverter [33-36]. Fig. 4.1(a) shows the ringing loop in a half-bridge class D resonant inverter which is formed by the parasitic inductances in the ringing loop of the power circuit and the output capacitor of MOSFETs. At 13.56MHz, with optimization PCB layout which is presented in chapter 3, the frequency of parasitic ringing in the power loop ranges from 60 to 150 MHz depending mainly on the operating voltage. As the analysis in chapter 2, the parasitic ringing in the power loop has many negative consequences on the performance of switching converter. The ringing in drain-source voltage of MOSFET causes the increasing switching power loss on the MOSFETs [22],[26],[33-35]. The ringing current in power loop causes the increasing of conduction power loss and peak current of MOSFET. The conduction power loss on the circuit due to skin effect also increases when the ringing current is high and un-damp able. Furthermore, the ringing in the power loop also generates electromagnetic interference (EMI) which will effect to the driver circuit and other device leads to the unstable of inverter. Therefore, the ringing damping design is always very

importance at high frequency.

A number of damping methods have been proposed [33-36]. However, in the 13.56 MHz resonant inverter, these methods are difficult to implement or harmful with inverter. The most popular method is adding an RC snubber circuit parallel to the MOSFETs as presented in [35]. This method is especially widely used in low frequency inverter. But at high frequency, as the analyses in chapter 2, it will need longer time to change/discharge the voltage across the MOSFETs when it turn on or turn off while the time to switching is very short. As a result, to obtain ZVS condition, the MOSFETs have to operate at higher dv/dt condition and higher switching power loss. The larger ringing is generated which may make the inverter unstable.

Tuning the rising time and falling time of MOSFETs Gate-source voltage can reduce the slew-rate of MOSFETs drain current di/dt. Therefore this method can reduce the peak voltage and ringing amplitude. However, this method has a trade off with the switching power loss. Therefore, this method is often used to combine with other methods.

Adding an $R-C$ circuit parallel to the input voltage source of inverter as mentioned in [33]. This method can turn the damping coefficient of ringing loop by changing the value of resistor. But at high frequency, the parasitic inductance in the resistor and the parasitic inductance of trace line which connect between $R-C$ circuit and inverters MOSFETs will make the impedance of $R-C$ circuit very high. Therefore, the effectiveness of this circuit is low.

Using a ferrite bead place serial with ringing loop can significantly damp the ringing in the power loop as mentioned in [33]. But with the 13.56 MHz fundamental frequency and the ringing frequency ranges from 60 MHz to 150 MHz, it is difficult to find the ferrite bead which can work well at this situation. Furthermore in resonant inverter, a part of power current also goes through the ringing loop when the body diode of MOSFET conducts. Therefore, if a ferrite bead is added serial with the ringing loop, the power loss on the ferrite bead will be very high at high power and high frequency condition. Ferrite bead cannot work well in this case.

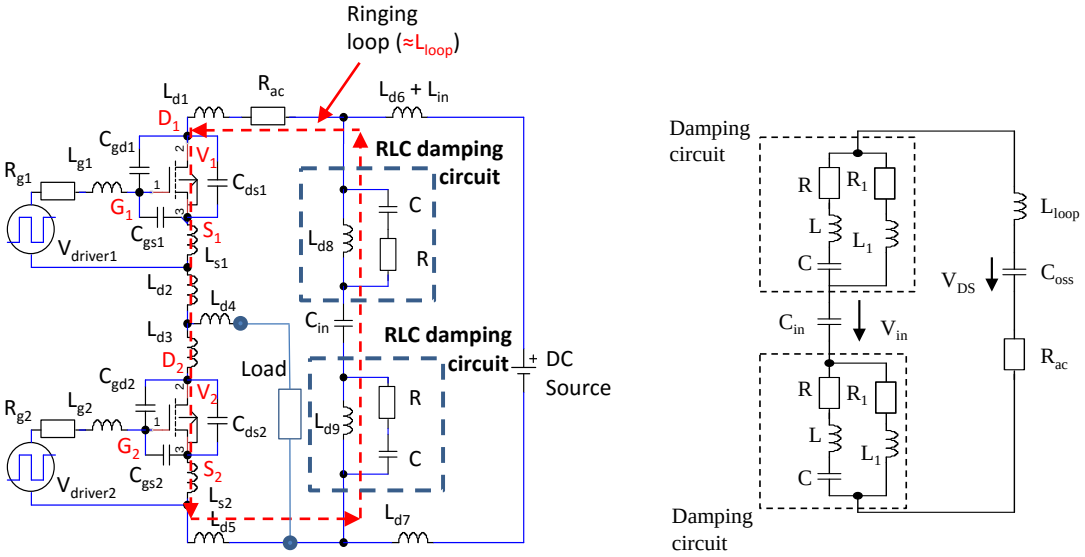
Adding a parallel resistor and inductor combination serial to the power loop as presented in [36]. This method can significantly suppress the ringing in power loop. However, this method is just appropriate with low power converter. At high power, when the power current is high, the power loss on the resistance will very high. Consequently, the efficiency will be low. Furthermore, when external inductor is added to the ringing loop, the parasitic inductance of ringing loop will be increased. It will affect to the performance of inverter.

In this chapter, a new ringing damping circuit is proposed which significantly damps the ringing in the circuit while keeps the low power loss on the damping resistor lead to the high efficiency of the inverter. The proposed circuit is presented in part 4.2. Then,the design method is shown in part 4.3. Part 4.4 illustrates the simulation results including FEA PCB simulation and circuit simulation. Finally, a 1.2 kW stable inverter with the efficiency of 93.1% is obtained in experiment which is presented in part 4.4.

4.2 Proposed ringing damping circuit

Fig. 4.1(a) shows the principle schematic of proposed method. Two RLC damping circuits are added to the DC-side of the inverter. Where L is the parasitic inductance of the trace lines which connect between input capacitors and MOSFET-Bridge. Therefore, in practical only two damping resistors R and and two capacitors C are added in the circuit. The capacitance of the capacitors will be calculated to resonate with the parasitic inductance of damping resistors at the ringing frequency. The value of resistor and inductance of trace lines are designed according to the damping coefficient and the power loss on the damping resistors. This proposed circuit obtains two advantages compare to the other methods as following:

- The power current of the inverter with the frequency of 13.56 MHz can not pass through the damping resistors because the RC circuit is designed to resonate at only the ringing frequency (around 100 MHz). Only the ringing current can pass through the RC circuits. Therefore the power loss on



(a) principle circuit (b) Equivalent circuit

Figure 4.1: Proposed damping circuit

the damping resistors is very small. By tuning the damping coefficient of the damping circuit, the ringing current will be consumed by the damping resistors and the ringing in the circuit will be damped. This circuit is able to apply in high power and high frequency inverter.

- The damping circuit is designed based on the trace lines which connect between input capacitors and MOSEFTs. The parasitic inductance of this trace lines are used as a component of damping circuit. Therefore the parasitic inductance inside the ringing loop can be controlled and the circuit board becomes more compact and stable.

4.3 Design the proposed damping circuit

The equivalent circuit of the ringing loop with damping circuit is shown in Fig. 4.1(b). Where the $L_1 = L_{d8} = L_{d9}$ is the parasitic inductance and R_1 is the parasitic resistance of the trace-lines which connect between the input capacitors

and MOSFET module, L is the parasitic inductance of damping resistor, R is the resistance of damping resistor and C is resonant capacitor in damping circuit. However, based on the calculation, the value of R_1 is about 0.00048 Ω which is very small in the comparison with the R_{ac}, R and the impedance of L_1 at the ringing frequency. Then it is negligible from the calculation to get the simpler equation. The transient of voltage across the MOSFETs can be calculated as shown in (4.1).

$$\frac{V_{DS}(s)}{V_{in}(s)} = \frac{(L+L_1)Cs^2 + RCs + 1}{[2LCL_1 + (L+L_1)CL_{loop}]C_{coss}s^4 + [2RL_1 + (L+L_1)R_{ac}]CC_{oss}s^3 + \\ + [(2L_1 + L_{loop} + RR_{ac}C)C_{oss} + (L+L_1)C]s^2 + \\ + (R_{ac}C_{oss} + RC)s + 1} \tag{4.1}$$

The (4.1) is too complicate to get the damping coefficient of the damping circuit. Therefore, the approximate calculation is required. In this design, the damping circuit is designed to damp the current at the ringing frequency where the L and C are resonance. Therefore, the L and C do not affect the damping coefficient of the damping circuit at the ringing frequency. To get the simpler calculation, the simple equivalent circuit of the ringing loop with the damping circuit is shown in Fig. 4.2(a). If the damping circuit is considered as a equivalent damping component in a normal RLC circuit, the transient of the voltage across the MOSFETs can be written as a second order system in (4.2) where the damping coefficient $\zeta(s)$ is the first order of the Laplace operator "s" included L_1 and R.

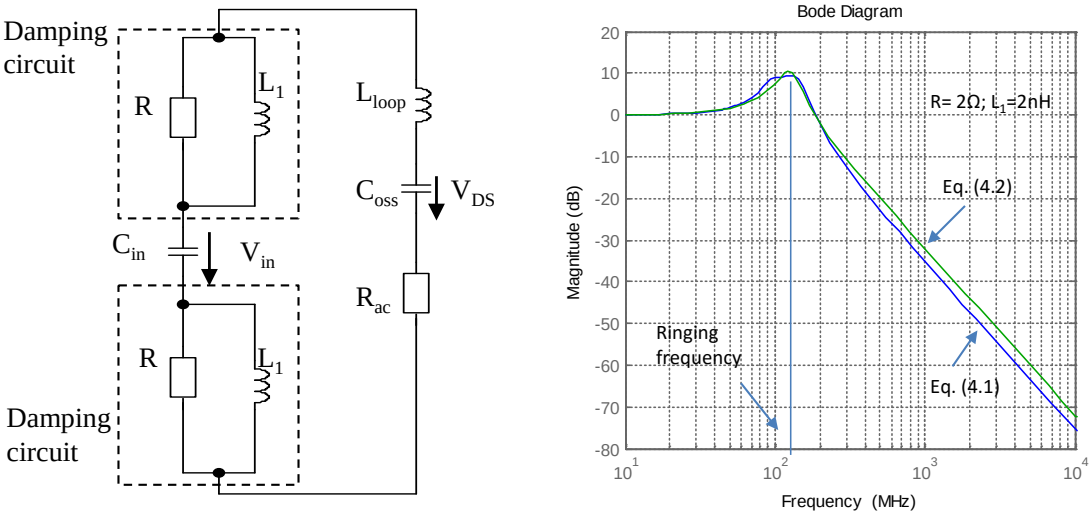
$$\frac{V_{DS}(s)}{V_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.2}$$

where

$$\omega_n = \frac{1}{\sqrt{L_{loop}C_{oss}}} \tag{4.3}$$

$$\zeta(s) = \frac{1}{2}\sqrt{\frac{C_{oss}}{L_{loop}}}\left(R_{ac} + 2\frac{RL_1 s}{L_1 s + R}\right) \tag{4.4}$$

Fig. 4.2(b) shows the frequency response of (4.1) and (4.2). The results show that the error of the damping coefficient between two cases are acceptable.



(a) Simple equivalent circuit

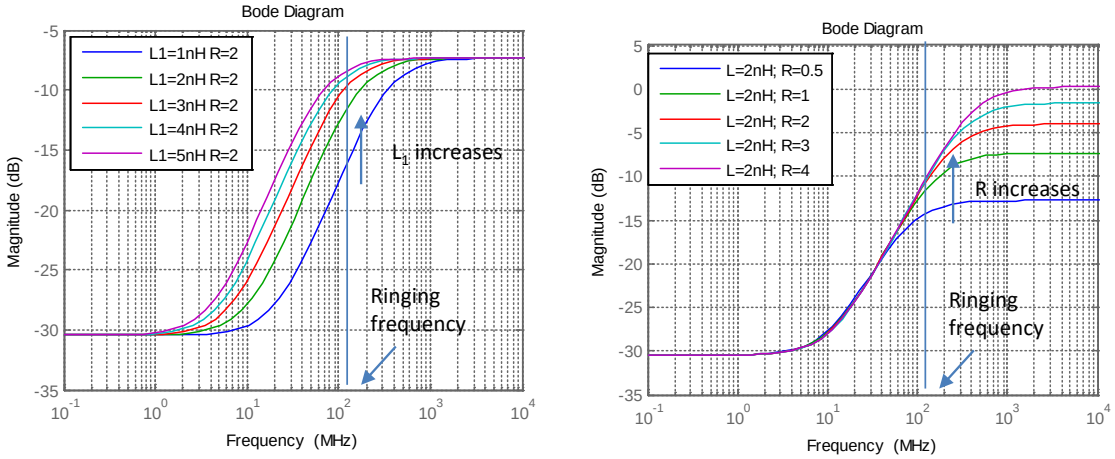
(b) Frequency response comparison

Figure 4.2: Simple equivalent circuit of the ringing loop with the damping circuit

Therefore, the (4.2) can be used to design the damping circuit based on the investigation of the damping coefficient which is shown in (4.4). With the parameters as shown in table 4.1, fig. 4.3 shows the frequency response of $\zeta(s)$ with the changing of the parameter of the damping circuit L_1 and R. The results show that at the ringing frequency, the value of the damping coefficient significantly increases when L_1 increase. However, with the changing of R, the damping coefficient does not increase so much from $R = 1\Omega$. Therefore, the damping resistor $R = 1\Omega$ was chosen.

Fig. 4.4 shows the frequency response of (4.1) with the changing of L_1. The results have the same trend with the results in fig. 4.3(a). The damping coefficient significantly increases when the inductance L_1 increases.

Fig. 4.5 shows the power loss on the damping resistors, the output power and the efficiency of inverter when the inductance L_1 increase. This is circuit simulation result when the damping resistance and the parasitic inductance of damping resistance are kept constant as shown in the figure. The resonant capacitor is



(a) Damping coefficient depends L_1

(b) Damping coefficient depends R

Figure 4.3: Frequency response of the damping coefficient $\zeta(s)$ with the changing of L_1 and R

calculated by (4.5)

$$C = (L_{mod} + L_1)C_{oss}/L \tag{4.5}$$

The other simulation parameters are shown in Table 4.1.

When the inductance L_1 increases, the damping coefficient is increased while the power loss on the damping resistor also increases which causes the reducing of the inverter's efficiency. Therefore the choosing of L_1 is the trace-off between damping coefficient and the efficiency of the inverter. The power loss on the damping resistor should be considered in experiment design. In this design, the inductor L_1=2 nH and the resonant capacitor $C = 470$ pF are chosen. The power loss on the damping resistors is 3.78 W as shown in fig. 4.5. Two 2 Ω/3 W metal foil resistors are used in parallel connection.

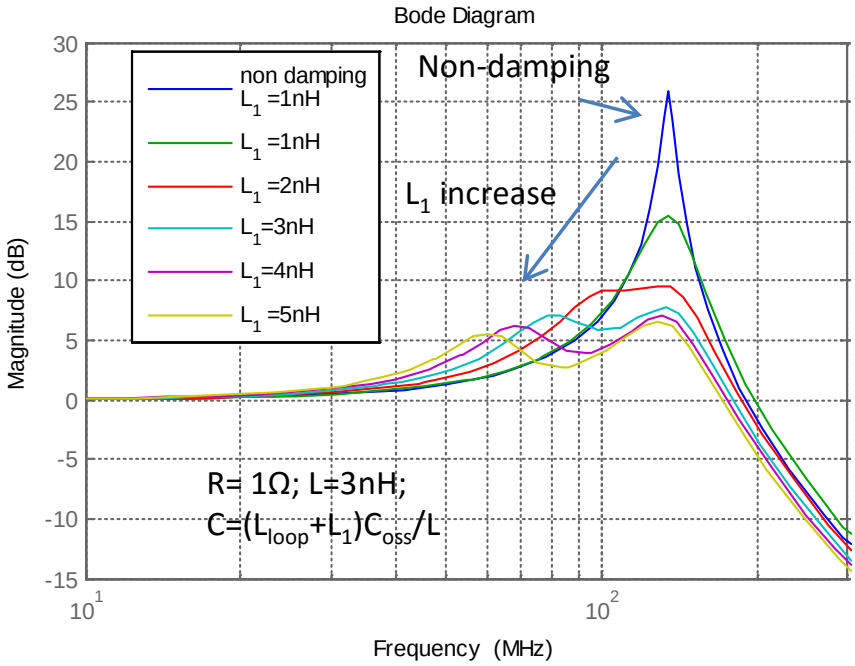
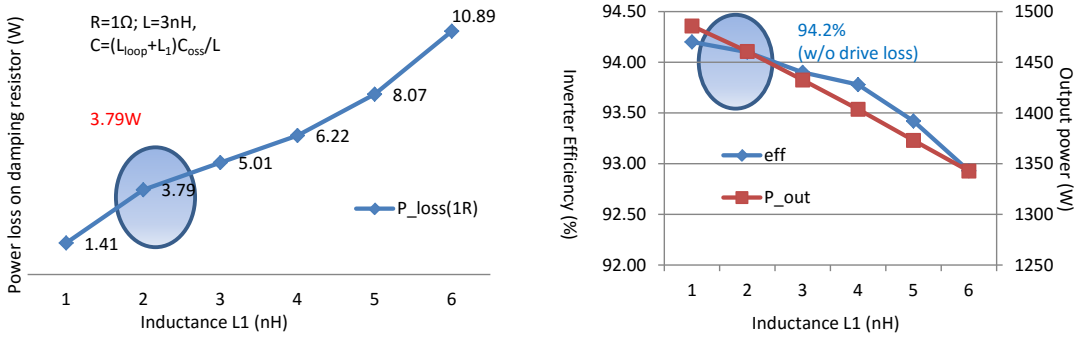


Figure 4.4: Frequency response of Eq. (4.1) with the changing of L_1

4.4 Simulation

4.4.1 PCB simulation

In the proposed damping circuit, the inductor L_{d8} and L_{d9} are made from the parasitic inductance of the PCB trace lines. To obtain the required value of these inductors, the PCB is designed and simulated by a full-wave electro-magnetic (EM) simulations using Sonnet em as shown in Fig. 4.6. The PCB simulation method and simulation parameter are the same with part 3.5 in chapter 3. The PCB trace lines are tuned to obtain the required valued as shown in Fig. 4.6.



(a) Power loss on damping resistor

(b) Efficiency and output power of inverter

Figure 4.5: Circuit simulation results with the changing of the inductor L_1

Table 4.1: Circuit simulation parameters

Parameter	**Non-damping**	**Proposed method**
Input voltage	250V	
Resonant load	L_5=228 nH; $C_3 = 1\mu$F;$C_4 = 800$ pF;$R = 50\Omega$	
MOSFET	DRF1400	
R_{ac}	0.3 Ω	
L_{loop}	$L_{d1} + L_{s1} + L_{d2} + L_{d3} + L_{s2} + L_{d5}$=4.8 nH	
$L_{d8} = L_{d9} = L_1$	1 nH	1 nH to 6 nH
R	none	1Ω +3 nH
C	none	Base on (4.5)

4.4.2 Circuit simulation

Fig. 4.7 shows circuit simulation results of the drain-source voltage and drain current waveform of the inverter in case of non-damping and damping design. Fig. 4.7(a) shows the results in case of non-damping design with the parameter of proposed PCB design (L_1=1 nH . Fig. 4.7(b) is the results when the proposed damping circuit is applied with the inductance L_1=2 nH. The results show that comparing with non-damping, when the damping circuit is applied, almost of ringing in current and voltage is damped. The peak voltage across the MOSFETs is reduced. As a result, the turn-off power loss on MOSFET will be reduced. The

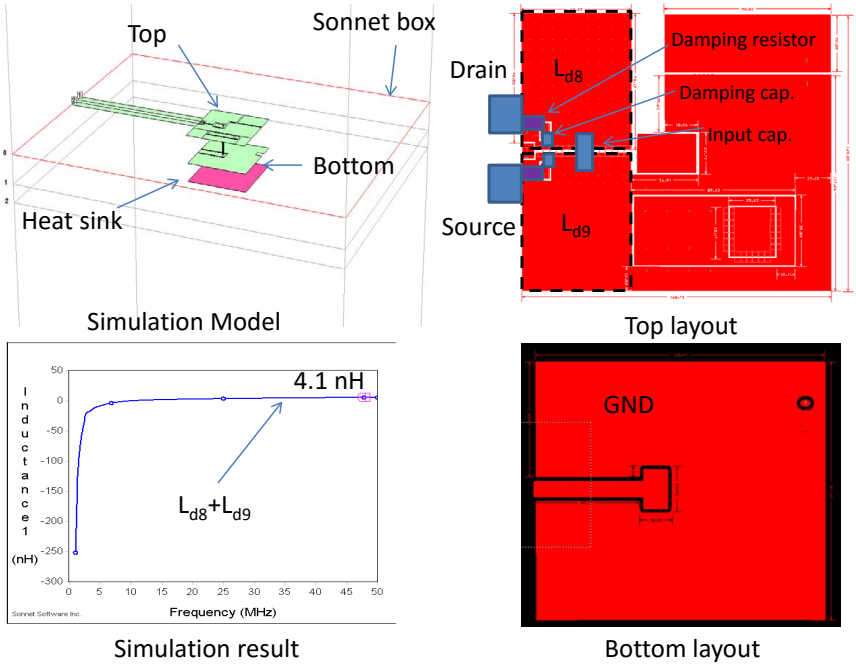
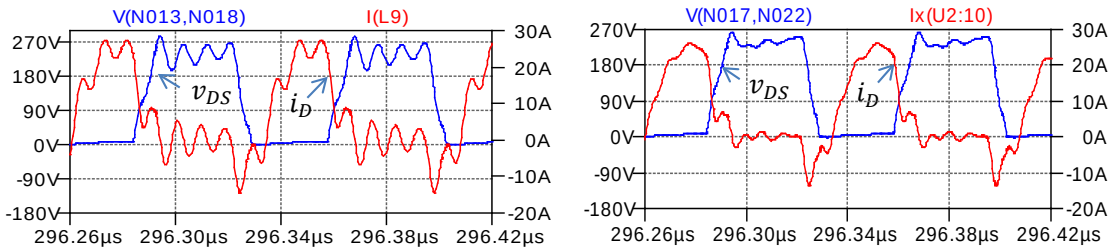


Figure 4.6: PCB simulation

ringing current in drain current of MOSFET significantly reduces. Therefore, the peak current and the conduction loss on the MOSFET are reduced.

Fig. 4.8 shows the circuit simulation results of the power loss on the components in the 1.5 kW 13.56 MHz resonant inverter in two cases. The results show that, when the damping circuit is applied, the power loss in the MOSFET is reduced from 4.51% to 3.76% because of the reducing of conduction loss and turn-off loss. The power loss on the resistors of the damping circuit is lightly smaller than the power loss which is reduced from MOSFETs. Therefore, the overall efficiency of inverter is lightly increased. The power loss on the MOSEFTs which is cause of ringing current is moved to resistors of damping circuit.



(a) Non-damping (b) Damping

Figure 4.7: Drain-source and drain current of MOSFETs

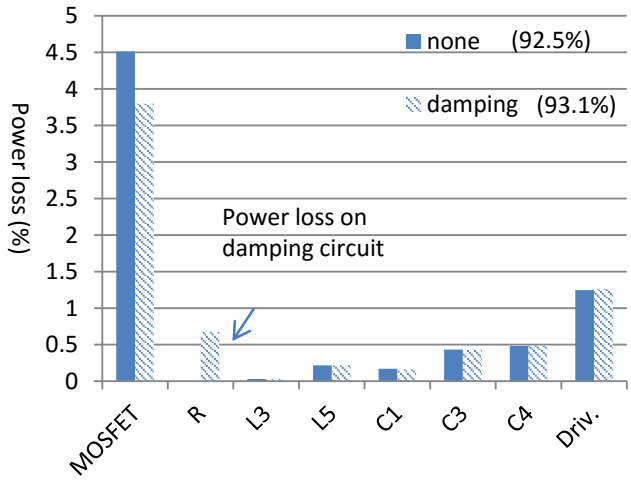


Figure 4.8: Power loss on 13.56 MHz resonant inverter at 1.5 kW

4.5 Experiment result

To verify the effectiveness of proposed damping circuit, two separate boards are compared:

- Board 1: Proposed PCB layout without damping circuit which is proposed in section 3.
- Board 2: Proposed PCB layout with proposed damping circuit

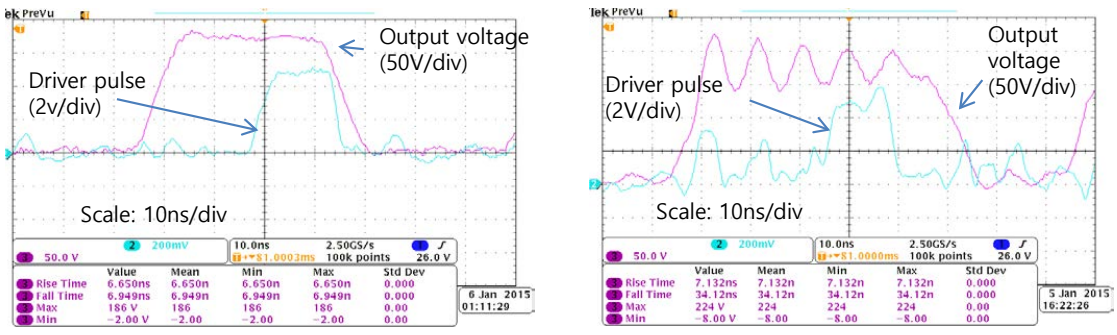
All of boards are made from the same type of copper board and all of devices using on each board are the same. Measurement point is shown in Fig. 4.1(a).

The output voltage waveform includes of the voltage across low-side MOSFET V_2 and the voltage across parasitic inductances as shown in Fig. 4.1(a). In this case, the current was not measured because the attaching of current measurement device in the ringing loop will increase the parasitic in this loop.

The experiment is performed with the parameter which is shown in Table 4.1. The damping resistor is made from two resistors in parallel which have resistance is 2 Ohm and parasitic inductance is 6 nH. The damping capacitor is very high Q capacitor. The capacitance is tuned around 470 pF.

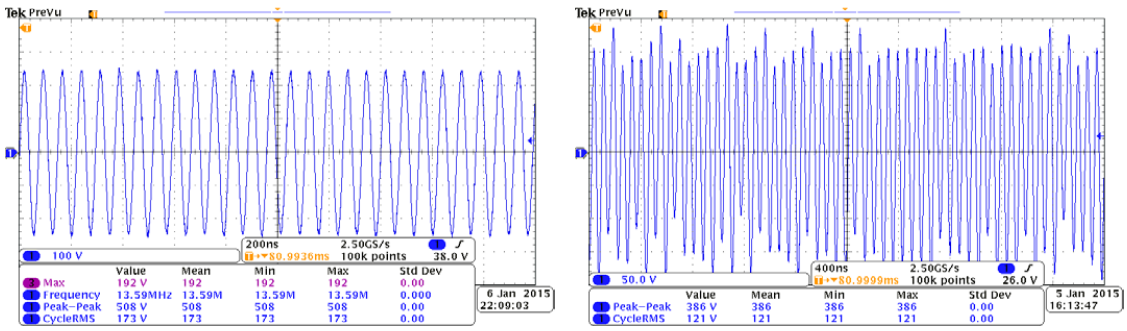
The experiment results show that in case of damping circuit is applied, the output voltage waveform and the driver pulse waveform are clear. The ringing is damped. Fig. 4.9 shows the output voltage waveform in two cases when the input voltage is 180 V. The driver pulse in case of non-damping circuit has noise and it makes the circuit unstable. Fig. 4.10(b) shows the load voltage in case of non-damping circuit when the circuit is unstable.

Fig. 4.11(a) shows the relationship between output power and efficiency of inverter in both simulation and experiment with damping and non-damping board. The results show that when the damping circuit is applied, the efficiency of inverter increases in both simulation results and experiment results. But in experiment the different of efficiency in two cases is much higher than simulation because in simulation we did not simulate the effect of EMI noise from power circuit to driver circuit and the noise in the isolation device due to high dv/dt.



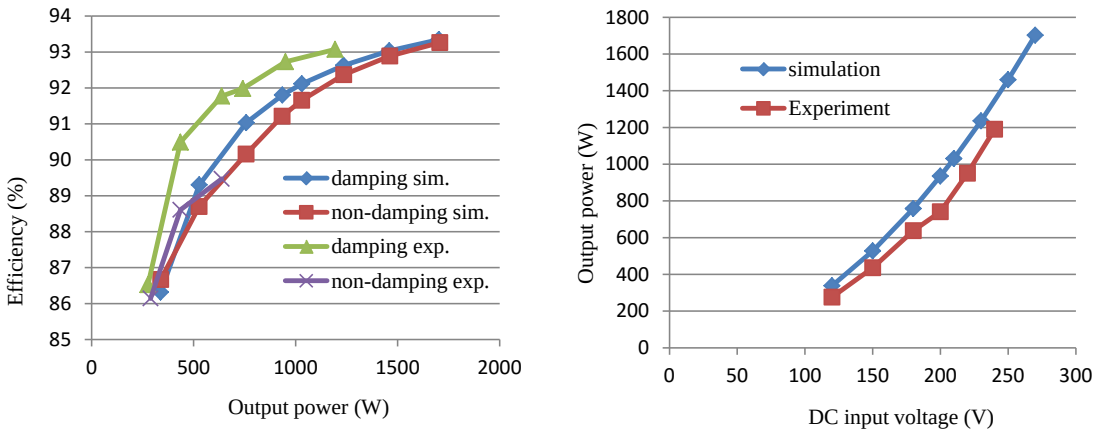
(a) Damping (b) Non-damping

Figure 4.9: Output voltage and drive pulse waveform (input voltage = 180V)



(a) Damping (scale: 200ns/div; 100V/div) (b) Non-damping (scale:400ns/div; 50V/div)

Figure 4.10: Load voltage waveform (input voltage = 180V)



(a) Output power and efficiency (b) Input voltage and output power

Figure 4.11: Power and efficiency test results

The noise in driver circuit effects to the driver pulse and reduces the efficiency of inverter. When the input voltage increase, the current inside the circuit is increased and the dv/dt is also increased. As a result, the noises which effect to the driver circuit also increase. Therefore, in experiment when the input voltage is increased, the different of efficiency between damping and non-damping circuit is increased. And when the input voltage reaches to 180 V, the non-damping circuit board is unstable. The root cause is confirmed that the signal from isolation device is noised.

The power loss on the damping resistor is recorded which ranges from 4-7 W when the input voltage increases while the efficiency of damping board is higher than non-damping board. Therefore, the power loss on the MOSFET will be reduced in damping board compare with non-damping board.

Fig. 4.11(b) shows the relationship between input voltage and output power. With the same DC input voltage, in experiment the output power is smaller than that in simulation because of error in output circuit parameter and the dead time of drive pulse. In experiment, the operating point of inverter is nearer class DE than that in simulation. Therefore the efficiency in experiment is higher while the output power is smaller than that of simulation.

4.6 Discussion

The ringing exists in the circuit event with the optimized PCB design. The proposed damping method can significantly attenuate the ringing in the power loop. The power loss on the MOSFETs is reduced. The EMI noise is suppressed and the circuit was more stable. With the proposed design, the parasitic inductance of the trace lines which connect between input capacitors and MOSFET module becomes a part of damping circuit. Therefore, the parasitic inductance in the ringing loop can be controlled and the circuit board becomes more compact and stable.

Finally, the efficiency of the inverter obtained 93.1% efficiency at 1.2 kW output power. This is an improvement in the comparison with the previous researches. However, it did not meet the required efficiency of over 95% for the dynamic charging system. Further researches are required to improve the efficiency and increase the output power of the inverter.

Chapter 5

Evaluation of 600V cascode GaN HEMT in 13.56MHz inverter

5.1 Introduction

At 13.56 MHz inverter, the switching power loss is the major part which impacts the efficiency of the inverter. As the presents in previous chapters, by optimized PCB design and ringing damping design, a 1,2 kW inverter with the efficiency of 93.1% is obtained using silicon MOSFET which is a significant improvement. However, it is difficult to obtain the efficiency of over 95% by using silicon MOSFET because of the limited of the switching speed. A faster switching device will improve the efficiency of inverter base on the reducing of switching power loss. It has been well documented that GaN devices have much less switching loss compared with silicon devices [13,15,37-41]. The GaN devices show potential for improving efficiency of 13.56 MHz inverter [13,15].

Recently, enhancement-mode (normally OFF) and depletion-mode (normally ON) GaN switches are available. The depletion-mode switches usually have a lower ON-resistance and a smaller junction capacitance than the enhancement-mode switches [38], therefore the depletion-mode GaN switches is better for high power and high frequency application to obtain high efficiency. To easily control the normally ON device by using commercial drive IC, a low-voltage silicon MOS-

FET is used in series to drive the GaN HEMT, which is well known as cascode structure which is shown in Fig. 5.1. This paper analyses the basic characteristics of Cascode GaN HEMT in section 2 in point of view of high switching frequency application.

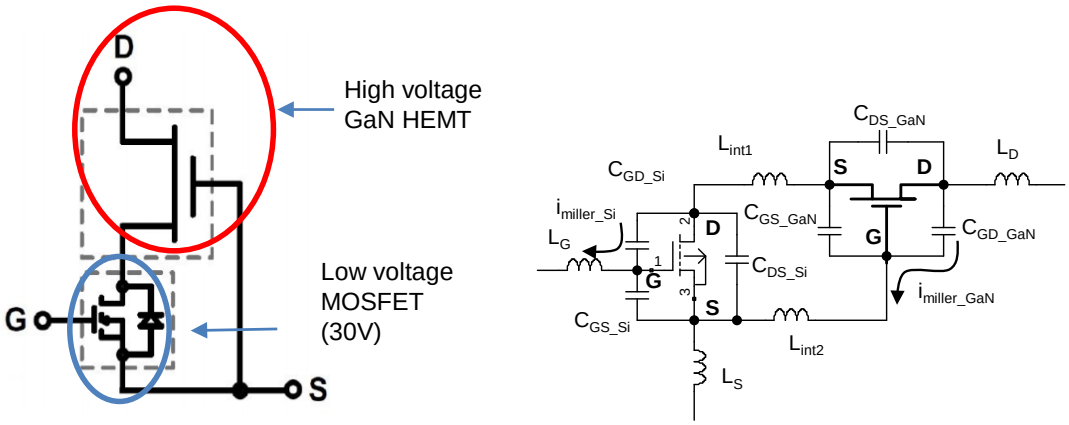
The first generation of cascode GaN HEMT from Transphom was packed in TO220 package type. The large parasitic inductance inside the devices is the disadvantage of this device when applying in high switching frequency converter. This chapter investigates the characteristic and evaluates the application potential of TO220 GaN HEMT in 13.56MHz inverter. The gate drive design for cascode GaN HEMT at 13.56 MHz half-bridge inverter is also presented in detail.

5.2 Characteristic of Cascode GaN HEMT

Fig. 5.1(a) shows the basic structure of cascode GaN HEMT. It includes one low voltage normally OFF Silicon MOSFET connected in series with a high voltage normally ON GaN HEMT. The Drain-Source voltage of the MOSFET controls the turn-on or turn-off process of the GaN HEM. The switching speed of the GaN HEMT is much faster than that of the MOSFET. Hence, the switching characterisitc of MOSFET does not affect the switching performance of the cascode GaN HEMT. Furthermore, in the cascode GaN HEMT, the power loss mainly takes place on the GaN HEMT because the low rate-voltage MOSFET has a low On-resistance and a low switching power loss due to the switching under a low voltage condition. Therefore, the gate resistor plays a negligible role on the switching characteristic of the cascode GaN HEMT[38-40].

The GaN HEMT channel does not have any body diode as shown in Fig. 5.1(a). The current can pass through the GaN HEMT channel in both directions when the gate is turned ON. This characteristic makes the low power loss in reverse mode of the cascode GaN HEMT when it is used in resonant inverter.

The miller capacitor always strongly affects the switching performance of silicon MOSFET at MHz range switching frequency. However, in the case of the



(a) Basic structure (b) Parasitic model

Figure 5.1: The structure of cascode GaN HEMT

cascode GaN HEMT as shown in Fig. 5.1(b), the parasitic capacitor in drain-gate of the GaN HEMT C_{GD_GaN} which causes the miller effect does not affect its gate-source voltage. The low voltage MOSFET naturally is affected by its miller capacitor. But as the previous analysis, the switching characteristic of low voltage MOSFET does not affect the switching characteristic of cascode GaN HEMT. Therefore the miller effect is negligible in cascode GaN HEMT structure. This is one of the advantages of the cascode GaN when applying in high frequency applications.

Table 5.1 shows the comparison of the key parameters between the first generation high voltage cascode GaN HEMT TPH3006 and the RF power Silicon MOSFET DRF1400. It shows that, all of the parasitic capacitors of the cascode GaN HEMT is much lower than that of the silicon MOSFET. Hence, the cascode GaN HEMT more suitable than the silicon MOSFET in high switching frequency applications. With the lower output capacitor, the cascode GaN HEMT have the faster switching speed which will reduce the switching power loss. In the half-bridge resonant inverter, the faster switching speed also can reduce the conduction power loss by the reducing of the dead time. With the lower input capacitor, the drive power loss of the cascode GaN HEMT will reduce. This is a suitable characteristic for the multiphase inverter with a large number of phase where the drive power loss takes a counted part in the power loss of the inverter.

The commutating dv/dt capability of cascode GaN HEMT is also much higher than that of Silicon MOSFET because the equivalent reverse transfer capacitance of GaN HEMT is 3.6 pF in the comparison with 75 pF of silicon MOSFET.

Table 5.1: Key parameter comparison between cascode GaN HEMT and RF silicon MOSFET

Parameter	TPH3006	DRF1400
V_{ds}(V)	600	500
I_D(A)(25^0C)	17	24
$R_{DS(on)}$(Ω)	0.15	0.24
C_{oss}(pF)(at 200 Vdc)	60	190
C_{iss}(pF)	740	1890
C_{rss}(pF)	3.6	75
Q_g(nC)	6.2	-

As the result in [40-41], the estimation value of the parasitic inductance in the TO220 packing type of GaN HEMT is shown in Table 5.2.

Table 5.2: Package parasitic inductance of TPH3006

L_D	0.6-1 nH	L_S	3.1-3.8 nH	L_G	1.6-1.9 nH
L_{int1}	0.2-0.4 nH	L_{int2}	0.5-1 nH	-	-

5.3 Half-bridge inverter with Cascode GaN HEMT

5.3.1 Inverter design

The half-bridge inverter using cascode GaN HEMT is shown in Fig 5.2. the ringing loop is formed by the parasitic inductance of the loop including of two switches, input capacitors and output capacitor of switching devices . In this case, the parasitic inductance of ringing loop is higher than 10nH. As the analysis in chapter 2, at 13.56 MHz the output voltage will be almost of ringing if the

inverter operates at class D mode. The switching characteristic of switching devices will depend on the ringing frequency. The switching loss will be very high and the switching devices may be broken. Due to the package structure of casecode GaN HEMT, it is difficult to reduce the parasitic inductance of ringing loop. Furthermore, as the simulation results shown in Fig. 5.3, the top picture

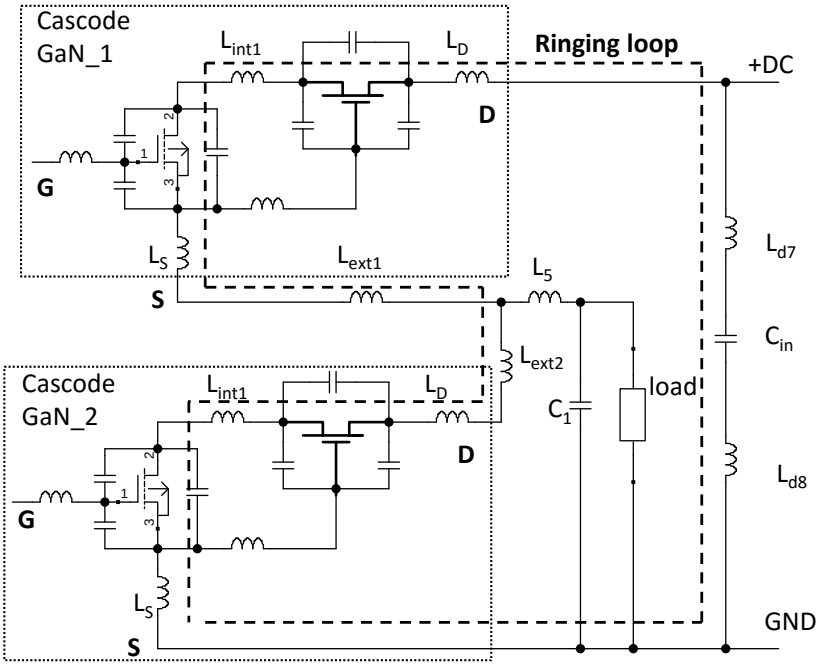


Figure 5.2: Half-bridge inverter using cascode GaN HEMT

is the voltage across the drain-source of MOSFET and the bottom picture is it in GaN HEMT and whole device. It shows that, when the inverter operates at class D mode with large parasitic inductance in the ringing loop , the ringing in the voltage across drain-source of low voltage MOSFET excess the maximum voltage of this MOSFET drive the MOSFET to avalanche operation mode. In this mode, the ringing current will pass through the body diode of MOSFET and make the additional power loss. Therefore, with TO220 packing type, the half-bridge inverter should not operate in class D mode due to the large parasitic inductance. Operating at Class DE mode is better solution in this case.

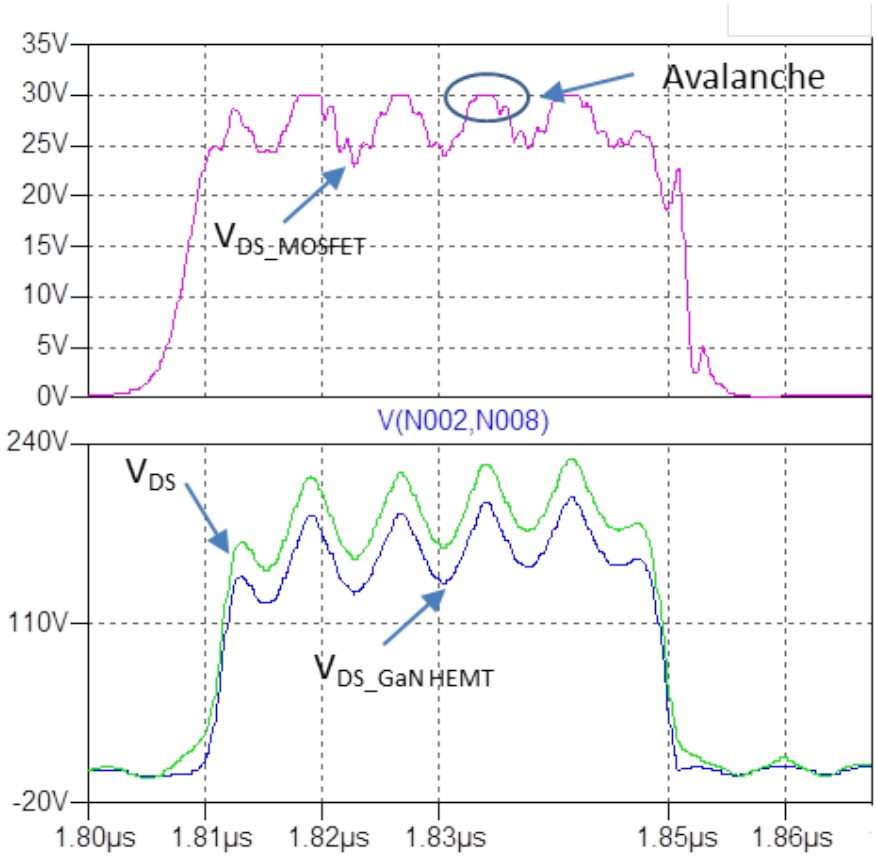


Figure 5.3: The avalanche problem

5.3.2 Gate drive design

Drive design is always the challenge for high switching frequency inverter design due to the effect of parasitic elements, high switching power loss on the drive IC and the unstable due to the common mode noise. At high switching frequency, the resonant drive circuit is recommended to use to reduce the drive power loss and the required peak current of drive IC. However, in this case, the GaN HEMT device is used for the power circuit. The drive power loss is much reduced. Furthermore, the dead time of the drive signals need to be controlled exactly to obtain class DE operation mode. Therefore, in this design, the conventional drive circuit is satisfied.

5.3.2.1 Drive IC selection

At high frequency applications, the choosing of the drive integrated circuit (IC) mainly depends on two parameters which are peak output current and the maximum allowable power dissipation of the drive IC. Normally, the output peak current of the drive IC is always considered because of the required drive voltage rise/fall time [42-43]. However, at very high switching frequency condition, the dissipation power on the drive IC is extremely high in the comparison with the low switching frequency case. Therefore, the consideration of the maximum allowable power dissipation of the drive IC is required.

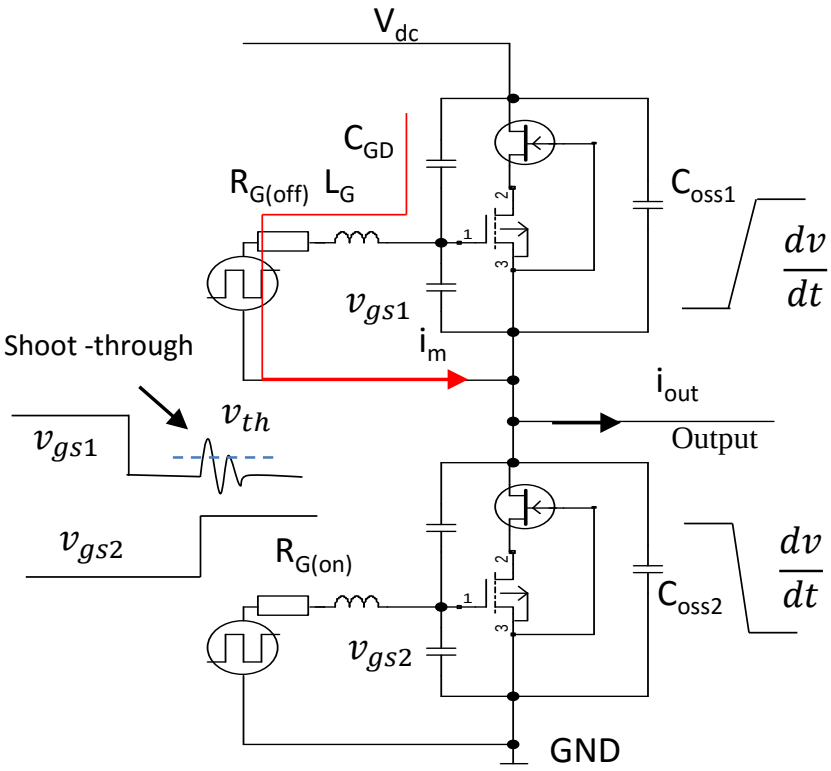


Figure 5.4: Miller effect in half-bridge inverter

As shown in Fig. 5.4, when the lowside switch is turned on, there is a current i_m pass through the drive circuit of high-side switch due to the changing voltage

across the miller capacitor C_{GD}. To avoid the shoot-through due to the feedback effect of miller capacitor, the turn-off resistor of gate drive circuit must be satisfied the condition as shown in (5.1).

$$L_g\frac{di_m}{dt} + R_{G(off)}i_m - v_{gs(off)} - L_s\frac{di_{ringing}}{dt} < V_{th} \tag{5.1}$$
$$i_m \approx C_{GD}\frac{dv}{dt}$$

where $v_{gs(off)}$ is the voltage of drive circuit apply to the MOSFET when turn it off; V_{th} is the threshold voltage of the cascode GaN HEMT; $R_{G(off)}$ includes the internal gate resistance of the cascode GaN HEMT R_{Gi} , internal resistance of drive IC R_{drv} and external turn-off gate resitance R_G .

Normally, the internal gate resistance is not defined in the datasheet. In this case, the internal gate resistance of the cascode GaN HEMT is measured by a network analyzer in impedance analyzer mode at 13.56 MHz as show in Fig. 5.5. Two ports of the network analyzer are connected to the gate and source terminals of the cascode GaN HEMT while the drain and source terminals are shorted together [44]. With 2.4 Ω internal gate resistance, 1.8 V threshold voltage and 100 V/ns slew rate voltage capacity, the no external gate resistance is required in this design. Then, the required peak output current of the drive IC is estimated as (5.2).

$$I_{peak} = \frac{V_{drive}}{R_G} \tag{5.2}$$

The dissipation power on the drive IC can be estimated as shown in (5.3)

$$P_{G_{loss}} = 2C_{iss}V_{drive}^2 f_{sw} \tag{5.3}$$

Normally, the allowable dissipation power of the drive IC is not defined in the datasheet. However, it can be estimated base on the thermal resistance value which is defined in the datasheet as shown in (5.4).

$$P_D = \frac{T_j - T_A}{\theta_{jA}} \tag{5.4}$$

where the T_j is the junction temperate; T_A is the ambient temperate and θ_{jA} is the thermal resistance between junction and ambient. In this design, IXRFD630 RF MOSFET drive from IXYS has been selected.

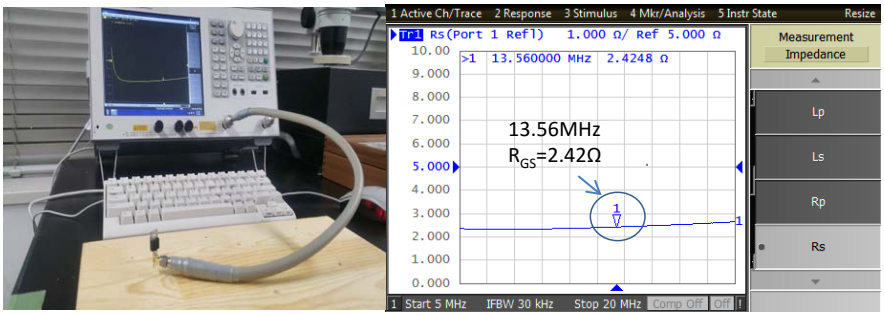


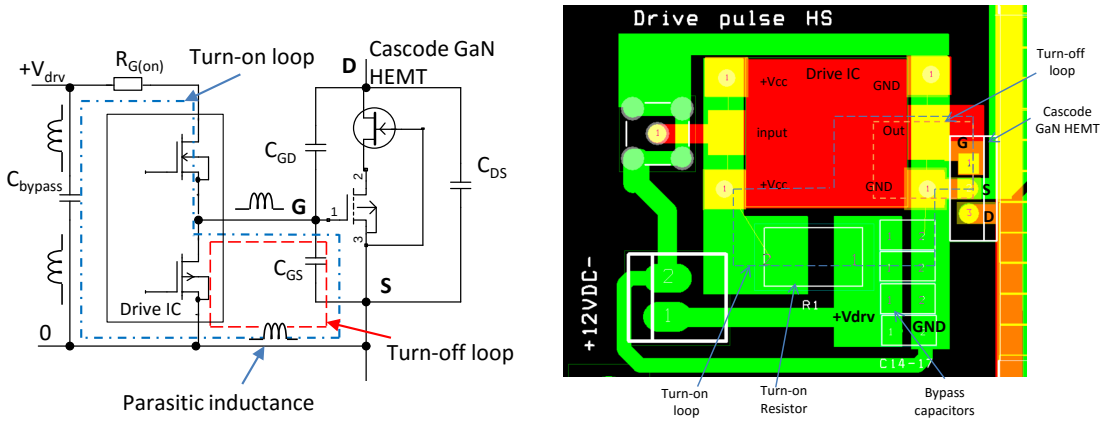
Figure 5.5: Internal gate resistance measuring

5.3.2.2 PCB design

The current loop in turn-on and turn-off process of the drive circuit is shown in Fig. 5.6(a). The PCB design and the devices selection must minimize the parasitic inductances in these loops. The parasitic inductance in the turn-on loop is larger than that of the turn-off loop due to the parasitic inductance of the bypass capacitor of the drive power source. Then, an existing ringing in the turn-on loop may make the drive circuit unstable. A resistor $R_{G(on)}$ is added which acts as the damping resistor in the turn-on loop while does not affect the condition (5.1) as shown in fig. 5.6(a). The PCB design is shown in Fig. 5.6(b). The metal foil resistor and the multilayer ceramic capacitors are used to obtain low parasitic inductance.

5.3.2.3 Isolation common mode noise immunity

It becomes a challenge in the high-side drive circuit design due to the floating high-side drive ground with very high dv/dt. The proposed design solution is shown in Fig. 5.7. The circuit design, components selection and PCB design become extremely critical. Fig. 5.7 shows the common mode current in the high-side drive circuit due to high dv/dt and the stray capacitor between ground of high-side drive circuit and ground of power circuit. The common mode current can be calculated by (5.5) and the effect of common mode current to the drive



(a) Turn-on and turn-off current loop in drive circuit

(b) Layout design

Figure 5.6: PCB design for drive circuit

pulse is expressed in (5.7).

$$i_{cm} = (C_{stray1} + C_{stray2}) \frac{dv}{dt} \tag{5.5}$$

$$i_{cm} = i_{cm1} + i_{cm2} + i_{cm3} \tag{5.6}$$

$$v_{p1} = v_p + i_{cm1} Z_2 - i_{cm2} Z_3 \tag{5.7}$$

To obtain high isolation common mode noise immunity, the optical fiber links or transformer are widely used. In this design, the proposed solution leads to more compact design by using integrated IC ISO721M. This device can obtain 50 kV/μs for typical common mode noise immunity, maximum delay skew of 2 ns and the isolation voltage up to 4000V RMS.

The structure of the drive pulse generator is shown in Fig. 5.8. The value of stray capacitor C_{stray2} which is shown in Fig. 5.7 depends on the isolation between the ground of drive pulse generator circuit and ground of the power circuit. Therefore, as shown in Fig. 5.8, the isolation device is also used for the low-side drive circuit to isolate two that grounds. The high isolation DC power source is used for drive pulse generator circuit that also reduces the stray capacitor C_{stray2}.

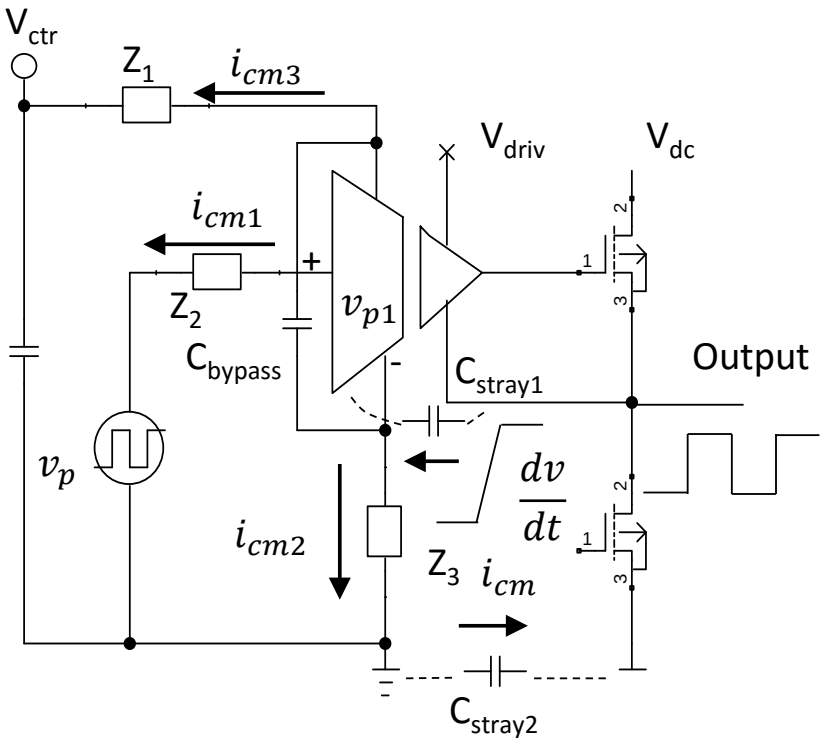


Figure 5.7: Common mode current in high-side drive circuit

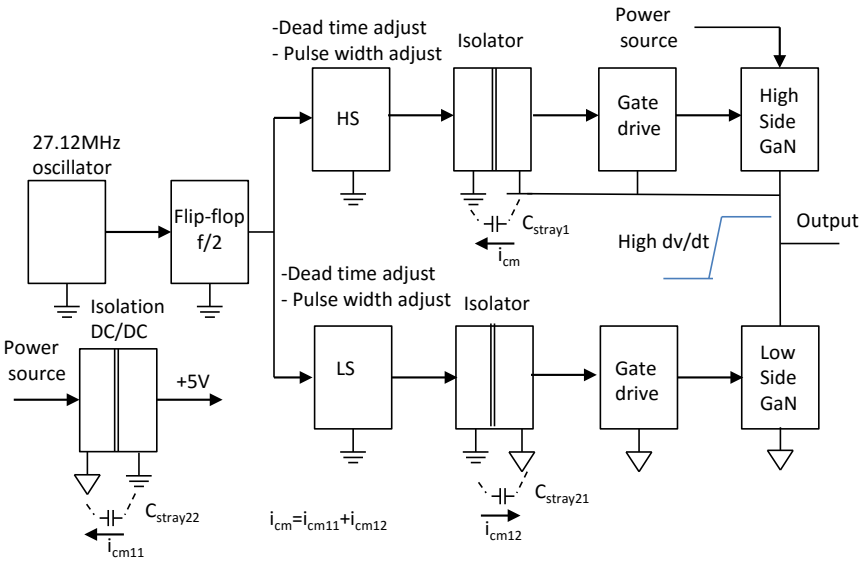


Figure 5.8: Structure of drive pulse generator circuit

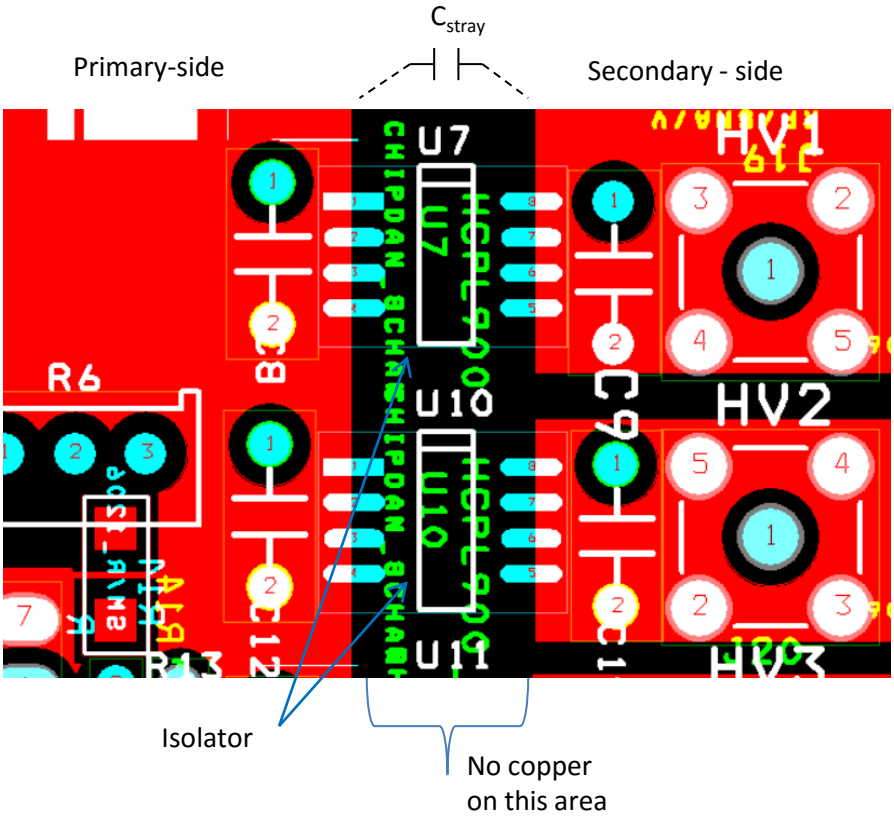


Figure 5.9: PCB design for drive pulse generator circuit board

The PCB design in drive pulse generator circuit is also very importance because that affects the value of the parasitic capacitors C_{stray1} and C_{stray2}. To obtain the low value of these parasitic capacitors, the PCB design must separate the PCB aria of each side where is isolated by the isolation devices. The distance among these arias is as large as possible. The PCB design around the isolation devices in the drive pulse generator circuit board is shown in Fig. 5.9. The aria between the primary-side and secondary-side of the isolation device is designed with no copper to obtain lowest parasitic inductance.

5.4 Evaluation of cascode GaN HEMT in 13.56 MHz inverter

To compare the GaN HEMT TPH3006 and the silicon MOSFET DRF1400, two inverters are tested at the same input dc voltage and the same output circuit. The dead time is turned for both of inverter operating at class DE mode. The experiment parameters are listed in the Table 5.3.

Fig. 5.10 shows the prototype of 13.56 MHz inverter using TPH3006. The PCB is design to minimize the parasitic inductance in the ringing loop. Fig. 5.11 shows the drain-source voltage and gate source voltage waveform of low side GaN switch in class DE operation mode. The rising time and falling time of drain-source voltage is 6.5 ns and 4.6 ns respectively at 200 V input voltage. It is difficult to exactly measure the rising time and falling time in this case because a few nanosecond will be added due to the rising / falling time of probe and oscilloscope. But it can be estimated that the dv/dt in this case is over 50 kV/μs and there is no commutating effect in the gate-source voltage of high-side MOSFET. It also was observed that the delay turn off time of the cascode GaN HEMT is about 11 ns. This is importance value to count on the dead time of the half-bridge inverter.

Fig. 5.12 shows the experiment result of the drain-source voltage in the comparison with the inverter using Silicon MOSFET. The results show that the rising

Table 5.3: Comparison experiment parameters

Parameter	TPH3006	DRF1400
Input voltage	100-200V	
switching frequency	13.56 MHz	
Drive voltage	0-12 V	
Dead time (t_{dm})	16	19
Resonant circuit	L=228 nH; C=800 pF	
Blocking capacitor (C_b)	0.01 μF	
RF load	50 Ω	

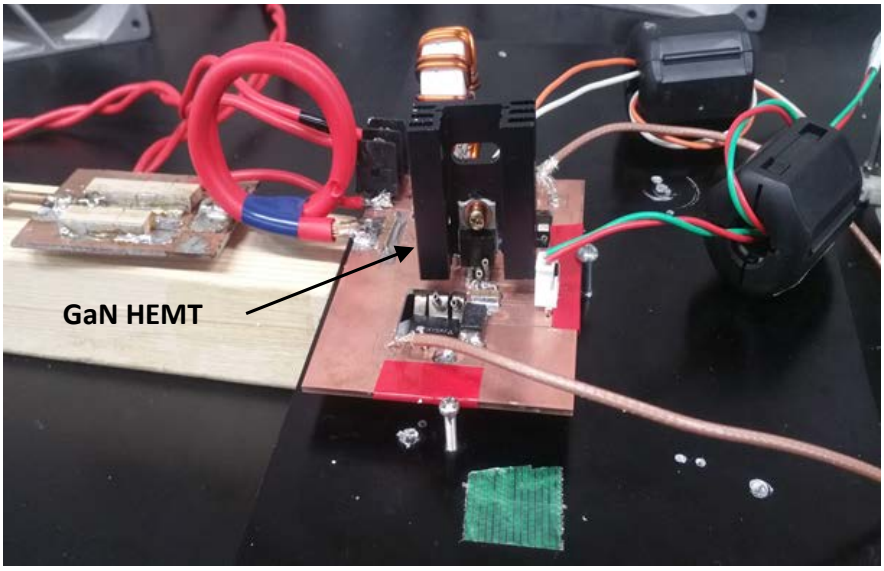


Figure 5.10: Prototype of 13.56 MHz inverter using cascode GaN HEMT

time and falling of the cascode GaN HEMT TPH3006 are always shorter than that of the RF silicon MOSFET DRF1400 about 3 ns. Therefore, to obtain the class DE operation mode, the required dead time of the silicon MOSFET inverter is longer than that of the GaN HEMT inverter about 3 ns. Hence, the conduction power loss increases at the same output power. In experiment results, without the consideration about the drive power loss, the efficiency of the GaN HEMT inverter is aways higher than that of the silicon MOSFET inverter about 2-3% as shown in Fig. 5.13(a). The drive power loss is 3.6 W with cascode GaN HEMT inverter and 18 W with RF silicon MOSFET inverter. Then the efficiency of the module using cascode GaN HEMT obtains 98.6% peak efficiency which is higher than that of the inverter using silicon-MOSFET about 3.5%. To change the output power, the input dc voltage is changed with the changing of the dead time to obtain the class DE mode. At low output power condition, the drive power loss takes a countable part in the total power loss of the inverter. Hence, the efficiency of the GaN HEMT inverter is much higher than that of the silicon MOSFET inverter.

Fig. 5.13(b) shows the output power versus the input dc voltage of the half-

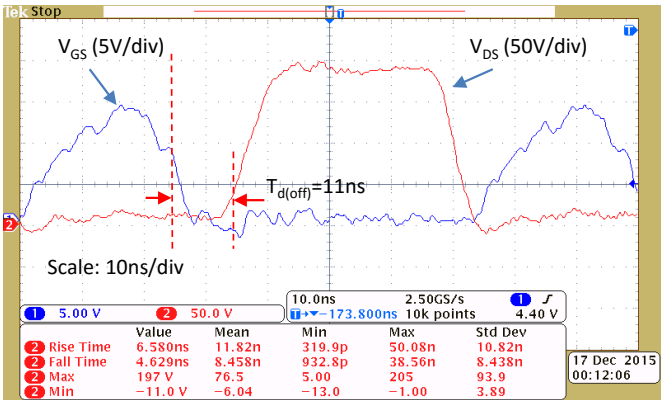


Figure 5.11: Key waveforms of half-bridge inverter

bridge inverter using cascode GaN HEMT at class DE operation mode. The inverter can stable work well at 864 W output power with a small heat sink as shown in Fig. 5.10. That also means a very high efficiency is obtained.

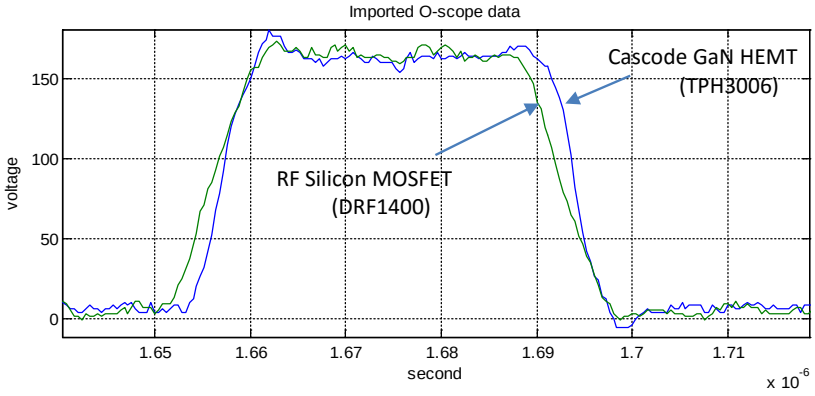
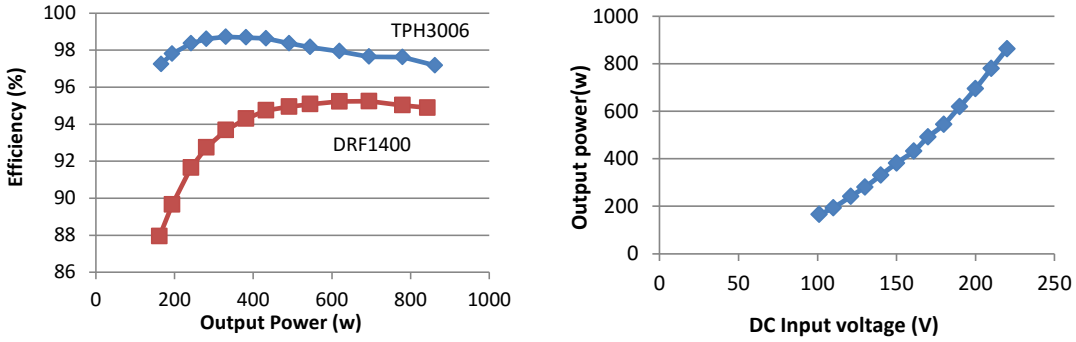


Figure 5.12: Comparison of Drain-source voltage of cascode GaN HEMT and RF silicon MOSFET



(a) Basic structure

(b) Efficiency and output power

Figure 5.13: Output power and input voltage

5.5 Discussion

This chapter analyses the basic characteristic and evaluates the application of TO220 cascode GaN HEMT in 13.56 MHz half-bridge resonant inverter. The inverter does not obtain high efficiency and high power in class D mode due to the large parasitic inductance of TO220 packing type. In class DE mode, the inverter using GaN HEMT can obtain high efficiency even in low load condition because of the faster switching speed and the lower drive power loss. The peak efficiency of inverter obtains 98.6% comparing with 95.1% of the inverter using RF silicon MOSFET. The results show that the cascode GaN HEMT is much suitable than silicon MOSFET at 13.56 MHz inverter. And the inverter with the efficiency of over 95% can be realized by using the cascode GaN HEMT.

Chapter 6

Design high power and high efficiency inverter

6.1 Introduction

As the evaluation in chapter 5, the inverter using the cascode GaN HEMTs has achieved the efficiency of over 95% at the switching frequency of 13.56MHz. It shows the high potential to meet the design targets. However, with recent technology, the cascode GaN HEMTs are only available in the relatively small rating current so that the output power of 3 kW required could only be achieved via a parallel circuit comprising several of these devices.

Parallel connection of switching devices has been studied by several researches [45-52]. The important design issue is the current distribution and thermal uniformity among the paralleled devices. An unbalance current distribution leads to the thermal inequality and result a low electrical properties of the switching devices [46-47]. The causes of the unbalance current distribution have been shown as the device parameters mismatch and the circuit parasitic parameters mismatch. The using of the same manufactures devices was recommended to reduce the device parameters mismatch [45-52], some PCB design is proposed to reduce the circuit parameters mismatch [49,50,52] and the active current balancing method is also proposed [48]. However, with the very fast switching speed,

the parallel connected of the SIC MOSFET or GaN HEMT devices still is the big challenge due to the unbalance distribution dynamic current[46, 47, 50, 51, 52]. The number of devices connected in parallel is also limited due to the circuit parasitic parameters mismatch. Furthermore, at very high switching frequency such as 13.56MHz, the PCB design must be optimized to minimize the parasitic components so that it is difficult to connect the devices in parallel. And it also is difficult to apply the active current balancing method.

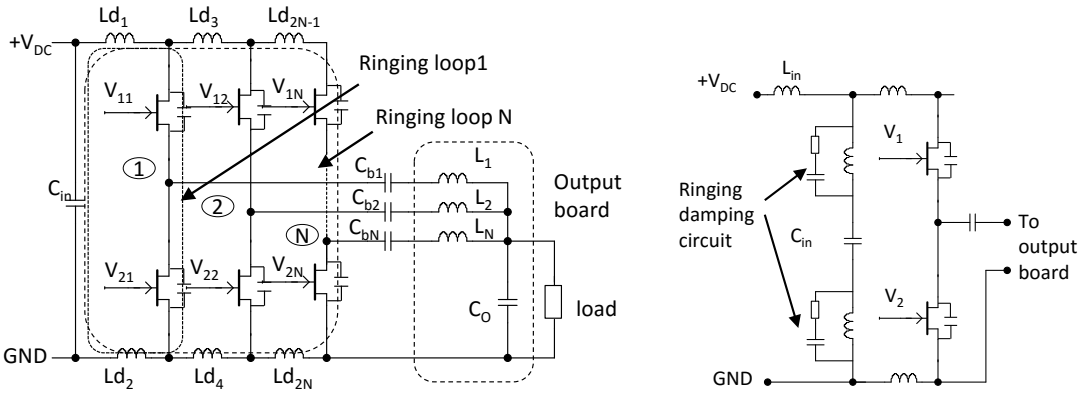
The parallel connection of the soft switching inverters which was proposed in [53-54] and the multiphase resonant inverter which was generalized study in [55-56], can easily expand the output power of the inverter by the increasing of the number of phase while still keeps high efficiency by achieving soft switching condition on each phase. There is no or negligible circulating currents, even if inverters switch non-synchronous that makes the equal power sharing among parallel-connected inverters [53]. However, at 13.56 MHz switching frequency, the switching power loss and driver power loss mainly affect the efficiency of the multiphase inverter. As a result, it is difficult to obtain a high efficiency when the number of switching devices increases. Furthermore, the stable of the inverter is also a challenge. This chapter presents a proposed design of a 3 kW inverter operating at 13.56 MHz based on the multiphase resonant inverter topology. That can easily expand the output power up to 10kW by the same design concept. The cascode GaN HEMT is used to improve the efficiency of the inverter by the faster switching speed and lower drive loss. The module design solution is proposed to avoid the influence of the parasitic inductance and keep the balance parameter among phases. The number of phase of the inverter is optimized based on the power loss analysis to obtain the highest efficiency. The switching condition is analyzed to obtain high efficiency and high stability for the inverter. The drive circuit is designed to obtain the uniform drive pulse among phases and the high stability of the inverter. Finally, a 3 kW inverter has been fabricated and tested. The inverter obtains the efficiency of 96.1% at 3025 W output power with the stable operation. The proposed design of a multiphase resonant inverter is presented in part 6.2 and the experiment results is shown in part 6.3. Finally, the discussions are presented in part 6.4.

6.2 Multiphase inverter design

6.2.1 Module design

Fig. 6.1(a) shows the topology of multiphase resonant inverter including the parasitic inductance in the real circuit. Each phase of inverter exits a ringing loop which is formed by the parasitic inductance and the output capacitor of the power switches. As the analysis in chapter 4, at high frequency, the damping circuit in the DC side is better than the damping circuit attached directly in the power switches due to the soft-switching condition. In the case of the multiphase resonant inverter, the ringing frequencies are different among the phases due to the different of the parasitic inductance. As the result, the DC-side of the multiphase resonant inverter exits several ringing with different frequencies. It is difficult to design the damping circuit. Furthermore, when the parasitic inductances in the phases are different, it is difficult to obtain the same switching condition in every phase to achieve highest efficiency for the multiphase inverter. When the number of phase increase, the parasitic inductance in the ringing loop of the N phase will also increase. Therefore, the number of phase will be limited due to large parasitic inductance in the ringing loop of the N phase and the mismatch of these inductance among phases.

The module design solution as shown in Fig. 6.1(b) is proposed. Each phase module can operate independently, it includes of the input filter circuit, damping circuit, drive circuit and two switches in the half-bridge topology. Every phase will connect with one output board to make a multiphase inverter as shown in Fig. 6.1(a). With this design, the parasitic inductance in the ringing loop of each phase is minimized and independent with the number of phase. The parameter of every phase will be the same. And the module design solution can easily expand the output power level of inverter unlimited by the increasing of the number of the modules. With the module design, the equivalent circuit of the multiphase resonant inverter approximating at the fundamental frequency is shown in Fig. 6.2.



(a) Multiphase resonant inverter topology (b) Phase module design

Figure 6.1: Multiphase resonant inverter module design

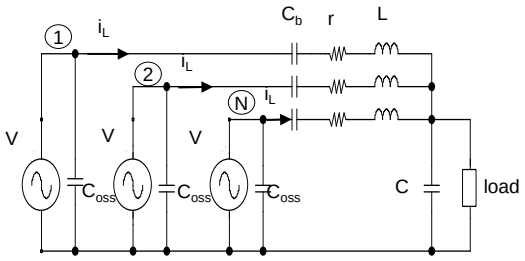


Figure 6.2: Equivalent circuit of multiphase inverter approximating at fundamental frequency

6.2.2 Switching condition

When the inverter operates at 13.56 MHz, the switching power loss on the power switches is much higher than the conduction power loss. Therefore, the zero voltage switching (ZVS) condition is the key technique to obtain high efficiency. Fig. 6.3 shows the simple equivalent circuit of a half-bridge including two switches accompany with its parasitic output capacitors and the charging/discharging process of the output capacitors when the high-side switch is turned off. Fig. 6.4 shows three possible switching conditions when the inverter operates above resonance frequency. Cases shown in Fig. 6.4(a) and Fig. 6.4(b) are the situations when the drain-source voltage of the low-side switch does not reach to zero before

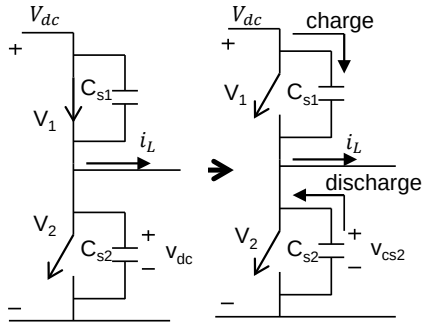
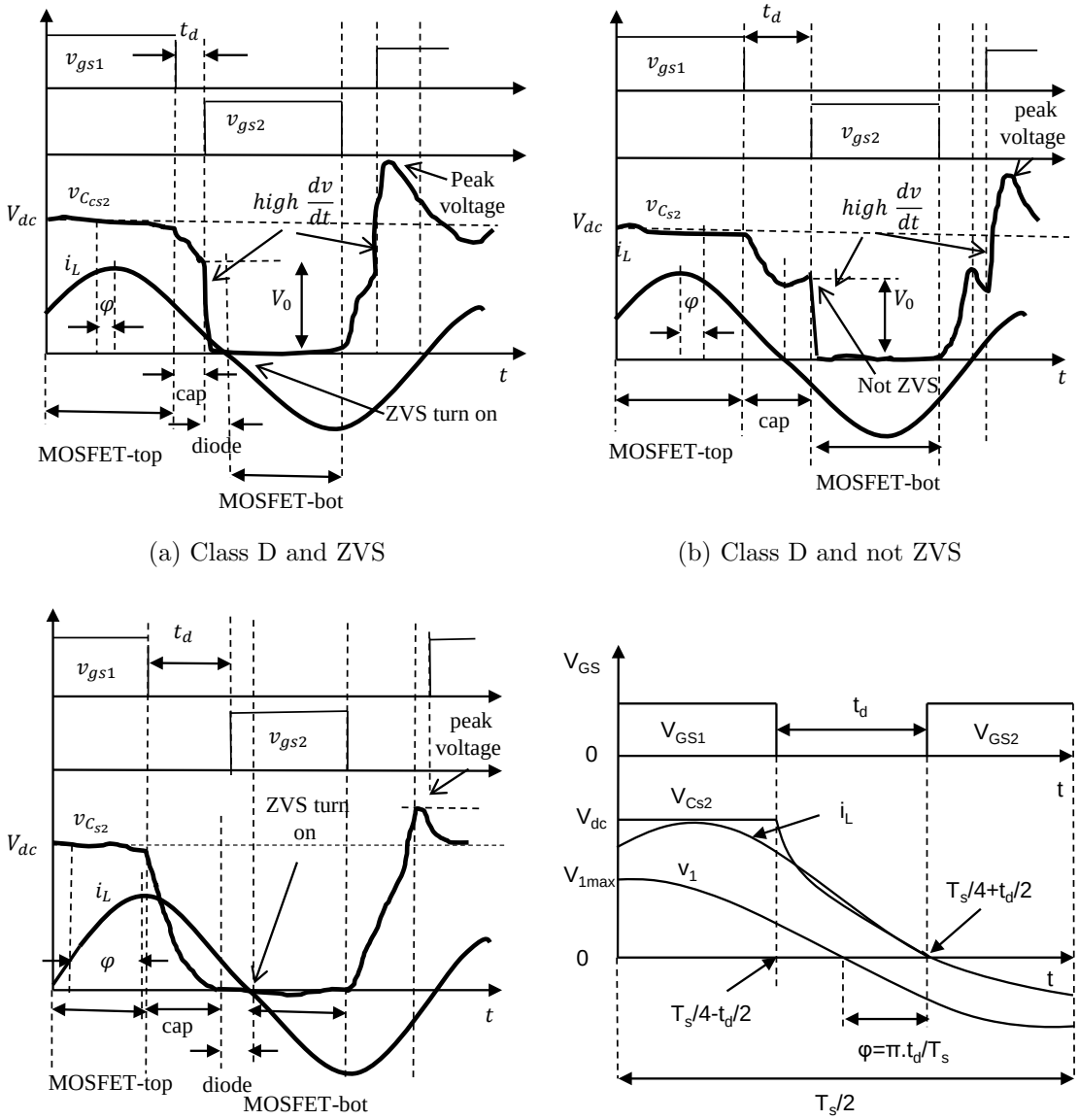


Figure 6.3: Charging process of output capacitor

the output current reverses. The difference between cases (a) and (b) is the dead time. In case (a), the dead time is very short. The low-side switch is turned on before the output current reverses. The output current will pass through the free wheel diode in low-side before it reverses. Then the ZVS condition is achieved. In case (b), the dead time is longer. The low-side switch is turned on after the output current reverses. In this case, the ZVS condition is not achieved. In both of case 6.4(a) and case 6.4(b), the output capacitors are shorted when they still have the voltage. Therefore, the charge and discharge power loss on the output capacitors make the additional switching power loss and reduce the efficiency of the inverter.

Fig.6.4(c) shows the situation when no charging and discharging losses are presented at turn on because the drain-source voltage of low-side switch reaches to zero before the output current reverses. The ZVS condition is achieved. When the dead time is turned exactly, the voltage of drain-source capacitor can reach to zero in time when the output current reverses. This case typically is called class DE operation as shown in Fig. 6.4(d). This is the perfect switching condition which is the most suitable for high frequency inverter where the switching power loss is minimized and the ringing is not presented in the circuit. It makes the circuit more stable. However, with the Silicon MOSFET at 13.56MHz, the charging and discharging time are comparable with switching period due to the large parasitic output capacitor. As the result, in this case, the phase lag is large which leads to low power corresponding at output of inverter. By using GaN HEMT, the



(a) Class D and ZVS

(b) Class D and not ZVS

(c) ZVS and ZVdS

(d) Class DE

Figure 6.4: The possible switching condition above resonance

parasitic output capacitor is much smaller than Silicon MOSFET, and then the charge/discharge time is much shorter. Furthermore in this design, the first generation of cascode GaN HEMT TPH3006 in TO220 packing type is used which has the large parasitic inductance [41]. Therefore, the class DE operation

mode is the best choice to obtain high efficiency and high stability for the half-bridge inverter [see chapter 2]. The output power of inverter can easily expands by increase the number of phase.

6.2.3 Power loss analysis

In the low operation frequency, the drive power loss is negligible. Hence, the efficiency of the multiphase inverter will increase when the number of phase increases due to the reducing of the conduction power loss [55]. However, in the case of the MHz operation frequency, the drive power loss takes a countable part in the total power loss of the inverter. That will affect the efficiency of the inverter when the number of phase increases. Furthermore, to obtain the class DE operation mode in each phase of the multiphase inverter, the input DC voltage, the output current of each phase and the dead time must be satisfied the relationship as shown in Fig. 6.4(d). With the same output power of the inverter, when the number of phase changes, these parameters also change which lead to the changing of the power loss. Therefore, the following analysis will investigate the changing of the power loss in the inverter with the changing of the number of phase to find out the optimum value which obtains the highest efficiency for the inverter. The analysis also gives the equations to design the multiphase inverter at class DE operation mode in the consideration of the devices safe operation area (SOA).

The voltage and current waveform of each module is shown in Fig. 6.4(d). The output current is defined as indicated in (6.1). The relationship between voltage across C_{s1} and C_{s2} is shown in equation (6.2).

$$i_L(t) = I_L \cos(\omega_s t - \varphi) \tag{6.1}$$

$$v_{dc} = v_{C_{s1}}(t) + v_{C_{s2}}(t) \tag{6.2}$$

where φ is the phase angle between the output current and the fundamental harmonic of output voltage of one module. The phase angle depends on the dead time as shown in (6.3)

$$\varphi = \frac{t_d}{T_s}\pi \tag{6.3}$$

To simplify, it can be assumed that C_{s1} and C_{s2} are charged and discharged by all of output current. Then the relationship among the input DC voltage, the output current and the dead time to obtain class DE operating mode is shown in (6.4) .

$$V_{dc} = \frac{1}{2C_{oss}} \int_{(T_s/4)-(t_d/2)}^{(T_s/4)+(t_d/2)} I_L \cos(\omega_s t - \varphi) dt \tag{6.4}$$

The integral in (6.4) is solved to give:

$$V_{dc} = \frac{I_L}{2\omega_s C_{oss}} [1 - \cos(2\varphi)] \tag{6.5}$$

The equation (6.5) shows the relationship among input DC voltage, output current of each phase and the dead time to obtain the class DE operation mode. This condition is given for one phase of the inverter. With the consideration of the output power of the inverter, the number of phase will be involved.

The amplitude of the fundamental harmonic of output voltage can be calculated as (6.6) when the output voltage waveform is approximated with trapezoidal waveform.

$$V_{1max} = \frac{4}{T_s} \int_0^{T_s/2} v_{cs2}(t) \cos(\omega_s t) dt = 2\frac{V_{dc}}{\pi\varphi} \sin(\varphi) \tag{6.6}$$

Then, based on the equivalent circuit in Fig. 6.2, the output power of the inverter can be expressed in (6.7)

$$P_0 = N\frac{1}{2} V_{1max} I_L \cos\varphi \tag{6.7}$$

where N is the number of phase of the multiphase inverter. From (6.5), (6.6) and (6.7), the relationship among the output current, output power and the dead time is given in (6.8).

$$I_L = \sqrt{\frac{4P_0\pi\omega_s\varphi C_{oss}}{N\sin(2\varphi)[1 - \cos(2\varphi)]}} \tag{6.8}$$

Submitting for I_L from (6.8) in (6.5), yields:

$$V_{dc} = \sqrt{\frac{P_0\pi\varphi[1 - \cos(2\varphi)]}{N\sin(2\varphi)\omega_s C_{oss}}} \tag{6.9}$$

Equations (6.8) and (6.9) give the required dc input voltage and the output current of each phase for a given output power of the inverter in the relationship with the number of phase, the dead time and the switching frequency to obtain class DE operation mode.

The conduction power loss on the resonant inductor can be merged with the conduction loss on the switches. The conduction loss in N phase inverter can be expressed in (6.10).

$$P_{c(loss)} = N\frac{1}{2}I_L^2 r \tag{6.10}$$

where, r is the turn on resistance of switches merging with the ESR of resonant inductor L and blocking capacitor C_b.

The gate drive power loss in N phase inverter can be calculated as (6.11)

$$P_{G(loss)} = N(2C_{iss}(V_{gate+} - V_{gate-})^2 f_{sw}) \tag{6.11}$$

With ZVS condition, no charging power loss on the output capacitors, no loss on the body diodes, theoretically, the switching power loss becomes lossless in class DE mode [58]. Therefore, the power loss analysis will find out the number of phase in which the total conduction power loss and the gate driver power loss is minimized. Then the inverter will obtain the highest efficiency.

In case of 3 kW inverter design, the basic design parameters are shown in Table 6.1. The parameters of the cascode GaN HEMT TPH3006 are looked up

Table 6.1: Basic inverter design parameter

Parameter	value
Switching devices	TPH3006
Output power	3 kW
Switching frequency	13.56 MHz
Output capacitor C_{oss} (at 200V)	60 pF
Drive voltage	0-12V
Input capacitor C_{iss}	740 pF
Turn-on resistance $R_{DS(on)}$	0.15

from the datasheet [57]. Fig. 6.6 shows the input dc voltage versus the dead time and the number of phase. The input dc voltage will be limited by two curves: one is the maximum operation voltage of the device and another is the maximum dv/dt value of the isolation device in the high-side drive circuit. Fig. 6.7 shows the output current versus the dead time and the number of phase. When the number of phase increases, the output current of each phase will reduce. If the dead time is constant, when the number of phase increases, the output current will not reduce in the linear rate because it has to satisfy the class DE condition (6.5). When the input dc voltage is constant, the output current of each phase will reduce in the proportion with the number of phase as shown in the dot curve. When the output current of each phase reduces, the required dead time will increase because the output capacitor of switches does not change.

Fig. 6.8 shows the total conduction power loss and the gate drive power loss versus the required dead time and the number of phase. This figure shows another viewpoint based on the changing of the required dead time. Each required dead time is calculated at the given required input dc voltage and output current which can be found on the Fig. 6.6 and Fig. 6.7. At the same output power, the increasing of the required dead time is the same meaning with the increasing of the required input dc voltage. As the results, the output current on each phase will reduce which lead to the reducing of the conduction power loss. Fig. 6.8 also illustrates the case of constant input dc voltage consideration in the dot curve. In this consideration, the total power loss will reduce when the number of phase increase from 1 to 5 because of the reducing of the conduction power loss. However, the total power loss will increase when the number of phase continuously increase due to the increasing of the gate drive power loss. The optimum number of phase to obtain highest efficiency depends on the choosing of the input dc voltage. Therefore, to obtain the highest efficiency, the input dc voltage should not be constant in the design consideration. The input dc voltage and the output current should be considered in the full range of the safe operation area (SOA) of the switching device as shown in Fig. 6.9. In this graph, the required dead time is changed from 1 ns to 20 ns. At each value of the required dead time, the required input dc voltage and the output current of each phase are looked up in

the Fig. 6.6 and Fig. 6.7. The optimum operation point to obtain the highest efficiency is the point in the SOA of the device where the total power loss which is shown in Fig. 6.8 is the minimum point. In this case, the optimum operation point is the point which is shown in Fig. 6.6, Fig. 6.7, Fig.6.8 and Fig. 6.9. The number of phase $N = 5$ is chosen. The required input DC voltage is V_{dc}= 267 V, the amplitude of the output current of each phase is I_L= 8 A, and the dead time is t_d= 10 ns. The power factor angle in this design which can be calculated based on (6.3) is $\varphi = 24.4^0$. The total power loss is 41.6 W. Then the inverter will obtain the efficiency of 98.6% in theory.

The operation point of the inverter is given by the output resonant circuit. The simple equivalent circuit of the inverter is shown in Fig. 6.5. The impedance of the output circuit is shown in (6.12)

$$Z_0 = \frac{R_L X_C^2}{R_L^2 + X_C^2} + \frac{r}{N} + j\left(\frac{X_L}{N} - \frac{R_L^2 X_C}{R_L^2 + X_C^2}\right) \tag{6.12}$$

where, R_L is the standard RF load: $R_L = 50\Omega$. and $X_L = \omega_s L; X_C = 1/\omega_s C$ Then, the output capacitor and the output inductor are calculated based on the impedance matching condition as shown in (6.13)

$$\begin{cases} \frac{R_L X_C^2}{R_L^2+X_C^2} + \frac{r}{N} & = \frac{V_{1max}}{I_L}\cos\varphi \\ \frac{X_L}{N} - \frac{R_L^2 X_C}{R_L^2+X_C^2} & = \frac{V_{1max}}{I_L}\sin\varphi \end{cases} \tag{6.13}$$

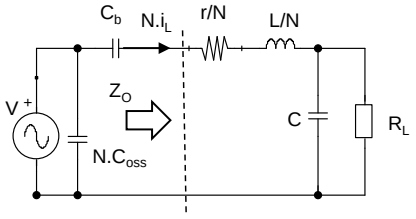


Figure 6.5: Equivalent circuit of multiphase resonant inverter (Assumption: The parameters are the same in every phase)

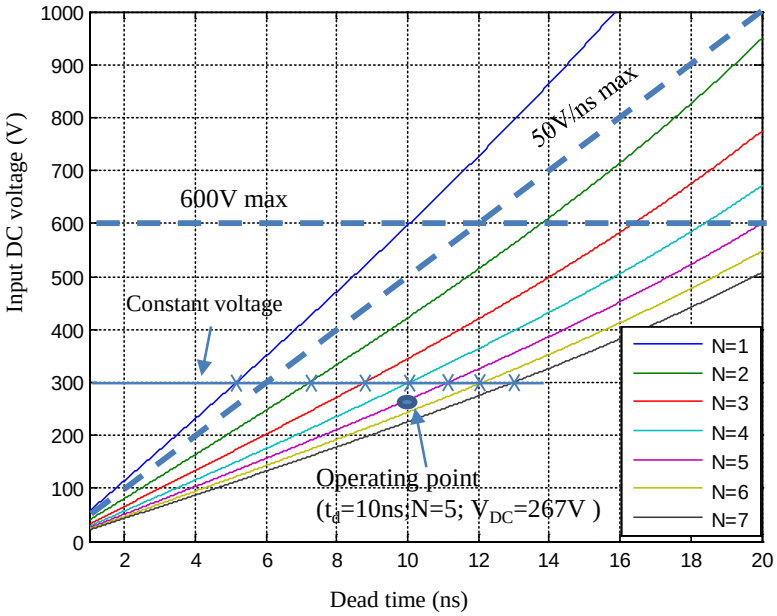


Figure 6.6: Input dc voltage versus dead time and number of phase

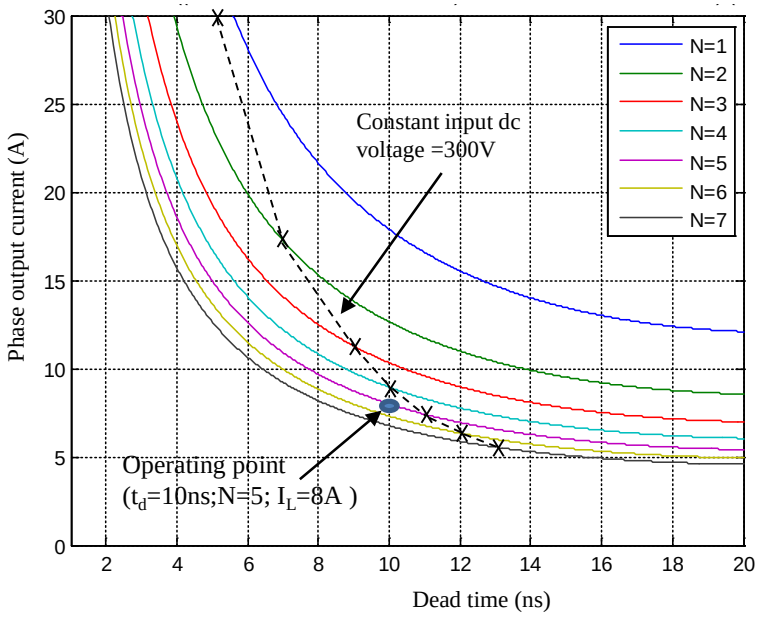


Figure 6.7: Phase output current versus dead time and number of phase

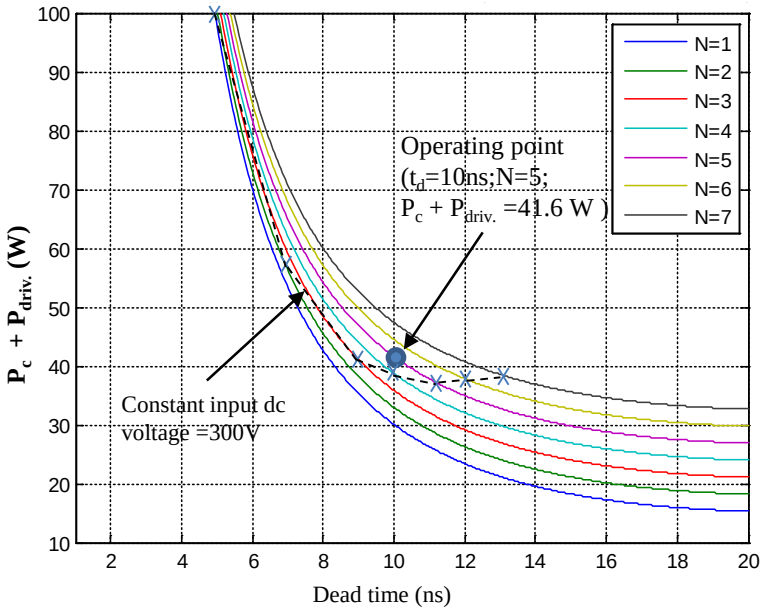


Figure 6.8: Total conduction and gate drive power loss versus dead time and number of phase

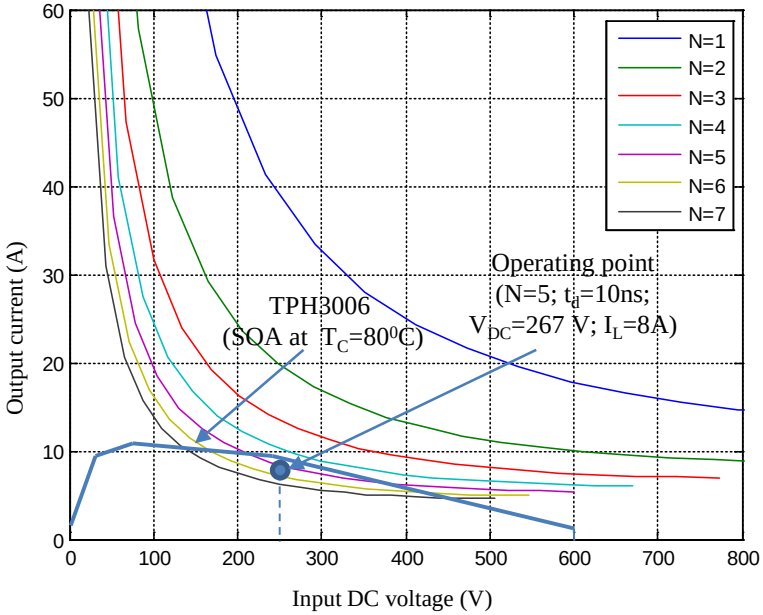


Figure 6.9: VI characteristic satisfying class DE switching condition for a output power of 3kW and SOA of device

6.2.4 Drive design

The drive circuit for each module is designed as the presentation in part 5.3.2. To obtain class DE operation mode for all phase in multiphase resonant inverter operating at 13.56 MHz, the drive pulse for all phase must be synchronized. It becomes a challenge in the high-side drive circuit design due to the floating high-side drive ground with very high dv/dt. The proposed design solution is shown in Fig. 6.10. The drive IC and the cascode GaN HEMT must be placed as near as possible to minimize the parasitic inductance of the connection between them. Therefore, the drive ICs are directly attached on each module. Then, in order to synchronize the drive pulses in every phase, every module is connected with the only one drive pulse generator board.

In the drive pulse generator board, the design of PCB is very critical to keep the impedance of the trace line is minimized and similar in two sides ($Z_{1N} = Z_{2N}$). In the case of multiphase, the impedance in each loop accompany with each module is designed to balance with the other loop. The ferrite beat is added in every loop to fill the high frequency noise and make the impedance more balance as shown in Fig 6.10. To connect from the drive board to the phase modules, the coaxial cable is used. The type and the length of all cable is the same to keep impedance balance. The pulse drive dead time and the effective dead time are always different due to the delay time of the switching devices and the mismatching in the delay time between the high-and low-side isolation devices. The delay time of the switching devices mainly depend on the gate drive voltage and the gate drive resistor. This value is given in the datasheet of the switching devices at the certain condition. If the design condition is different, it should be gotten from the experiment. The mismatching in delays among the isolation device is a very typical problem that is given by the pulse skew parameter in the datasheet of the isolation device. The pulse skew parameter is the worst case of the delay mismatching between the device units at the different output states. Finally, the dead time of the drive pulse must be modified as shown in (6.14)

$$t_{dm} = t_d + (t_{d(off)} - t_{d(on)}) + t_{psk} \tag{6.14}$$

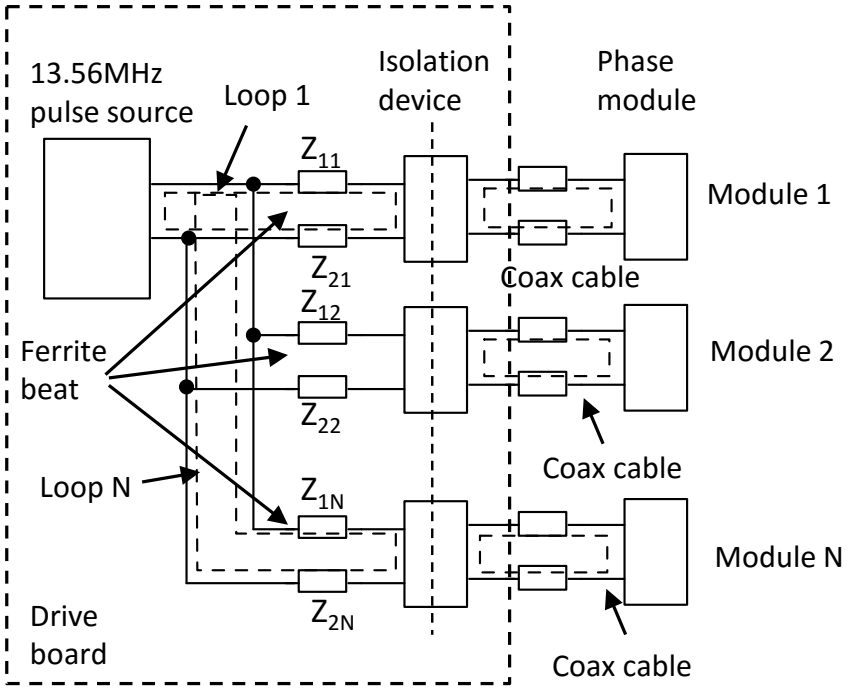


Figure 6.10: Drive pulse generator board design

where: t_{dm} is the modification dead time; $t_{d(on)}$ and $t_{d(off)}$ are the turn-on and turn-off delay time of switching device; t_{psk} is the pulse skew parameter of the isolation devices.

In the experiment at high frequency, the dead time should be pre-set at the maximum value which is calculated by (6.14). Then it must be fine-turned to achieve highest efficiency.

6.3 Experiment results

The five phase inverter is fabricated from five half-bridge modules as shown in Fig. 6.11. The design parameter is chosen as the analysis in part 6.2.3. The output inductor and capacitor are calculated based on equations (6.12) and (6.13). The experiment parameters are listed in Table 6.2. Fig. 6.12 shows the experimental results of the drive board test. It shows that, the drive signals are accurate

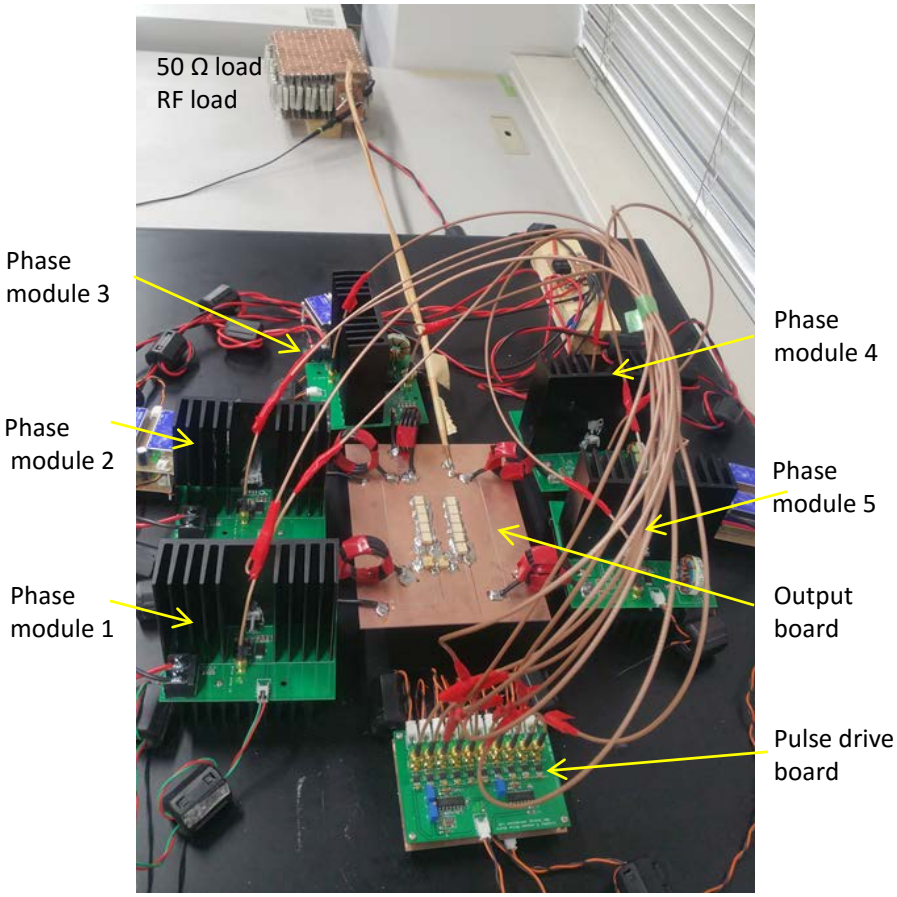


Figure 6.11: Prototype of 5 phase 3kW inverter

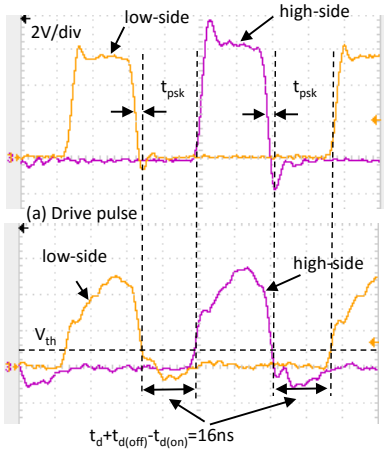
and clean at 13.56 MHz. The drive pulse from the drive board is shown in Fig. 6.12(a). The drive pulse for high-side and low-side are little different because the isolation devices for high-and low-side drive circuit are different. The high common mode noise immunity device ISO721M is used for high-side drive circuit. While the lower common mode noise immunity device HCPL0900 is used for low-side drive circuit because the low-side drive circuit does not work in high dv/dt condition. The dead time is fine-turned according (6.14). Fig. 6.12(b) shows the gate-source voltage of cascode GaN HEMT in one phase module. The re-turn on pulses in the high-side gate-source voltage which is caused by the miller capacitor CGD is not observed. Therefore, the circuit is stable at high voltage condition

Table 6.2: Five phases inverter experiment parameter

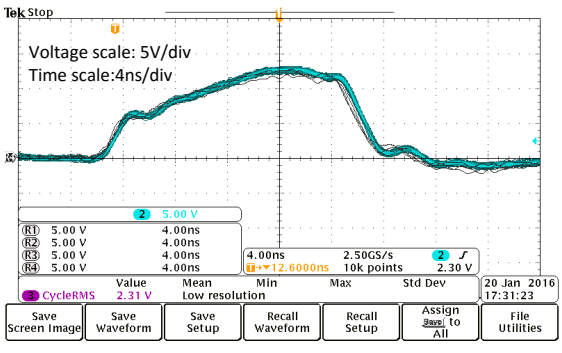
Parameter	value
Output power	3 kW
Switching frequency	13.56 MHz
Number of phase	N=5
Drive voltage	0-12V
Input DC voltage	267V
Resonant circuit	L=870 nH; C= 850 pF; C_B=0.01 μF
RF load	50Ω
Dead time (t_{dm})	18 ns

with the unipolar drive voltage. This is one of the importance advantages of the GaN HEMT device when it is applied in high frequency application because the threshold voltage of cascode GaN HEMT is low.

The gate-source voltage of five phases is measured and compared together to confirm the dead time on each phase and the synchronous among phases. Fig. 6.12(c) shows the measurement results of gate-source voltage at high-side drive circuit of five phase modules. It is totally synchronous. This is the condition to



(b) Gate-source voltage in phase module (5V/div) (time scale: 10ns/div)



(c) High-side gate-source voltage in five phases

Figure 6.12: Drive signal

obtain the class DE switching condition in every module.

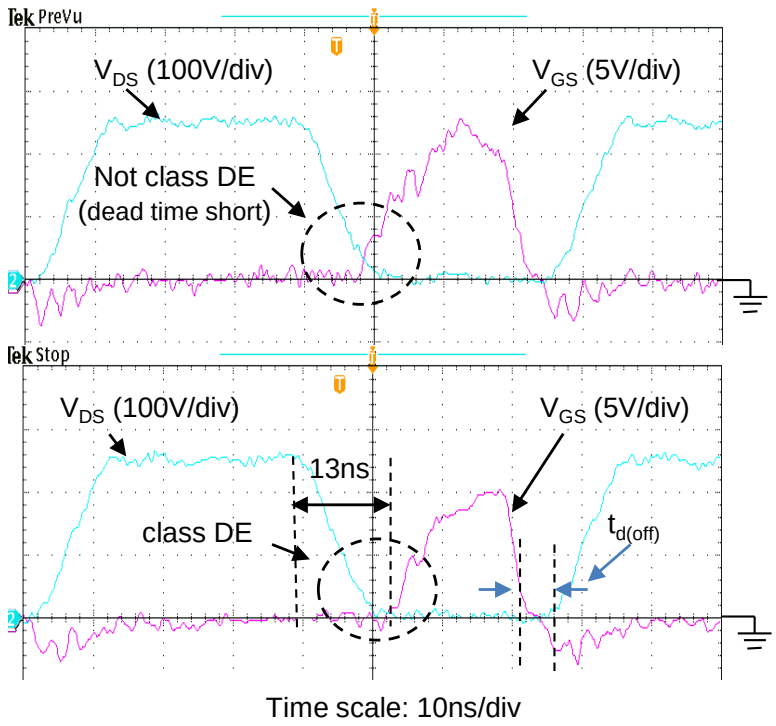


Figure 6.13: The drain-source and gate-source voltage of low-side switch with the changing of the dead time
Upper: dead time: 16 ns
Lower: dead time: 18 ns

Fig. 6.13 shows the drain-source voltage of the low-side switch and its gate-source voltage in one phase. In the upper case, the dead time is 16 ns. This value is not enough to obtain class DE mode. Then the switch is turned on before its drain-source voltage reaches to zero. As a result, the charge/discharge loss is presented in the circuit and the efficiency is low. In the lower case, the dead time is 18 ns. The module obtains class DE operation mode. The falling time of the drain-source voltage of the GaN is about 13ns. It is different with 10ns as the analysis in part 6.2.3. The reason take from the assumption to get equation (6.4). In fact, a part of the load current will flow through the conduct channel of the switch when it is turning off. Therefore, the real charging/discharging

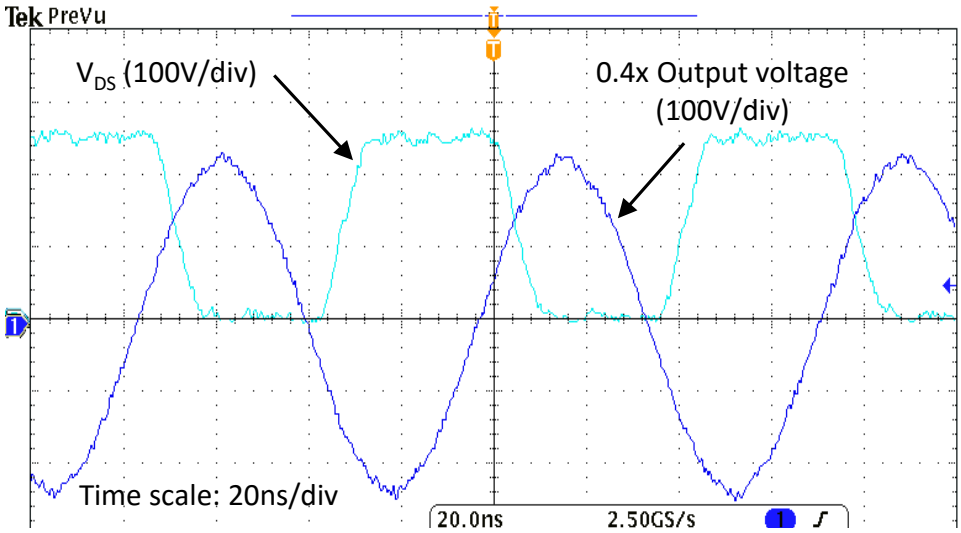
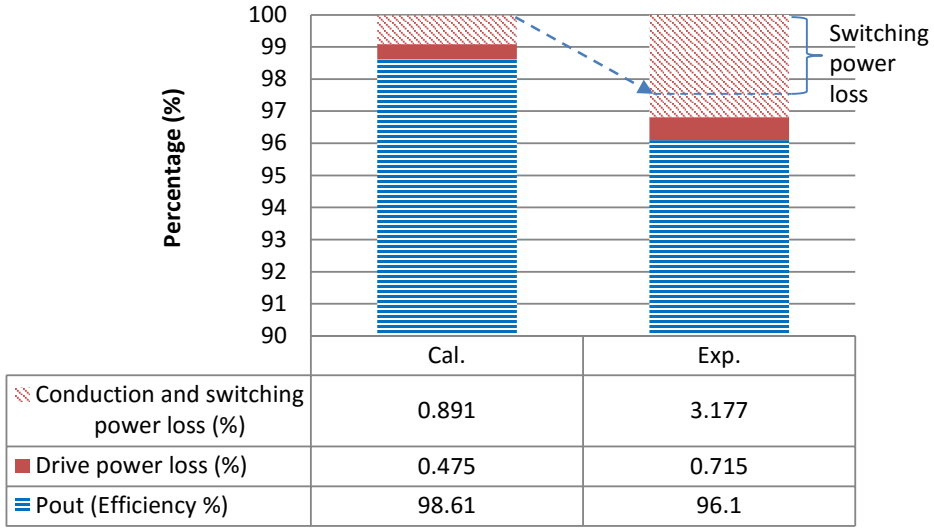


Figure 6.14: Output voltage waveform of five phase inverter

current of the output capacitors is smaller than the load current. As a result, the charging/discharging time will be longer than the calculation value. Furthermore, the real output parasitic capacitor of the cascode GaN HEMT is greater than the datasheets value due to the parasitic capacitors between these devices and the heat sink. And the delay time of the oscilloscope and the probe which were used to measure the waveform also may make the error. The inverter is stable at 3025 W output power with the drain efficiency of 96.8%. The output voltage waveform of five phase inverter is shown in Fig. 6.14. The total power dissipated in the drive circuits in experiment is 22.5W while the calculation value is 14.45 W. The different in the drive power loss calculation is taken from the power loss on the dc/dc power sources for the driver circuit. Therefore, the overall inverter efficiency is 96.1% as shown in Fig. 6.15. This value is smaller than 98.6% which was estimated in part 6.2.3. As shown in Fig. 6.15, in the calculation results, the power loss on the power circuit is only the conduction loss because the switching power loss is zero in idea class DE mode. However, in the experimental results, the power loss on the power circuit increase 2.3% beyond the calculation value. This is a result of the switching power loss. In fact, the class DE operation mode was not obtained in every phase of the inverter because the absolute balance of the output



	Cal.	Exp.
Conduction and switching power loss (%)	0.891	3.177
Drive power loss (%)	0.475	0.715
Pout (Efficiency %)	98.61	96.1

Figure 6.15: Power loss distribution in experiment results

inductors, the drive pulse in every phase is impossible. Therefore, the dead time is turned to obtain the highest efficiency in the experiment results. Furthermore, the idea class DE operation mode still is difficult to exactly confirm by experiment due to the error of the high frequency current measurement. Therefore, the switching condition of the inverter may be similar with the case as shown in Fig. 6.4(c). Then the conduction loss will be higher than the calculation value.

Fig. 6.16 shows the drain-source voltage and gate-source voltage of low-side switch in three cases when the dead time is constant at 18 ns with the changing of the input DC voltage. In the upper figure, the input DC voltage is 280 V, the output power is increase and the falling time of the drain-source voltage is shorter due to the lager output phase current. In this case, the switch is also turned on when its drain-source voltage equals to zero. There is no charge and discharge loss. However the efficiency reduces due to the increasing of the conduction power loss. In the middle figure, the input voltage is 267 V as the design. The class DE is achieved, the inverter obtains highest efficiency of 96.1%. In the lower figure, the input DC voltage is 200 V, the output current reduces. Therefore, the class DE operation mode is not achieved. The efficiency of the inverter also reduces. This is a direct confirmation of the correctness of the analysis in part 6.2.3.

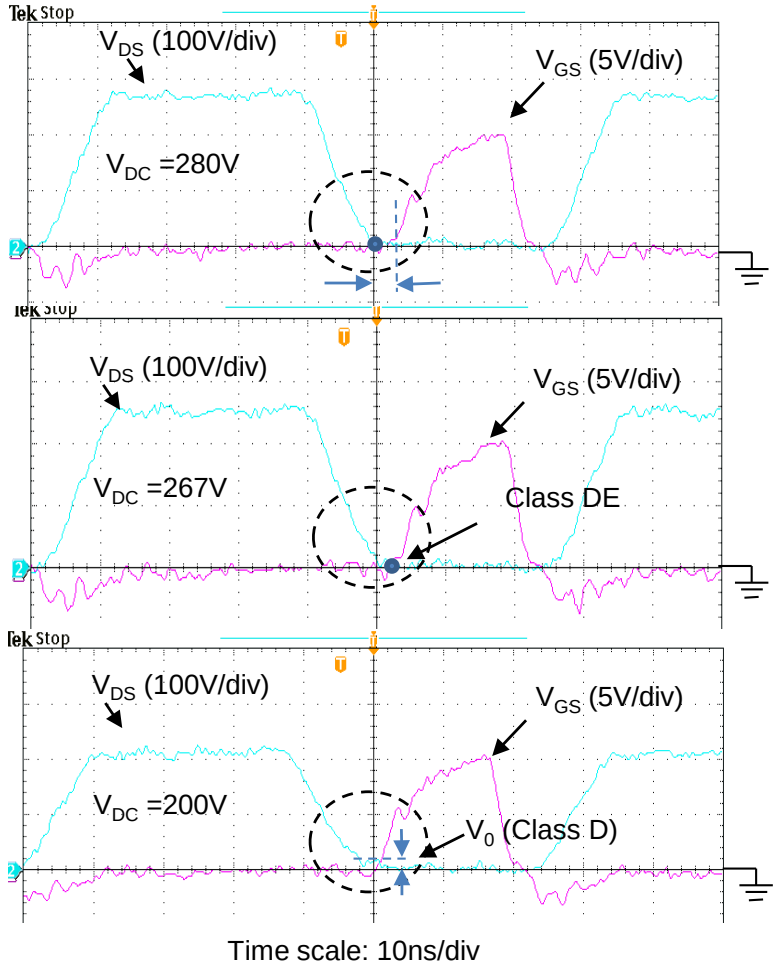


Figure 6.16: The drain-source and gate-source voltage of low-side switch with the changing of the input DC voltage
Upper: Input DC voltage: 280 V; dead time: 18 ns
Middle: Input DC voltage: 267 V; dead time: 18 ns
Lower: Input DC voltage: 200 V; dead time: 18 ns

6.4 Discussion

This chapter presents a proposed design of a high power and high efficiency inverter operating at 13.56 MHz which can adapt the demands of the EV wireless charging systems. The GaN device is used to improve the efficiency of the in-

verter. The influence of the parasitic inductance is solved by the proposed module design method. The efficiency of the inverter is optimized based on the switching condition analysis and the power loss analysis. A stable drive circuit is designed to overcome the challenge at a very high frequency condition. The full design equations for very high efficiency inverter based on the multiphase topology is also developed. Finally, a 3 kW inverter operating at 13.56 MHz is fabricated and tested in an experiment. The efficiency of 96.1% and the stable operating of the inverter at 13.56 MHz are achieved that directly verify the proposed design method. In the future work, a 10 kW inverter operating at 13.56 MHz with the efficiency of over 95% will be developed by following this design method.

Chapter 7

Conclusion and future work

7.1 Conclusion

This thesis presented a design process of a 3 kW 13.56 MHz inverter with the efficiency of over 95% for the dynamic charging systems. The summary of the thesis research works as following:

- The parasitic components always exist in the practice circuit because of the physical connections. At 13.56 MHz switching frequency, the parasitic components strongly affect the switching performance of the switching devices. The analysis shows that the force charge/dis-charge process of the parasitic output capacitors of the switching devices and the parasitic inductances in the ringing loop are the root cause of the peak voltage and the ringing in the half-bridge inverter. The ringing is un-damp able by the nature way. When the parasitic inductance in the ringing loop is large, the switching waveform of the switching devices is almost of ringing. The switches may be damaged by a very high switching power loss. Furthermore, the high frequency ringing current also affect the gate-drive signal due to the EMI noise and may make the instability of the inverter.

- When the parasitic inductance of the ringing loop is recognized as one of the root cause of the ringing in the circuit. The proposed PCB design is

presented to minimize that parasitic inductance. The simulation and experiment results show that the conventional PCB design which has the ringing current traveling on the large PCB area and multi PCB layer makes the large parasitic inductance in the ringing loop and also several sub-oscillators at low frequencies. With the proposed PCB design, the ringing loop is designed on only the top layer and in the minimize PCB area. The parasitic inductance of the traces line in the ringing loop reduces 33.9%. The sub-oscillator was not observed in both of simulation and experiment results. Furthermore, a bypass board is also proposed which uses the field self-cancellation effect to reduce the parasitic inductance in-side the MOSFET module. Finally, the proposed PCB design provides a reduction of 23.4% in the ringing loop parasitic inductance in the comparison with the conventional PCB design.

- The simulation and experiment result show that the ringing always exists in the circuit even with the proposed PCB design. And the ringing makes the instability of the inverter at high voltage operation condition due to the high EMI noise and high dv/dt on the gate-drive circuit. A new damping circuit is proposed to damp the ringing in the circuit. The proposed damping circuit significantly attenuate the ringing in the power loop while dissipates a very low power loss at 13.56 MHz inverter. Furthermore, the proposed PCB design uses the parasitic inductance of the PCB trace lines as a part of the damping circuit so that the parasitic inductance of the ringing loop is not affected by the damping circuit and the circuit becomes more stable. Finally, the efficiency of the inverter obtained 93.1% efficiency at 1.2kW output power. This is an improvement in the comparison with the previous researches. However, it did not meet the required efficiency of over 95% for the dynamic charging system.

- When the inverter using silicon MOSFET can not meet the required efficiency of over 95%, an inverter using the high voltage cascode GaN HEMTs is evaluated at 13.56 MHz as a replacement solution to improve the efficiency of the inverter. The GaN HEMT devices with the faster switching speed and much lower gate-drive power loss show the high potential to improve

the efficiency of the inverter. A gate-drive circuit design for the cascode GaN HEMT was also presented. In the experiment, the peak efficiency of inverter using the GaN HEMTs obtains 98.6% comparing with 95.1% of the inverter using RF silicon MOSFET in class DE operation mode. The results show that the GaN HEMT is much suitable than silicon MOSFET at 13.56 MHz inverter. And the inverter with the efficiency of over 95% can be realized by using the cascode GaN HEMT.

- By using the GaN HEMT devices, the efficiency of over 95% was achieved. However, the cascode GaN HEMTs are only available in relatively small rating current so that the output power of 3 kW required could only be achieved via a parallel circuit comprising several of these devices. The parallel connection of the switching device is the popular solution at low switching frequency. At very high frequency such as 13.56 MHz, the unbalance distribution of dynamic current among the parallel connected devices becomes serious and difficult to solve due to the strong effect of the parasitic inductance. The multiphase inverter was used to expand the output power of the inverter base on the low power GaN HEMT devices. The module design solution is proposed to avoid the influence of the parasitic inductance and keep the balance parameter among phases. The number of phase of the inverter is optimized based on the power loss analysis to obtain the highest efficiency. The switching condition is analyzed to obtain high efficiency and high stability for inverter. The drive circuit is designed to obtain the balance drive pulse among phases and the high stability of the inverter. Finally, a 3 kW inverter has been fabricated and tested. The inverter obtains the efficiency of 96.1% at 3025 W output power with the stable operation.

7.2 Future work

A 3 kW inverter with the efficiency of over 95% has been achieved by using the cascode GaN HEMT devices and the multiphase resonant inverter topology

with class DE operation mode. However, the Class DE operation mode requires exactly parameter of load, resonant circuit and several turning in the experiment process. Therefore, it is difficult to apply in the dynamic charging systems where the parameters of the coupling system will always change in the operation. The inverter behavior analysis in the operation with the dynamic coupling system is necessary in the future work. Then further researches to keep the soft switching condition of the inverter in the dynamic systems will also be done.

With the multiphase inverter, the output power of the inverter can be controlled by control the phase shift of drive pulse among phases while still keep the soft switching condition in each phase of the inverter. In the future work, the control system will be considered in the whole dynamic charging system to obtain the highest energy transfer efficiency.

To obtain a 10 kW inverter with the efficiency of over 95% at 13.56 MHz, the combining of several 3 kW inverters will be studied. However, with the standard 50 Ω RF impedance, the output voltage of the inverter will be very high at 10 kW input power which is the design challenge with the high frequency output capacitors of the inverter. The lower output impedance or using a RF transformer in the output will be considered to reduce the voltage across the output capacitors.

Appendix A

Measurement method

At 13.56 MHz, the measurement technique is very important to properly measure the waveform and the efficiency of the inverter. The measurement results have been performed with Tektronix MSO3014 which the bandwidth and sample rate are 100 MHz and 2.5 GS/s respectively. The voltage probe is Tektronix P6139B. The parameters of probe are shown in Table A.1. The probe is directly soldered on the measurement point with the shortest ground lead wire.

Table A.1: The parameters of probe

Name	BW(-3dB)	R_{in}/C_{in}	CM range
Tektronix P6139B	500 MHz	10 MΩ/8 pF	$300V_{RMS}$

The load resistance was obtained by paralleling 240 12-$k\Omega$ 10-W resistor. These resistors were mounted on two parallel copper boards as shown in Fig. 15 to obtain low parasitic inductance. The load resistance was measured by the Agilent E5061B network analyzer in the impedance measurement mode at the frequency of 13.56 MHz. The equivalent circuit of the resistance load is shown in Fig. A.1. Therefore the voltage across the equivalent resistor can be calculated by (A.1).

$$V_{Req} = V_{mea}\frac{R_{eq}}{\sqrt{R_{eq}^2 + (\omega L_{eq})^2}} \tag{A.1}$$

where the V_{mea} is the output voltage which is measured on the load by using oscilloscope. The real output power on the load can be calculated by (A.2)

$$P_{out} = V_{Req}^2 / R_eq \tag{A.2}$$

Then the efficiency of the inverter is calculated based on the input DC power measurement and the real output power on the load.

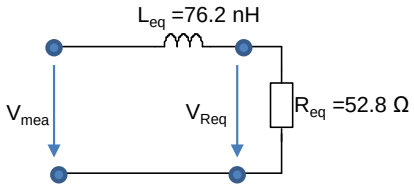


Figure A.1: Equivalent circuit of RF load

Appendix B

1.5 kW inverter experiment setup

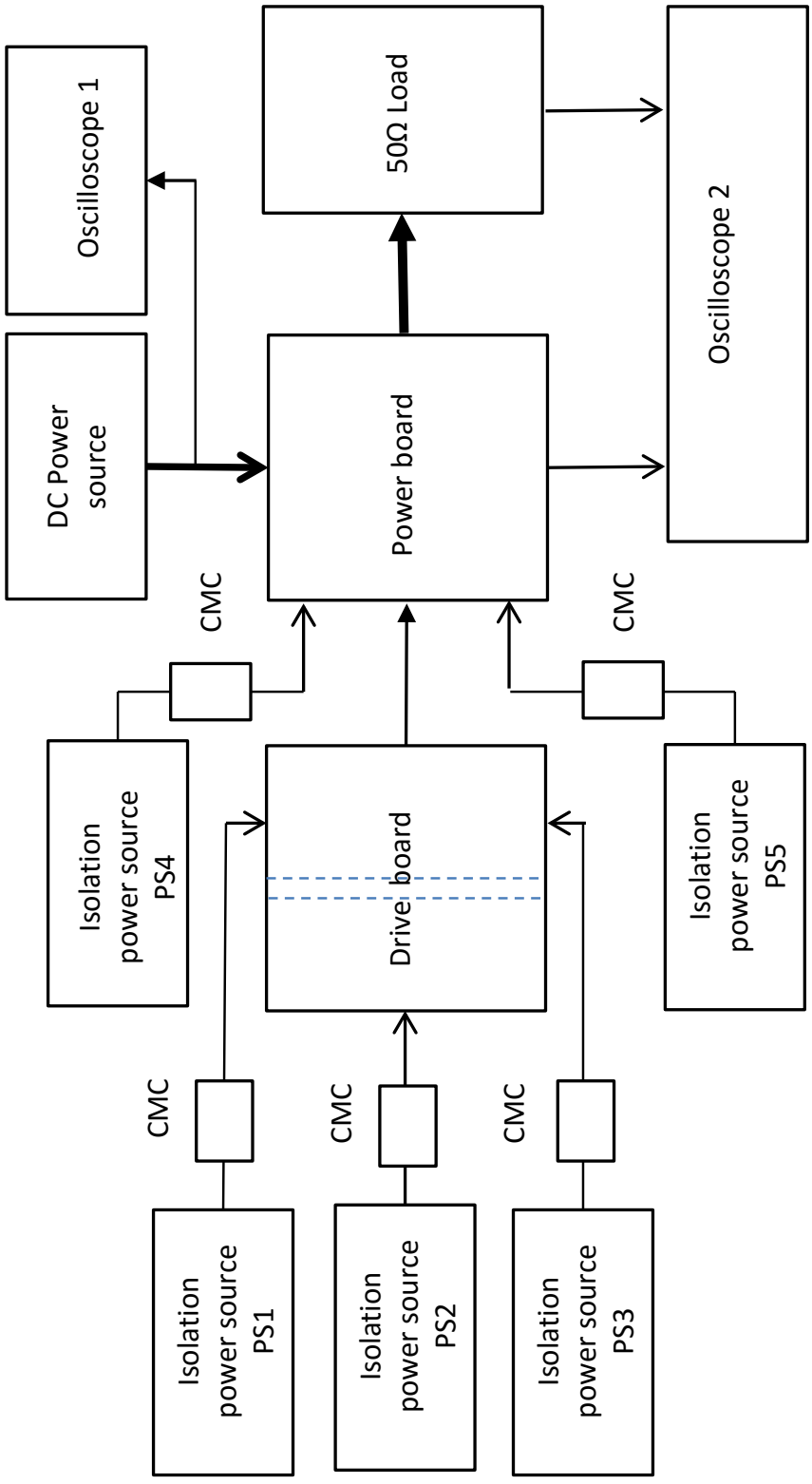


Figure B.1: Structure of experiment setup

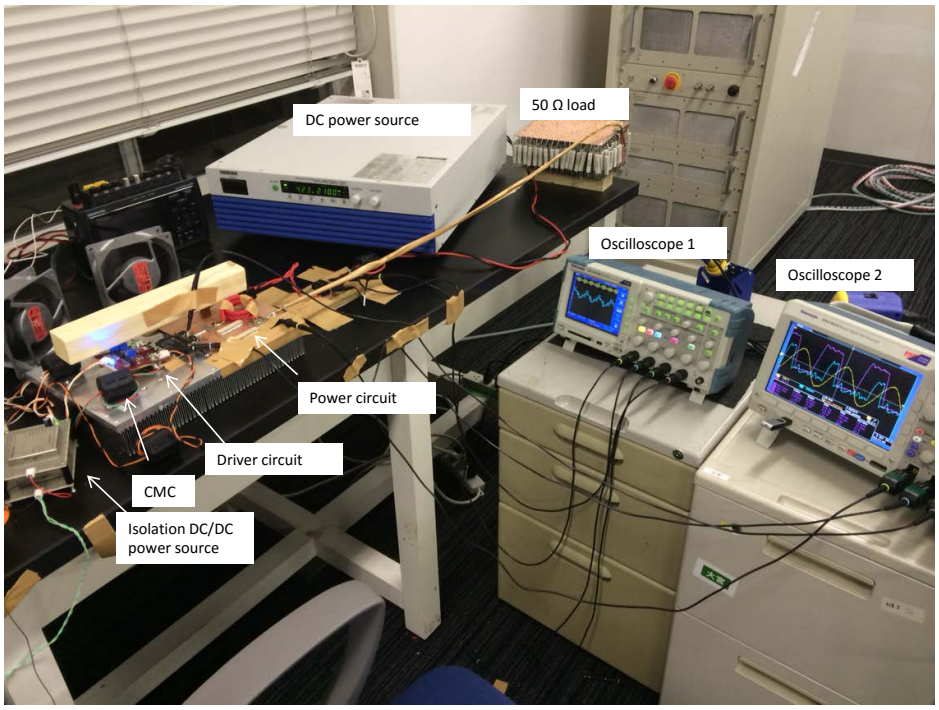


Figure B.2: Picture of experiment setup

Table B.1: List of devices

Device	Spec.	Manufacture	Part number
Oscilloscope 1	200 MHz/ 2 GS/s	Tektronix	Tektronix TPS 2024B
Voltage probe 1	200 MHz - 100 MΩ/¡12 pF	Tektronix	Tektronix TPP 0201
Oscilloscope 2	100 MHz/ 2.5 GS/s	Tektronix	MSO 3014
Voltage probe 2	500 MHz - 10 MΩ/¡8 pF	Tektronix	Tektronix P6139B
Isolation Power source (PS1,PS2, PS3)	5.1V/3A	Traco Power	TEL 15-2411
Isolation Power source (PS4,PS5)	12V/5A	Recom	RP30-240512TA
Ferrite clamp filter (CMC)	31 Material	Fair-rite corp.	0431164181

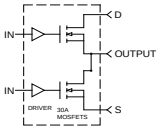
Microsemi
POWER PRODUCTS GROUP

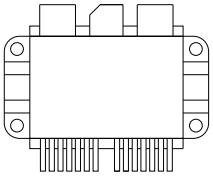
DRF1400

500V, 30A, 30MHz

MOSFET Half Bridge Hybrid

The DRF1400 is a half bridge hybrid containing two high power gate drivers and two power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, anti-Ring function Invert and Non-invert select pin provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.





FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Inverting Non-Inverting Select**
- **Low Pulse Width Distortion**
- **Single Power Supply (Per Section)**
- **1V CMOS Schmitt Trigger Input 1V Hysteresis**
- **Switching Speed 3-4ns**
- **B_{Vds} = 500V**
- **I_{ds} = 30A avg. Per-section**
- **$R_{ds(on)}$ ≤ .24 Ohm**
- **P_D = 550W Per-section**
- **RoHS Compliant**

TYPICAL APPLICATIONS

- **Class D Half Bridge RF Generetors**
- **Switch Mode Power Amplifiers**
- **HV Pulse Generators**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**

Driver Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	15	V
IN, FN	Input Single Voltages	-.7 to +5.5	
$I_{O\,PK}$	Output Current Peak	8	A
T_{JMAX}	Operating Temperature	175	°C

Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	8	12	15	V
IN	Input Voltage	3		5	
$IN_{(R)}$	Input Voltage Rising Edge		3		ns
$IN_{(F)}$	Input Voltage Falling Edge		3		
I_{DDQ}	Quiescent Current		2		mA
I_O	Output Current		8		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
R_{IN}	Input Parallel Resistance		1		mΩ
$V_{T(ON)}$	Input, Low to High Out	0.8		1.1	V
$V_{T(OFF)}$	Input, High to Low Out	1.9		2.2	
T_{DLY}	Time Delay (throughput)		38		ns
t_r	Rise Time		5		ns
t_f	Fall Time		5		
T_D	Prop. Delay		35		

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MOSFET Absolute Maximum Ratings (Per-Section) **DRF1400**

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain Source Voltage	500			V
I_D	Continuous Drain Current T_{HS} = 25°C			30	A
$R_{DS(on)}$	Drain-Source On State Resistance		0.24		Ω

Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance		1800		pF
C_{oss}	Output Capacitance		335		
C_{rss}	Reverse Transfer Capacitance		75		

Thermal Characteristics (Total Package)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	.06	°C/W
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance	.134	
T_{JSTG}	Storage Junction Temperature	-55 to 150	°C
P_D	Maximum Power Dissipation @ T_{SINK} = 25°C	1.1	KW
P_{DC}	Total Power Dissipation @ T_C = 25°C	2.5	

Section A and B Output Switching Performance

Symbol	Characteristic	Min	Typ	Max	Typ
T_{ON}	Leading Edge 10% to 90%	2	3	4	ns
T_{OFF}	Trailing Edge 10% to 90%	45	TBD	49	
$T_{DLY(ON)}$	Total Throughput Delay Time, ON	47	TBD	45	
$T_{DLY(OFF)}$	Total Throughput Delay Time, OFF	49	50	51	
$\Delta T_{DLY(ON)}$	Delta T_{ON} Delay between Section A and B	-0.5	0	1.5	
$\Delta T_{DLY(OFF)}$	Delta T_{OFF} Delay between Section A and B	0	0.6	1.3	

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

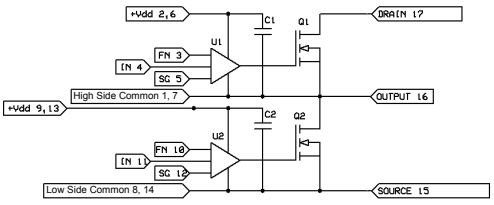

Figure 1, DRF1400 Test Circuit Diagram

The DRF1400 is configured as a Half Bridge Hybrid incorporating two independent channels consisting of a driver, a high voltage MOSFET and by-pass capacitors. The function of the by-pass capacitors C1 and C2 is to reduce the internal parasitic loop inductance. This coupled with the tight geometry of the hybrid allows optimal gate drive to the MOSFET. This low parasitic approach coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG) and the Anti-Ring function; provide improved stability and control in Kilowatt to Multi-Kilowatt high frequency applications. The IN pin should be referenced to the Kelvin Ground (SG) and is applied to a Schmitt Trigger. The SG pin is a Kelvin return for the IN pin only. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. To further increase the utility of the device the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn on and propagation delays.

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None of the inputs to U1 or U2 of the DRF1400 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to the application is the responsibility of the end user.** It is imperative that high output currents be restricted to the Drain (17), Source (15) Output (16) and the C3 Bypass (18, 19) connection pins by design. See DRF100 for more information on Driver IC used in the device.

The Function (FN, pin 3 or pin 9) is the invert or non-invert select Pin, it is Internally held high.

Truth Table * Referenced to SG		
FN (pin 3)	**IN (pin 4)**	**MOSFET**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

Truth Table * Referenced to SG		
FN (pin 9)	**IN (pin 10)**	**MOSFET**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

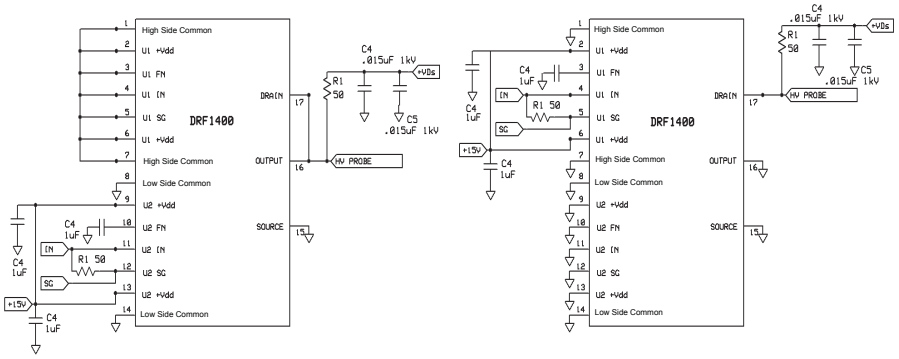

Figure 2, DRF1400 Test Circuit

The test circuit illustrated in Figure 2 was used to evaluate the DRF1400. The input control signal is applied via IN and SG pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The $+V_{DD}$ inputs (pins 2, 6, 8 and 12) should be heavily by-passed by 1uF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load. A 50 Ohm (RL) load is used to evaluate the output performance.

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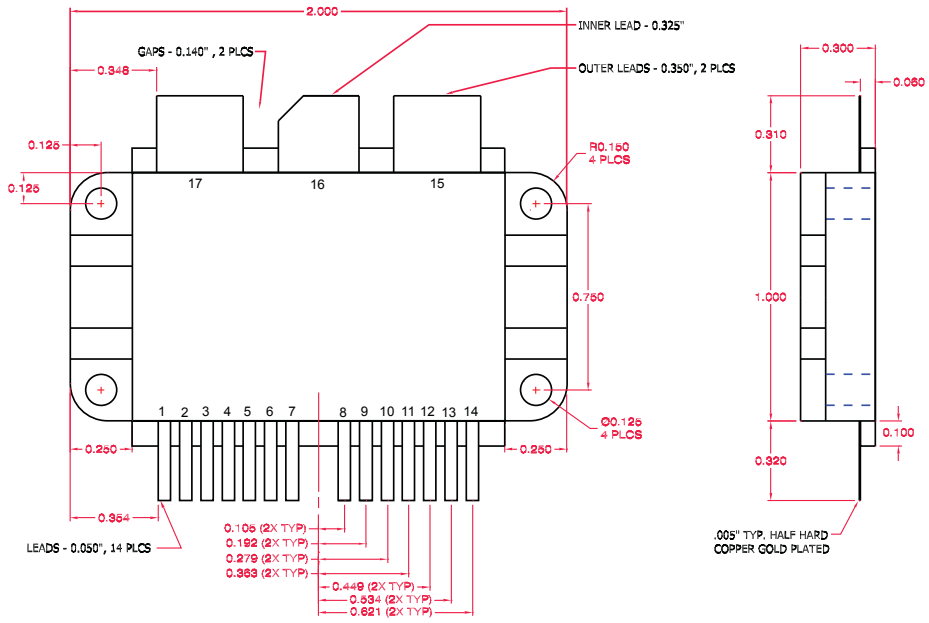
Pin Assignments	
Pin 1	High Side GND
Pin 2	U1 +Vdd
Pin 3	U1 FN
Pin 4	U1 IN
Pin 5	U1 SG
Pin 6	U1 +Vdd
Pin 7	High Side GND
Pin 8	Low Side GND
Pin 9	U2 +Vdd
Pin 10	U2 FN
Pin 11	U2 IN
Pin 12	U2 SG
Pin 13	U2 +Vdd
Pin 14	Low Side GND
Pin 15	Source
Pin 16	Output
Pin 17	Drain



All dimensions are ± .005

Figure 4, DRF1400 Mechanical Outline

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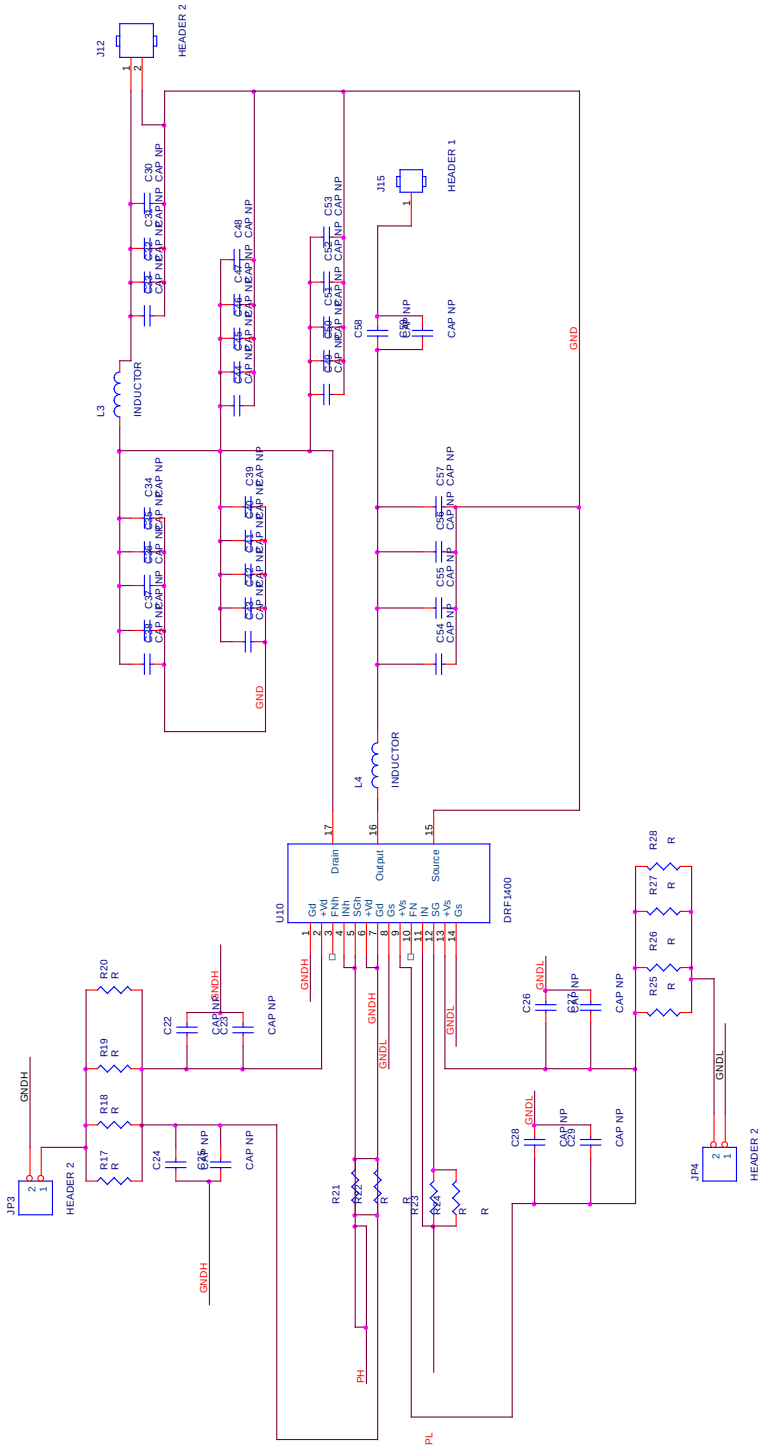


Figure B.3: Schematic of power circuit

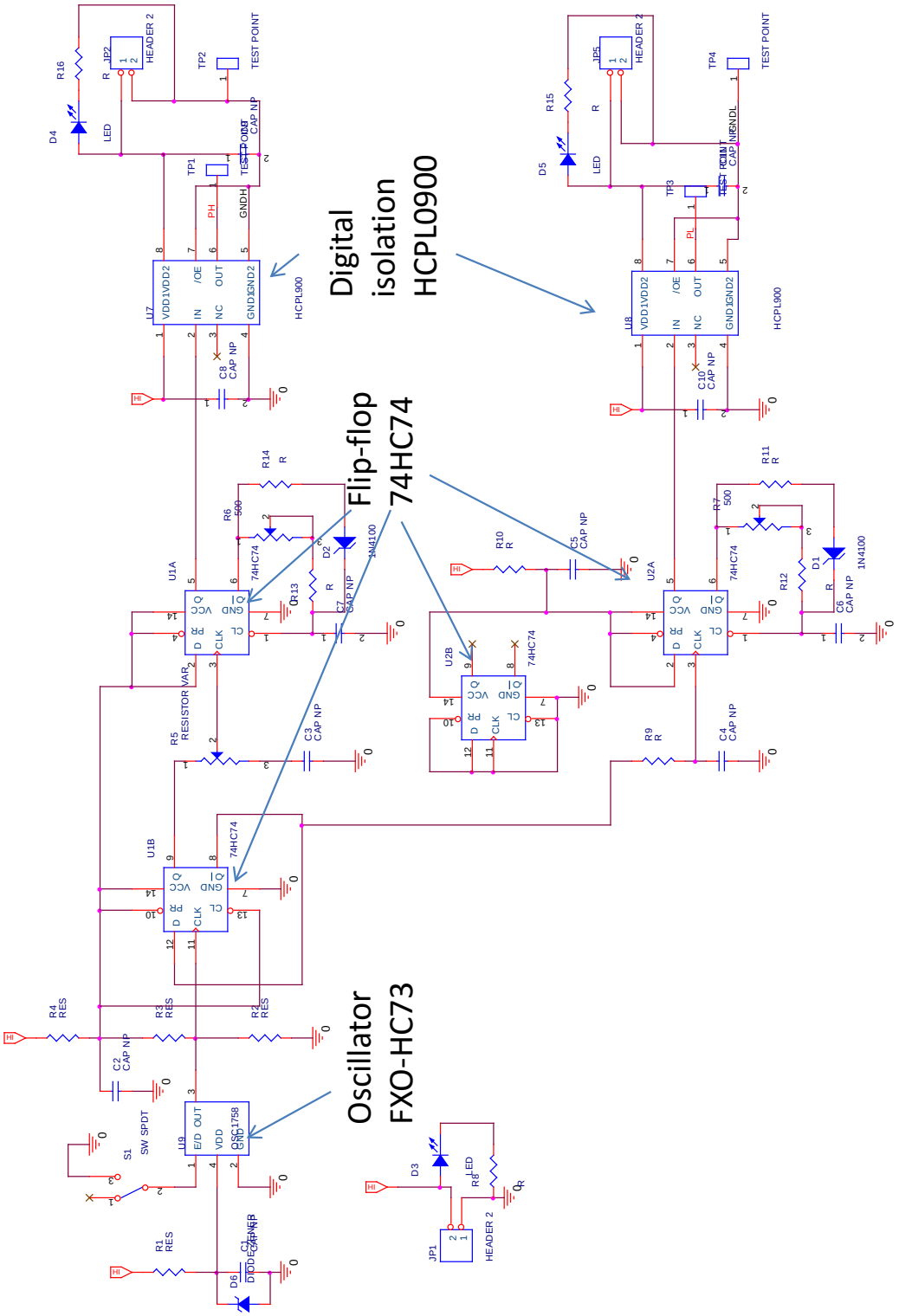


Figure B.4: Schematic of drive circuit

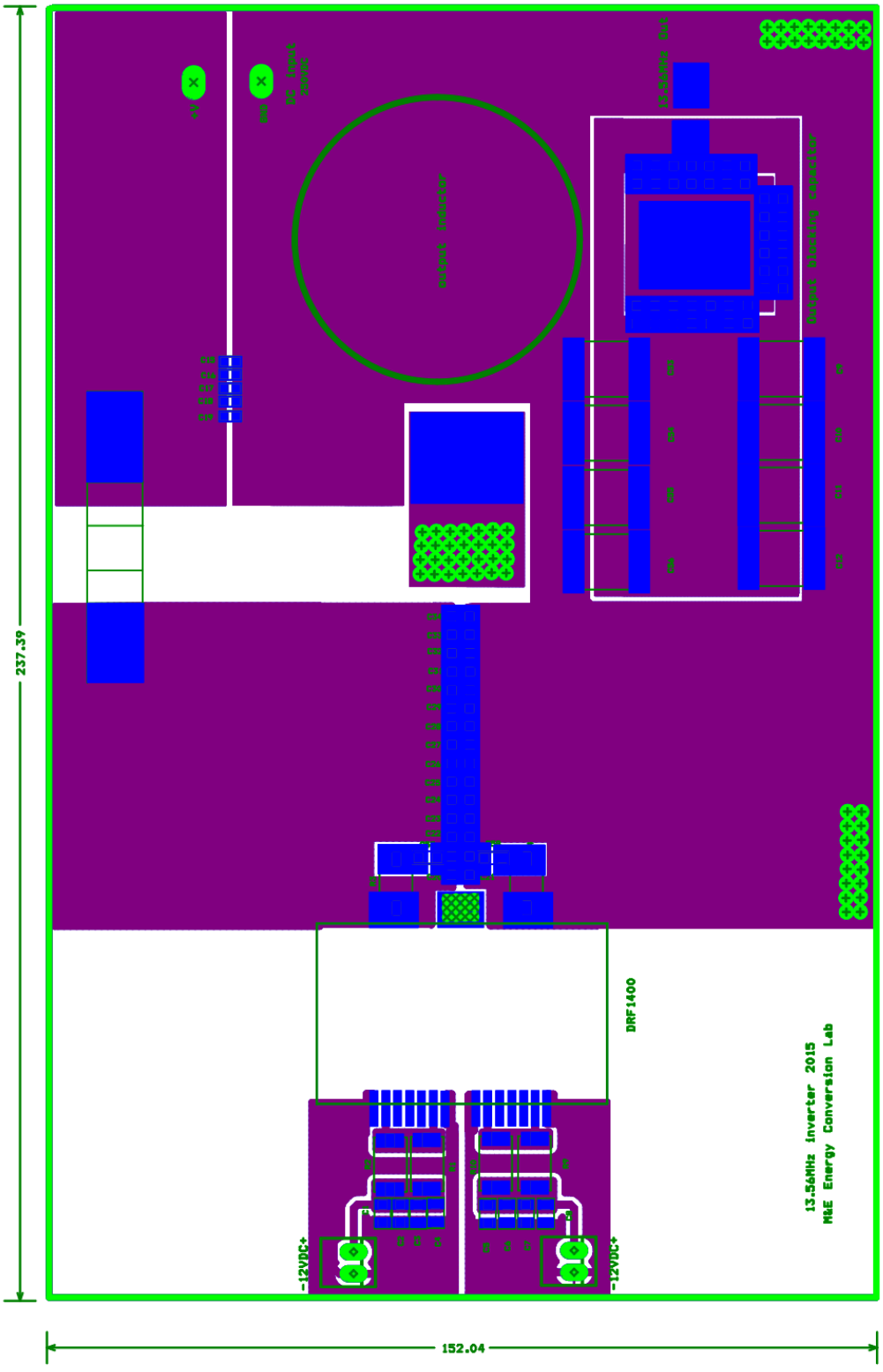


Figure B.5: PCB design

Appendix C

3 kW inverter experiment setup

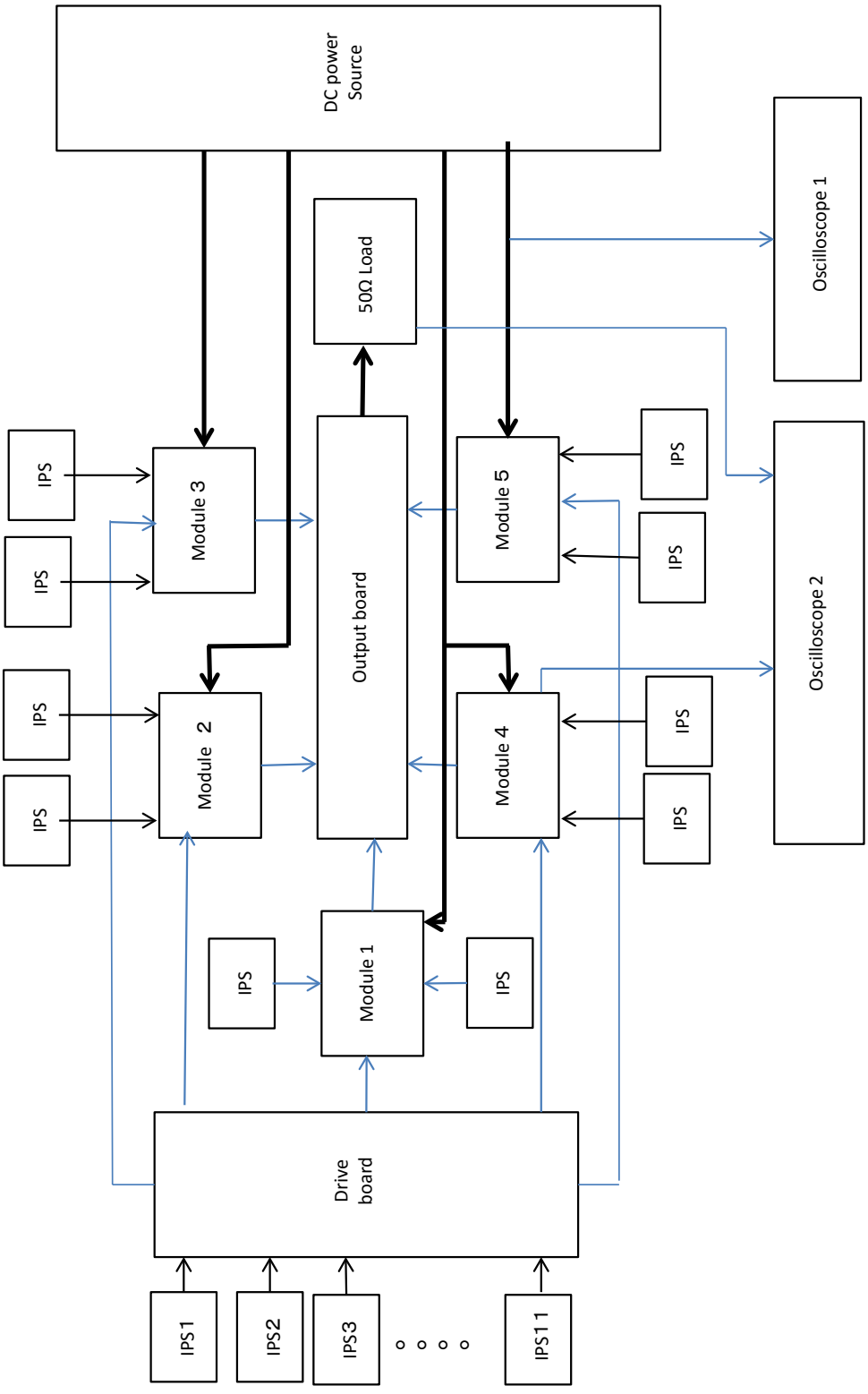


Figure C.1: Structure of experiment setup

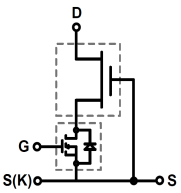
Table C.1: List of devices

Device	Spec.	Manufacture	Part number
Oscilloscope 1	200 MHz/ 2 GS/s	Tektronix	Tektronix TPS 2024B
Voltage probe 1	200 MHz - 100 MΩ/¡12 pF	Tektronix	Tektronix TPP 0201
Oscilloscope 2	100 MHz/ 2.5 GS/s	Tektronix	MSO 3014
Voltage probe 2	500 MHz - 10 MΩ/¡8 pF	Tektronix	Tektronix P6139B
Isolation Power source (IPS1,IPS2,...IPS11)	5 V/0.4 A	Murata	NMK1205SAC
Isolation Power source (IPS)	12V/2.5A	Cosel	MGS302412
Ferrite clamp filter (CMC)	31 Material	Fair-rite corp.	0431164181

Preliminary

PRODUCT SUMMARY (TYPICAL)	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	0.15
Q_{rr} (nC)	54

GaN Power
Low-loss Switch



TO-220 Package

Features

- Low Q_{rr}
- Free-wheeling diode not required
- Quiet Tab™ for reduced EMI at high dv/dt
- GSD pin layout improves high speed design
- RoHS compliant
- High frequency operation

Applications

- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies

Absolute Maximum Ratings (T_C=25 °C unless otherwise stated)				
Symbol	**Parameter**		**Limit Value**	**Unit**
$I_{D25°C}$	Continuous Drain Current @T_C=25 °C		17	A
$I_{D100°C}$	Continuous Drain Current @T_C=100 °C		12	A
I_{DM}	Pulsed Drain Current (pulse width:100 μs)		60	A
V_{DSS}	Drain to Source Voltage		600	V
V_{TDS}	Transient Drain to Source Voltage [a]		750	V
V_{GSS}	Gate to Source Voltage		±18	V
$P_{D25°C}$	Maximum Power Dissipation		96	W
T_C	Operating Temperature	Case	-55 to 150	°C
T_J		Junction	-55 to 175	°C
T_S	Storage Temperature		-55 to 150	°C
T_{Csold}	Soldering peak Temperature [b]		260	°C

Thermal Resistance			
Symbol	**Parameter**	**Typical**	**Unit**
$R_{\Theta JC}$	Junction-to-Case	1.55	°C /W
$R_{\Theta JA}$	Junction-to-Ambient	62	°C /W

Notes
a: For 1 usec, duty cycle D=0.1
b: For 10 sec, 1.6mm from the case

Electrical Characteristics (T_C=25 °C unless otherwise stated)						
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**	**Test Conditions**
Static						
$V_{DSS-MAX}$	Maximum Drain-Source Voltage	600	-	-	V	V_{GS}=0 V
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS}=V_{GS}, I_D=1 mA
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 25 °C)	-	0.15	0.18	Ω	V_{GS}=8V, I_D =11A, T_J = 25 °C
$R_{DS(on)}$	Drain-Source On-Resistance (T_J = 175 °C)	-	0.33	-	Ω	V_{GS}=8V, I_D =11A,T_J = 175 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 25 °C	-	2.5	90	µA	V_{DS}=600V, V_{GS}=0V, T_J = 25 °C
I_{DSS}	Drain-to-Source Leakage Current, T_J = 150 °C	-	10	-	µA	V_{DS}=600V, V_{GS}=0V, T_J = 150 °C
I_{GSS}	Gate-to-Source Forward Leakage Current	-	-	100	nA	V_{GS}= 18 V
	Gate-to-Source Reverse Leakage Current	-	-	-100		V_{GS}= -18 V
Dynamic						
C_{ISS}	Input Capacitance	-	740	-	pF	V_{GS}=0 V, V_{DS}=100 V, *f* =1 MHz
C_{OSS}	Output Capacitance	-	133	-		
C_{RSS}	Reverse Transfer Capacitance	-	3.6	-		
$C_{O(er)}$	Output Capacitance, energy related [a]	-	56	-		V_{GS}=0 V, V_{DS}=0 V to 480 V
$C_{O(tr)}$	Output Capacitance, time related [a]	-	110	-		
Q_g	Total Gate Charge [b]	-	6.2	9.3	nC	V_{DS} =100 V [a], V_{GS}= 0-4.5 V, I_D = 11 A
Q_{gs}	Gate-Source Charge	-	2.1	-		
Q_{gd}	Gate-Drain Charge	-	2.2	-		
$t_{d(on)}$	Turn-On Delay	-	4.5	-	ns	V_{DS} =480 V , V_{GS}= 0-10 V, I_D = 11 A, R_G= 2 Ω
t_r	Rise Time	-	3.1	-		
$T_{d(off)}$	Turn-Off Delay	-	12	-		
t_f	Fall Time	-	5.2	-		
Reverse operation						
I_S	Reverse Current	-	-	11	A	V_{GS}=0 V, T_J=100 °C
V_{SD}	Reverse Voltage	-	2.3	2.8	V	V_{GS}=0 V, I_S=11 A, T_J=25 °C
V_{SD}	Reverse Voltage	-	1.6	1.9	V	V_{GS}=0 V, I_S=5.5 A, T_J=25 °C
t_{rr}	Reverse Recovery Time	-	30	-	ns	I_S=11 A, V_{DD}=480 V, di/dt =450 A/µs, T_J=25 °C
Q_{rr}	Reverse Recovery Charge	-	54	-	nC	

Notes
a: Fixed while V_{DS} is rising from 0 to 80% V_{DSS} ;
b: Q_g does not change for V_{DS}>100 V.

Typical Characteristic Curves 25 °C unless otherwise noted

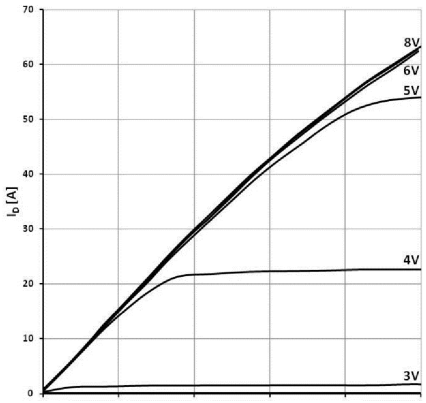


Fig. 1. Typical Output Characteristics T_J= 25 °C
Parameter: V_{GS}

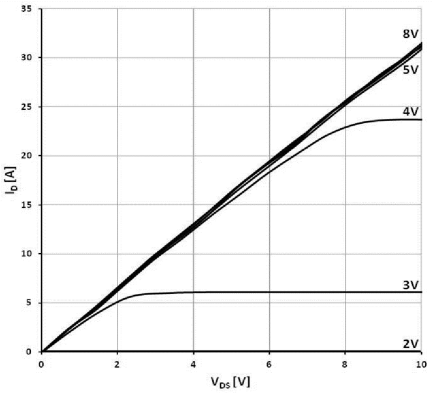


Fig. 2. Typical Output Characteristics T_J=175 °C
Parameter: V_{GS}

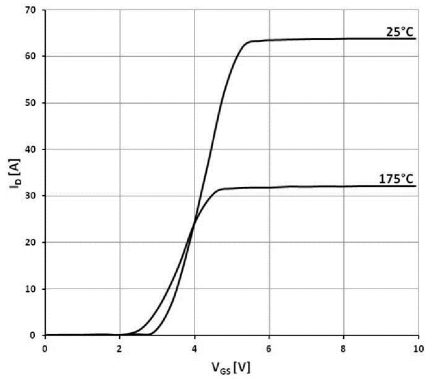


Fig. 3. Typical Transfer Characteristics
V_{DS}=10 V, Parameter: T_J

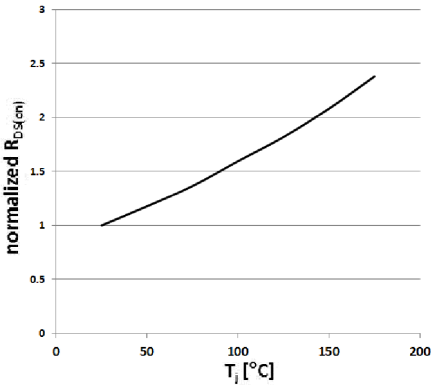


Fig. 4. Normalized On-Resistance
I_D=12 A, V_{GS}=8 V

Typical Characteristic Curves 25 °C unless otherwise noted

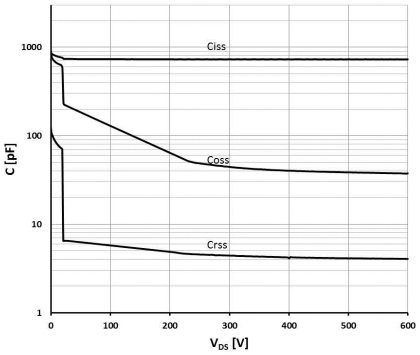


Fig. 5. Typical Capacitance
V_{GS}=0 V, f=1 MHz

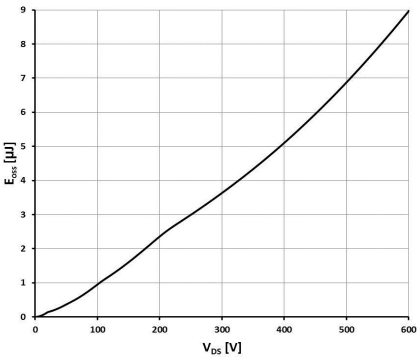


Fig. 6. Typical C_{OSS} Stored Energy

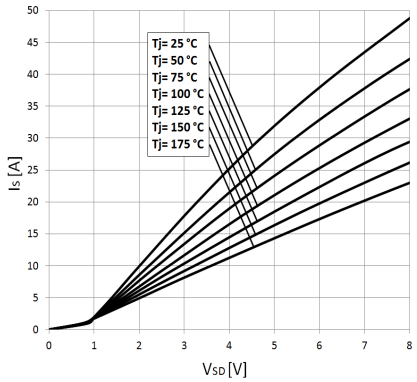


Fig. 7. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$; parameter Tj

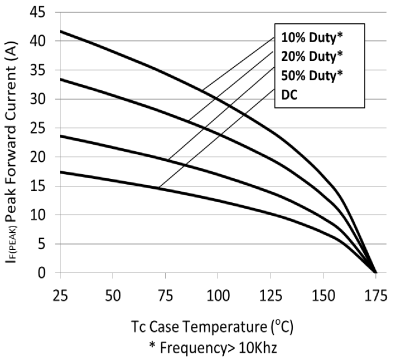


Fig. 8. Current Derating

Typical Characteristic Curves 25 °C unless otherwise noted

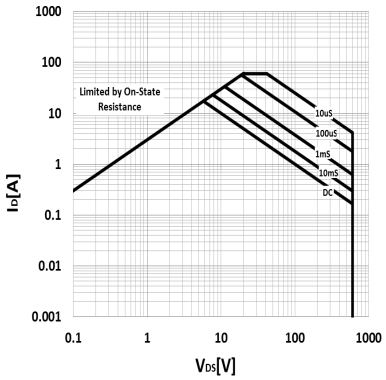


Fig. 9. Safe Operating Area T_C = 25 °C

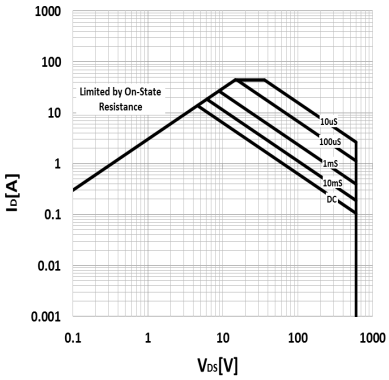


Fig. 10. Safe Operating Area T_C = 80 °C

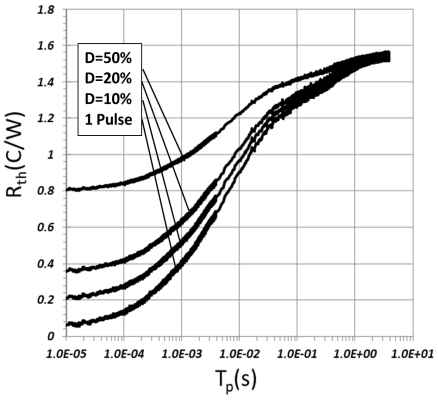


Fig. 11. Transient Thermal Resistance

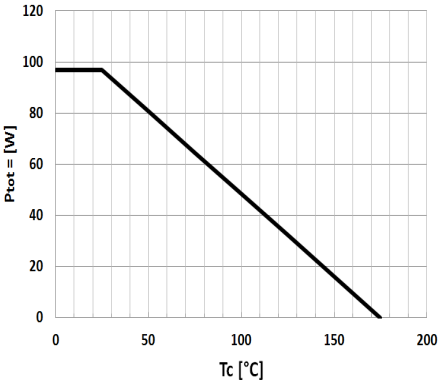


Fig. 12. Power Dissipation

Test Circuits and Waveforms

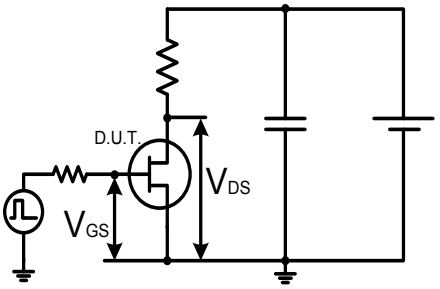


Fig. 13. Switching Time Test Circuit

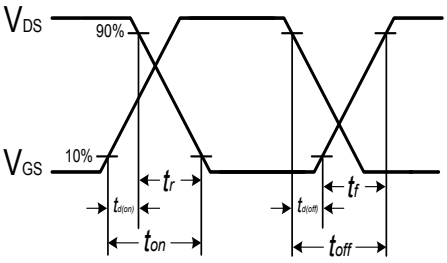


Fig. 14. Switching Time Waveform

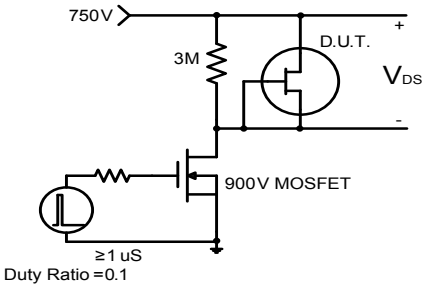


Fig. 15. Spike Voltage Test Circuit

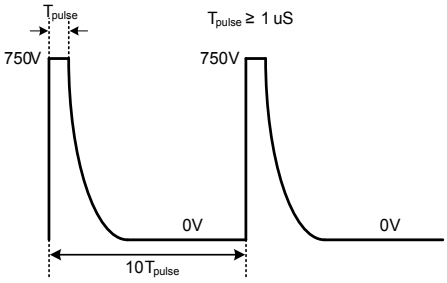


Fig. 16. Spike Voltage Waveform

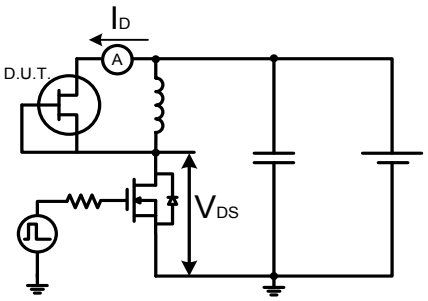


Fig. 17. Test Circuit for Diode Characteristics

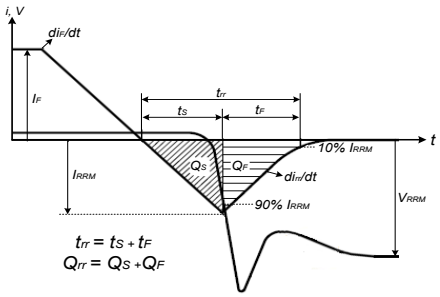
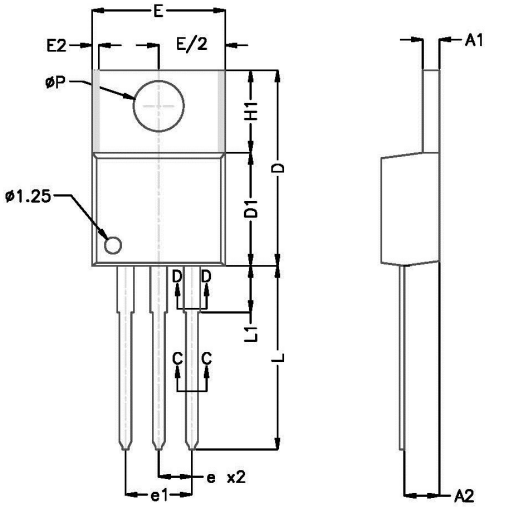
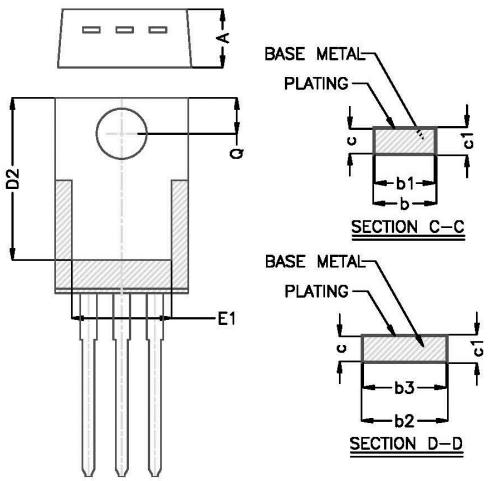


Fig. 18. Diode Recovery Waveform

MECHANICAL TO-220 Package





SYMBOL	MILLIMETERS			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	3.56	4.45	4.83	0.140	0.175	0.190
A1	0.51	1.27	1.40	0.020	0.050	0.055
A2	2.03	–	2.92	0.080	–	0.115
b	0.38	–	1.01	0.015	–	0.040
b1	0.38	–	0.97	0.015	–	0.038
b2	1.14	–	1.78	0.045	–	0.070
b3	1.14	1.27	1.73	0.045	0.050	0.068
c	0.38	–	0.61	0.014	–	0.024
c1	0.38	0.38	0.56	0.014	0.015	0.022
D	14.22	–	16.51	0.560	–	0.650
D1	8.38	8.64	9.02	0.330	0.340	0.355
D2	11.68	–	12.88	0.460	–	0.507
E	9.85	10.19	10.67	0.380	0.401	0.420
E1	6.86	–	8.89	0.270	–	0.350
E2	–	–	0.76	–	–	0.030
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	5.84	6.30	6.86	0.230	0.248	0.270
L	12.70	14.05	14.73	0.500	0.553	0.580
L1	–	–	6.35	–	–	0.250
øP	3.54	3.84	4.08	0.139	0.151	0.161
Q	2.54	–	3.42	0.100	–	0.135

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. DIMENSIONS E2 & H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
3. OUTLINE CONFORMS TO JEDEC TO–220AB.

TO-220 Package

Pin 1: Gate, Pin 2: Source, Pin 3: Drain, Tab: Source

Important Notice

Transphorm Gallium Nitride (GaN) Switches provide significant advantages over silicon (Si) Superjunction MOSFETs with lower gate charge, faster switching speeds and smaller reverse recovery charge. GaN Switches exhibit in-circuit switching speeds in excess of 150 V/ns and can be even pushed up to 500V/ns, compared to current silicon technology usually switching at rates less than 50V/ns.

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN Switches requires adherence to specific PCB layout guidelines and probing techniques .

Transphorm suggests visiting application note “Printed Circuit Board Layout and Probing for GaN Power Switches” before evaluating Transphorm GaN switches. Below are some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Switches	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing. Attach the probe and its ground connection directly to the test points	Use differential mode probe, or probe ground clip with long wire

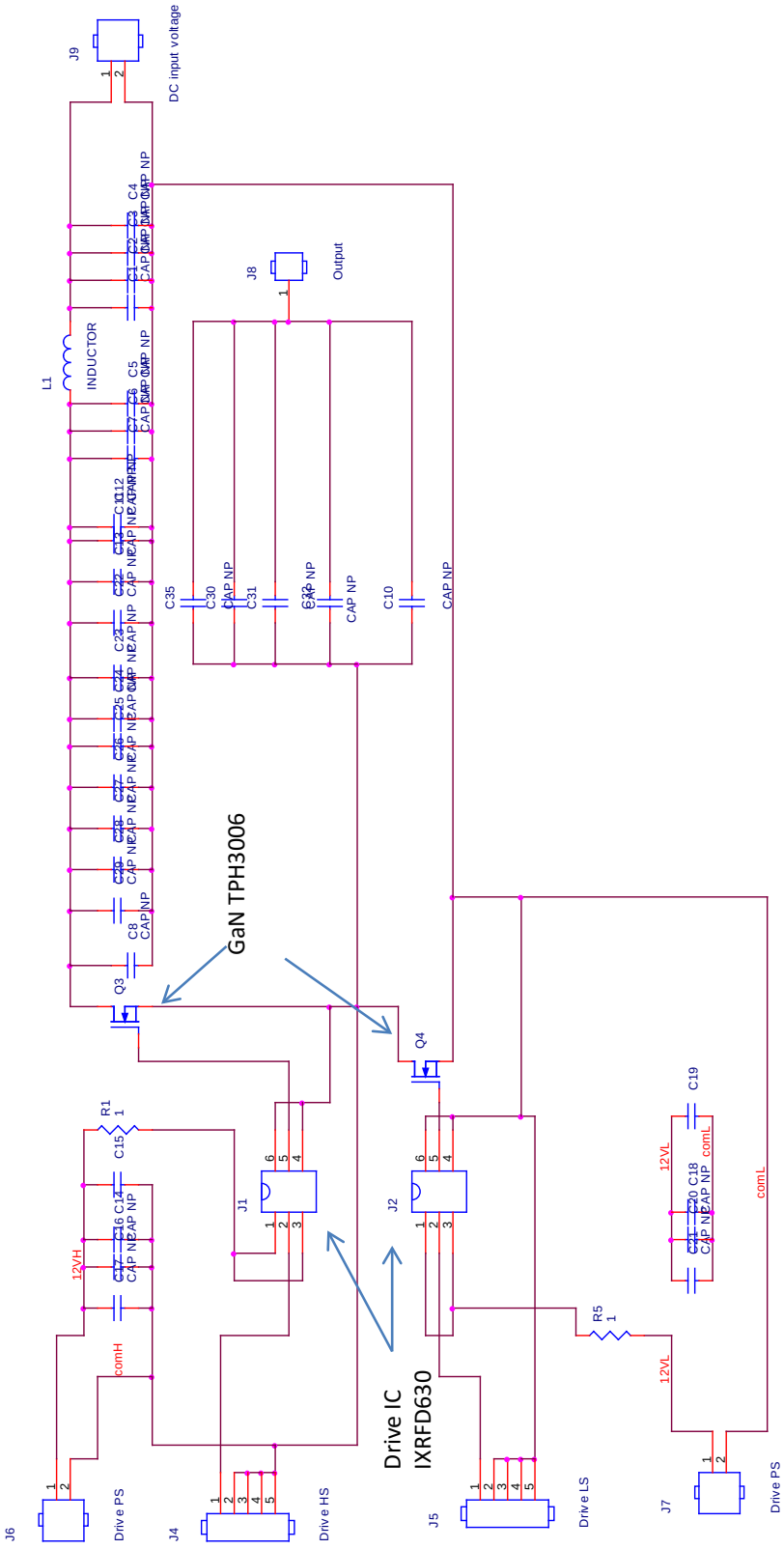


Figure C.2: Schematic of module

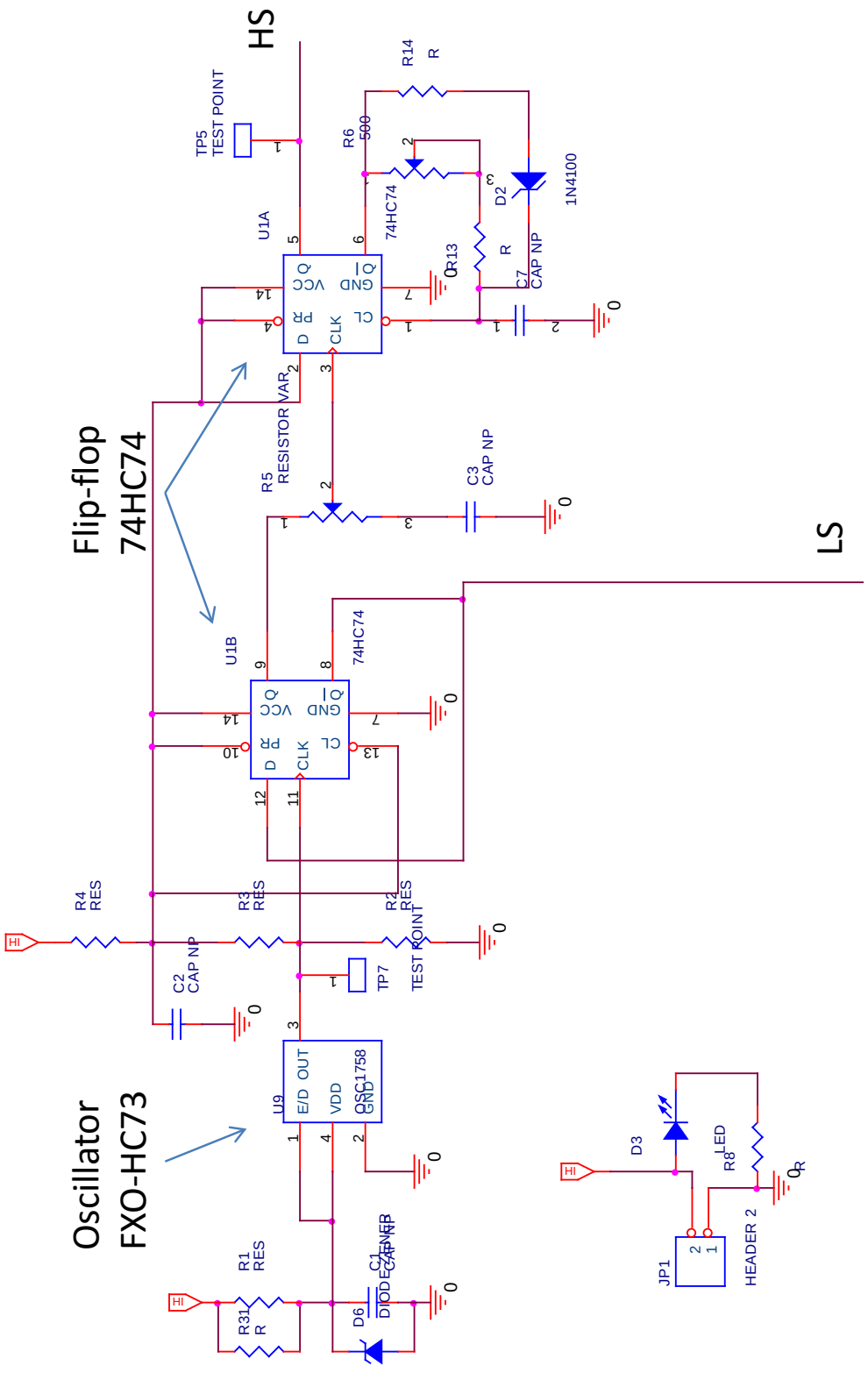


Figure C.3: Schematic of drive circuit

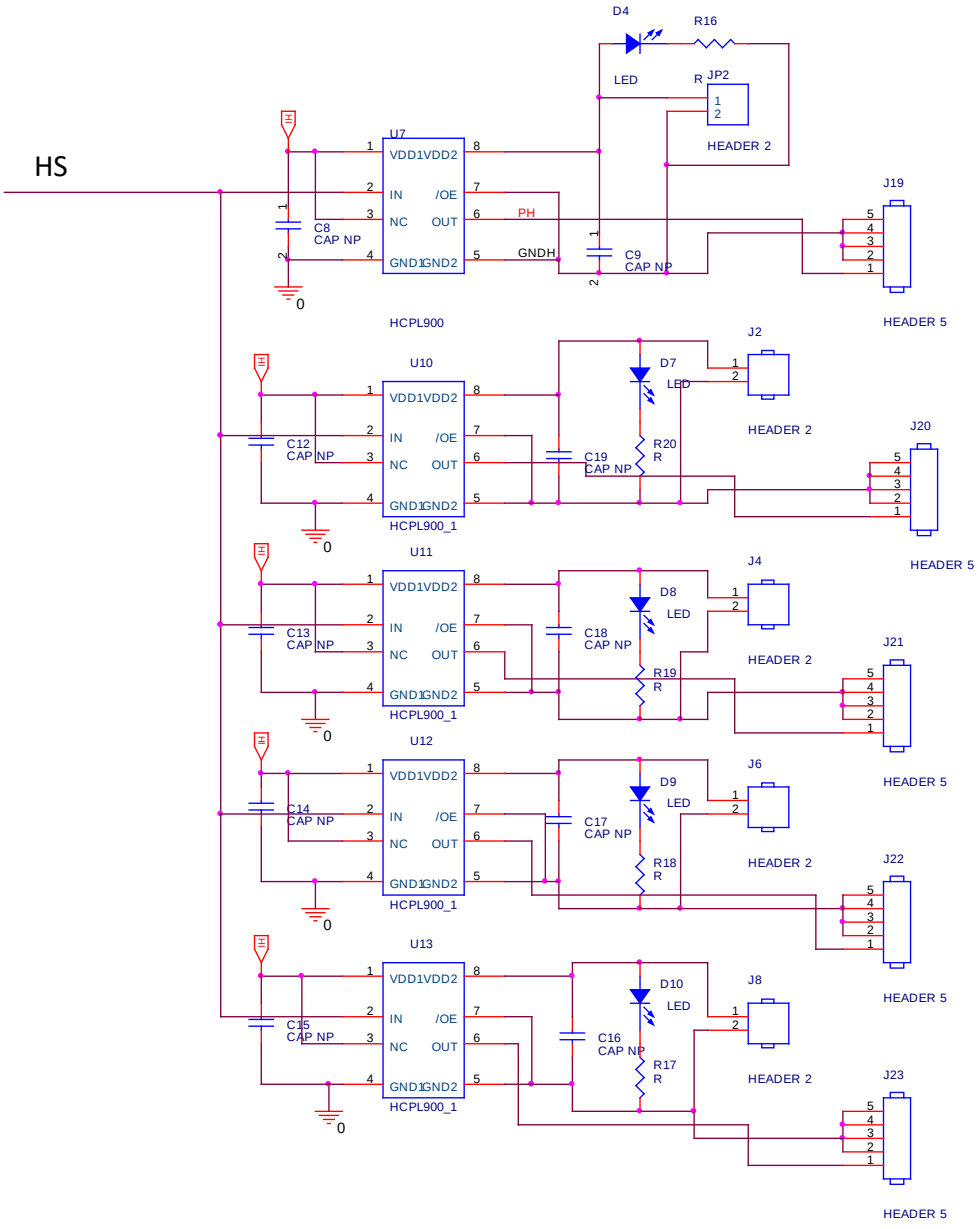


Figure C.4: Schematic of drive circuit (continue)

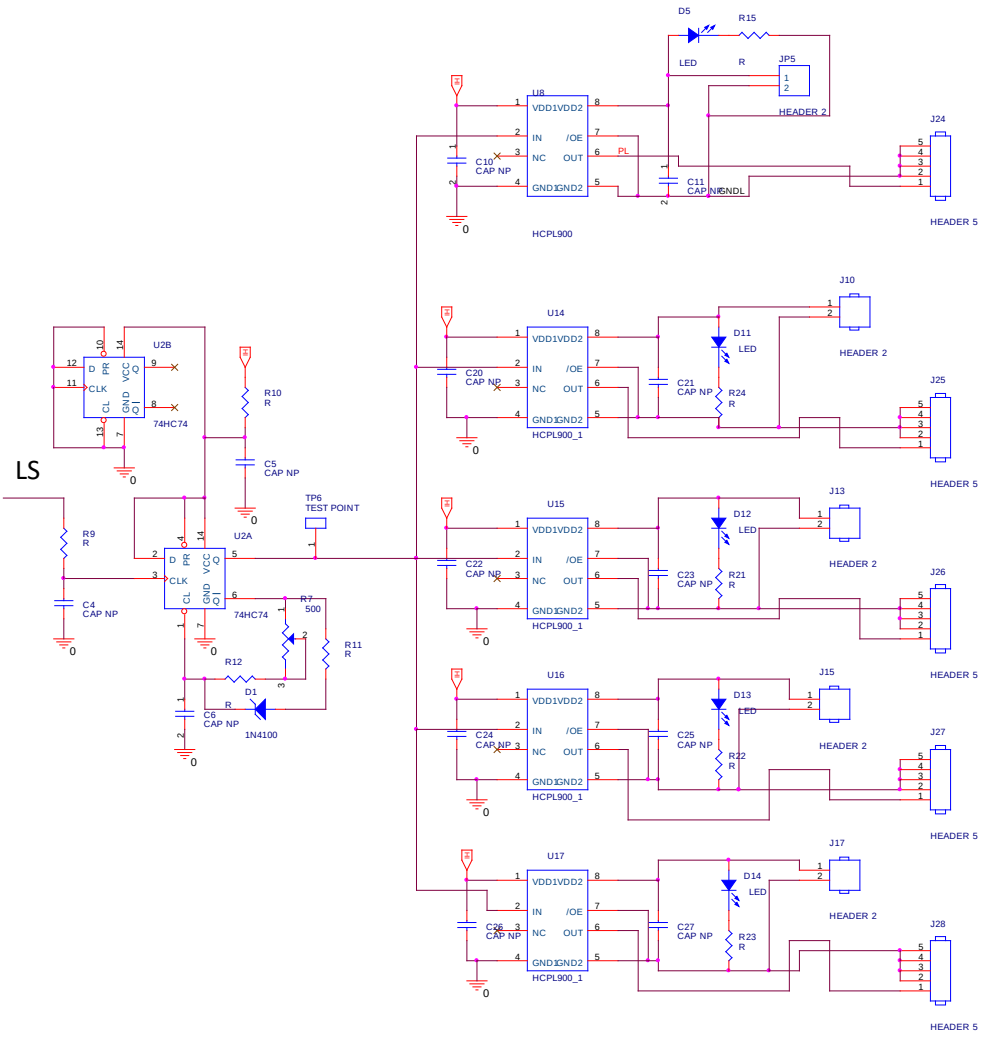


Figure C.5: Schematic of drive circuit (continue)

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List of Publications

Transaction paper

[T.1] N. K. Trung, T. Ogata, S. Tanaka, K. Akatsu, "Analysis and PCB Design of Class D Inverter for Wireless Power Transfer Systems Operating at 13.56 MHz", *IEEJ Journal of Industry Application*, Vol. 4, No. 6, 2015, pp. 703-713.

[T.2] N. K. Trung, T. Ogata, S. Tanaka, K. Akatsu, "Attenuate influence of parasitic elements in 13.56MHz inverter for wireless power transfer systems", *IEEE Transaction on Power Electronic* (Under-review)

[T.3] N. K. Trung and K. Akatsu, "Design high power and high efficiency inverter operating at 13.56MHz for wireless power transfer systems", *IEEE Transaction on Power Electronic* (Under-review)

International Conference Paper

[I.1] N. K. Trung and Kan Akatsu,"Analysis and design of a 13.56 MHz resonant inverter for wireless power transfer systems",*in proc. South East Asian Technical University Consortium (SEATUC)*, p.[OS10]13-16,2014

[I.2] N. K. Trung, T. Ogata, S. Tanaka and K. Akatsu, "PCB design for 13.56MHz half-bridge class D inverter for wireless power transfer system", *9th International conference on power electronic-ECCE Asia (ICPE- 2015 ECCE Asia)*,June 1-5, 2015, Seoul, Korea, pp. 1692-1699.

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[I.5] N. K. Trung and Kan Akatsu, "Design high power and high efficiency power source for dynamic wireless charging systems", *in proc. EVtec 2016 & APE*, 2016 Japan, p[2016-9015], pp. 1-6.

[I.6] N. K. Trung and Kan Akatsu, "Design high power and high efficiency inverter operating at 13.56MHz for wireless power transfer systems ", *IEEE Energy Conversion Congress and Exposition (ECCE) 2016* (Accepted)

Domestic Conference Paper

[D.1] N. K. Trung and Kan Akatsu, "Design 1.5kW 13.56MHz class D resonant inverter for wireless power transfer systems", *in proc. IEE-Japan Industry applications Society Conference (JIASC2014)*, p.367-370, 2014

[D.2] N. K. Trung and Kan Akatsu, "Analysis and ringing suppressing method in 13.56MHz resonant inverter for wireless power transfer systems",*in proc. 2nd green innovation symposium*, poster section, 2015

[D.3] N. K. Trung, T. Ogata, S. Tanaka and K. Akatsu, "Attenuate influence of parasitic elements in 13.56MHz inverter for wireless power transfer systems",*in proc. IEE-Japan Industry applications Society Conference (JIASC2015)*,2015, pp.131-134.

[D.4] N. K. Trung and Kan Akatsu, "13.56MHz high efficiency inverter for wireless power transfer systems using cascode GaN HEMT", *in proc. 3rd green innovation symposium*, poster section, 2016

[D.5] N. K. Trung and K. Akatsu, "13.56 MHz Multiphase resonant inverter design",*in proc. IEE-Japan Industry applications Society Conference (JIASC2016)*,2016, pp.367-370.

[D.6] M. Sato, N. K. Trung and K. Akatsu, "An Examination of wireless power transfer system for receiving side operating at 13.56 MHz",*in proc. IEE-Japan Industry applications Society Conference (JIASC2016)*,2016, pp.323-326.