American Scientific Research Journal for Engineering, Technology, and Sciences (ASRJETS)
ISSN (Print) 2313-4410, ISSN (Online) 2313-4402

http://asrjetsjournal.org/

Implementing Transimpedance Amplifier in 0.35 µm CMOS Technology

Omar Humaid Al Ali[a*], Omar Abdul aziz Al Ali[b]

[a,b,c]*College of Engineering, Department of Electrical and Computer Engineering, Abu Dhabi University – Abu Dhabi, UAE*

[a]*Email: 1069941@students.adu.ac.ae*

[b]*Email: 1070932@students.adu.ac.ae*

Abstract

The following will be the design mechanism of the transimpedance amplifier and the RF resistor feedback, as well as how it is performed using the 0.35µm CMOS technique. The NMOS transistor has been placed from the conventional transimpedance amplifier as an active feedback contractor. We apply 3.3V voltage and 0.5µA photocurrent works in a circuit. The transimpedance amplifier is proposed after noise reduction, thus quantitating the larger dynamic range and in same time large gain. The simulation work of the transimpedance gain results in both of the single-phase and three-phase transimpedance amplifiers at the voltage gate which is 4.43 cubic meters and 4.39 cubic meters. Then the one-phase power dissipation and three-phase transimpedance amplifier is 602.04 µW and 1.781mW in the voltage gate of 2.0V [1,2].

Keywords: CMOS; negative feedback; Technology; low noise amplifier; optical receive; Transimpedance amplifier.

1. Introduction

Transimpedance amplifier (TIA), which is done by a circuit that converts the input current signal to a output signal of the voltage which depends on the current size. We also note that in the modern era the rate of demand for the transfer of data via the Internet has become very high as a result of the rapid development of optical communication system with High speed. Transimpedance that the amplifiers located within the circuit is very important for the visual communication system. The front of the shake, Transimpedance amplifier (TIA) is one of the most important blocks of construction in electricity to be an optical interface on the receiver side. To perform the identification process to perform the entire system.

---

* Corresponding author.

Of speed, sensitivity, noise, gains etc. Optical performance, the interconnection system depends on the bandwidth and gain of the receiver, noise and power. Consumption. Silicon-based CMOS Technology, the level of integration can be achieved with the speed and reasonable cost of energy consumption through it only. Transimpedance amplifier as shown In Figure 1 the circuit is used as a closed loop and this circuit helps to obtain a trade-off between high and low resistance configuration and help to avoid the problem of dynamic range. It relatively dynamic range and high bandwidth as well as good noise level.

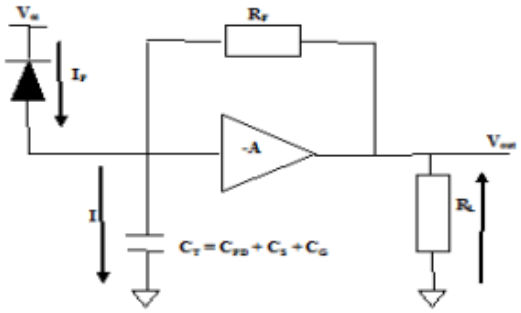

Figure 1: Block diagram of transimpedance amplifier used in an optical receiver

By increasing the open loop we can improve the bandwidth and the gain of amplifiers. Increasing the number of stages of amplifier configuration thus the transmission speed. Transimpedance amplifier parameters such as transimpedance gained power consumption and output voltage in 0.35µm CMOS technology.

2. Circuit discription

Note the CMOS transimpedance amplifier circuit The inverter is used to push the pull on the input to maximize the The Transconduction of the amplifier to increases its gain and to Product bandwidth (GBP) See Figure 2

The transimpedance amplifier get a current from input and converts the current into a voltage signal. The transistor Transistor 1 and Transistor 3 from the inverter while Transistor 2 is added to minimize the miller effect and also to increases the bandwidth.

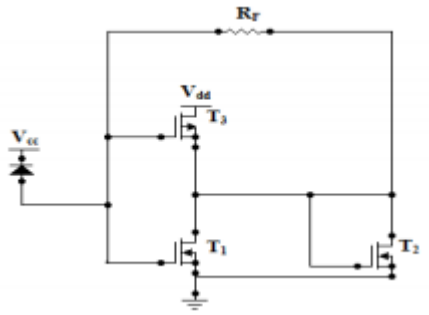

Figure 2: CMOS transimpcdance amplifier

The transimpedance amplifier get a current from input and convert the current into a voltage signal. The transistor 1 and transistor 3 from the inverter while Transistor 2 is added to increases the bandwidth and minimizes the miller effect.

The expression of gain for transimpedance amplifier will be:

$$A_O = \frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{m2}}{g_{m2}} \qquad (1)$$

where: gm1, gm2, gm3 = transconduction of Transisitor 1, Transisitor 2 and Transisitor 3, The other expression for geeting the gain for transimpedance amplifier given by:

$$A_o = \alpha + \sqrt{\frac{\mu p}{\mu n}\beta\,(1+\alpha)} \qquad (2)$$

where:

$$\alpha = \frac{W_1 L_2}{W_2 L_1} \quad \textbf{and} \quad \beta = \frac{W_3 L_2}{W_2 L_3} \qquad (3)$$

2.1 Proposed Single Stage Transimpedance Amplifier

Our amplifier component of single transimpedance consists of three different NMOS single transistor and one PMOS transistor and is used in the photocurrent circuit of 0.5µA in the process of switching the TIA circuit from a single phase RF circuit with the NMOS transistor to act as a resistor to the active reaction biased to the VG voltage gate. For each PMOS transistor, a 3.3V VVD voltage source and using a 1.0µm transistor width and a 0.35µm length for the NMOS transistor in the circuit. Amplifies the signal from input in the circuit to output of it. Transimpedance amplifier output is taken in the Terminal of the Vout, and part of the output is given input by amplifier input, as shown in Figure 3.

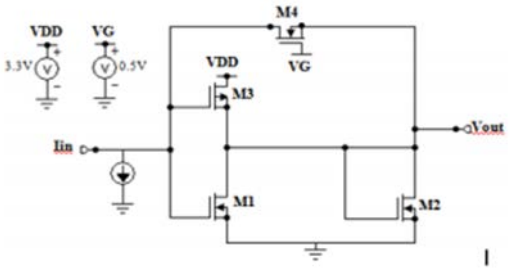

Figure 3: Proposed single stage CMOS transimpedan amplifier

2.2 Proposed Three Stages Transimpedance Amplifier

Here the three-phase amplifier consists of three PMOS transistors and three consecutive stages identical to seven NMOS transistors. We used photocurrent of 0.5µA in the circuit. The frequency of the TIA radio feeder is replaced by the NMOS transistor in the three stages proposed as an active feedback resistor biased by VG voltage gate. There is a voltage source of 3.3V VDD that is applied to each PMOS transistor. NMOS transistor widths 1µm and length Of 0.35µm and PMOS transistor widths of 2µm and 0.35µm are used in the circuit. See figure 4.

The feedback resistor will be determined using

$$R_F = \frac{1}{\frac{W}{L}\mu C_{OX}(V_{GS} - V_T)} \qquad (4)$$

where W =width, L = length, VGS = gate to source voltage,VT =threshold voltage

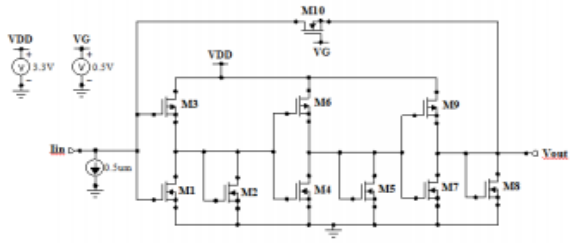

Figure 4: Three stages CMOS transimpedance amplifier

To find the bandwidth of transimpedance amplifier is equal approximately to:

$$f_{-3dB} = \frac{1 + A}{2\Pi R_F C_T} \qquad (5)$$

Also to find the stability of the system which's related to A, and total gain of the system must be controlled. This is given by

$$A = A_0^3 \qquad (6)$$

Where A0 is the open loop gain of the single stage

3. Results and discussion

3.1 Single Stage TIA

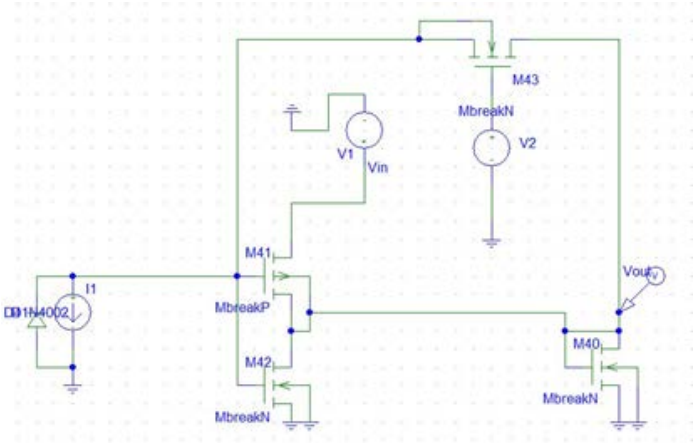

Figure 5

With different voltage volt gate size from [0.4 - 2.0] V for single stage Transimpedance amplifier [Figure 3]. The consumption of the power varies from [1.51 – 1.34] µW with the gate voltage change in from [0.4 - 2.0] V. The output voltage varies from [3.03 – 2.68] V with a difference in the VG gate size of [0.4 - 2.0] V. The Transimpedance gain changed from [6.06 – 5.36] M with the change in gate voltage size for the voltage of [0.4 - 2.0] V

Gate voltage

VG (V) Power consumption (µW) Output voltage Transimpedance gain (MΩ)

0.4 1.51 3.03 6.06

0.8 1.48 2.97 5.94

1.2 1.44 2.89 5.78

1.6 1.39 2.78 5.56

2.0 1.34 2.68 5.36

Table 1: changing of power and transimpedance gain with gate voltage

Gate voltage VG (V)	**Power consumption (µW)**	**Output voltage**	**Transimpedance gain (MΩ)**
0.4	1.51	3.03	6.06
0.8	1.48	2.97	5.94
1.2	1.44	2.89	5.78
1.6	1.39	2.78	5.56
2.0	1.34	2.68	5.36

Table 2 shows the output voltage, consumption of the power, and level of transimpedance gain with differing NMOS transistor width [0.5-3.0] µm for single phase TIA [Figure 3]. The power consumption of the amplifier

changes from [1.65 – 1.35] µW varies with the contrast in the NMOS transistor width from [0.5 - 3.0] µm as in figure 11 . The output voltage of [3.3-2.65] V varies with the contrast in the NMOS transistor width of [0.5 - 3.0] µm as in figure 9. The Transimpedance gain varies from [6.06 – 5.30] M with contrast In the NMOS transistor width of [0.5 -3.0] µm as in figure 10.

Table 2: Changing of power and transimpedance gain with width of NMOS

Width Wn (µm)	Power consumption (µW)	Output voltage Vout (V)	Transimpedance gain (MΩ)
0.5	1.35	3.3	6.6
1.0	1.37	3.15	6.3
1.5	1.51	2.96	5.92
2.0	1.59	2.78	5.56
2.5	1.625	2.67	5.34
3.0	1.65	2.65	5.30

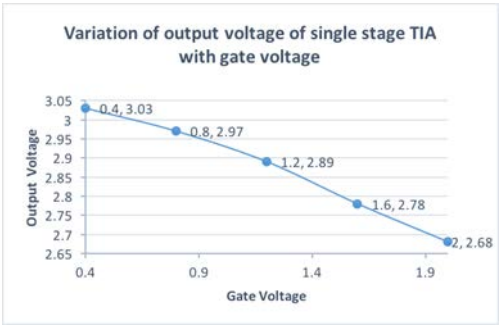

Figure 6

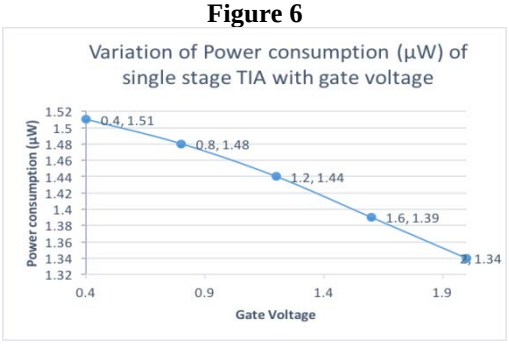

Figure 7

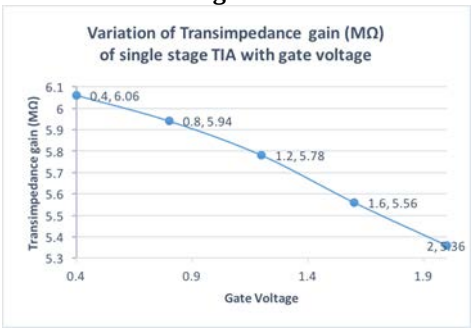

Figure 8

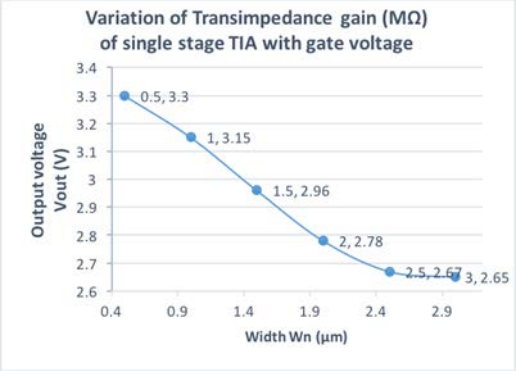

Figure 9

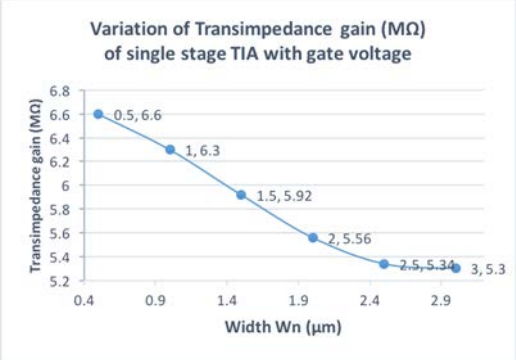

Figure 10

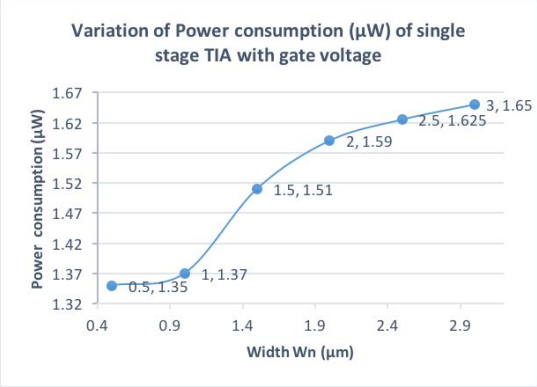

Figure 11

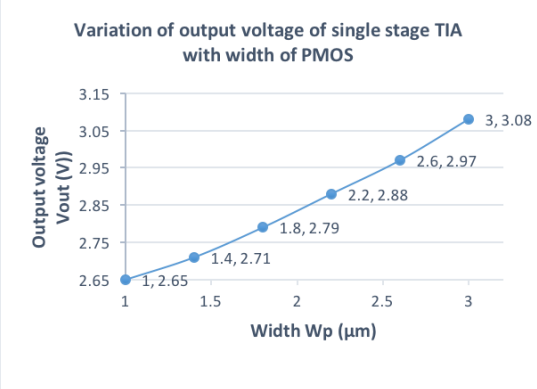

Figure 12

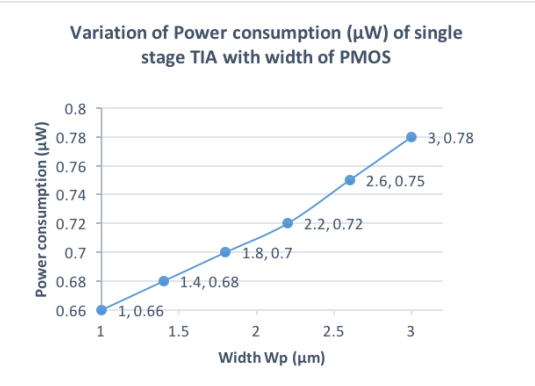

Figure 13

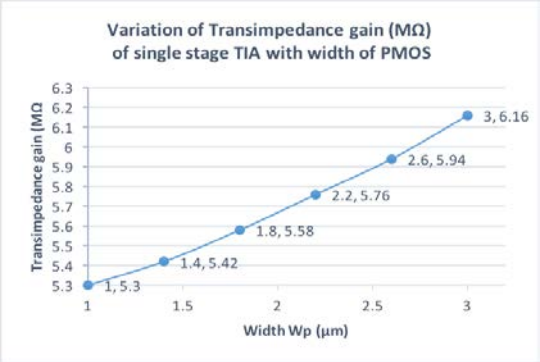

Figure 14

Width Wn (µm)	Power consumption (µW)	Output voltage Vout (V)	Transimpedance gain (MΩ)
0.5	1.35	3.3	6.6
1.0	1.37	3.15	6.3
1.5	1.51	2.96	5.92
2.0	1.59	2.78	5.56
2.5	1.625	2.67	5.34
3.0	1.65	2.65	5.30

Table 3 shows the voltage output, ,transimpedance gain level consumption of the power with change width of PMOS transistor [1.0 – 3.0] µm for single stage TIA [Figure 3]. Transimpedance gain change from [5.3– 6.16] MΩ with the changing in the width of PMOS transistor from [1.0 – 3.0] µm as in figure 14. Also the Power consumption change from [0.66 – 0.78] µW with the changing in the width of PMOS transistor from [1.0 – 3.0]µm as in figure 12.The voltage output change from [2.65 –3.08] V with the changing in the width of PMOS transistor from [1.0 – 3.0] µm as in figure 13.

Width Wp (µm)	Power consumption (µW)	Output voltage Vout (V)	Transimpedance gain(MΩ)
1.0	0.66	2.65	5.3
1.4	0.68	2.71	5.42

1.8 0.7 2.79 5.58

2.2 0.72 2.88 5.76

2.6 0.75 2.97 5.94

3.0 0.78 3.08 6.16

Table 3: changing of power and transimpedance gain with width of PMOS

Width Wp (μm)	Power consumption (μW)	Output voltage Vout (V)	Transimpedance gain(MΩ)
1.0	0.66	2.65	5.3
1.4	0.68	2.71	5.42
1.8	0.7	2.79	5.58
2.2	0.72	2.88	5.76
2.6	0.75	2.97	5.94
3.0	0.78	3.08	6.16

Gate voltage (V) Power consumption (μW) Output voltage (V) Transimpedanece gain (MΩ)

0.4 3.656 3.01 6.02

0.8 3.583 2.98 5.86

1.2 3.486 2.83 5.72

1.6 3.365 2.71 5.37

2.0 3.244 2.62 5.29

3.2 Three Stage TIA

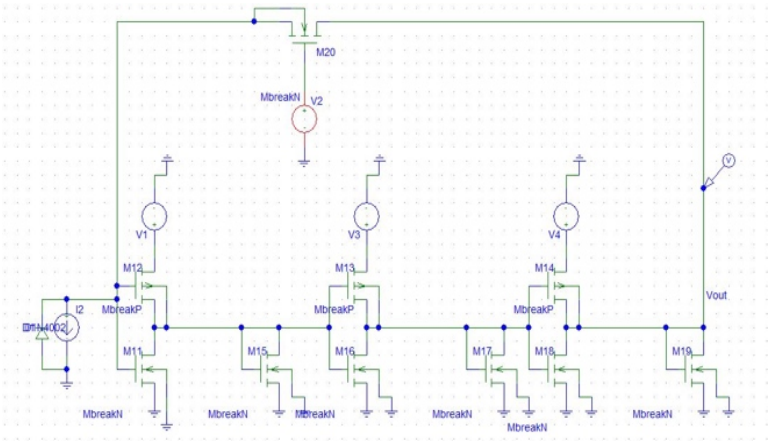

Figure 15

As shown in table 4 the transimpedance gain level change with changing in the magnitude of gate voltage VG [0.4 – 2.0] V for three stage TIA [Figure 4]. Consumption power change from [3.656– 3.244] µW with the changing in magnitude of gate voltage VG from [0.4 – 2.0] V as shown in figure 17.

Also the voltage output change from [3.01–2.62] V with the changing in magnitude of gate voltage VG from [0.4 – 2.0] V as shown in figure 16.

The Transimpedance gain change from [6.02 – 5.29] MΩ with the changing in magnitude of gate voltage VG from [0.4 – 2.0] V as shown in figure 18.

Table 4: changing of power and transimpedance gain with gate voltage

Gate voltage (V)	Power consumption (µW)	Output voltage (V)	Transimpedance gain (MΩ)
0.4	3.656	3.01	6.02
0.8	3.583	2.98	5.86
1.2	3.486	2.83	5.72
1.6	3.365	2.71	5.37
2.0	3.244	2.62	5.29

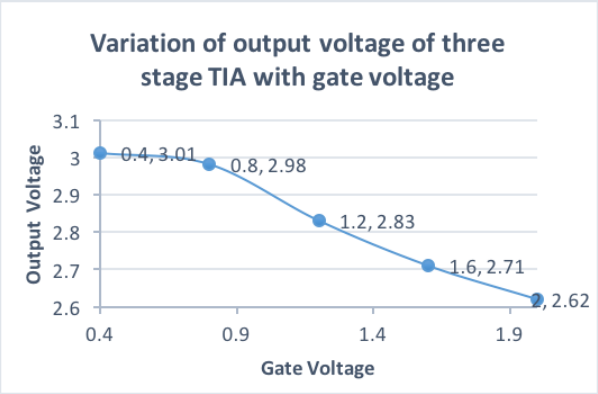

Figure 16

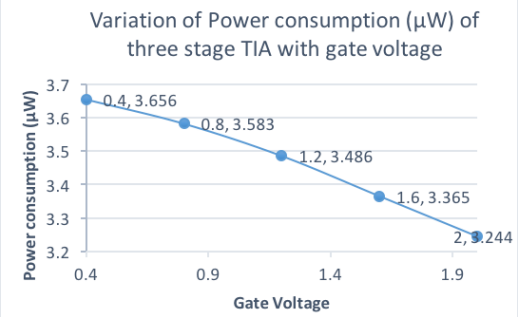

Figure 17

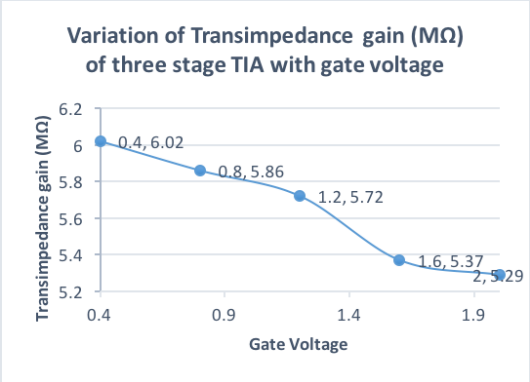

Figure 18

Table 5 shows the voltage output, Consumption power, transimpedance gain level change with changing in the width of NMOS transistor [0.5 – 3.0] µm for three stage Transimpedance amplifier [Figure 4]. The Output voltage change from [3.20 –2.58] V with the variation in the width of NMOS transistor from [0.5 – 3.0] µm as shown in figure 20. Also Power consumption change from [2.952–3.607] µW with the changing in the width of NMOS transistor from [0.5 – 3.0] µm as shown in figure 19. Transimpedance Gain change from [6.54 – 5.25] MΩ with the changing in the width of NMOS transistor from [0.5 – 3.0] µm as shown in figure 21.

Table 5: changing of power and transimpedance gain with width of NMOS

Width Wn (µm)	Power consumption (µW)	Output voltage (V)	Transimpedanece gain (MΩ)
0.5	2.952	3.20	6.54
1.0	2.996	3.12	6.23
1.5	3.301	2.87	5.86
2.0	3.476	2.75	5.49
2.5	3.553	2.63	5.30
3.0	3.607	2.58	5.25

Width Wn (µm) Power consumption (µW) Output voltage (V) Transimpedanece gain (MΩ)

0.5 2.952 3.20 6.54

1.0 2.996 3.12 6.23

1.5 3.301 2.87 5.86

2.0 3.476 2.75 5.49

2.5 3.553 2.63 5.30

3.0 3.607 2.58 5.25

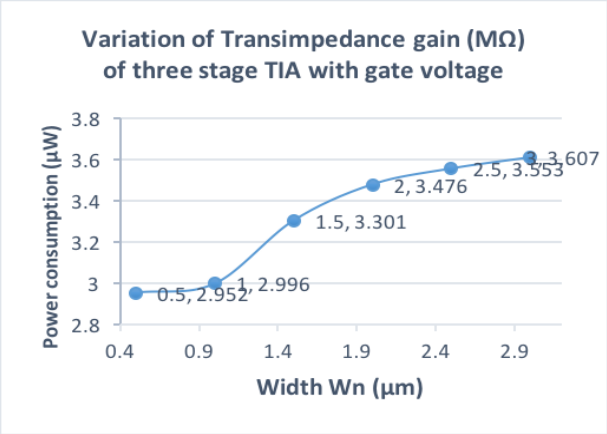

Figure 19

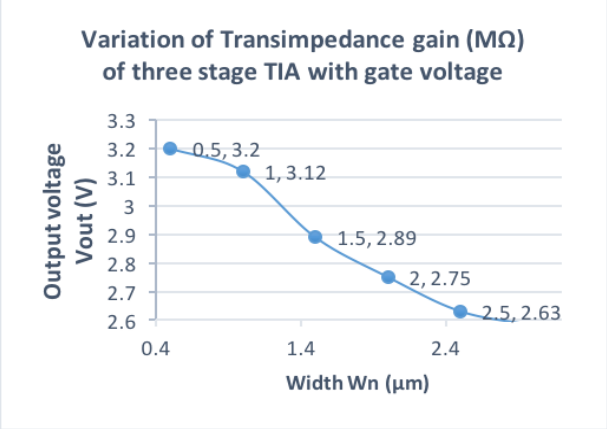

Figure 20

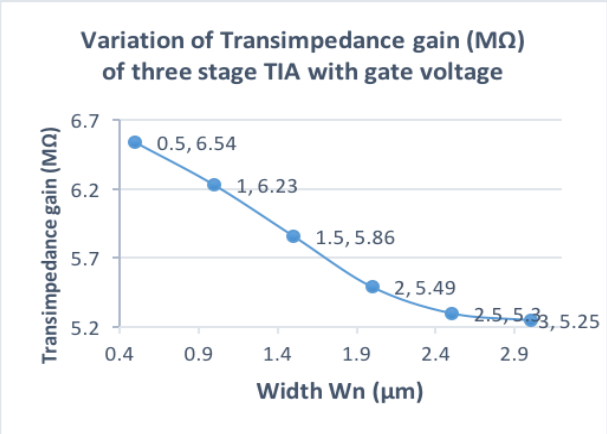

Figure 21

Table 6 shows voltage output change from [2,62 –3.01] V with the changing in the width of PMOS transistor from [1.0 – 3.0] µm as shown in figure 22. Also the transimpedance level gain change from [5.27– 6.05] MΩ with the changing in the width of PMOS transistor from [1.0 – 3.0] µm as shown in figure 23. Power

consumption change from [1.381 – 1.632] µW with the changing in the width of PMOS transistor from [1.0 – 3.0]µm as in figure 24.

Table 6: changing of power and transimpedance gain with width of PMOS

Width Wn (µm)	Power consumption (µW)	Output voltage (V)	Transimpedanece gain (MΩ)
0.5	2.952	3.20	6.54
1.0	2.996	3.12	6.23
1.5	3.301	2.87	5.86
2.0	3.476	2.75	5.49
2.5	3.553	2.63	5.30
3.0	3.607	2.58	5.25

Width Wp (µm)	Power consumption (µW)	Output voltage (V)	Transimpedanece gain (MΩ)
1.0	1.381	2.62	5.27
1.4	1.423	2.69	5.38
1.8	1.465	2.76	5.51
2.2	1.506	2.84	5.67
2.6	1.569	2.95	5.89
3.0	1.632	3.01	6.05

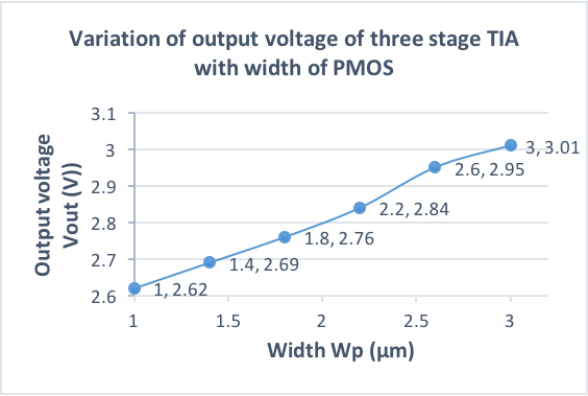

Figure 22

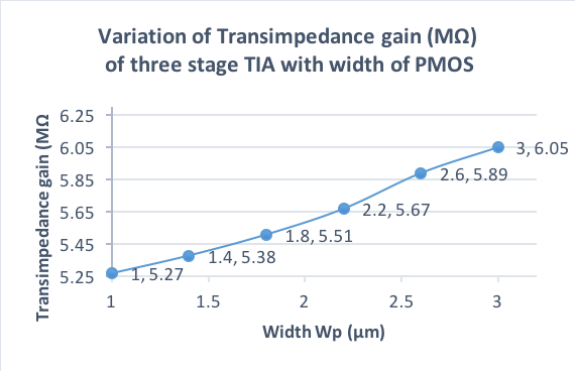

Figure 23

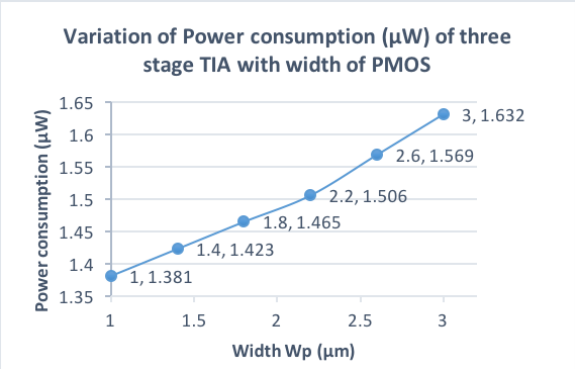

Figure 24

4. Conclusion

To conclude what we have provided, We can recommend a component of the transimpedance amplifier circuit that offers good performance in the parameter such as the total power consumption and output Electric voltage and gain transimpedance The different simulation results provided by Pspice tools, Indicates that the proposed amplifier with the NMOS transistor displays a good active feedback resistor performance optimization in terms of gain transimpedance, output voltage and power consumption. The best working ability in the microampere range is the Transimpedance amplifier CE and finally simulation shows the result that the transimpedance amplifier provides gain transimpedance in different range.

References

[1] C. R. Calvo, "unrestricted CCalvo," wpi, May 2003. [Online]. Available: https://web.wpi.edu/Pubs/ETD/Available/etd-0424103-110517/unrestricted/CCalvo.pdf.

[2] AR_rfmicrowave, "us," arworld, 2018. [Online]. Available: https://www.arworld.us/html/00000.asp?gclid=CjwKCAiAz7TfBRAKEiwAz8fKOMcK3vEnLaRqsswqvS7WjONnoceiqOxpLv8iX2s5Ydlut5c-PCnvSBoCTDoQAvD_BwE.

[3] J. HEATH, "faq converting current to voltage the role of transimpedance amplifiers," analogictips, 4 Nov 2016. [Online]. Available: https://www.analogictips.com/faq-converting-current-to-voltage-the-role-of-transimpedance-amplifiers/.

[4] P. P. DASH, "download pdf," core, 2013. [Online]. Available: https://core.ac.uk/download/pdf/18406344.pdf.

[5] V. E. Paul, "webclient StreamGate," mcgill, Sep 2017. [Online]. Available: http://digitool.library.mcgill.ca/webclient/StreamGate?folder_id=0&dvs=1542289514547~80.

[6] Youran Tijtgat, Niels Rossey, "fulltxt," ugent, 2014. [Online]. Available: https://lib.ugent.be/fulltxt/RUG01/002/153/724/RUG01-002153724_2014_0001_AC.pdf.

[7] R. K. PALANI, "bitstream handle Palan umn pdf," umn, June 2015. [Online]. Available: https://conservancy.umn.edu/bitstream/handle/11299/190512/Palani_umn_0130E_16148.pdf?sequence=1.

[8] D. Groeneveld, "thesis D Groeneveld," utwente, Sep 2010. [Online]. Available: https://essay.utwente.nl/59736/1/MA_thesis_D_Groeneveld.pdf.

[9] K. Das, "unsworks," unsw, Sep 2013. [Online]. Available: http://unsworks.unsw.edu.au/fapi/datastream/unsworks:11588/SOURCE01?view=true.

[10] Azez, Baker, "Team2 Slides," courses, 12 Nov 2015. [Online]. Available: http://mgh-courses.ece.gatech.edu/ece3400/F15/Exam/Team2_Slides_ECE3400_F15.pdf.

[11] A. Manasreh, "The Differential Transimpedance Amplifier Design based," International Journal of Applied Engineering Research , vol. 12, no. 0973-4562, pp. 14095-14100 , 2017.

[12] K. LaFevre, "LaFevre asu," repository, July 2011. [Online]. Available: https://repository.asu.edu/attachments/56952/content/LaFevre_asu_0010N_10920.pdf.

[13] Jacob P. Petersen, S. Alex Kandel, "doi," scitation, 31 Dec 2017. [Online]. Available: https://avs.scitation.org/doi/am-pdf/10.1116/1.4981017.

[14] S. Franco, "In defense of the current feedback amplifier," edn, 23 Aug 2017. [Online]. Available: https://www.edn.com/design/analog/4458753/In-defense-of-the-current-feedback-amplifier.