On the Mitigation of Single Event Transients on Flash-based FPGAs

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***Abstract*—Thanks to the immunity against Single Event Upsets in configuration memory, Flash-based FPGA is becoming widely adopted in mission- and safety-critical applications, such as in aerospace field. However, the decreasing of device feature size leads to an increasing of the device sensitivity regarding Single Event Transients (SETs). In this paper, we developed a new workflow to evaluate SET phenomena in a specific convergence case and introduce a new mitigation of SET pulse without introducing any performance penalization to the original netlist.**

***Key words*—Flash-based FPGAs, Convergence Single Event Transient, SET mitigation.**

I. Introduction

When Flash-based FPGAs are used in mission-critical application, dependability of these devices is one of the major constraints. In harsh environments, such as the one of aerospace applications, radiation is an important factor to consider regarding system reliability. Due to charge deposition of particles inside the device, a voltage glitch known as Single Event Transient(SET) is generated. The induced SET may reach to the output of the circuit, provoking misbehavior of the circuit [1]. Several studies have been dedicated to analysis of SET focusing on electrical modeling which did not take into account the Pulse Induced Propagation Broadening (PIPB) effect [2]. Further studies focused on the radiation test experiment and electrical fault injection for generation and propagation of SET on custom circuits designed specifically to observe SET [4].

For SET mitigation, there are already several mitigation solutions existing. The first kind of methods is based on the classical fault-tolerance approach such as Triple Modular Redundancy (TMR) using redundant modules [5][5]. However, methods based on redundancy usually involve high resources overhead and/or performance degradation etc.. Solutions based on SET filtering schema can lead to tighter time and resources constraints [3] while those based on modification of physical layout require fine granularity control over the resources.

The present work covers two main innovative concepts. First one is devoted analysis of the convergence SET phenomenon which happens due to overlapping of SET pulses, while the second is a new SET mitigation solution based on charge sharing gate insertion into the circuit netlist.

The paper has the following organization: Section II describes SET phenomenon, propagation and convergence of SET. Section III introduces the methodology for mitigation of SET. Section IV presents experimental results. Finally, conclusion is discussed in Section V.

II. Single Event Transient

When a highly charged particle crosses the silicon junction, it releases the energy in one of the transistor sensitive nodes which can cause a glitch of the voltage level at the output of the transistor, i.e. SET, as examples in Fig. 1. When SET pulses traverse the logics and routing resources, the pules undergo severe pulse width modulation which is knows as Propagation Induced Pulse Broadening (PIPB). The PIPB coefficient is typically associated to a gate and it reports the ration between the output pulse width and the input pulse width: if the PIPB coefficient is greater than 1 ns, the SET pulse is broadened otherwise (partially) filtered.

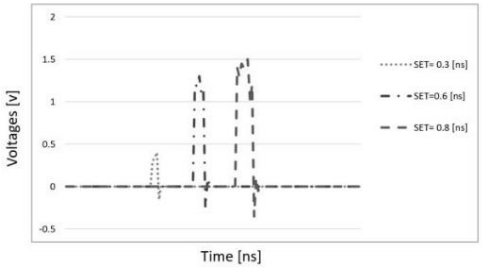

Figure 1. Examples of transient pulses.

A. Single Event Transient propagation

When SET pulse reaches to a divergence node, it propagates through several logic paths in the output cone as in illustrated Fig. 2 using part of a full adder as example. Once the propagated pulses reach to the convergence logic cell, the pulses may unit together and create a new phenomenon named as Convergence-SET (C-SET).

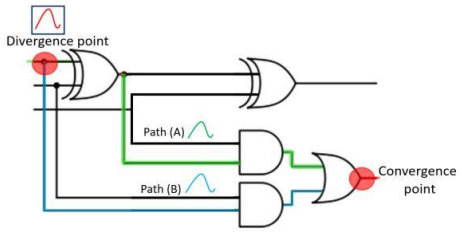

Figure 2. Logical Scheme of full adder affected by SET in the divergence point reaching to the convergence point.

III. Developed Methodology

This work is dedicated to analyzing the SET phenomena, in

particular the C-SET, and introducing an effective methodology to mitigate SET pulses. The developed environment includes three group of tools: Physical Design Description Annotated (PDDA), C-SET Analyzer (C-SETA) and charge sharing based mitigation tool, with the flow as illustrated in Fig. 3.

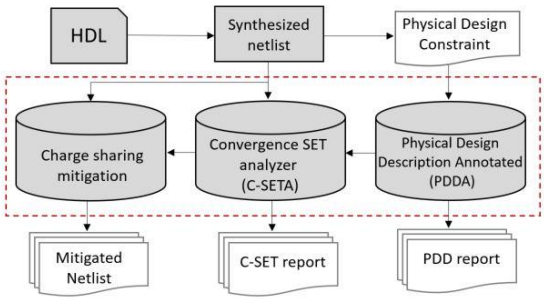

Figure 3. Overall view of the developed flow including analysis and charge-sharing mitigation.

A. *Convergence-SET Analyzer*

In order to elaborate the design architecture, a commercial tool is used to generate synthesized netlist from the HDL source file and extracting the Physical Design Constraints (PDCs). Based on the generated netlist and SDF timing file, we extracted the PDDA file containing the delay information of the routing and logics. The developed C-SETA tool then extracts all the path of the design under study in order to identify the possible occurrences of C-SET in the netlist. As a result, all the design paths starting from the same divergence node and reaching to the same convergence node, i.e. where the C-SET may happen, are extracted, classified and finally reported by C-SETA tool.

B. *Charge-Sharing Mitigation Algorithm*

The developed mitigation algorithm is based on the concept of charge-sharing phenomenon on Flash-based FPGAs which is due to the higher packing density, reduced nodal charge and space between device resources. The proximity of device nodes results in different charge collections in multiple logic switches when a single heavy ion strikes a node. This phenomenon results in different transient pulse shapes related to LET absorbed by the switch junction. The proposed mitigation solution is based on placement modification of the circuit by inserting programmed logic gates in ad-hoc netlist nodes.

To mitigate, the tool selects suitable nodes for the logic charge sharing insertion based on the performed SET analysis, calculating the PIPB coefficients w.r.t. the original netlist and estimating the expected number of charge sharing gates for each node. The netlist of the design is then modified by inserting proper numbers of logic gates to the selected locations.

IV. Experimental Results

The proposed flow has been experimentally evaluated by means of SET analysis and electrical injection using an A3P250 Flash-based FPGA manufactured by Microsemi. We select four circuits from ITC99 benchmark collection [6] and we performed the analysis considering SETs of three different widths: 0.3, 0.6 and 0.8 ns.

The results are reported in Table I, which presents the number of Flip-Flops affected by the SETs whose width is lower than 1ns: *Logic Masked*, *Filtered* indicates the FF is not affected by the SETs as they are masked or filtered respectively, during propagation; *Partially Filtered and Broadened* indicate the FF is affected by partially filtered or broadened SETs. The percentage of C-SET observed is also reported.

TABLE I
Comprehensive FF SET Sensitivity using The Static Analysis Tool

Circuit	SET width lower than 1 ns				
	Logical Masked [#]	Filtered [#]	Partially Filtered [#]	Broadened [#]	C-SET unfiltered [%]
B05	46	9	3	8	9
B09	47	3	6	11	18
B12	102	1	7	13	8
B13	21	14	8	7	38

Four circuits selected above have been mitigated using the proposed approach. Electrical pulse injection platform has been used to inject SETs in random sensitive nodes of the circuits. In total 5,000 SETs lower than 1 ns for each circuit were injected and results are reported in Table II where it shows the percentage of wrong answers.

TABLE II
SET Fault Injection Wrong Answers Comparison

Circuit	Wrong Answers [%]	
	Original	Proposed Method
B05	68.5	4.3
B09	72.6	2.6
B12	83.2	3.1
B13	54.8	4.1

V. Conclusions and Future Works

In this paper, we introduced the C-SET phenomenon and proposed a new mitigation solution for Single Event Transient affecting Flash-based FPGAs capable to reduce the sensitivity against SET. The developed solution has been validated by electrical fault injection of SET into four different circuits, which shows reduction of more than 10 times sensitivity comparing to original circuit implementation.

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