Controlled data storage for non-volatile memory cells embedded in nano magnetic logic

Controlled data storage for non-volatile memory cells embedded in nano magnetic logic

Fabrizio Riente, Grazvydas Ziemys, Clemens Mattersdorfer, Silke Boche, Giovanna Turvani, Wolfgang Raberg, Sebastian Luber, and Stephan Breitkreutz-v. Gamm

Citation: AIP Advances **7**, 055910 (2017); doi: 10.1063/1.4973801

View online: http://dx.doi.org/10.1063/1.4973801

View Table of Contents: http://aip.scitation.org/toc/adv/7/5

Published by the American Institute of Physics

Controlled data storage for non-volatile memory cells embedded in nano magnetic logic

Fabrizio Riente,[1,a] Grazvydas Ziemys,[1] Clemens Mattersdorfer,[1] Silke Boche,[1] Giovanna Turvani,[1] Wolfgang Raberg,[2] Sebastian Luber,[2] and Stephan Breitkreutz-v. Gamm[1]

[1]*Institute for Technical Electronics, Technical University of Munich, Munich 80333, Germany*
[2]*Infineon Technologies AG, Sense & Control, Am Campeon 1-12, Neubiberg 85579, Germany*

(Presented 3 November 2016; received 23 September 2016; accepted 23 October 2016; published online 5 January 2017)

Among the beyond-CMOS technologies, perpendicular Nano Magnetic Logic (pNML) is a promising candidate due to its low power consumption, its non-volatility and its monolithic 3D integrability, which makes it possible to integrate memory and logic into the same device by exploiting the interaction of bi-stable nanomagnets with perpendicular magnetic anisotropy. Logic computation and signal synchronization are achieved by focus ion beam irradiation and by pinning domain walls in magnetic notches. However, in realistic circuits, the information storage and their read-out are crucial issues, often ignored in the exploration of beyond-CMOS devices. In this paper we address these issues by experimentally demonstrating a pNML memory element, whose read and write operations can be controlled by two independent pulsed currents. Our results prove the correct behavior of the proposed structure that enables high density memory embedded in the logic plane of 3D-integrated pNML circuits. [http://dx.doi.org/10.1063/1.4973801]

I. INTRODUCTION

Nano Magnetic Logic is an innovative technology, currently under investigation by the research community as a possible alternative to traditional CMOS devices. Among its different implementations, perpendicular Nano Magnetic Logic (pNML) seems to be the most effective.[1,2] In pNML, elementary devices are characterized by a perpendicular magnetic anisotropy (PMA) obtained with a Co/Pt multilayered structure.[3] Binary information is propagated through pNML circuits by applying a global external magnetic field that is perpendicular to the structure's plane.[4] Fig. 1.A depicts the pNML elementary cells able to store binary information into two stable magnetization states. In Fig. 1.C, a pNML nanomagnet and its artificial nucleation centers (ANCs) are shown. Indeed, the univocal propagation direction is guaranteed thanks to defined ANCs, where the anisotropy is lowered. Those ANCs are obtained by a partial Focused Ion Beam (FIB) irradiation on a specific spot of the magnet, enabling the control of the switching process.[5,6] In this technology, logic computation and signal routing are achieved by controlling the domain wall (DW) nucleation and their subsequent motion.

pNML technology is characterized by a very low power consumption and by the capability of storing non-volatile logic information.

Another interesting characteristic resides in its intrinsic capability of combining logic and memory onto the same device. Thanks to the ferromagnetic properties of the material, the magnetic information is retained even without supplied energy. Moreover, 3D devices can be monolithically

[a]Electronic mail: fabrizio.riente@polito.it

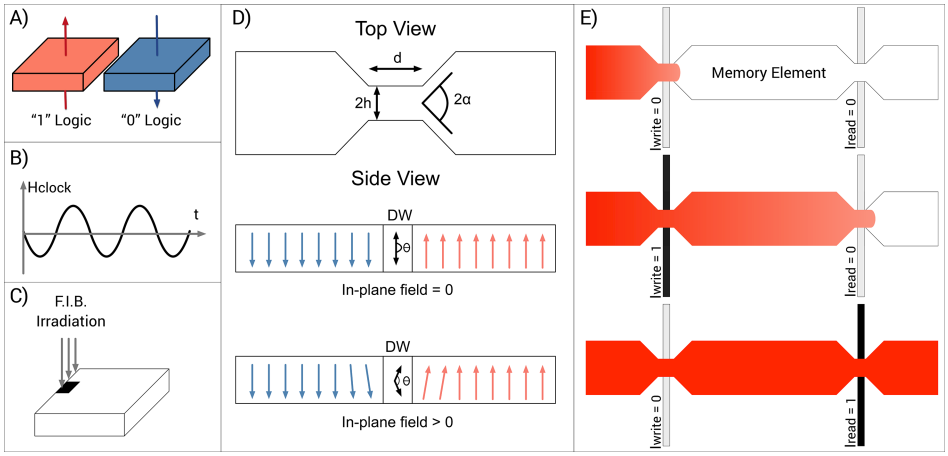

FIG. 1. A) pNML elementary cells; B) Perpendicular out-of-plane clocking field; C) Definition of the ANC by FIB irradiation; D) Schematic representation of a notch with its main parameters (up) and side view of the notch (down) showing the magnetic moment before and after the in-plane field is applied; E) Proposed memory element where the write and read out process can be controlled by short current pulses.

integrated as demonstrated in.[7,8] This characteristic makes it possible to design magnetic circuits exploiting the novel Logic-in-Memory (LIM) concept.[9,10] Indeed, monolithic 3D integrated majority gates have been experimentally demonstrated to execute NAND or NOR operations depending on the value of one programmable input.[11]

However, in order to build realistic circuits, a control unit should be able to control the information storage and its read-out process by means of specific signals. This characteristic is often ignored when exploring beyond-CMOS devices.

In pNML technology, signal propagation and synchronization can be controlled by pinning DWs in magnetic notches, or depinning them by means of a tuned in-plane field.[12,13]

A notch is a geometrical deformation of the magnetic wire able to induce the energy barrier to pin propagating DW. Without supplied external fields, the nucleated DW tries to minimize its energy barrier settling down in the notch.[14] The Zeeman energy supplied by an external out-of-plane field can provide the energy required to overcome the notch barrier[15] and is expressed as:

$$E_{Zeeman} = -\mu_0 \int_V \vec{M}\vec{H_{ext}} dV = -\mu_0 M_s H_{clock} A_{dw} t_{layer}, \tag{1}$$

where M_s is the saturation magnetization, H_{clock} the applied out-of-plane field, A_{dw} the area of the DW in the magnetic film and t_{layer} its thickness. The energy associated to the DW that has to be minimized is equal to:

$$E_{dw} = \sigma_{dw} t_{layer} l_{dw}, \tag{2}$$

where σ_{dw} is the DW energy density and l_w its length. The energy density for a 180° Bloch wall in thin films is equal to $\sigma_{dw} = \pi\sqrt{2}\sqrt{A_{ex}/K_{eff}}$, with exchange stiffness A_{ex} and effective anisotropy K_{eff}. Therefore, the DW tries to expand its area while reducing its length resulting in a bent DW at the notch. The field required to depin such DW comes from the competition between the Zeeman and the DW energy. As reported in,[14] the depinning field B_{dep} can be computed as:

$$B_{dep} = B_{int} + \frac{\sigma_{dw} sin(\alpha)}{2M_s(h + \frac{1}{2}\sigma_{dw} sin(\alpha)}, \tag{3}$$

where α represents the notch apex angle, h its width and B_{int} is the intrinsic field for DW propagation at 0K. However, the DW energy barrier does not depend only on the DW type, but also on the DW angle according to:

$$\sigma_{dw,\theta}(\widetilde{\theta}) = \sigma_{dw,180^\circ} sin^2\left(\frac{\widetilde{\theta}}{2}\right). \tag{4}$$

As depicted in Fig. 1.D, $\sigma_{dw,180^\circ}$ represents the 180° DW energy and θ the DW angle. In-plane magnetic fields lower the energy barrier of the DW by tilting the $\widetilde{\theta}$ angle.

In this paper, we propose a magnetic memory cell where the write and read operations can be controlled by two current pulses. Notches are created within the magnetic wire to store information permanently. To have a working pNML memory element, it is important that the nucleation field (B_{nuc}) is lower than the depinning field (B_{dep}). If this condition is not satisfied, the nucleated DW will flow towards the output of the magnetic wire without pinning at the notch. The depinning of the stuck DW should be controlled by applying in-plane field pulses. The out-of-plane global clock field alone should not influence the DW depinning, but should only guarantee the correct information propagation. The depinning field of notches should be higher than the nucleation field in order to block every propagating DW.

By using local in-plane field pulses, it is possible to depin the blocked DW by lowering the notch energy barrier. This process restores the propagation of the stored information. Fig. 1.E shows a schematic representation of the fabricated memory cell. Here, two notches have been cascaded within the same magnetic wire. The current flowing through buried wires should generate the field required to depin the stuck DW. Wires are placed perpendicularly under the notches in order to enable the depininng of information, maximizing the in-plane field component. Indeed, in normal operating mode, the propagating DW is blocked were notches are placed. The current I_{write} flowing through the first wire generates an in-plane magnetic field which unblocks the stuck DW. The information is then blocked on the second notch, completing the actual write operation. Afterwards, to enable the DW depinning, the same approach is exploited. I_{read} generates the second in-plane field that read out the stored information, restoring the propagation of the stuck DW. The use of these memory elements makes it possible to design architectures where logic and memory are integrated within the same device. In particular, it is possible to build 3D structures in which memories, logic circuits and interconnections are separated into different layers, implementing the so-called LIM concept.[9,10] With this approach, it is possible to remarkably improve both circuit performance and circuit compactness. In the next sections we report the measurements of the fabricated memory element depicted in Fig. 1.E, with Wide-field-MOKE (WMOKE) images that show the correct behavior of the proposed device.

II. EXPERIMENT

A. Sample preparation

In this section, we experimentally demonstrate the pNML memory element where the read and write operations can be controlled by using two pulsed signals, I_{read} and I_{write}. We show that the propagating DWs are pinned in the first notch. The storage process can be controlled by depinning the stuck DWs by a pulsed I_{write} current. At this point, the unblocked DWs propagate until they reach the second notch. Here, the information propagation stops again. The memory element is represented by the magnetic material between the two notches. The read out operation can be obtained by applying a short I_{read} pulse.We started from a Si wafer where a big coil and two current wires have been previously fabricated (Fig. 2.A). The magnetic structures are obtained by RF magnetron sputtering of an ultra-thin film of $Ta_{1.7nm}Pt_{2.8nm}[Co_{0.85nm}Pt_{1.4nm}]_{x2}Pt_{2.8nm}$, getting a $K_{eff} = 1.16 \cdot 10^5 J/m$.[3] Co was sputtered at 4 μbar, whereas the adhesion layer (Ta) and Co were sputtered at 2 μbar. The Pt enforces the < 111 > texture direction. The multilayer stack sputtered on the substrate has been patterned using FIB-lithography after spin coating PMMA resist. The resist is exposed to gallium $(Ga)^+$ ions with a computer-pattern mask. The ANCs of the magnetic structures are defined during the lithography by Ga^+ FIB radiation with a dose of $2.5 \cdot 10^{13}$ ions/cm^2. The area of the irradiated spot is 40 x 40 nm_2. The resist is developed for 18s before evaporating a thin layer of Ti (5nm). The Ti is evaporated via electron beam physical vapor deposition. It serves as hard mask for the lift-off process. The remaining resist is lifted off by immersing the sample in a heated N-Methyl-2-pyrrolidone ultrasonic bath. At this point, only the structures defined by FIB lithography are still covered by the Ti hard mask. The magnets are then structured by Ion Beam Etching. Here, Ar^+ ions accelerated by an electric field remove the unwanted material. The SEM image of the fabricated and measured magnetic device is reported in Fig. 2.B. Here, the nanowire width is about 300 nm and the notch width about 20 nm.

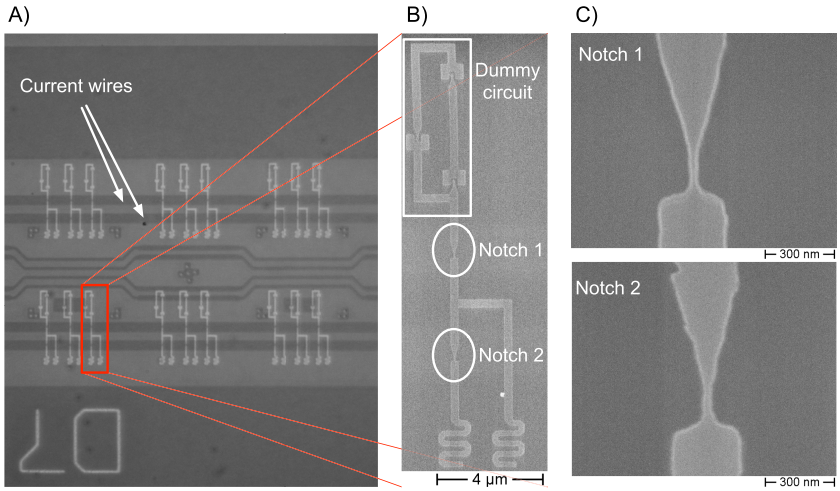

FIG. 2. A) Optical micrograph of the sample; B) Close-up view (SEM image) of the fabricated magnetic memory cell; C) SEM images of both notches.

B. Measurement setup

The measurement setup is composed of a WMOKE microscope with a 2-channel programmable nanopulser connected to a special chip carrier for current pulses (read/write). In addition, an external magnet for out-of-plane field pulses (i.e. the clocking field) is used. Once the sample is bonded to the chip carrier, it is possible to apply in-plane field pulses in the ns-range by using the 2 available channels.

C. Results

The first measurements that we conducted were related to the nucleation field and the depinning field of both notches. The average nucleation field of the fabricated dummy circuit reported in Fig. 3.B is 42.5mT. We observed the depinning from both notches by applying an average out-of-plane field of 57.4mT. We carried out the measurements of the proposed memory cell by applying a fixed out-of-plane field and by pulsing the I_{write} or the I_{read} according to the operation to be performed. We applied a clocking field of 54.5mT for 30ms, which guarantee the nucleation and the complete reversal of the dummy circuit (Fig. 3.B). At this point, the propagating DW is pinned at the first notch,

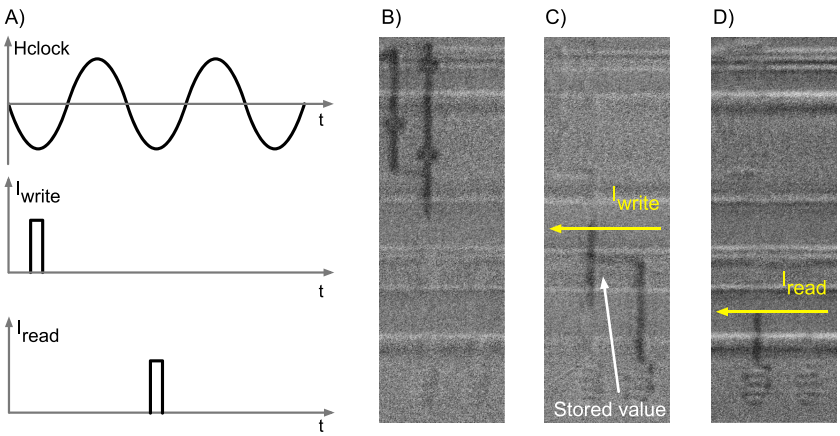

FIG. 3. A) Timing diagram of the applied signals; B)WMOKE image of nucleated and pinned DW at the notch; C) WMOKE image of the depinned DW from the first notch after write operation; D) WMOKE image of the depinned DW from the second notch after the read operation.

as depicted in the difference image taken with the WMOKE. The storage operation is obtained by pulsing I_{write} for 30ns. The estimated in-plane field generated by the I_{write} at the first notch is 18mT ±5.18mT. This field is enough to unblock the stuck DW that is pinned again on the second notch. Fig. 3.C shows the WMOKE image of the stored information in the memory cell, obtained as a difference image with Fig. 3.B. In a similar way, the read-out process can by performed by pulsing the I_{read} current. After applying a 30ns current pulse we observed the depinning of the stored information (Fig. 3.D). In this case the estimated in-plane field required at the second notch is in average 11.3mT ±3.83mT. We successful performed the write and read-out process with both logic 0 and 1 several times proving the concept of embedding the memory plane in pNML LIM architecture.

III. CONCLUSIONS

In this paper we have experimentally demonstrated the proposed magnetic pNML memory cell. The results prove that is possible to control the read and write operations by means of two independent current pulses within the clocked pNML circuit. These pulses, in the ns-range, retain or release the stored magnetic information which could be also located in separate layers to fulfil the LIM concept. This magnetic memory cell takes a step forward in the research of Nano Magnetic Logic devices.

[1] D. E. Nikonov and I. A. Young, "Benchmarking of beyond-cmos exploratory devices for logic integrated circuits," IEEE Journal on Exploratory Solid-State Computational Devices and Circuits **1**, 3–11 (2015).
[2] Semiconductor Industry Association, The International Technology Roadmap of Semiconductors: Emerging Research Devices (ERD), 2013.
[3] S. Breitkreutz, J. Kiermaier, S. Vijay Karthik, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Controlled reversal of co/pt dots for nanomagnetic logic applications," Journal of Applied Physics **111** (2012).
[4] F. Cairo, G. Turvani, F. Riente, M. Vacca, S. B. v. Gamm, M. Becherer, M. Graziano, and M. Zamboni, "Out-of-plane nml modeling and architectural exploration," in *Nanotechnology (IEEE-NANO), 2015 IEEE 15th International Conference on* (2015), pp. 1037–1040.
[5] S. Breitkreutz, J. Kiermaier, X. Ju, G. Csaba, D. Schmitt-Landsiedel, and M. Becherer, "Nanomagnetic logic: Demonstration of directed signal flow for field-coupled computing devices," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)* (2011), pp. 323–326.
[6] M. Becherer, G. Csaba, W. Porod, R. Emling, P. Lugli, and D. Schmitt-Landsiedel, "Magnetic ordering of focused-ion-beam structured cobalt-platinum dots for field-coupled computing," IEEE Transactions on Nanotechnology **7**, 316–320 (2008).
[7] M. Becherer, S.Breitkreutz-v. Gamm, I. Eichwald, G. Ziemys, J. Kiermaier, G. Csaba, and D. Schmitt-Landsiedel, "A monolithic 3d integrated nanomagnetic co-processing unit," Solid-State Electronics **115**, 74–80 (2016).
[8] S. Breitkreutz-v. Gamm, G. Ziemys, I. Eichwald, G. Csaba, W. Porod, M. Graziano, D. Schmitt-Landsiedel, and M. Becherer, "Towards signal routing in 3d-integrated magnetic logic circuits," in 13th Joint MMM Intermag Conference, San Diego, CA, USA (2016).
[9] D. Pala, G. Causapruno, M. Vacca, F. Riente, G. Turvani, M. Graziano, and M. Zamboni, "Logic-in-memory architecture made real," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)* (2015), pp. 1542–1545.
[10] M. Cofano, G. Santoro, M. Vacca, D. Pala, G. Causapruno, F. Cairo, F. Riente, G. Turvani, M. R. Roch, M. Graziano, and M. Zamboni, "Logic-in-memory: A nano magnet logic implementation," in *2015 IEEE Computer Society Annual Symposium on VLSI* (2015), pp. 286–291.
[11] I. Eichwald, S. Breitkreutz, G. Ziemys, G. Csaba, W. Porod, and M. Becherer, "Majority logic gate for 3d magnetic computing," Nanotechnology **25**, 335202 (2014).
[12] R. Fabrizio, Z. Grazvydas, G. Turvani, M. Graziano, D. Schmitt-Landsiedel, and S.Breitkreutz-v. Gamm, "Towards logic-in-memory circuits using 3d-integrated nanomagnetic logic," IEEE International Conference on Rebooting Computing, San Diego, CA, USA (in press).
[13] J. J. W. Goertz, G. Ziemys, I. Eichwald, M. Becherer, H. J. M. Swagten, and S.Breitkreutz-v. Gamm, "Domain wall depinning from notches using combined in- and out-of-plane magnetic fields," AIP Advances **6**, 056407 (2016).
[14] K.-J. Kim and S.-B. Choe, "Analytic theory of wall configuration and depinning mechanism in magnetic nanostructure with perpendicular magnetic anisotropy," Journal of Magnetism and Magnetic Materials **321**, 2197–2199 (2009).
[15] R. O'Handley, *Modern Magnetic Materials: Principles and Applications* (Wiley, 1999).