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Accurate Analysis of SET effects on Flash-based FPGA System-on-a-Chip for Satellite Applications

S. Azimi, B. Du, L. Sterpone

Abstract— **In this paper, we propose a methodology for executing simulation using analytical models for the execution of SET propagation on System-on-a-Chip implemented on Flash-based FPGAs. Analysis performed on EUCLID-based circuit design demonstrated its effectiveness.**

I. INTRODUCTION

Nowadays, space satellites embed hundreds of Systems-on-a-Chip which dispatches various functionalities ranging from avionic controls and on-board communications to data elaboration and image analysis. Due to their flexibility and performances, as reported by the European Space Agency (ESA) technology roadmap [1], Field Programmable Gate Arrays devices are progressively adopted in geostationary orbit (GEO) and interplanetary spaceships with an exponential request of area size and device complexity.

Among the various available FPGA technologies, FPGAs with Flash-based configuration cells are particularly suitable for these applications since they are almost immune to permanent loss of the configuration data. However, these devices are composed of floating gate switches that can suffer transient effects, also called Single Event Transient (SET) [2].

This phenomenon has been investigated in various research works, demonstrating that the SET pulse-width is modulated and modified when it traverses different types of logic gates and routing switches. The accurate modeling of the SET propagation would have several fundamental benefits on two sides: the former is the evaluation of the radiation-induced SET sensitivity and the latter is the effective application of mitigation techniques. In previous work, the Single Event Transient (SET) sensitivity of the FPGA fabric was investigated also including Flip-Flops (FFs) and the large static RAM memory blocks. The characterization was done at various frequencies (ranging from 1 to 10 MHz) providing different probabilities of capturing SET within the combinational gates [3]. Several specific benchmarks were investigated under radiation test campaigns, while the unique SoC evaluated until now consists on an ARM-based Cortex-M3 processor and this was evaluated only with respect to the Single Event Functional Interrupt (SEFI) phenomena. However, previous works did not provide a realistic and effective model of the SET phenomena.

In this paper, an analysis environment has been developed which allows modeling the Single Event Transient source phenomena and analyzing the sensitiveness of complex SoCs. The proposed environment is based on two distinguishable improvements: the former consists in a new SET model that has been analytically described in relation to electrical injection campaigns and that is now able to effectively model the Propagation Induced Pulse Broadening (PIPB) effect; the later consists in an accurate topological analysis of the Flash-based FPGA architecture under test which results in a validated interconnections routing structure.

The proposed developed analysis environment has been applied to a SoC mapped on a MicroSemi ProASIC3 Flash-based FPGAs that is currently under development within the frame work of the Euclid mission oriented to the map of the geometry of the dark Universe [15]. The experimental results provide an effective estimation of the module error cross-section on the basis of the Euclid radiation environment and the overview of the SET phenomena that will affect the circuit on its realistic operational life.

II. RELATED WORKS

Several studies have been done in order to analyze the SET phenomenon [2], the propagation of the transient pulse through the combinational logic data path and routing resources [3] on flash-based FPGA. Previous studies focus on the nature of these events. New insight on flash-based FPGA is investigated in [4]. A new methodology for effectively measuring the width of radiation-induced transient faults has been proposed in [5] [6]. However, they are not effective for a representative example of realistic designs. In these considerations, only the effect related to delay of SET has been investigated without respect to the filtering and broadening effects.

Recent studies reported radiation test experiment and electrical fault injection of SET propagation on custom circuits designed specifically to observe SETs [7].

Previous work of accurate SET pulse electrical injection shows a strong SET pulse-width modulation when SET pulse traverses logic gates [8]. In addition, it has been concluded that the SET pulse width at the input of the storage element is strictly dependent on the propagation and type of traversed logic gates [9]. This SET pulse width is also dependent on the routing structure of the used technology [8]. In [10], an

analytical model for analyzing the sensitivity of SET nonmetric technology has been proposed. This model has been used for the accurate simulation of GPGPUs applications against the occurrence of transient errors. Using this model, it is possible to propagate SET pulse from the affected location to the registers involved in the computation allowing to determine the right influence of SEE in the GPGPU architecture [11].

In this paper, we propose a methodology based on electrical model of the FPGA logic cells and routing resources to estimate PIPB effects. Using the proposed method, it is possible to reproduce the behavior of SETs propagation through the logic and routing resources.

III. THE DEVELOPED ANALYSIS ENVIRONMENT

The aim of this work is to propose an effective model of SET phenomena generated by radiation particles within the silicon structure of the devices in order to investigate the SET propagation behavior with respect to the effects of routing resources.
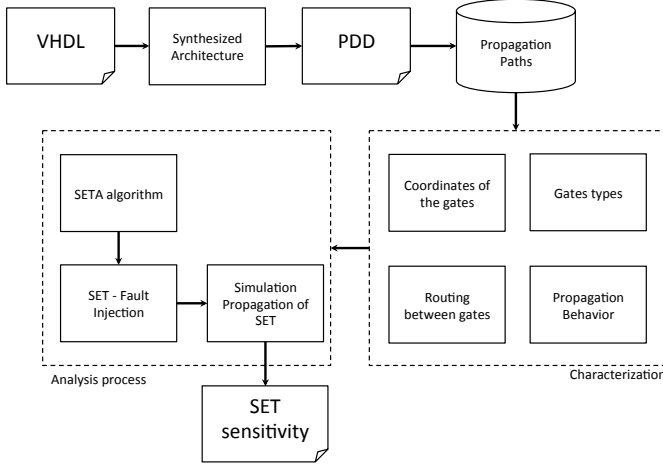

Figure 1. The developed analysis flow for the accurate evaluation of SET effects on SoC implemented on Flash-based FPGAs.

As illustrated in Figure 1, we developed a workflow to analyze the sensitivity of a FPGA design against SET phenomena. This process requires the elaboration of the FPGA architecture. Therefore, for the preliminary phase a commercial tool is used to generate synthesized netlist from the VHDL source files. Using a tool developed by us, we are able to create a Physical Design Description (PDD) file from the netlist. From this PDD file, all the paths in the design, coordinates and types of the gates are extracted. Taking into account the coordinates of the gates and information extracted from the FPGA architecture database (included in the commercial tool by the FPGA vendor), we are able to estimate the routing resources used in the design and assign proper delay to them. In addition, we developed a Matlab model to simulate the SET propagation behavior when it traverses different types of gate.

In order to explore the propagation of SET pulses, the advanced model generates SET pulses for injecting in simulation environment of the design under investigation. At this phase, a Matlab algorithm is applied to perform the SET propagation and analyze a circuit mapped on FPGA. This algorithm locates all the combinational gates as injection points and identifies the nodes along the propagation path until a storage element is reached. Then a SET pulse is generated. Considering routing delay effects and the filtering and broadening effects for each node, the generated SET propagate along the path until input of a storage element. As a result of this algorithm, the profiles reaching at the storage elements are used for assessing the SET sensitivity of the circuit.

A. Logic Model

The main idea behind the proposed work is based on the accurate modeling of the SET phenomena induced by the radiation particles within the silicon structure of the nanometer devices. Since SPICE is not able to simulate broadening effects, Matlab has been used to provide the physical evaluation of this effect. In order to do this, the technology and design information is required such as thickness, area, resistance and capacitance of interconnection and device layers. However, in our developed model, some of these parameters are currently under definition.

For the first step of this model, SET pulse is generated according to the characterization provided in (1) [12].

As the next step, propagation behavior of each logic cell and the routing effects is needed. This issue is elaborated in the next parts.

As a result, by using the propagation behavior of gates and routing delay among functional logics, it is possible to inject the SET pulse at the sensitive nodes and analyze their widths at the input of storage elements if they can ever reach any.

The model consists of three phases: the generation of the SET pulse phenomena which is modeled as a transient pulse shape, the localization of a combinational gate and the execution of the propagation of the SET pulse starting from each sensitive node of the circuit and traversing the logical gates and routing interconnection until an input of a storage element is reached.

In order to generate the pulse shape, the developed model elaborates the physical layout description of each circuit logic gate, described by standard Graphic Database System for IC layout (GDS-I).

$$1. if\,(\tau_n < k\,\tau_p) \rightarrow \tau_{n+1} = 0$$

$$2. if\,(\tau_n > (k+3)t_p) \rightarrow \tau_{n+1} = \tau_n + \Delta t_p$$

$$3. if\,((k+1)\,t_p < \tau_n < (k+3)t_p) \rightarrow \tau_{n+1} = \frac{(\tau_n^2 - r_p^2)}{\tau_n} + \Delta t_p \tag{1}$$

$$4. if\,(kt_p < \tau_n < (k+1)t_p) \rightarrow \tau_{n+1} =$$

$$(k+1)\,t_p(1 - e^{(k-(\tau_n/\tau_p))}) + \Delta t_p$$

B. Routing Model

The developed routing model is based on an accurate calculation of the propagation delay of routing system. Based on this investigation of routing structure, Figure 2, there are four level of hierarchy: extra array long lines (d) which consist

of the longest interconnection, intra array long lines (b) allowing long connections through the whole device, medium lines (a) and short lines (c) for local routing resources. These four levels have been extracted using Actel Libero Software tool. For considering the effect of the routing on the whole circuit, we extracted the coordinate of the logic functions. Using these coordinates, it is possible to know the number and the kind of the segments used between two logic functions. By calculating the propagation delay of routing segments, we are able to assign the propagation delay to the related kind of routing. We reported in Table I the data obtained from the ProASIC3 MicroSemi device family. Considering the routing structure in this family, it is possible to analyze the routing effect on SET propagation on the whole device.
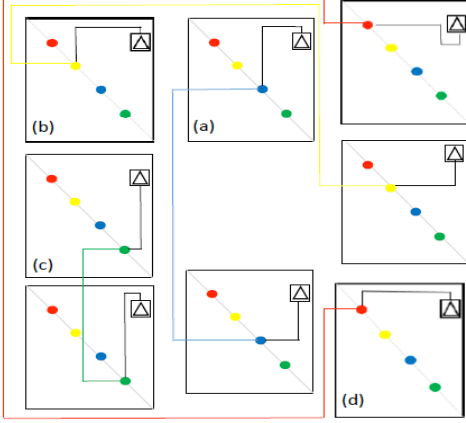

Figure 2. the device routing topology of the Microsemi ProASIC3 family

C. Physical characterization

The purpose of this part is to analyze the SET propagation behavior considering a 1-0-1 transition SET pulse.

It is known that each gate has different SET propagation behavior related to the difference between the propagation delays of t_{pHL} and t_{pLH}, [8]. For investigating the SET behavior, we consider a chain of 5,652 inverters in the experiment. We inject SETs of different durations at the start of the chain and measured the pulse durations at the end of the chain. In Table II we reported the SET injection and the output pulse durations.

TABLE I
ROUTING TOPOLOGY ORGANIZATION ON PROASIC3 DEVICES

Label	Kind	Delay [ns]	Distance [#Block]
(a)	Short	0.8	1
(b)	Medium	1.01	2
(c)	Intra long	1.265	6
(d)	Extra long	1.239	12

As can be seen from results in the table II, the transient pulse broadening effects occur when the SET pulse traverses through the chains. Regarding to the model proposed in [12], for a 0-1-0 transition, the transient pulse broadening at a node is approximately the difference between the propagation delays.

$$\Delta t_p = t_{pLH} - t_{pHL}$$

$$if(t_{SET} > (k+3)t_{pHL}) \rightarrow t_{out} = t_{SET} + \Delta t_p$$

In the proposed model, considering the number of the inverters (n) used in the experimental results, we are able to estimate the behavior of the inverter. Using the injected SET, the SET duration at the output and the number of inverters, t_{pHL} and t_{pLH} can be calculated for each SET pulse.

$$\Delta t_p(total) = n * (t_{pLH} - t_{pHL})$$

$$t_{pHL} < t_{SET}/7$$

Comparing the simulation results and experimental results, by means of t_{pHL} and t_{pLH}, for each SET pulse at the input of the first inverter, we are able to estimate the pulse duration in the output of the 5,652 inverters chain. The comparison between the experimental analysis and the results of the simulation are reported in Table II.

TABLE II
COMPARATIVE ANALYSIS

Input Pulse [ns]	Output Chain Pulse [ns] Experimental Result	Output Chain Pulse [ns] Simulation Result	t_{pLH} [ns]	t_{pHL} [ns]
19.57	26.84	26.93	2.80	2.80
12.35	18.69	18.74	1.77	1.77
8.33	16.70	16.75	1.19	1.19
4.25	12.35	12.39	0.61	0.61
3.34	12.47	12.47	0.47	0.47
2.49	12.59	12.61	0.36	0.36
1.89	12.33	12.34	0.27	0.27
19.57	26.84	26.93	2.80	2.80
12.35	18.69	18.74	1.77	1.77

IV. EXPERIMENTAL RESULTS

The experimental evaluation of the proposed methodology has been performed on a SoC that will be embedded in the Euclid space mission and has been implemented on Microsemi ProASIC3 A3P3000 Flash-based FPGA device [15]. We performed two different analyses: the first is the evaluation of the error cross-section of the SoC divided per module, while cross-section is considering as a calculation of the sensitive area of our testes circuit. The second analysis is a detailed SET estimation. Both the analyses have been performed considering the synthesized netlist.

The SoC design implemented on the ProASIC3 Flash-based FPGA consists on a data elaboration core. The overall resource usage of the entire SoC occupies around the 68% of the overall available logic element.

The SoC resource hierarchical organization is divided into 12 modules implemented on the Flash-based FPGAs. In details, the design embeds two SpaceWire cores [16] surrounded by different processing elements devoted to data sampling and transmission to the Euclid external unit. Please note that the two SpaceWire components (SPW_CTRL_1 and SPW_CTRL_0) are two copies of the same unit; the number of different sequential and combinational is due to the synthesizer simplification. The SoC under test has been evaluated estimating the error cross-section sensitivity. In order to perform this computation, we analyzed the integral

fluency expected for the nominal duration of the mission, which is 6.25 years. For that purpose, the CREME/CREME96 method has been used [17] to obtain the Linear Energy Transfer (LET) spectra for the three levels of activity during the entire Euclid lifetime. In general, in order to compute the upset rate of a circuit from the predicted fluxes, it is necessary to known specific design characteristics, in particular the size of the sensitive volume and the equivalent critical charge.

Thanks to the characterization previously performed in [7] [11], we were able to estimate the normalized SET error-cross section for each single ProASIC3 Versatile and routing segment. The SET normalized cross-section coefficients have been elaborated with the topological architecture extracted by the proposed methodology obtaining an overall SoC transient error cross-section of 1.77E-4. Figure 3 illustrated the transient error cross-section per module. It is necessary to notice that the Control Block module is the most sensitive ones nevertheless it is not the module with the greater number of sequential or combinational element. The explanation of this result is related to the intrinsic complexity of the routing interconnections that significantly contribute to the final transient cross-section count.
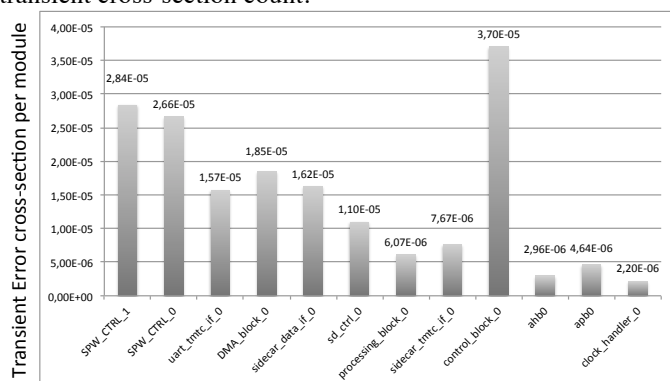

Figure 3. The transient cross-section overview of the Euclid-based ProASIC3 A3P3000 design.

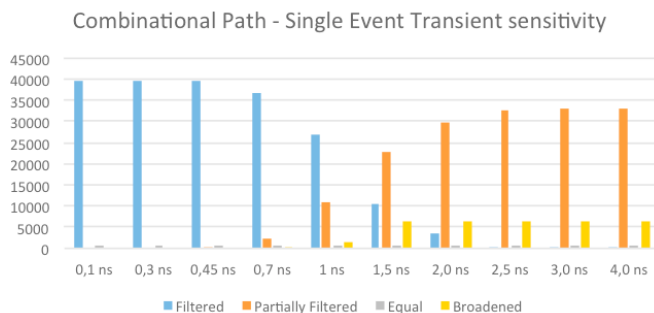The proposed method has been used to individuate the

Figure 4. Combinational Path-Single Event Transient Sensitivity.

effective SET distribution. The obtained results are illustrated in Figure 4, where the propagation of various SETs pulse width are considered on the overall count of the circuit combinational paths. As it is possible to notice all the SETs having width minor or equal than 0.45 ns are completely filtered. This phenomenon is due to the electrical behavior of the 130nm cells which are going to filter signal transitions lower than 0.45 ns. On the other hand, SETs are progressively

not filtered starting from 0.7 ns.

V. CONCLUSIONS AND FUTURE WORKS

In this paper we presented an analysis environment developed to effectively model the Single Event Transient (SET) phenomena and to analyze the sensitiveness of a complex SoCs mapped on Flash-based FPGA. The developed environment has been evaluated on a realistic space-oriented SoC for the Euclid deep-space mission. At first, the obtained results demonstrated that the new developed SET model has been correctly modeled and accurately satisfies data coming from fault injection. Secondly, experimental results demonstrated that our environment integrates different PIPB effects with an effective level of accuracy. As future works, we plan to perform further radiation test experiments to validate our simulation environment.

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