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Politecnico di Torino

Doctoral Thesis

ISPET: Interface Sintering Process Enhanced Technology

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Emilio Mattiuzzo

A thesis submitted for the degree of
Doctor of Philosophy in Electronics and Telecommunication Engineering

XXVIII cycle: 2013-2016

"Hay hombres que de su ciencia
Tienen la cabeza llena;
Hay sabios de todas menas,
Mas digo sin ser muy ducho:
Es mejor que aprender mucho
El aprender cosas buenas"

José Hernández - "Martín Fierro"

POLITECNICO DI TORINO

Abstract

Department of Electronics and Telecommunication

Doctor of Philosophy in Electronics and Telecommunication Engineering

ISPET: Interface Sintering Process Enhanced Technology

by Fernando COSIANSI

The research presented in this thesis was carried out in VISHAY Semiconductor Italiana S.P.A.[1] at Borgaro Torinese - Italy.

The framework of this thesis is the study of new materials for power electronics application, analysing their thermal, mechanical and electrical properties. Emerging application of high power systems requires new methods for power electronics integration and packaging. Stringent requirements in size and weight, reliability, durability, ambient and operation temperatures are pushing to go beyond the limits in industrial applications. As a consequence, our studies are focused on power modules, incorporating new materials and technology processes (sintering) for dies or chips (silicon), substrates and interconnection materials (wire bonding).

This thesis work starts introducing the power semiconductor devices used in power electronics and their integration on Power Integrated Circuits (low and medium power density) and Power Modules (medium, high and very high power density). This chapter will explain technology evolution, power semiconductor device utilization mode and some applications.
Chapter 2 will be focused on power modules packages. They have an important role for providing cooling, electrical connection and correct insulation, between the internal semiconductor devices and the external circuit. Isolated and non isolated packages are analysed and compared.
Chapter 3 will make a point on the methods of thermal characterization and reliability tests, that were implemented to evaluate the impact of the introduction of new materials and processes into the device.
In chapter 4, first experimental results, related to the sintering process will be discussed. In this chapter the attention will be focused on the Chip to substrate Joint of the device, analysing methods to mechanically fix die to substrate. The sintering process will be

[1]For more information http://www.vishay.com/

treated, analysing the process and the results will be thermally and mechanically characterized.

The chapter 5 will present the experimental part oriented to the combinations of materials to produce a better heavy wire bonding, supported by a Design of Experiments (DOE). The behaviour of different wires will be compared through thermal characterization methods and reliability test.

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Firstly, I would like to thank my supervisor Fabrizio Pirri from Politecnico of Torino, for the interest and trust in carrying out this project.

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Because this thesis work is the result of three years in VISHAY Semiconductor Italiana S.P.A., I would like to thank who had a key role in developing this work: Marisa Carlevaro, Adriana Aimone, Oscar Belletti, Sebastiano Ferrero, Alessio Verna, Zina Randazzo, Francesca Mastrouomo, Barbara Bernardini, Sara Martorana, Massimo Dosio, Isabelle Suberbielle, Giancarlo Di Leo, Vito Tambone, Nabil El Baradai, Carmelo Sanfilippo, Enzo Trentin, Marco Nebiolo, Domenico Cavaiuolo, Paolo Mercaldi and a special thanks in memory of Anna Maria Bonardo.
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Abbreviations

AC	**A**lterning **C**urrent
AES	**A**uger **E**lectron **S**pectroscopy
ASP	**A**g **S**inter **P**aste
BJT	**B**ipolar **J**unction **T**ransistor
BLDC	**B**rushless **DC**
BSM	**B**ack**s**ide **M**etallization
C-SAM	**C**-Mode **S**canning **A**coustic **M**icroscopy
CTE	**C**oeficient of **T**hermal **E**xpansion
DBC	**D**irect **B**ond **C**opper
DC	**D**irect **C**urrent
DOE	**D**esign **O**f **E**xperiments
ECM	**E**lectro**c**hemical **M**igration
EDX	**E**nergy-**D**ispersive **X**-ray
EMI	**E**lectro**m**agnetic **I**nterference
EV	**E**lectric **V**ehicles
FA	**F**ailure **A**nalysis
FRED	**F**ast **R**ecovery **E**pitaxial **D**iodes
GTO	**G**ate **T**urn-Off **T**hyristors
HEV	**H**ybrid **E**lectric **V**ehicles
HF	**H**igh **F**requency
HR	**H**umidity **R**elative
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
IOL	**I**ntermittent **O**peration **L**ife
LTJT	**L**ow **T**emperature **T**echnical **J**oint
mAgic	**M**icrobond **Ag** **I**nterconnect

MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PCB	**P**rint **C**ircuit **B**oard
PCT	**P**ower **C**ycling **T**est
PIC	**P**ower **I**ntegrated **C**ircuit
RFI	**R**adio-**f**requency **I**nterference
SCR	**S**ilicon **C**ontrolled **R**ectifier
SEM	**S**canning **E**lectron **M**icroscopy
TCT	**T**emperature **C**ycling **T**est
TRIAC	**T**riode of **A**lternating **C**urrent
TSM	**T**op**s**ide **M**etallization
TTF	**T**ime **T**o **F**ailure

Dedicated to Chiara and my Dear family

Chapter 1

Introduction

This chapter will firstly introduce the power semiconductor devices used in power electronics, considering their evolution along the history and their classification regarding the utilization mode.

Secondly, Power Integrated Circuits (PICs) will be presented in order to describe the semiconductor device integration on a single chip (low and medium power density) and finally, the attention will be focused on Power Modules technology (medium, high and very high power density) representing the subject of this thesis.

1.1 Power Semiconductor Device

A **power semiconductor device** is a solid state semiconductor able to control output parameters, such as high current, voltage or frequency [4]. As a matter of fact, power electronics technology converts electric power from one form to another, employing electronic power devices. It constitutes the heart of modern power electronics apparatus [5].

1.1.1 History

1948 Is introduced by William Shockley the first bipolar transistor device with substantial power handling capabilities.

1952 Appears the first power semiconductor device. The power diode was introduced by R.N. Hall: it was made of Germanium and it had a voltage capability of $200V$ and a current rating of $35A$.

1957 The thyristor appears. It could withstanding very high reverse breakdown voltage and it could carry high current. One of the disadvantage of the thyristor, for switching circuits, is that once it is "latched-on" in the conducting state it cannot be turned off by external control. The thyristor turn-off is passive, i.e., the power must be disconnected from the device.

1960 Appears the called Gate Turn-Off Thyristors (GTO), which could be turned off. Unfortunately, these components overcame some limitations of the thyristors because they can be turned on or off with an applied signal [6].

1970 With the improvements of the Metal Oxide Semiconductor technology (initially developed to produce integrated circuits), appear the power MOSFETs.

1975 The power module is introduced [7]. As a result of the isolated construction this new architecture penetrated the market.

1978 International Rectifier introduces a $25A$, $400V$ power MOSFET. This device allows operation at higher frequencies than a bipolar transistor, but it is limited to low voltage applications [8].

1980s The Insulated Gate Bipolar Transistor (IGBT) is developed.

1990s IGBT became widely available. This component has the power handling capability of the bipolar transistor, with the advantages of the isolated gate drive of the power MOSFET [1].

2000s New types of large band-gap materials, such as silicon carbide "SiC" and gallium nitride "GaN" [9], became promising for the future generation of devices.
SiC material has faster minority carrier lifetime, high carrier mobility and high thermal and electrical conductivities. These properties allow high-voltage and high-power capabilities, low conduction drop, fast switching (for example, high switching frequency), high junction temperature (i.e., up to $350°C$) and good radiation hardness.
This material started to be applied on devices, such as diodes, power MOSFETs, thyristors, GTOs, IGBTs, etc. [5].

It is interesting to note that, the evolution on power electronics technology has generally followed the evolution of power semiconductor devices. The improvement of industrial microelectronics has strongly contributed to the knowledge of power device materials, processing, fabrication, packaging, modelling, and simulation [5].

Power devices are almost exclusively based on silicon material and according to their controllability degree can be classified into three groups:

Uncontrolled - This group includes diodes. The driving of the diode state, closing (ON) and opening (OFF), depends on the external power circuit to which it is connected. Therefore, these devices do not have any external control terminal.

Semi-controlled - Thyristor, Silicon Controlled Rectifier (SCR) and Triode of Alternating Current (TRIAC) belong to this group. In this case start-conduction (OFF to ON) is due not only to its external power circuit, but also to an external control signal applied to one of the terminals of the device, commonly called 'gate'. However, the set blocking (from ON to OFF) is determined by the power circuit itself that only allows an external control start driving.

Full controlled - This group includes bipolar transistors Bipolar Junction Transistor (BJT), MOSFET, IGBT and GTO, among others. In this case the set blocking can be controlled also by their driving terminal.

Another possible classification could be made considering the utilization mode, because a power semiconductor device is used as a switch or rectifier in power electronics.

1.1.2 Rectifier Mode

This group is composed by power diodes and it is a two-terminal device (Anode "A" and Cathode "K").
On forward-biased (conduction state), diodes must be able to support an high current intensity with a low drop voltage (V_D). On the contrary, on reverse-biased (rectifier state) condition, they must be able to support an high negative voltage drop, with a little leakage current. Furthermore, if the reverse voltage applied is higher than the Break Voltage drop (V_{BR}), the leakage current increases quickly up to break the device. Summarizing, the blocking voltage capability of a power diode depends on the polarity of the applied voltage [4].

In the figure 1.1, the electric symbol shows the anode and cathode connection, that corresponds to the top and the bottom side of the die. In addition, the graphic of the diode behaviour shows a static characteristic that could be described by three zones:
- **Forward condition.** High current increases when $V > V_D$.
- **Reverse condition.** Low leakage current while $-V < V_{BR}$.
- **Breakdown condition** High leakage current with high negative voltage drop $-V > V_{BR}$.

The characteristic to provide an uncontrolled power rectification, makes them suitable for applications as electroplating, battery charging, welding, power supplies (DC and AC), variable frequency drives, etc [5].

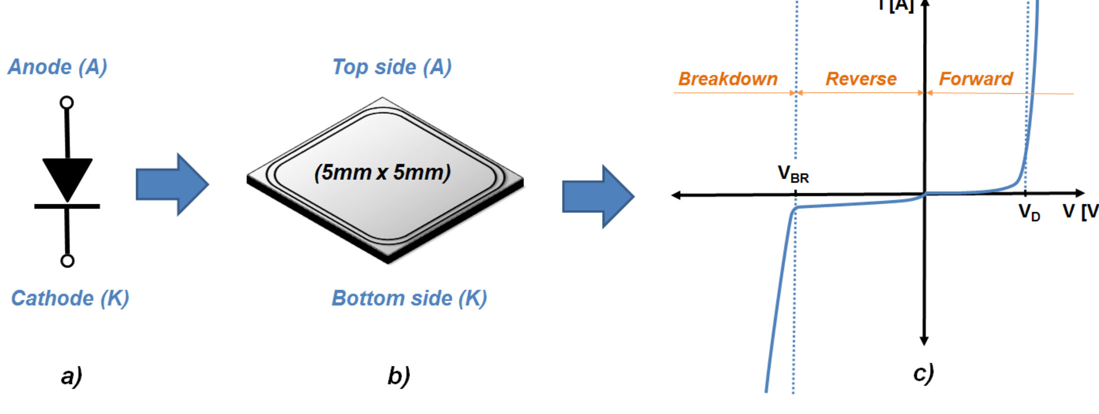


FIGURE 1.1: Diode - (a) Electronic symbol, (b) Die representation and (c) Operating wave form.

1.1.3 Switch Mode

This group is composed by semi-controlled and full controlled semiconductor devices, used as a switch. Power devices behave like a statically operating switch, without moving contacts [4].

The various combination of on-off switches in a matrix form, allows to create a vast amount of power electronic converters. For example, to convert power from $AC{-}to{-}DC$ (rectifier), $DC - to - DC$ (chopper), $DC - to - AC$ (inverter), and $AC - to - AC$ at the same (AC controller) or different frequencies (cycloconverter) [5].

In many converter types, the individual switches are operated in a particular sequence, on one time period, and this sequence is repeated at the switching frequency of the converter. For example: The figure 1.2 shows an electric scheme DC/AC converter, also called "inverter" because an "inverted power conversion" is obtained.

The electric scheme shows four switches $S_1 - S_4$, powered by a DC voltage source (V) connected to the input terminals P (positive) and Q (negative). The timing of the switches shows that, during $t = t_1$, S_1 and S_4 are kept ON, then the input DC voltage appears at the output terminals with terminal A positive ($V_{AB} = +V = V_{PQ}$). On the next time interval $t = t_2$, S_1 and S_4 are kept OFF and S_2 and S_3 are kept ON. Therefore, the input DC voltage appears at the output terminals with terminal A negative ($V_{AB} = -V$ but $V_{PQ} = +V$).
If this sequence of switching is repeated during the time, the DC voltage present on the input and also on the terminals PQ, describes on the output (terminals AB) an AC square wave voltage [4].

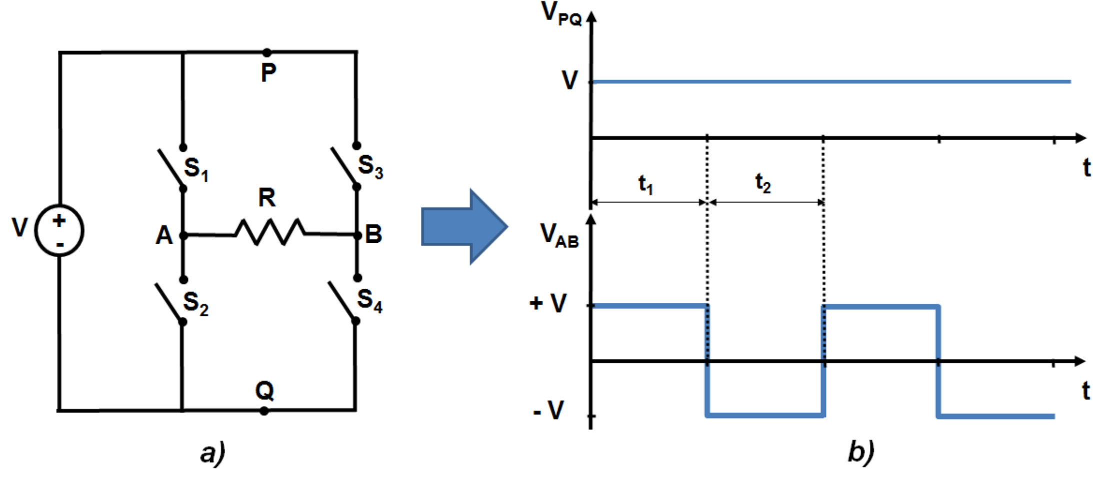


FIGURE 1.2: Switch Mode - (a) Schematic electric and (b) Wave forms of Inverter configuration.

However a rectifier circuit could be obtained (see the figure 1.3)changing the DC voltage with an AC generator, and exchanging it with the load "R" position.

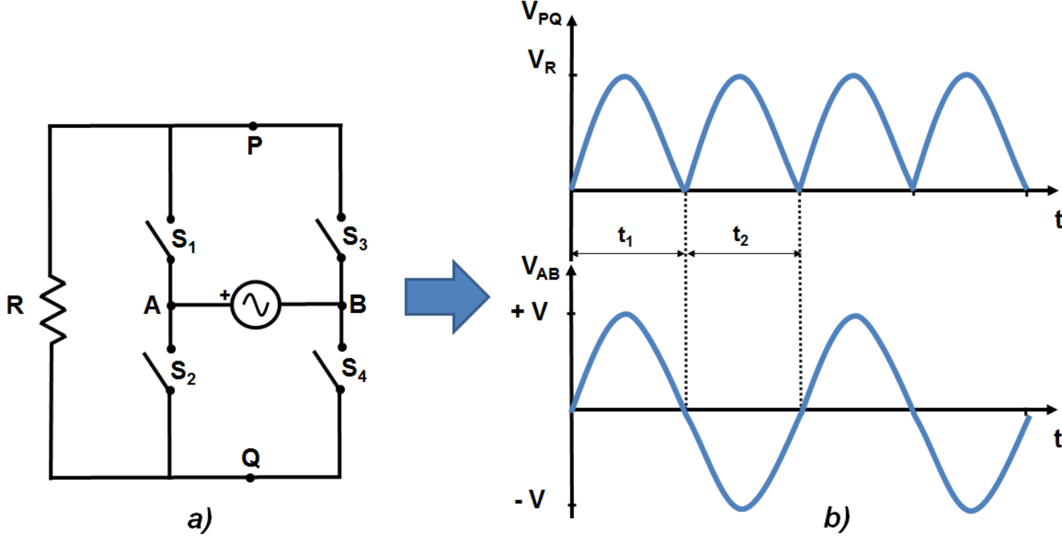


FIGURE 1.3: Rectifier circuit obtained with Switch Mode - (a) Schematic electric and (b) Wave forms.

This circuit is called rectifier because the alternate wave form ($V_{AB} = AC$ current) is transformed on only positive cycles (V_{PQ}).
The switches $S_1 - S_4$ operate following the same timing explained before. Therefore, the input AC voltage presented in the input terminal "AB" is now as a unidirectional voltage at the output terminals "PQ".
In this case, it should be noted that the current direction through the switches is opposite [4].

The switching mode power conversion is characterized for allowing high efficiency, but switches are not ideal. The non linearity of switches, causes at both sides, harmonics generation (the supply and load sides). In addition, switching losses happen during the turn-on and turn-off state [4].

Characteristic of "Semi-controlled" and "Full-controlled" devices, as switching frequency, voltage range or current range, leads to classify the devices on a practical application range. The figure 1.4 illustrates this practical application range of each type of power silicon device in power converters [1].

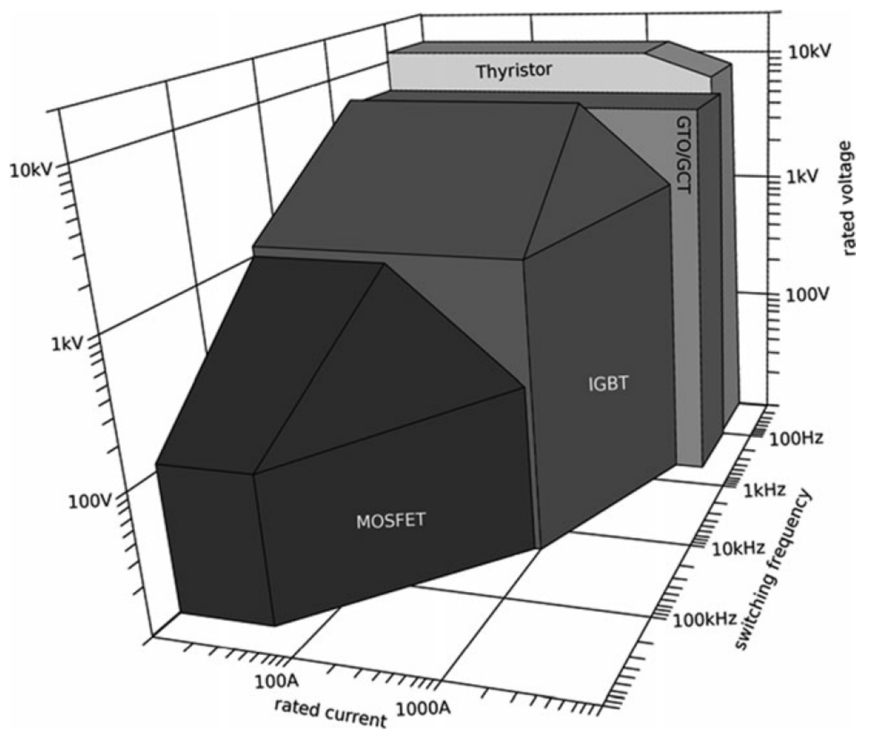


FIGURE 1.4: Operating rate of "Semi-controlled" and "Full-controlled" devices (Extracted from [1]).

Converters can be used in applications such as *AC* and *DC* power supplies or motor drives, heating and lighting controls, static VAR generation, electrochemical processes, active harmonic filtering, etc [5].

1.2 Power Integrated Circuits (PIC)

Due to the interest of the industrialized countries to reducing their greenhouse gas emission and for using energy more efficiently and intelligently [10][11], power integrated circuits (PICs) appeared on the market, offering a combination of control and power electronics monolithically integrated on the same chip [12].

Called also as "smart" power circuits or power ICs, these integrated circuits consist of a level-shifting and drive circuit that translates logic-level input signals from a microprocessor to a voltage and current level, enough to control a power load [5][13][14].
The motivations behind a PIC are reduction in size, cost and improvement in reliability.

On the other hand, the PIC manufacture presents two main problems:
- isolation between high-voltage and low-voltage devices,
- thermal management.

The key feature that differentiates it from other semiconductor technologies is its ability to handle power conversion and to control high voltages and high currents in automobiles, audio equipment and television, heat transfer, home appliances, aircraft, robotics, motors, traction, flat-panel, electroluminescent displays, switching devices, electrostatic printing, and power systems (transmission, distribution, and conditioning of energy) etc. An example of this is an automotive multiplexed bus system with distributed power integrated circuits for control of lights, motors, air conditioning, etc. [14][13].

The power delivered by the PIC into a load can be tens, hundreds, or even thousands of watts; PICs can deliver either high-output current at low supply voltage, low-output current at high supply voltage, or medium-output current at medium supply voltage.

Recently, a large family of PICs that includes power MOSFETs or IGBT smart switches, two-phase step or three-phase brushless DC motor drivers, half-bridge inverter drivers, one-quadrant choppers for DC motor drives, etc. has become available.

Figure 1.5 shows a monolithic PIC (into the dotted rectangle) for driving a brushless dc motor: the simplified block diagram describes a $40V$, $2A$ PIC that consists of a six-switch power stage, current-regulated Pulse With Modulated (PWM) control of the lower switches, Hall sensor decoding logic and thermal/undervoltage protection features [5].

1.3 Power Modules

Introduced by Semikron[1] in 1975, this new architecture got into the power devices market [7][1].

A **power module** or **power electronic module** is a set of power electronic devices (so-called dies or chips), able to drive high voltage and current, doing a particular function. As a consequence a high power density is manipulated.

The main function of the "module" is to provide a physical containment, id est their

[1] For more information http://www.semikron.com/

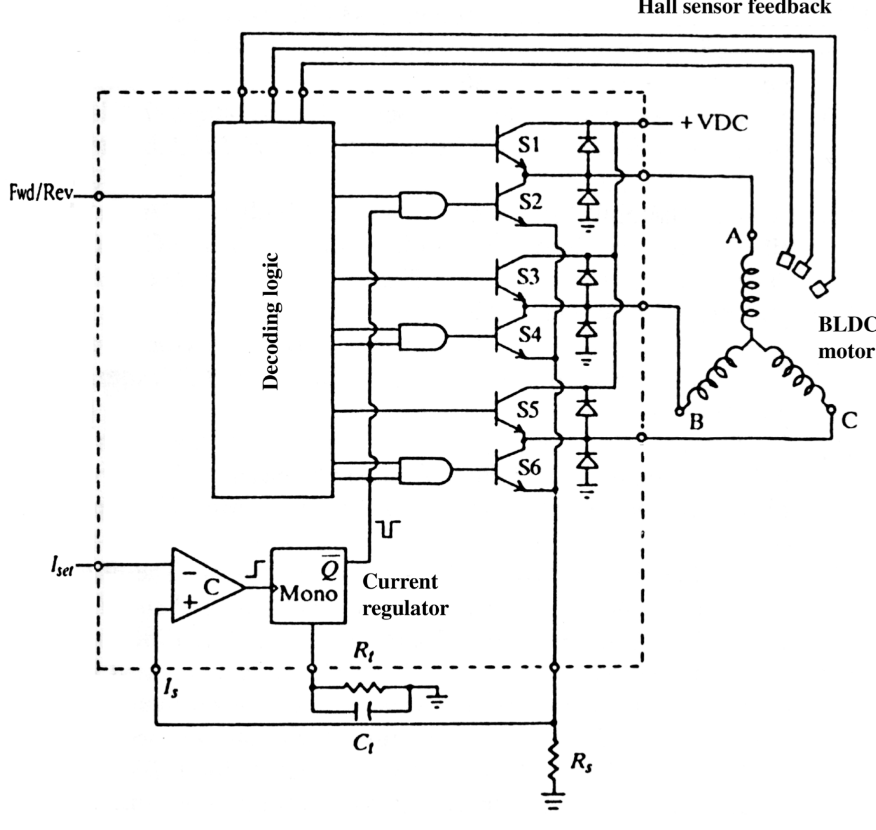


FIGURE 1.5: PIC application example - Monolithic PIC for brushless dc (BLDC) motor drive [5].

structure, commonly called package, must be able to provide and guarantee cooling, electrical connection and insulation between the internal device and the external circuit.

Comparing this kind of structure with the discrete components, while them are suitable for: lower current applications, low volume applications (no tooling) and looser Electromagnetic interference (EMI) requirements, power modules are suitable for:
- high current application,
- high volume applications,
- high power density requirements,
- unconventional shape requirement.

Furthermore, power modules present multiples advantages as for example:

Form Factor - Modules could be designed to optimize layout,

Power Density - Offer a more compact and easy mounting solution,

Additional Functionality - Shunt, thermistor, capacitor, gate resistor can be integrated,

Lower Risk - Sub-assembly/Assembly have inner cost to be counted.

1.3.1 Applications

The overall power electronics market grew, during the last years, thank to the continuous growth of the technology, allowed power electronic to embrace every day more and more applications.
However, time-to-market differs from application to application as a function of value proposals for cost, specifications, availability, etc. [15].

Multiple circuit configurations or devices can be contained into a single module, from a single power electronic switch (as MOSFET, IGBT, BJT, Thyristor, GTO or JFET) or diode, to multiple semiconductor dies that are connected to form a specific electrical circuit.
Hence, numerous examples that include a single or multiple power modules can be described. The table 1.1, for example, shows an idea about applications and requirements connected to a kind of power module that can be involved.

Thereby, the market requirements of power modules could be summarized as:
- Long lifetime,
- Low thermal impedance,
- High power density,
- Optimized cost,
- Optimized packaging for low internal and external stray inductance,
- Optimized chip technology, high current density,
- Optimized coefficient of thermal expansion (CTE) [16].

Though, the mentioned applications on the table 1.1 covers a wide range of market, there is one sector that concentrates an elevate number of power modules. This is the Automotive application [15].

The incursion of power electronics in Electric Vehicles and Hybrid Electric Vehicles (EV/HEV) gave the possibility to control efficiently different parts of the car, reducing the consumes and including also the possibility to consider all electrically controlled (since electric power train to electric “fuel”).

The figure 1.6 shows a short description about where power modules are applied in EV/HEV application:

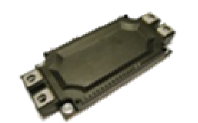
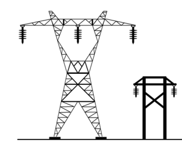
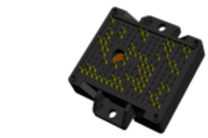
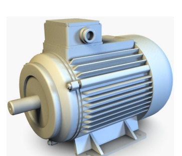
Application	**Requirements**	**Power Module Solution**
Solar panels and inverters	Long life High power density Small size Safety approvals	 Inverter modules
Energy exploration	Long life High temperature operation Safety approvals	 Inverter modules
 Power Transmission and Distribution	Long life High voltage capability Custom design	 Phase-leg thyristors; SCR/IGBT modules
 Intralogistics Lift trucks	Very robust Long life Transient resistant High power and current density	 IGBT/MOSFET/diode modules
 Windmills and large inverters	Safety approvals High reliability Custom design High power density	 Phase-leg thyristors; SCR/IGBT modules
 Efficient Motor drives	High voltage capability High power and current density Transient resistant Long life	 Bipolar SCR/IGBT/MOSFET diode modules

TABLE 1.1: Power modules applications.

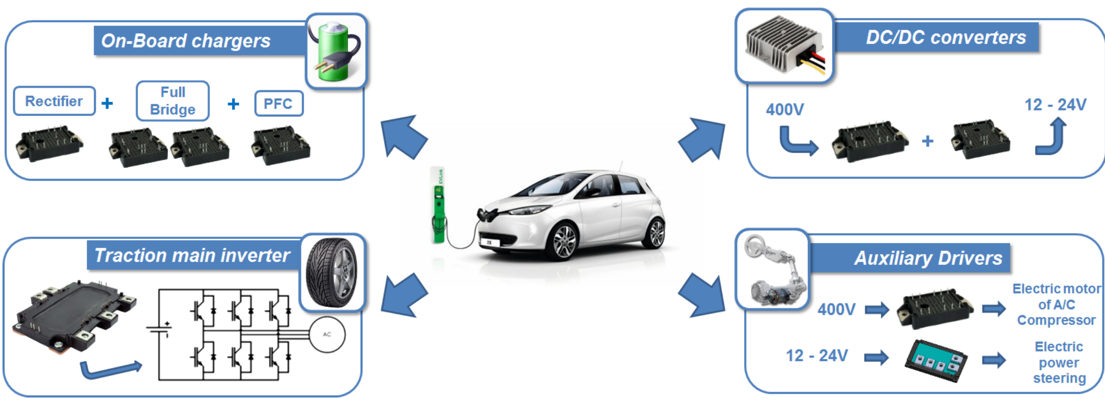


FIGURE 1.6: Example of HEV automotive application.

Auxiliary Inverters - Former belt-driven devices, as alternator, water pump, aircon, etc. have been electrified and integrated in the power system.
Aircon Compressor Driver - High voltage main batteries are connected to the power module (IGBT + diodes) in order to drive an electric motor ($3 - 7kW$).
Electric Power Steering - In this case the power module (power MOSFET) is connected to a low voltage auxiliary battery and drives the electric motor of the electric power steering.

DC/DC converters - Different voltage levels are required for various electronic components in an EV. The power module (IGBT + diodes) supplies the $12V$ power system from the high voltage battery ($400V$).

On-Board chargers - With On-board battery charger unit (power MOSFETs/-Diodes), the battery can be charged from a standard power outlet (Plug-in Hybrid). Charging via the main grid calls for design flexibility given the different voltage and current levels.

Traction main inverter - Featuring an electric power train, the inverter controls the electric motor. It also captures energy released through regenerative breaking and feeds this back to the battery.

v

Chapter 2

Power Modules

This chapter presents the different power modules packages used and studied in this thesis work (isolated and non isolated), paying a particular attention to describe their critical and improvable points.

2.1 Packages

As explained in Chapter 1, the power module package has an essential role: it is responsible for provides cooling, electrical connection and a correct insulation, between the internal semiconductor devices and the external circuit.

There are many typologies of packages and, the selection of an appropriate one depends on the contained semiconductor device range performance [1].

This work is focused on analysing and comparing three different packages, divided in two big categories: Isolated and Non Isolated. Note that the isolation corresponds to the possibility to electrically isolate the package with external circuit.

However, before starting with the packages description, it is interesting to spend some words about their internal circuit.

2.1.1 Non isolated and isolated - Internal electronic configuration

Both in the isolated and non isolated category, the internal electronic configuration is composed by two diodes connected in common cathode.

Internal diodes are classified as "Ultrafast Soft Recovery Diode, 60A FRED[1]" and they are optimized to reduce losses and Radio-frequency/Electromagnetic Interferences (RMI/EMI) in high frequency power conditioning systems. Furthermore, the softness of the recovery eliminates the need for a snubber in most applications. These devices are ideally suited for High Frequency (HF) welding, power converters and other applications, where switching losses are not a significant portion of total losses.

Features and benefits:

- $200x200mils$ die size and $14mils$ of thickness
- Bondable front side metal and sonderable back side metal
- Ultrafast recovery time
- Low forward voltage drop
- $175°C$ operating junction temperature
- Designed and qualified according to JEDEC® - JESD 47.
- Reduced RFI and EMI
- Higher frequency operation
- Reduced snubbing
- Reduced parts count.

In the following table 2.1 absolute maximum ratings of diodes are showed:

Parameter	**Symbol**	**Test condition**	**Values**	**Units**
Cathode to anode voltage	V_R		400	V
Continuous forward current	$I_{F(AV)}$	$T_C = 127°C$	60	A
Single pulse forward current	I_{FSM}	$T_C = 25°C$	600	A
Maximum repetitive forward current	I_{FRM}	Square wave, $20kHz$	120	A
Operating junction and storage temperatures	T_J, T_{JStg}		$-55to+$ 175	$°C$

Table 2.1: Absolute Maximum Raitings of a Ultrafast Soft Recovery Diode, 60A FRED.

2.1.2 Non Isolated Package

This kind of package is called non isolated, because the metal base plate (that fixes the dies internally) is not electrically isolated and it represents the cathode of diodes.

The figure 2.1 shows the called TO-244 package.

Internally there are 8 diodes (4 for each leg) connected in a parallel common cathode

[1]For more information: http://www.vishay.com/

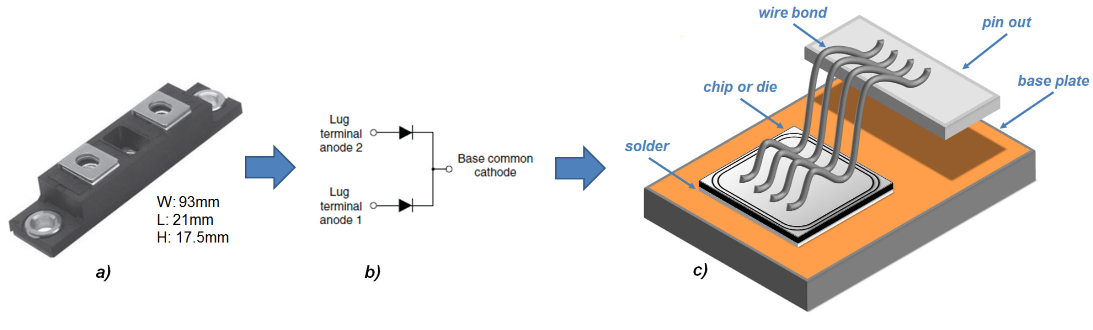


FIGURE 2.1: Non isolated power module - (a) Real device, (b) Internal electronic configuration and (c) Internal composition.

and, as it is possible to observe, this typology of power module is composed by different parts:
Wire bonding - It connects the top of dies among other dies and with the external pin (pin out),
Dies or chips - Electronic components making a particular function.
Pin out or terminals - Mechanically stronger then the wire bond, the pin out connects the power module with the external circuit. It is inserted on the box (not soldered on the structure) and it provides a mechanical connection with the external circuit, not soldered.
Solder or die attach - A commonly conductive metal leg (AgSn(3.5))makes an electrical connection between the bottom of the die and the base plate.
Base plate - Composed by Cu metal with external nickel finish, it guarantees the thermal dissipation and the mechanical fixing of the package with the heat sink.

2.1.3 Isolated Packages

This kind of package is called isolated, because a Direct Bond Copper (DBC) is included inside.

The DBC, produced by Curamik[2], is composed by two external metal layers and an insulated one between of them. The standard structure includes a copper “Cu” bonded (thickness $0.3mm$) to a ceramic substrate such as alumina Al_2O_3 (thickness 0.38mm).

This material is adapted for high power and temperature applications. In addition, it offers the following advantages:
- great heat conductivity and temperature resistance,
- high heat spreading,
- adjusted Coefficient of Thermal Expansion (CTE) between chip and substrate. The

[2]For more information: http://www.curamik.com

mechanical stress on silicon chips mounted directly on the substrate (chip on board) is very low, since the CTE of the ceramic substrate is better matched to the CTE of silicon, compared to substrates using metal or plastic basis.
- High flexibility to obtain various circuits layout. Different electrical configurations can be obtained by chemical etching.

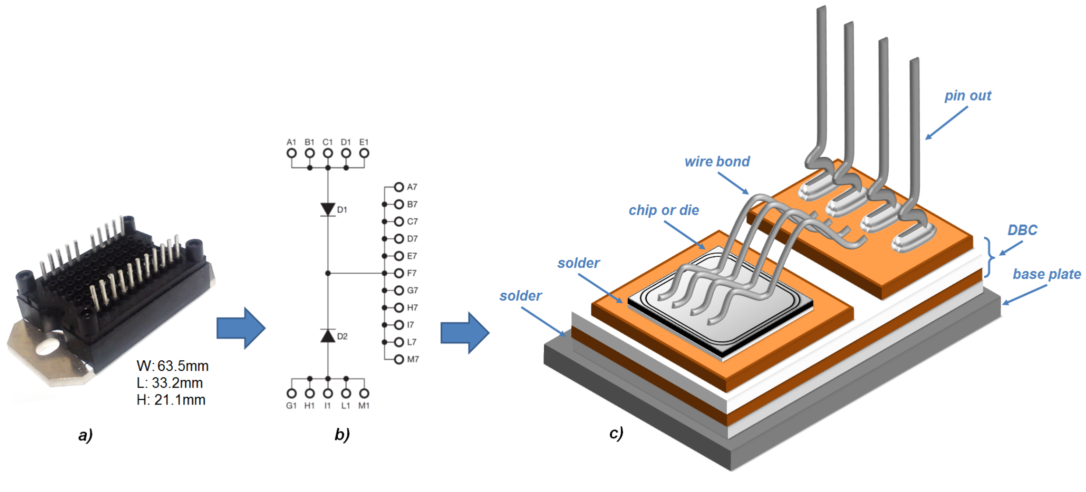


FIGURE 2.2: Isolated power module - (a) Real device, (b) Internal electric scheme and (c) Internal composition.

The figure 2.2 shows the called MTP package.
This kind of package presents the same internal circuit showed on the TO-244 package, but it provides some advantages:
- Ceramic fully insulated package ($V_{ISOL} = 3500 V_{AC}$)
- Print Circuit Board (PCB) solderable terminals
- Direct mounting of heatsink

Therefore, looking at the representation of the internal composition in the figure 2.2, and comparing again with the TO-244 package (explained in 2.1), it is possible to observe that MTP package differs by having:
Wire bonding - Bonded between dies and dies-substrate,
Pin out - This electrical connection with the external circuit is soldered to the DBC and can be soldered on the external circuit.
Solder layers - The metal contact (AgSn(3.5)) is located between die/DBC and DBC/base plate.
DBC - Situated between the solder layers, it guarantees the electrical isolation.
Base plate - Soldered with the DBC.

The last package included in this thesis work is the called ADD-A-PAK (see figure 2.3). This kind of package, isolated package, is a sort of combination of TO-244 and MTP. It combines the external pin out of TO-244 and the electrical isolation of MTP packages.

Furthermore, its principal advantage is the excellent thermal performance obtained by the usage of exposed DBC substrate directly mounting with the heatsink.

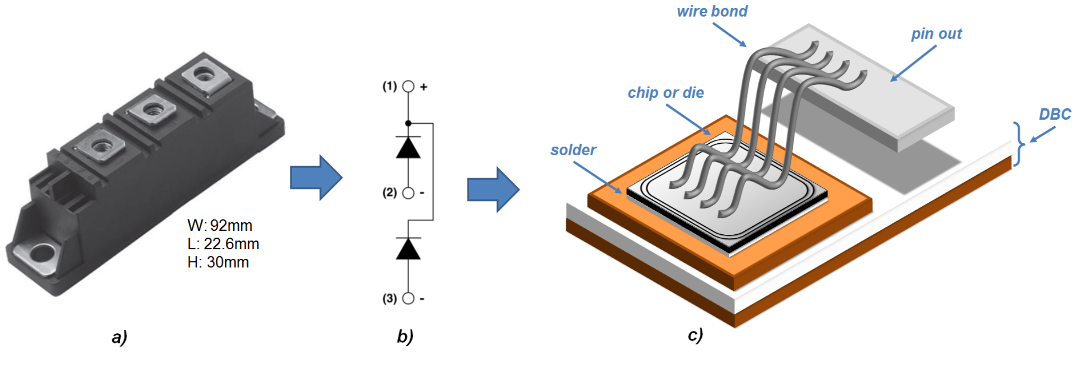


FIGURE 2.3: Isolated power module without base plate - (a) Real device, (b) Internal electric scheme and (c) Internal composition.

Finally, in order to conclude about the internal composition of this packages, all of the boxed structures (2.1 and 2.2) are fill in with silicone dielectric gel SYLGARD 527. This kind of gel, produced by Dow Corning[3], is a bi-component material, with excellent dielectric properties, low viscosity and adapted to industrial production.
It is used to provide long term sealing against moisture and atmospheric contaminants.

2.1.4 Critical and improvable points

Hard conditions on which power modules applications are subjected (modules placed in inaccessible locations and subjected to harsh environments), combined with the increasing power density (from the combination of increased device power levels and reduced packaging), lead to higher junction temperatures and reduced reliability [17][18].
Furthermore, power losses, generated during on-state and blocking state of a device and the additional losses, caused by the transition between these states, are deposited as thermal energy in the chip and must be extracted along the package [3][19].

The study of new materials for packages design in "isolated and non isolated" (chip, interconnections substrates, wire bonding, etc) must take into account the above described hard conditions.
This thesis work will be focused on study the application of new materials, with the aim to improve the interconnections related to the die (see figure 2.4):

1 - Chip to substrate layer

2 - Bond Connection

[3]For more information: http://www.dowcorning.com

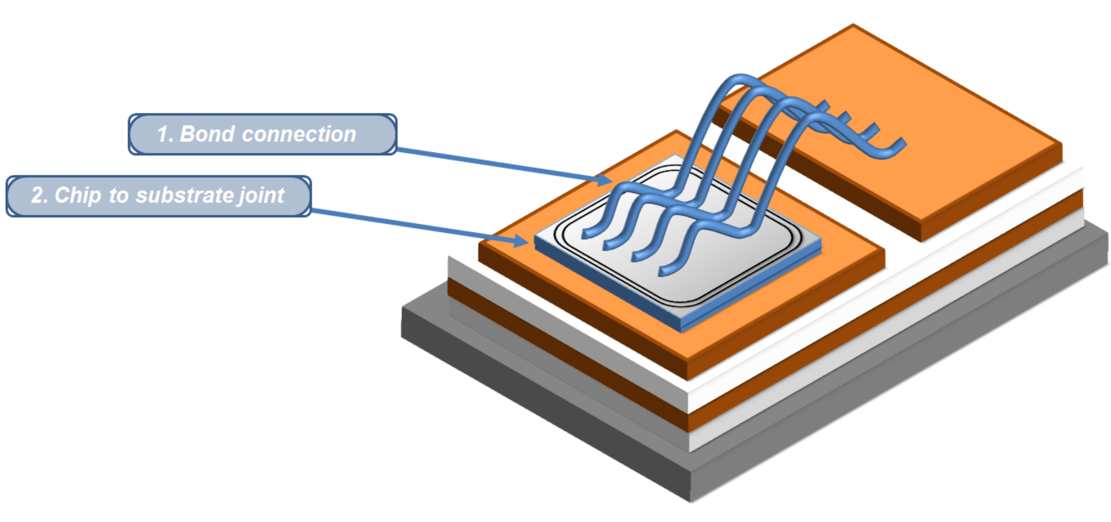


Figure 2.4: Improvable points on an isolated power module.

Chapter 3

Thermal Characterization and Reliability

The increasing power density, on which the power module is submitted, put its internal constituent material under stress condition.
As a consequence, if an higher lifetime device is required, a particular attention has to be focused on the thermal, electrical and mechanical properties of the new materials involved.

This chapter will introduce the methods of characterization and the reliability tests that were employed to evaluate the power module lifetime and the impact of the change on bond connection and chip to substrate layer on the power module characteristics.

3.1 Thermal Characterization - Test Method

The purpose of this test is to thermally characterize the power module[19].

Thermal resistance (Rth) is defined as the ratio of temperature rising along a thermal path (die/DBC/base plate, die/DBC or die/base plate) to the heat flowing in that same path, namely, it is a measurement of a temperature difference (ΔT) for which an object or material resists to a heat flow.

Therefore, this test can be associated to the heat dissipation capability of one or more materials (as for example a power module).

Equivalent thermal circuits
The heat flow can be modelled by analogy to an electrical circuit where: heat flow is represented by current, temperatures are represented by voltages, heat sources are

represented by constant current sources and absolute thermal resistances are represented by resistors.

Considering a power module cross section, it could be represented as an equivalent thermal circuit (see the diagram in figure 3.1).

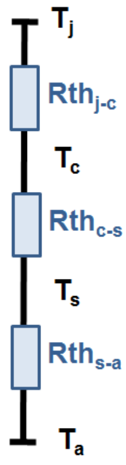


FIGURE 3.1: Thermal circuit of a power module.

Thermal circuit references:
- T_j junction temperature, T_c case temperature, T_s sink (hatesink)temperature and T_a ambient temperature.
- Rth_{j-c} thermal resistance junction-case, Rth_{c-s} thermal resistance case-sink and Rth_{s-a} thermal resistance sink-ambient.

In the above figure 3.1, it is possible to observe that the only one parameter not directly measurable, is the junction temperature (T_j), then an indirect method is necessary to determine this value.

Considering that this work treats power modules, composed by diodes in common cathode configuration, it exists one parameter that has a linear correlation with the module junction temperature: the forward voltage drop[1] (V_f) at fixed bias current (I_b). Note that the current bias shall be chosen to assure that the diode junction is turned on, but not that high to cause a significant self-heating.

To build this correlation, one method is showed in the following picture (see figure 3.2). The device is fixed on a hot plate in order to have a temperature set-up, a DC power supply is applied to provide the current, assuring that the diode junction is turned on, a digital multimeter to measure the forward voltage drop and finally a digital thermometer to measure the hot plate temperature are included.

[1]The forward voltage drop decreases nearly linearly when the temperature increases (see figure 3.2), because in this condition the recombination of charges (electrons and holes) reduces the potential barrier.

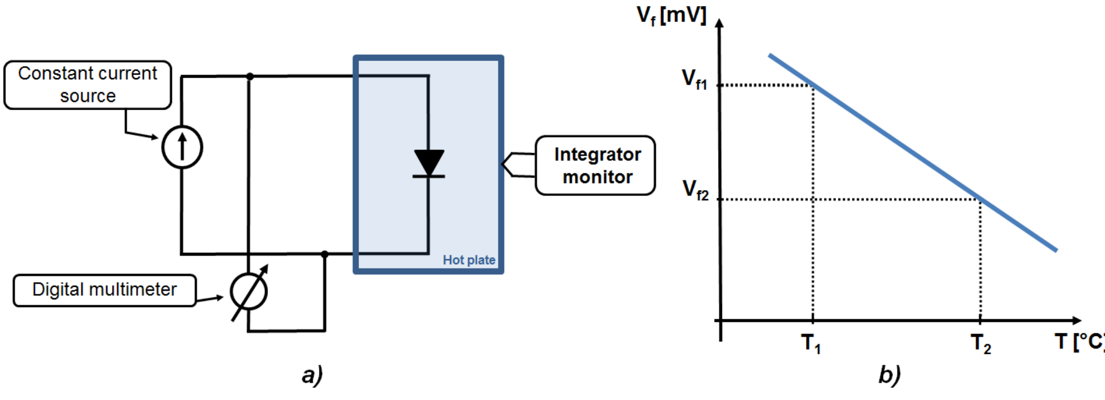


FIGURE 3.2: Coefficient of Thermal Expansion (CTE) - (a) Schematic draw of tools connection and (b) Measured V_f in function of temperature.

Firstly, V_1 is measured (that correspond to the fixed T_1), then another temperature is set (where $T_1 < T_2$) and again the voltage drop (V_2) is measured.

From the plotted curve it is possible to calculate the Coefficient of Thermal Expansion (CTE), that is represented by the slope of the curve[2].

$$m = \frac{V_2 - V_1}{T_2 - T_1} \qquad \left[\frac{mV}{°C}\right] \tag{3.1}$$

Using this coefficient, it is possible to obtain the ΔT_j by the variation of the voltage forward drop (it will be demonstrated later on).

Coefficient of Thermal Expansion (CTE)

Solids mostly "expand", in response to heating and "contract" on cooling. This response to temperature is expressed as coefficient of thermal expansion.
The differences in thermal expansion of the material layers along the package generate mechanical stress in the interfaces between layers (bond connection, chip to substrate joint and substrate to base plate joint).

To minimize the stress induced by thermal expansion between different adjacent layers, their CTE should be comparable (or more precisely in the presence of thermal gradients inside a stack of layers: the difference of the product of layer temperature and the CTE in adjacent layers should be as small as possible) [1].
The figure 3.3 shows for example, the corresponding CTEs of the materials frequently used in power module packages.

[2]Logically it is possible to improve the linear fit, measuring more than two points.

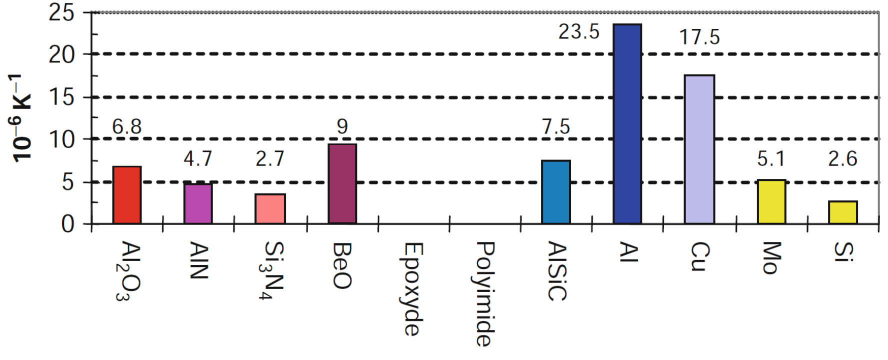


FIGURE 3.3: Coefficient of Thermal Expansion (CTE) of materials frequently used in package technologies.

3.1.1 Thermal Resistance R_{th}

Considering the thermal circuit presented before in the figure 3.1, it is possible to observe the equivalence to an electrical circuit, where Rth $[°C/W]$ corresponds to R $[\Omega]$, the power dissipated P_d $[W]$ corresponds to I $[A]$, and T $[°C]$ corresponds to V $[V]$. As a consequence the thermal resistance, between junction-case, is defined as:

$$Rth_{j-c} = \frac{T_j - T_c}{P_d} \tag{3.2}$$

If all the power input is dissipated by the module (the heatsink is nearly ideal):

$$P = V \cdot I = P_d \tag{3.3}$$

The process to measure the thermal resistance between the "junction" and "case" is similar to the process used by thermal coefficient, but in this case, the device is heated with current I_{test} (see figure 3.4) flowing across the dies and fixed to an appropriate hatesink water cooled.

It is necessary performing two holes to measure the temperature T_c and T_s (one into the case of power module base plate and the other into the hatesink). These holes, showed in the figure 3.5, will be done in correspondence to the center of the junction, then under the die position (when it is possible).

The machine "Thermal Resistance Meter", controlled by computer, gets the current test ($I_{test_{max}} = 500A$) necessary for heating the device, measuring the temperature of the thermocouple and sensing the forward voltage drop when get the current bias ($I_{bias_{max}} = 25A$).

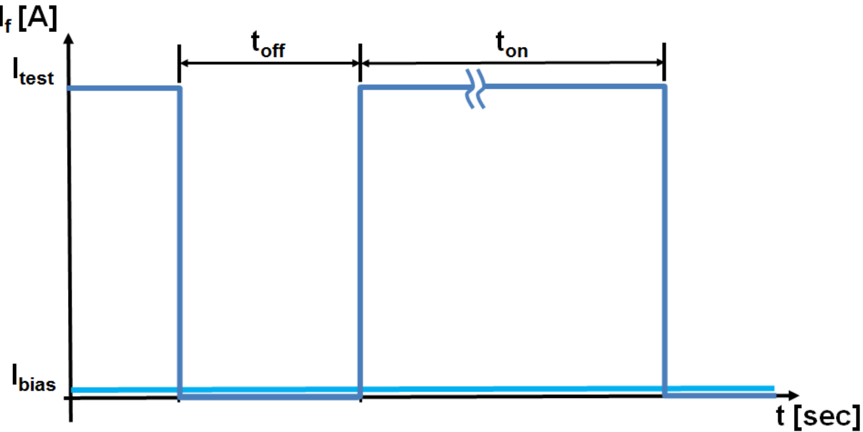


FIGURE 3.4: Thermal Resistance (Rth) - Current description used during the measure.

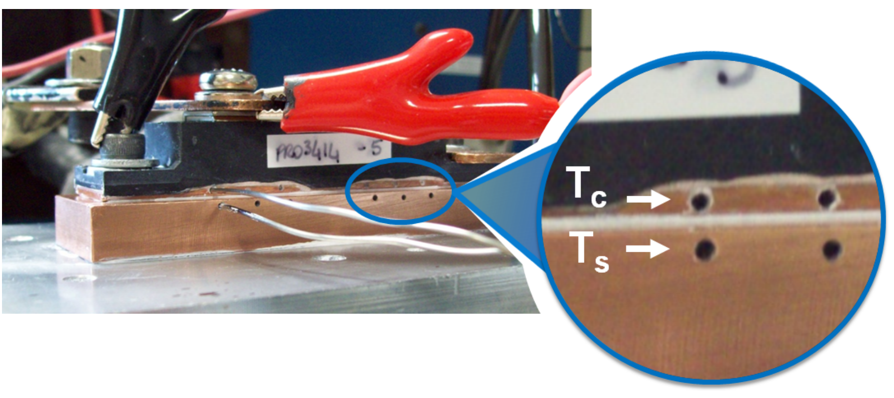


FIGURE 3.5: Thermocouple locations.

The test procedure consists of:
- reading the initial values of $V_{f_{ref}}$ and $T_{c_{ref}}$ (it is possible to assume that this temperature is equal to T_j) when $I_{test} = off$.
- Starting the current flow across the device ($I_{test} = on$ during $t_{on} = 900ms$). This is called "steady state".
- Measuring in "steady state" conditions ($I_{test} = off$, $I_{bias} = 100mA$ during $t_{on} = 500\mu s$) the value of V_f[3], T_{c_2} and V_{bias}.

As a consequence it is possible to note the duty cycle[4] is near to 1 (one), in this way it is assumed that the test was made in DC current.

Now, considering the equation 3.1, therefore:

$$\Delta T = \frac{\Delta V}{m} = \frac{V_{ref} - V_{bias}}{m} \tag{3.4}$$

[3] V_{fm} is the measure of the drop voltage, few μsec before the current test turning off.
[4] "Duty cycle" is defined as $D = t_{on}/\left(t_{on} + t_{off}\right)$

On the other hand, considering that all the power input is dissipated by the inter system

$$P = V_{f_m} \cdot I_{test} = P_d \tag{3.5}$$

and considering also that

$$T_{j_{max}} = \Delta T + T_{c_{ref}} \tag{3.6}$$

it is possible to find the R_{th} equation combining 3.1, 3.2, 3.5 and 3.6

$$R_{th_{j-c}} = \frac{\left(\frac{V_{ref} - V_{bias}}{m} + T_{c_{ref}}\right) - T_c}{V_{f_m} \cdot I_{test}} \tag{3.7}$$

Now, it is possible demonstrating the relationship between ΔT_j, ΔV_f and m (CTE).

If $T_{j_{min}} = T_{c_{ref}}$ is closed to start t_{on} and ΔT_j is defined as:

$$\Delta T_j = T_{j_{max}} - T_{j_{min}} \tag{3.8}$$

Then

$$\Delta T_j = T_{j_{max}} - T_{c_{ref}} \tag{3.9}$$

On the other side $T_{j_{max}}$ is defined as:

$$T_{j_{max}} = T_{rise} + T_{c_{ref}} \tag{3.10}$$

Therefore, substituting 3.10 on 3.9 is obtained that

$$\Delta T_j = T_{rise} \tag{3.11}$$

Considering also that T_{rise} is defined as:

$$T_{rise} = \frac{\Delta V_f}{m} \tag{3.12}$$

Finally, substituting 3.12 on 3.11 is obtained the desired relationship:

$$\Delta T_j = \frac{\Delta V_f}{m} \tag{3.13}$$

3.2 Reliability - Test Methods

The reliability of power electronic devices and components is a prerequisite for the performance in applications: "reliability" is the ability of a system or component to perform its required functions under stated conditions for a specified period of time [1]. Furthermore, the lifetime of the full power electronic system depends on the reliability of each of its component parts [17].

There are two different methods to study the reliability of a power module, they are **Power Cycling Test (PCT)** and **Temperature Cycling Test (TCT)**. These ones are used to determine the resistance of a semiconductor device under thermal and mechanical stress, due to cycling the power or temperature dissipation of the internal connectors and the internal semiconductor die. Furthermore, all the reliability tests cause wear-out along the time and are considered destructive.

Employing PCT is possible to simulate the typical applications in power electronics and to estimate the real operation lifetime [20]. However, this test may not induce the same failure mechanisms as exposure to TCT.

3.2.1 Power Cycling Test

Called also "active" cycling test or IOL (Intermittent Operation Life), the power cycling test provides thermal and mechanical stress due to the periodical power dissipation on the internal semiconductor dies and internal connectors.
Namely, during the test, rapid temperatures changes are induced on the devices and on the interconnections, while low-voltage operating biased for forward conduction (loads current) are continually applied and removed.

For the set-up conditions and implementation was indispensable following the **International Standard International Norm IEC 60749-34**.

Temperature extremes		**Cycle period**	$\Delta T_j\,[°C]$	**Example of failure mode**
$\Delta T_c\,[°C]$	$T_j\,[°C]$			
< 30	$45(\pm5)$ to 125	$1s$ to $15s$	60 ± 5	Sensitive to wire bond fatigue
< 30	$45(\pm5)$ to 150	$1s$ to $15s$	80 ± 5	
$50(\pm20)$	$45(\pm5)$ to 125	$1min$ to $15min$	75 ± 5	Sensitive to soft solder and wire bond fatigue
$60(\pm20)$	$45(\pm5)$ to 150	$1min$ to $15min$	95 ± 5	

Table 3.1: Power Cycling Test Conditions of International Standard International Norm IEC 60749-34.

The table 3.1 shows that the test parameters shall be selected depending on which failure mode has to be analysed. Namely:
- if the interest is centred to obtain wire bond fatigue, $\Delta T_c < 30°C$ and the cycle period must be $\leq 15s$.
- If the interest is to have soft solder and wire bonding fatigue, $\Delta T_c > 30°C$ and the cycle period must be $1min < time < 15min$.

Thereby, since different failure modes are related to power cycling conditions, improvements of power module technologies will be investigated in different lifetime [17][21]. Parameters, as "time" and "current" must be fixed in order to obtain the ΔT desired, making attention on not exceed the maximum levels of the tested device ($I_{f_{max}}$, $P_{d_{max}}$, $T_{j_{max}}$, etc.).

3.2.1.1 Long Power Cycling Test

Long power cycling tests are mainly characterised by a larger ΔT_c and by the cycle period.

Devices are individually mounted on a heat sink, with air convection cooling (as in a real application).
Then, all power modules, which are connected in series configuration to have the same load current (I_{test}), will be heat up by the power losses of the chip. When the maximum target temperature ($T_{c_{max}}$) is reached, the load current is switched off and the system cools down to a minimum temperature ($T_{c_{min}}$). The reaching of the minimum temperature completes the cycle and the next cycle begins by starting I_{test} again.

During each cycle, stressing thermally and mechanically the structure, considerable temperature gradients are generated inside the module. An exemplary temperature evolution is shown in the figure 3.6.

In order to explain more into details the utilized system, the figure 3.7 represents the schematic connection.

In the scheme the "voltage generator" provides the necessary current to heat the device, the "multimeter" measures the temperature of the thermocouple located on the base plate and heatsink (T_c and T_s) and senses the forward voltage drop (V_f) of the devices.

Therefore, the "timer" switches the I_{test} between ON/OFF, controlling also the system coolers. Thereby, it is able to set-up the ΔT_c or ΔT_j desired:
- Switch Closed. t_{on} - Modules are heated by I_{test} and the system coolers are off.
- Switch Opened. t_{off} - I_{test} turns off and system coolers turn on.

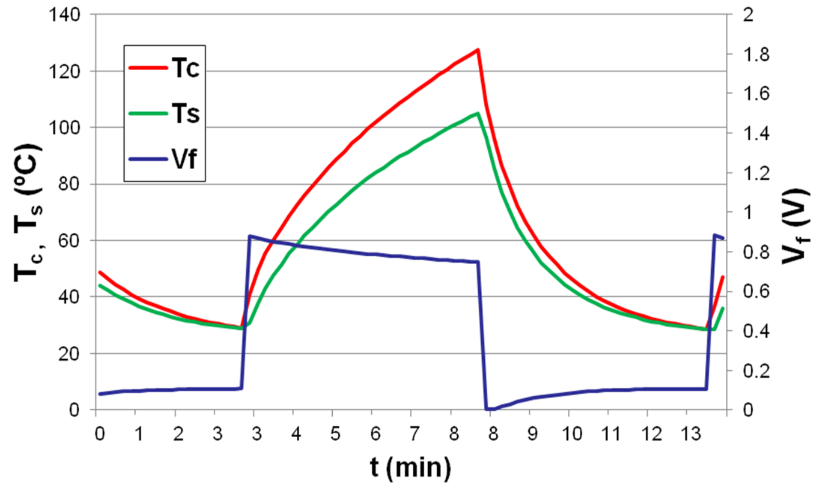


FIGURE 3.6: Typical temperature excursion of Power Cycling Test set-up.

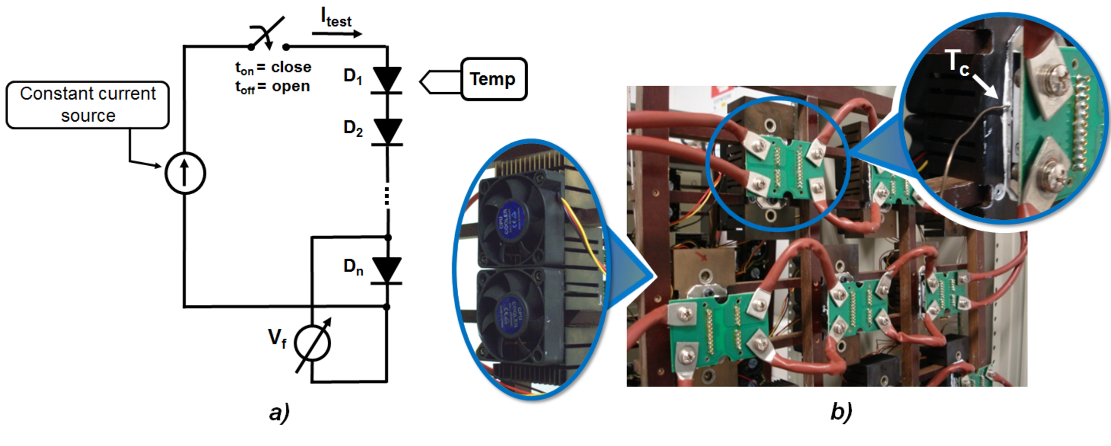


FIGURE 3.7: Large Power Cycling Test (PCT) - (a) Schematic draw of tools connection and (b) Example of power modules connection and thermocouple location.

The PCT has to be continuous except when parts are removed from the test fixtures for interim electrical and thermal measurements (V_f, V_{BR}, $I_{leackage}$, Rth_{j-c}, etc).

The numbers of cycles until to a damaged condition (for example $\Delta V_f > 20\%$ or $\Delta Rth_{j-c} > 50\%$), define the lifetime of the power module.

3.2.1.2 Short Power Cycling Test

In terms of functionality, Short and Long Power Cycling Test are similar, but the target is different.
As showed in the previous table 3.1, the interest of Short PCT is mainly focused on

"sensitive wire bond fatigue", obtaining a defined ΔT_j, during $t_{cycles} \leq 15s$ and maintaining also $\Delta T_c < 30°C$. Then, under this test conditions a short and higher current pulse I_{test} is required.

Thereby, the need to have strong and faster current pulse and to measure the voltage drop V_f, instantaneously before and after (with a smaller current I_{bias}), brought the necessity to employ a dedicated tester machine.

In collaboration with MRS Electronics GmbH[5] a new tester was introduced.

MRS Tester

This kind of machine (see figure 3.8) combines the possibility to stress periodically the power module structure and to realize an accurate electric measurement.

Electrical connection

The connection plate is composed of 10 DUT's water cooled, where each one has a thermocouple for temperature measurement and 8 electrical connections: BF+ (Positive Force), BS+ (Positive Sense), G_{HS} (Gate High Side), BF− (Negative Force), BS− (Negative Sense), G_{LS} (Gate Low Side), PF (Phase Force) e PS (Phase Sense).

The power module, under test, must be connected following the electrical scheme "(c)" in figure 3.8, because the tester executes a dedicated program, following, as a reference, the circuit in the figure.

Therefore, the machine applies a special program considering that the circuit is divided in two sides (High and Low), where on each side are presented power, sense and gate controls terminals.

Example: in the figure 3.9 an isolated power module is connected in order to measure each "leg" with a single connection.

Test Program

The test program is composed by three levels:

SEQUENCE EDITOR (Low Level). Generates a defined file that brings together "actions" doing a particular function ("sequences").

PROGRAM EDITOR (Medium Level). Creates an another file that contains the sequences to follow with the respective test limits and settings.

MMP-Editor (High Level). This file associates each "DUT" (or device to be measured) with the test program and the respective thermocouple.

[5]For more information: http://www.mrs-electronic.de

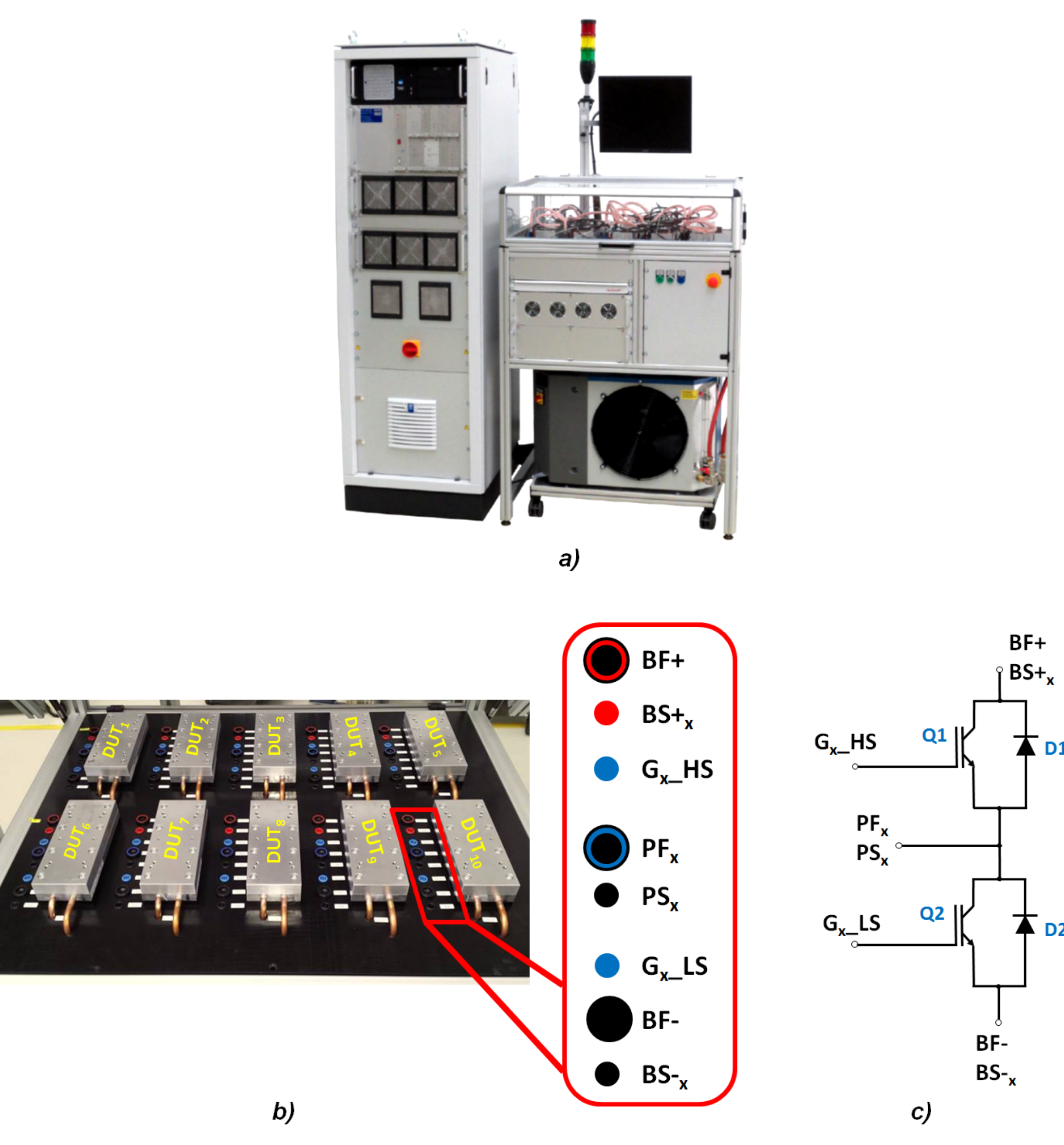


Figure 3.8: Short Power Cycling Test (PCT) - (a) MRS Tester, (b) Internal connection possibilities and (c) Electric scheme reference.

The principal advantage of this tester machine is that the power devices must not be removed until the end of test.

3.2.2 Temperature Cycling Test

Temperature swings are an essential stress condition to be probed for every power electronic component during application. The cyclic mechanical deformation, generated by temperature cycles due to the difference in CTE of the material layers, causes stress in the functional layers themselves and in the interconnection layers.

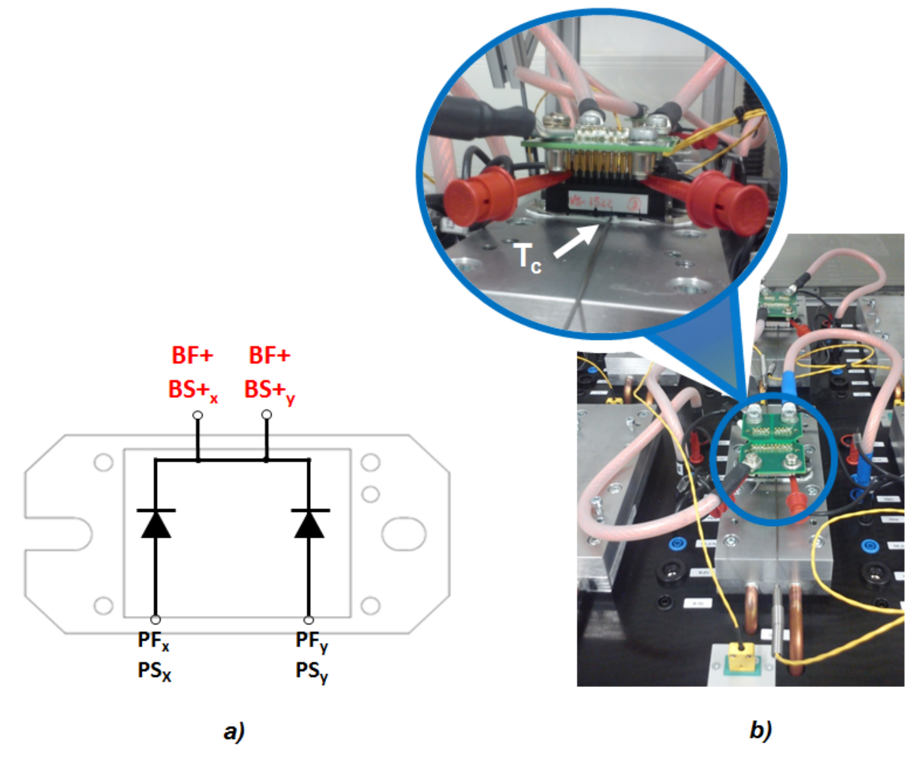


FIGURE 3.9: Example connection - (a) Scheme electric of isolated power module on test (b) Thermocouple location.

The temperature cycling test is able to simulate ambient temperature swings during the field lifetime [1].

Called also "passive" cycling test, this method provides a thermal excursion during a time cycle (without current), applying the same temperature variation to all constituent layers of the power module [22]. Normally the rate of temperature change is slow in the range of 10–40°C/min.

To perform the TCT a Test Chamber, made by ACM Angelantoni Climatic Systems s.p.a[6], was employed.

This machine (see figure 3.10) is composed by two programmable chambers (Heating and Cooling) where temperature and time can be setting.

Therefore, the test consists on setting: T_{min}, T_{max} and the cycling time (for example 30 min each temperature). Then, the devices are deposited in the internal metal box and the "elevator" carried it between the two chambers in the setting time interval.

Test condition

The table 3.2 shows the two possible test conditions realized in Reliability Lab. of VISHAY Semiconductor S.p.A.

[6]For more information: http://www.acsenvironmentaltestchambers.com/

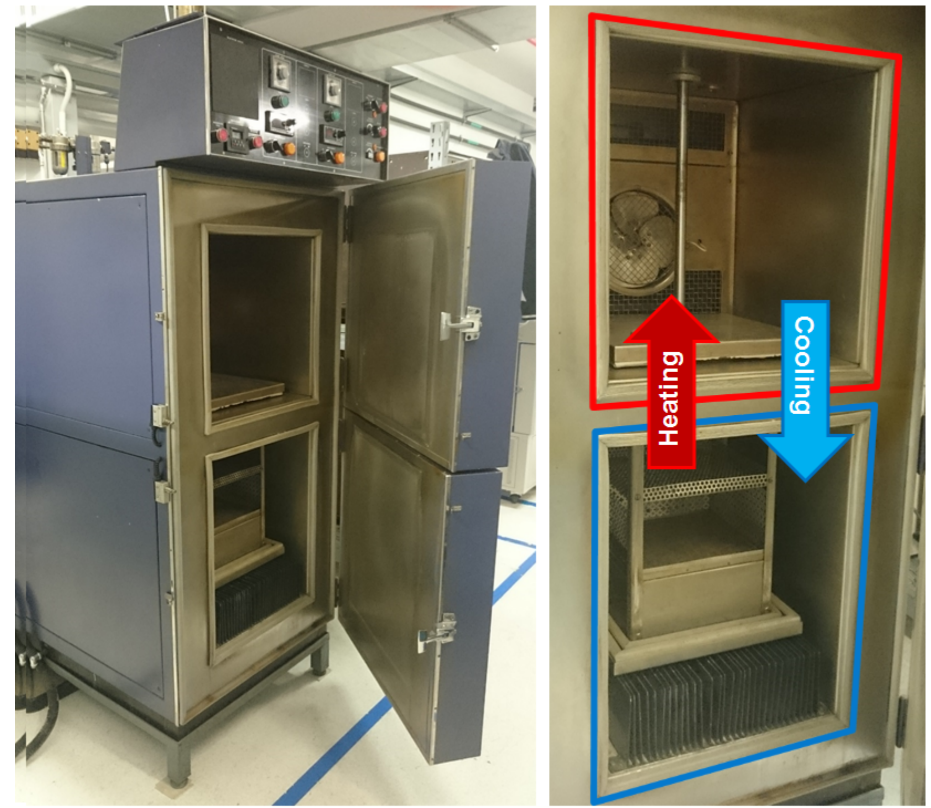


FIGURE 3.10: Test chamber utilized for Temperature Cycling Test.

T_{min} $[°C]$	Timing $[min]$	T_{max} $[°C]$	Timing $[min]$
-40	30	-125	30
-55	15	$+150$	15

TABLE 3.2: Temperature Cycling Test conditions.

The TCT shall be continuous except when parts are removed from the test for interim electrical measurements (V_f, V_{BR}, $I_{leackage}$, etc).

The combination of different materials with different coefficients of thermal expansion results in high mechanical stress in the system.

The test will be stopped when devices reach a damage condition (for example $\Delta V_f >$ 20%).

3.3 Conclusion

To conclude thermal resistance allows the module characterization, evaluating the ageing of devices when exposed to a reliability test; this means, the ageing during PCT and TCT.

These last two methods give information on the reliability of devices. PCT is defined as "active test", because the thermal stress is induced by electrical current. The power impulse could be short, to stress only bonding wires , long to stress wires and substrates. On the other hand, the TCT is a "passive test", without current able to stimulate the entire structure through changes of temperature.

Chapter 4

Chip to substrate Joint

New materials for dies, substrates and interconnection represents another important key for power module development. The need to drive high power density, following also the trend of the electronic market (small dimension, less cost and high reliability), lead to study the incorporation of new materials and technology processes in power module device.

As a consequence, as already mentioned, not only bond connection, but also the interface at the bottom side of the device, play an important role. This chapter will be focused on the interface at the die bottom side: **Chip to substrate Joint**.

This work was carried out in collaboration with HERAEUS Materials Technology[1]. The idea was to study advantages and disadvantages of silver powder sintering process applied to the presented packages in Chapter 3.
The final objective was to adapt this particular and renowned technology to a standard solder technology, evaluating the answer of the the device to a thermal stress (Long PCT and TCT). A failure analysis was led on the obtained microstructures.

4.1 Materials

Concerning the interconnection technologies applied in power modules devices, the role of the layer between die and DBC or Base Plate is substantial. They have to guarantee high electrical and thermal conductivities and high mechanical strength to ensure the smooth operation of the power module.

"Chip to substrate Joint" is responsible of mechanically fix the dies to the substrate, providing cooling and electrical connection through the bottom layer. Thereby, it is very

[1] For more information: http://www.heraeus.com

important, as 'Bonding Connection", in order to improve the overall module performance in terms of reliability and power capability.

In industrial production, **soldering** is still today the most popular technique as die-attach process.

Initially, for low and high temperature applications, brazing alloys, based on tin and lead were used, for example: Sn63Pb37 alloy for high temperature and Pb95Sn5 for low temperature. The ranking was based on the alloy melting temperature, which depends on the lead alloy content: a different melting point was obtained varying the lead alloy.

However, in the year 2006, the RoHS EU Directive forbade the use of lead in electrical and electronic equipment as well as 5 other chemicals (cadmium, mercury, polybrominated biphenyls, hexavalent chromium and polybrominated diphenyl ethers). So, the research tried to substitute these chemicals with other materials able to meet the requirements of the Directive [23].

Since the RoHS entered into force, new alloys' solders and new joining techniques have emerged, as SnAg(3.5) material, which is still today the most widely used in high volume production, for the good reliability (high Young Modules) and lower CTE.

4.1.1 SnAg(3.5)

This solder alloy is in the form of paste, cream or wire and the preform contains various additives. These facilitate the power module interfaces wetting and prevent oxide formation.

SnAg(3.5) lead free solder is composed by 3.5% of silver, 96.5% of tin and flux material:
Tin "Sn" - It is the main structural metal of the alloy. It is characterized by good strength and wetting. Readily it dissolves silver, gold and less, but still significantly many other metals, e.g. copper.

Silver "Ag" - It provides mechanical strength, but it has worse ductility than lead. In absence of lead, it improves resistance to fatigue from thermal cycles. The addition of silver to tin significantly lowers solubility of silver coatings in the tin phase.

Flux - It facilitates the soldering process. One of the obstacles to obtain a successful solder joint is impurity at the site of the joint, for example, dirt, oil or oxidation. Impurities can be removed by mechanical cleaning or by chemical means, but the elevated temperature required to melt the filler metal (the solder) encourages the work piece (and the solder) to re-oxidize. This effect is accelerated as the soldering temperatures increase and can completely prevents the solder from joining to the work-piece. One of the earliest

forms of flux was charcoal, which acts as a reducing agent and helps to prevent oxidation during the soldering process. Some fluxes go beyond the prevention of oxidation and also provide some form of chemical cleaning (corrosion).

SnAg(3.5) is also called "No-clean fluxes", mild enough to not require removal due to their non-conductive and non-corrosive residue. These fluxes are called "no-clean" because the residue left after the solder operation is non-conductive and would not cause electrical shorts; nevertheless they leave a plainly visible white residue that resembles diluted bird-droppings. Therefore, for assemblies that required cleaning, the flux residue of SnAg3.5 can be completely removed by any solvent type flux cleaner.

	SnAg(3.5)	**mAgic sinter layer**	**Units**
Melting temperature	$\simeq 220$	> 960	$°C$
Electrical resistivity	$0.01 - 0.03$	≤ 0.008	$m\Omega \cdot cm$
Thermal conductivity[2]	$20 - 50$	> 100	$\frac{W}{m \cdot K}$
Elastic Modulus @25$°C$	~ 30	> 35	GPa
Thermal expansion	$25 - 30$	≤ 25	$10^{-6}/K$
Effective residue free	No	Yes	

TABLE 4.1: Some physical properties of SnAg(3.5) vs mAgic sinter layers [24].

The good thermal and electrical properties of this material (see Table 4.1) make it a good candidate in high power density application, but with some limitations [25]. The introduction of the power module into the automotive market, brought the necessity to reduce the dimension of the die, to increment power dissipation and the necessity to increase the lifetime of the power module. In addition, with the development of new generations of semiconductors (e.g. based on wide band gap materials like SiC and GaN), the operation temperature will increase up to more than 200$°C$. This leads to a significant decrease of the solders' strength and reliability (solder fatigue).

Therefore, in the structure, the solder layer becomes an important point to be improved and the researchers put attention to study new materials and new technology processes to substitute to the standard one.

4.1.2 mAgic Paste

Since a few years, silver sintering represents a promising improvement in power electronics packaging. It is becoming an attractive alternative to soldering, specially for high temperature applications and high reliability, because it offers: better electrical and thermal properties than a standard solder material, good thermo-mechanical stability, it provides higher melting point which means that sintered joint can withstand environment with relatively high operation temperature (see Table 4.1) [26][25] and it is also a lead-free material.

A couple of years ago Heraeus Materials Technology[3] presented a possible solution to substitute the SnAg3.5 solder layer: mAgic Sinter Paste with pressure [27][28][25] or without pressure [26], applied for high and medium power range.

Microbond Ag Interconnect (mAgic) materials, also called Ag Sinter Paste (ASP), are products mainly formulated by micro or nano particles of silver, mixed with appropriate additives (thinner, binder, dispersant), that enable sintering at low temperatures and low process pressures.
Depending on the formulation and on power electronics design they can be sintered with or without pressure, id est, reducing the particle size higher specific surface (more particle surface per powder volume) are obtained, thus accelerates the diffusion process.

ASP material would connect the silver metallization on both the die and substrate surface, forming a pure silver sintered joint. Therefore, the 100% pure silver is a higher quality solution if compared to solder material paste.

4.2 Processes

In wide terms, if soldering and sintering processes are compared, the important difference that could be noticed is that during soldering, two physic phase changes occurs: solid to liquid and liquid to solid (see figure 4.1). On the other hand, in sintering process any phase fluid to solid transition occurs (see figure 4.1).

The phase changes in soldering process could represent a problem when a large area is soldered, because the liquid phase generates surface tension or gap forces causing a substrate tilting.
On the contrary, it does not happen using sintering material which does not present uncontrolled swimming of chips (less movement of the chips during assembly) and no

[3]For more information: http://www.heraeus.com

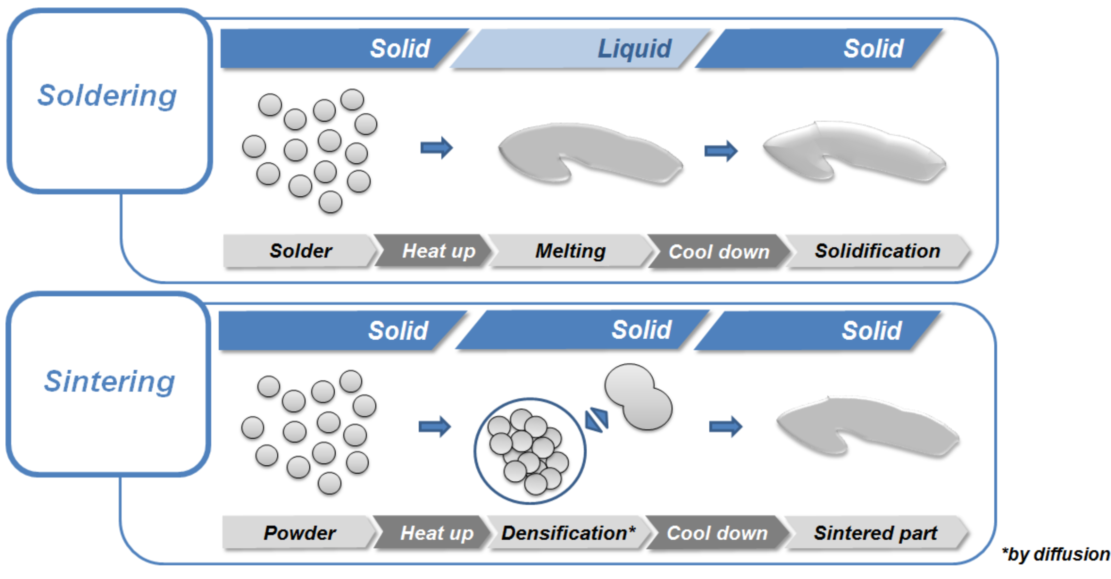


FIGURE 4.1: Solder Vs. Silver Sintering - Scheme of Physical Phases during the processes.

problems in large area (as substrate tilting), because there are not surface tension or gap forces.

4.2.1 Soldering

This kind of process flow could be described by four principal steps (see figure 4.2):

Printing/dispensing - Solder paste is screen printed or dispensed on the substrate (DBC or Base Plate) using a conventional printing equipment. This step allows a regular surface in the die position.

Die placement - In this step each die is located in the corresponding position, using an automatic die place with a standard tooling.

Vacuum reflow - the reflow of the assembly parts according to an adapted temperature/time profile (brazing), using a conventional box oven and subsequently cooled to room temperature.

Cleaning - This step is necessary to remove various contaminants (organic or inorganic residues such as fluxes) that typically remain on substrate surfaces and on chips.
A common drawback of all solder paste is the flux residues on the DBC after soldering and the flux residues which condensate in the re-flow oven. The cleaning of flux residues and condensates creates non-negligible cleaning costs and rework efforts.

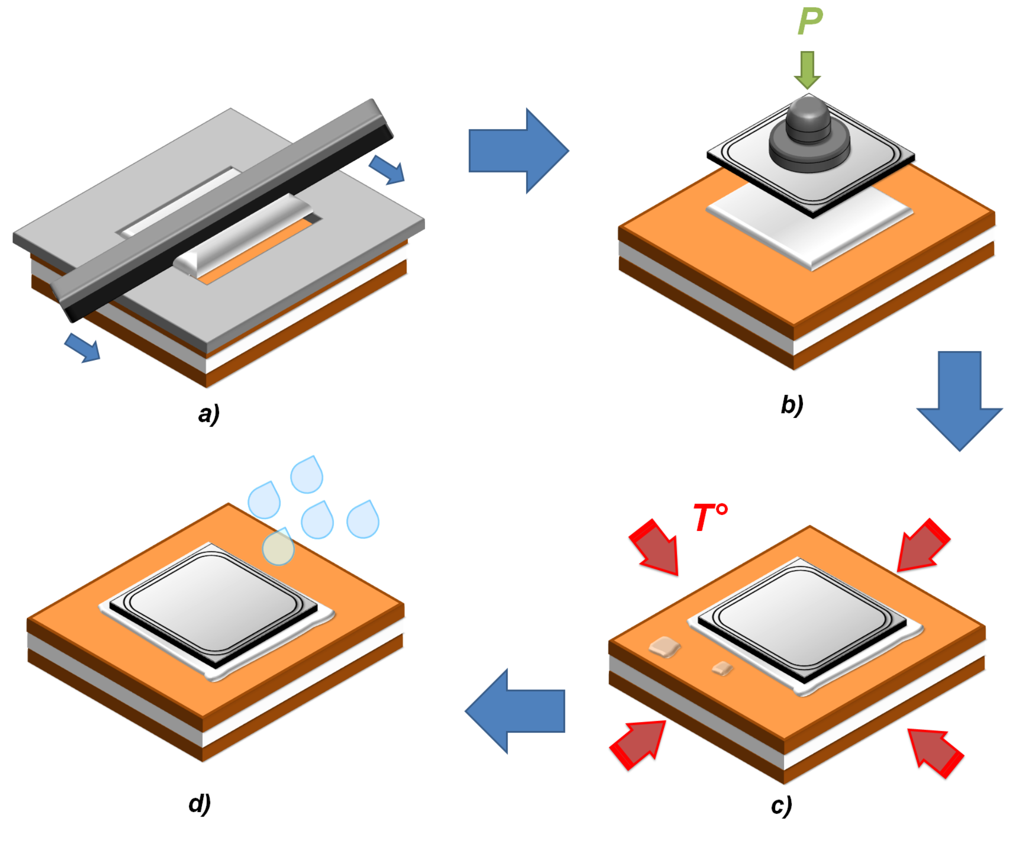


FIGURE 4.2: Solder Process Scheme - a) Printing/dispensing, b) Die placement, c) Vacuum reflow and c) Cleaning.

4.2.2 Sintering

4.2.2.1 Overview

The application of a thermal energy densifies the compact powder, increasing the average grain size. The phenomena occurring during this process are called sintering densification and grain growth [29].

Sintering is a process of metallurgical transformation of powder without state change, allowing the production of a solid mass from more or less fine powder by performing a temperature rise.
The powder is agglomerated into a preform and then heated to a temperature below its melting temperature to provide the cohesion and densification, through bonds creation among grains. The obtained parts have the characteristic of being hard, fragile, chemically inert and porosity controlled [2].

From a physical-chemistry point of view, sintering could be classified as:
Solid phase sintering - The constituents are and remain in solid form. Due to their

high purity grain boundary, this technique is used, for example, in the manufacture of technical ceramics as cutters, dielectric, optical, etc. [30].

Liquid phase sintering - In this case the components, in liquid form, chemically react together due to the effect of an external pressure. This technique also allows the manufacture of technical ceramic (nitride, carbide, borides) that are not feasible in solid phase.

Vitrification or viscous phase sintering - One of the mixture constituent passes into liquid form during sintering. This transition allows reconciliation of grains and, therefore, facilitates the creation of bonds among grains [23].

In this thesis, the assembly technique is based on the same principle of the solid phase sintering (see figure 4.1).

4.2.2.2 Solid phase sintering

The solid phase sintering could be represented as three steps: debinding, sintering and sample expansion. Each step is accompanied by a change in volume of the sintered solid mass.

Debinding - In this step are evacuated various organic compounds, as dispersants, additives or binders present around the sinterable powder. These chemical compounds are evaporated through temperature, according to their time/temperature profile [29]. An excessive debinding speed could cause cracks in the sintered sample due to trapped gas bubbles [31].

Sintering - Sintering takes place, immediately after, in three steps differentiated by the density[4] (or porosity) of the solid mass over time: initial state, intermediate state and final state.
The solid phase sintering is a mechanism in which the combination of powders involves the formation of a grain boundary. It occurs a displacement of matter (and opposed vacancy displacement) from the inside of the grain to the outside, with a progressive approach of the centres of adjacent granules.
As a consequence, sintered materials present excellent mechanical strength properties at high temperatures because of the absence of a secondary inter-granular phase; nevertheless the diffusive mechanism is rather slow and often it requires thermal and mechanical energy (hot pressing) to compensate the activation energy (corresponding to the transfer of matter).

[4]Densification is the physical dimension able to define the quality of sintering. For example: if the density of a sintered sample is closer to 100% (porosity close to 0%) the purity of it is higher, that means that the sample contains less quantity of pores that may limit its properties.

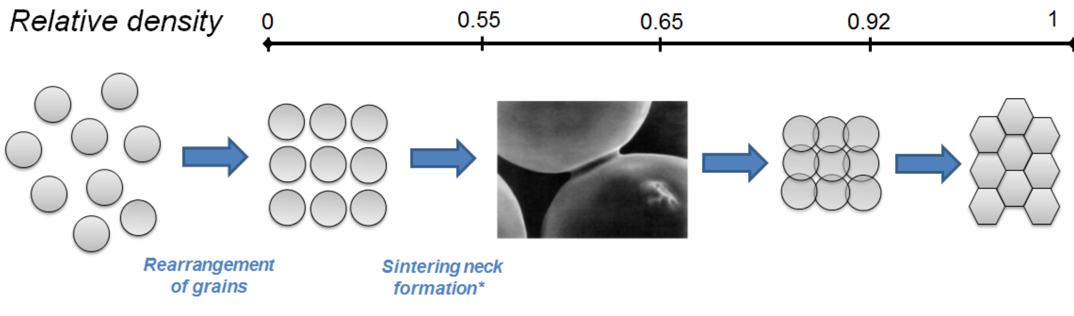


FIGURE 4.3: Scheme of initial stage of sintering process in solid phase (example of sintering "neck" formation from www.turkcadcam.net/rapor/otoinsa/sinterleme.html).

Initially, up to 65% of the theoretical density, a rearrangement of grains starts and the adjacent particles are connected, forming a "neck" of sintering (see figure 4.3). The mechanism of necks formation is due to the different concentration of vacancies and atoms between contact points and interstitial spaces[5]: atoms diffuse from the surface to the interstitial spaces, vacancies diffuse from the interstitial spaces to the grains surface. The necks formation does not determine an effective approaching between the centers of grains, namely it is not a phenomenon that constitutes "densification". It is produced by the transport of material from inside to outsides of grains, by migration of atoms and holes in the grain boundary, by migration of atoms from the center of the grains or by movements of dislocations in the crystal lattice. Recent movements result in a "deformation" of the grains [30].

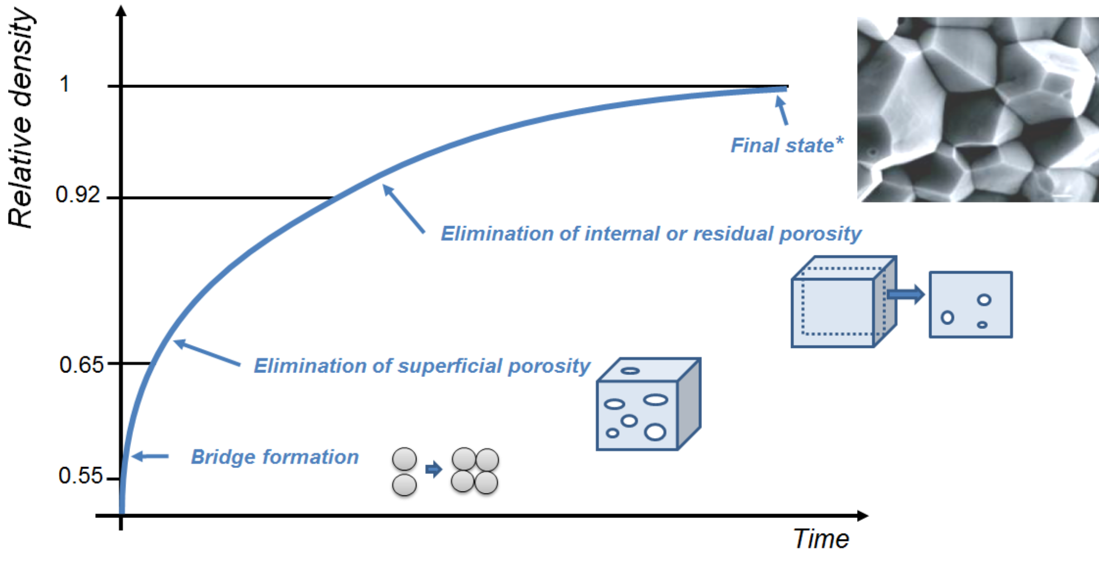


FIGURE 4.4: Density evolution during sintering process in solid phase [2](*from www.grc.nasa.gov).

[5]Interstitial spaces are the areas with a greater concentration of vacancies or holes, of course, given that in these spaces there is no matter; zones of contact are points of concentration of matter

Subsequently, a significant densification (up to 92%) of the theoretical density characterizes the second step of sintering: the completed grains deformation of the starting powder could be displayed as several superimposed polyhedra (see figure 4.4. The porosity is now concentrated at the grain boundaries, thus constituting a network of "channels" for the movement of atoms and/or vacancies. In this situation the residual porosity is shaped by a logarithmic dependence from the sintering time $P = -C \cdot log(t)$ where $C = cte$. The model is valid until the porosity remains "interconnected", or until the network of channels remains defined.

The final stage of sintering corresponds to the isolated pores, mostly at the meeting points between 4 grains. The "absorption" of such residual porosity could not be represented in a precise mode; generally only for a very long sintering time is possible to obtain a full densification. In addition a secondary phenomenon involving the abnormal enlargement of the grains could happen, which may avoid a completed sinterization. The grain boundaries, constituted by a network of small channels, interposed between isolated pores, can move. Large grains (generally more than 6 sides) tend to incorporate smaller grains, and this is thermodynamically favoured by the decrease of the specific surface[6]; residues pores can find themselves "buried" in a single grain which becomes "unalterable" (the movement of the subject and/or vacancies is more efficient at the grain boundaries, where the atomic spacing is irregular).

Dilatation - In some metal alloys, an expansion of the sintered part can occur, during cooling, through a reorganization of the atoms with the creation of new atomic bonds [2].

4.2.2.3 Sintering parameters

The process previously described is controlled by different parameters such as temperature, pressure and the sintering time and particle size.

Temperature - Since diffusion mechanisms are thermally activated, temperature plays a key role during sintering and it could be demonstrated through the Arrhenius law, that relates the temperature and the diffusion coefficient. In a ideal case, the diffusion mechanism Di is equal to the ideal distribution $D0$ of the same mechanism; it is possible to approach to this case increasing the sintering temperature. This provides a faster and also increased sintering kinetics of diffusion.

[6] Remember that every surface corresponds to a certain energy content: large grains, in which the surface/volume ratio is reduced, minimizing the total energy of the system

$$Di = D0 \cdot e^{-\frac{Q \cdot i}{R \cdot T}} \tag{4.1}$$

Where D_i is the diffusion, D_0 is the theoretical diffusion, Q_i is the energy of activation of the i mechanism, T is the temperature and R is the ideal gas constant.

Pressure - The application of pressure during sintering enables bringing particles together, ensuring the cohesion during sintering. In addition, increasing the applied pressure enables a temperature reduction in the process.

Particle size - The particle size of the utilized powder influences the kinetics of the sintering and this could be represented by the similarity law of Herring (see figure 4.5). This law relates the necessary time (t_1 and t_2) to reach the same progress of sintering on two different particle sizes (r_1 and r_2):

$$\frac{t1}{t2} = \left(\frac{r1}{r2}\right)^m \tag{4.2}$$

"m" depends on the type of matter movement and it could variate from 1 to 4.

Particles with small diameter take a reduced time to obtain a given state of sintering progress (if compared with a larger sizes). For example, if it is assumed that $r_1 >> r_2$ ($r_1 = r2 \cdot 10$) and $m = 4$ (diffusive transport to the predominant grain boundaries), is obtained that $t2$ (corresponding to the size of grains $r2$) is ten thousand times shorter than $t1$ (corresponding to $r1$).

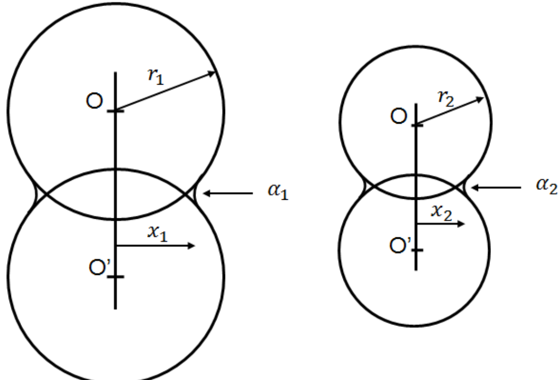


FIGURE 4.5: Scheme of Herring law illustrating the influence of the particles diameter of the powder to be sintered [2].

4.2.2.4 Sintering Process of Silver Powder

The silver sintering, for power electronics applications, was developed by Schwarzbauer Khunert in 1990s, under the necessity to develop seals operating at temperatures greater than $300°C$. Their studies were based on the use of a micrometer silver paste because of the excellent properties of silver (see Table 4.1), but in spite of their superior performance, compared with solder used in the industry, this method was not directly used [23].
Subsequently, as a consequence of the RoHS Directive, sintering was a new approach, appearing as a possible alternative solution for power modules packages.

This process, also called Low Temperature Technical Joining (LTJT) [32], is a method that uses pressurised micrometric silver pasta, comparable to the solid phase sintered under pressure. Therefore it is a combined surface, volume, and grain boundary diffusion process [32].

Sintering combines high performance with an easy handling process and the process flow can be described by four principal steps: paste application, pre-drying, die placement and sintering (see figure 4.6).

Paste application - As soldering process the silver paste is dispensed on the substrate (DBC or Base Plate) using a conventional printing equipment, in order to obtain a regular and controlled surface.
- Equipment: conventional printing equipment

Pre drying - As explained in 4.2.2.2, typically the additives/organic residues are removed by applying heat treatment prior to die placement; therefore a pre-drying step in a convection oven is necessary.
- Equipment: conventional Box Oven

Die placement - Using a die attach equipment, the dies are placed in their corresponding areas. From this step the silver powder starts to be sintered.
- Equipment: die placement with heated substrate holder

Sintering - In this step all the "sandwich" (die + sinter + substrate) is located into the sinter press and the paste is processed under temperature and pressure.
- Equipment: sinter press

Comparing the process above described with soldering (explained in 4.2.1) some advantages are possible to enumerates:
Low processing temperature - The applied temperature is lower compared with the

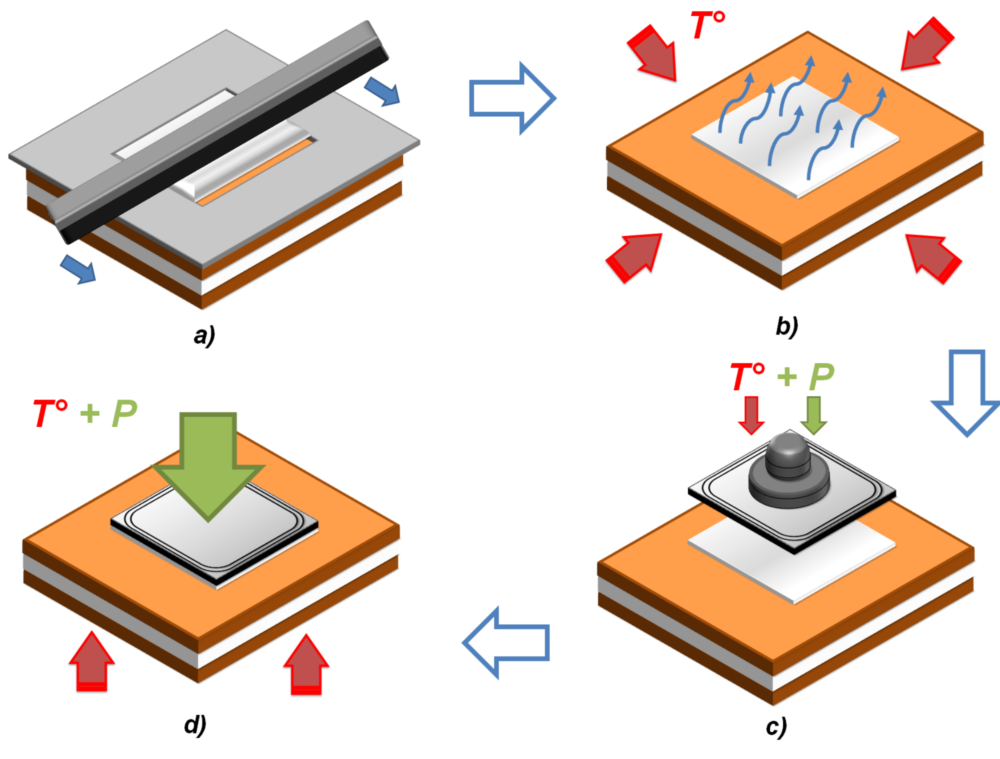


FIGURE 4.6: Sinter Process Scheme - a) Paste application, b) Drying, c) Die placement and d) Pressure Assisted sintering.

soldering. Normally solder process temperature is $250°C$ while the sinter temperature process is $200 - 230°C$.

No flux residues or splattering - Sintering does not have flux residues.

No need of cleaning - Cost and cycle time could be reduced in industrial production.

Layer thickness reduction - Sintered layer thickness is 50% reduced (is 4.5 times thinner than soldering).

No formation of macroscopic voids

In addition, because of the formation of a pure silver compacted layer:

No different CTE with the die Backside Metallization (BSM) is obtained - This reduce the mechanical stress during thermal excursion.

Excellent thermal and electrical properties - See Table 4.1.

Very high melting point ($961°C$) **-** That improves the reliability at high operating temperatures.

Low porosity - Approximately less than 15%. The absence of voids in the die attach reduces the thermal resistance of the power module, improving the thermal dissipation [28].

Since the porosity and the pull strength are a function of applied pressure, both properties can be adjusted to a certain extent. Increasing the porosity, the Young's Modulus

and the pull strength decrease; thereby the impact on the pull strength is higher than on the elasticity.
Low temperature sintered samples, at a given strain, present a damage rate of high porosity layers higher than in low porosity sintered structures. Therefore, for a high reliability (during thermal cycling) a low porosity is preferable [33].

To evaluate the mechanical parameters of a sintered layer, it is possible to measure their porosity by the weighting method. This is extracted from an exact volume and mass measurement:

$$P = 1 - \frac{m_{NTV}/V_{NTV}}{\rho_{Ag}} \tag{4.3}$$

The obtained porosity depends on the process parameter that, if optimized, could lead to a porosity in the range of $10 - 15\%$ [33].

Thermo-mechanical stability - It is also considered mechanical stable because of the homologous temperature is below than 40% [34] [35] [36] [37].
The homologous temperature is considered as the ratio of operating temperature of a material and the melting temperature, considering both temperatures related to the absolute temperature scale.
With an operation temperature of $150°C$, the homologous temperature of SnAg(3.5) with a solidus temperature of $221°C$ is 86%. Even for high-melting solder alloys as AuGe(3), with a solidus temperature of $363°C$, the homologous temperature is 67%. In contrast, the sinter layer Ag exhibits a homologous temperature of only 34% (see figure 4.7).

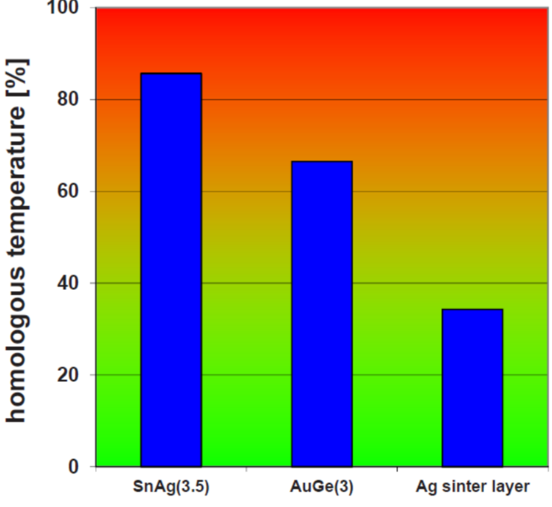


Figure 4.7: Homologous temperature comparison between solders and sinter materials, for an operation temperature of $150°C$ (extracted from [3]).

Therefore,it is possible to classify the mechanical proprieties of the materials as:

Homologous temperature $< 40\%$ - Mechanically stable

$40\% <$ Homologous temperature $< 60\%$ - Material sensitive to strain

Homologous temperature $> 60\%$ - Material unable to bear mechanical stress

4.3 Experimental Procedure

As mentioned, the reliability of a power module can be limited by the ageing, in terms of electrical and mechanical properties of interconnections, such as "Chip to substrate Joint".
For this reason, the experimental part of this chapter is focused on analysing the advantages and disadvantages of the Silver Sintering Process integrated into a standard power module compared to the standard product (solder process).

4.3.1 Silver sintering adapting

In collaboration with HERAEUS Materials Technology the experimentation started adapting their "mAgic paste" material (described on 4.1.2) to their sintering process and into three standard packages: TO-244 as non isolated, MTP and ADD-A-PAK as isolated power modules.
As explained in chapter 2, this packages are composed by 8 diodes with dimension $200x200mills$ or $25mm^2$ in common cathode connection.

Concerning the process, the first step consisted to apply the standard sintering process (explained before in 4.2.2.4 and showed in more details in figure 4.8) in order to define the sinter paste to adapt. To find the best solution proposal, the mechanical characteristics of the sintered layer were evaluated measuring their adhesion force with a "Shear Test".

This particular and renowned technology applied to a non-laboratory sample (not standard dummy), probed that sinterization depends, not only on the process itself, but also on the morphological surface and on metallization thickness of the bottom die. The die shear test of assembled samples outlined a weak die shear strength, less than $2N/mm^2$ and an adhesion breakage on the die metallization was observed.

For this reason the die BSM was checked with a Scanning Electron Microscope (SEM) and analysed by an Auger Electron Spectroscopy (AES)(see figures 4.9 and 4.10).

Looking at Figure 4.10 it is possible to observe that the die shows a rough surface. This is caused by the sandblasting, necessary to reduce the silicon thickness in the die production. Furthermore the AES (see figure 4.9) describes a contaminated surface,

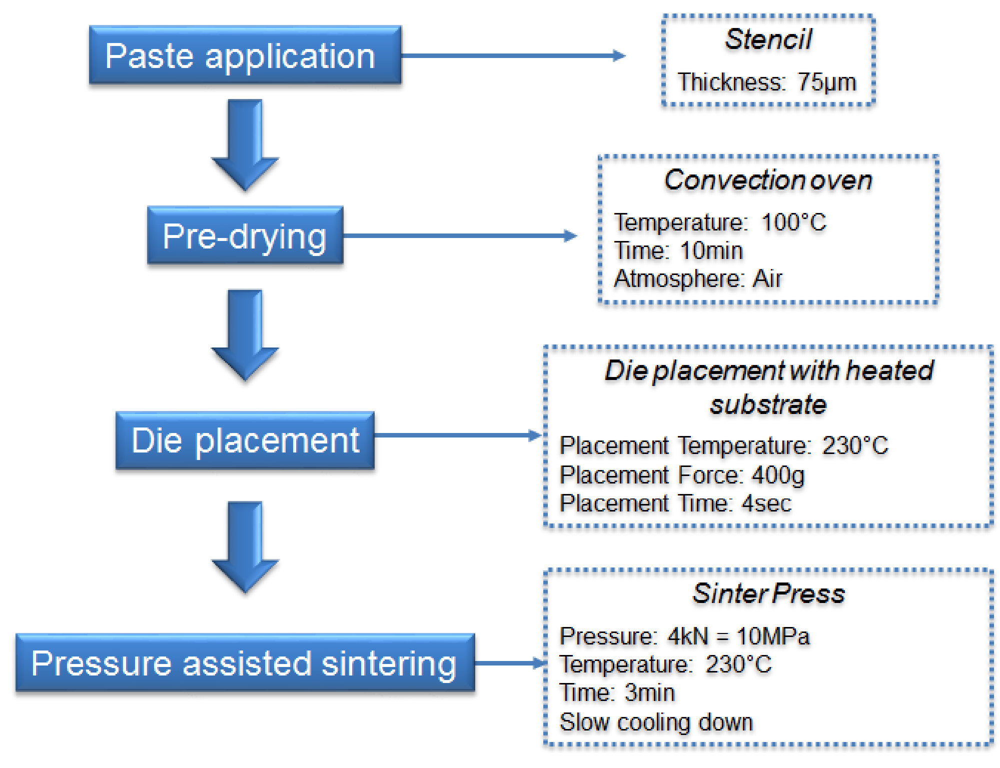
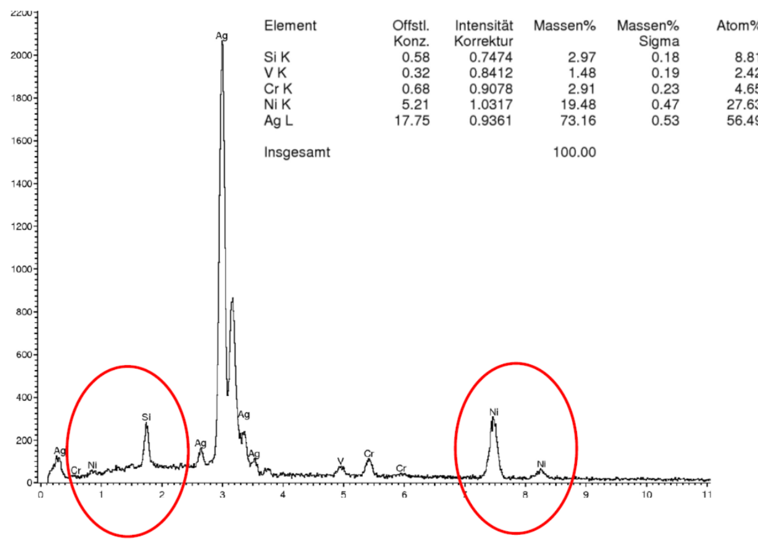


FIGURE 4.8: Description of silver sintering process flow used in collaboration with HERAEUS Materials Technology



Element	Offstl. Konz.	Intensität Korrektur	Massen%	Massen% Sigma	Atom%
Si K	0.58	0.7474	2.97	0.18	8.81
V K	0.32	0.8412	1.48	0.19	2.42
Cr K	0.68	0.9078	2.91	0.23	4.65
Ni K	5.21	1.0317	19.48	0.47	27.63
Ag L	17.75	0.9361	73.16	0.53	56.49
Insgesamt			100.00		

FIGURE 4.9: AES image of Element Analysis of die BSM.

which is not only silver metal but, beside silver, contains an important percentage nickel "Ni". The "Ni", as well as Silicon "Si", seems to be the responsible of the lack of adhesion.

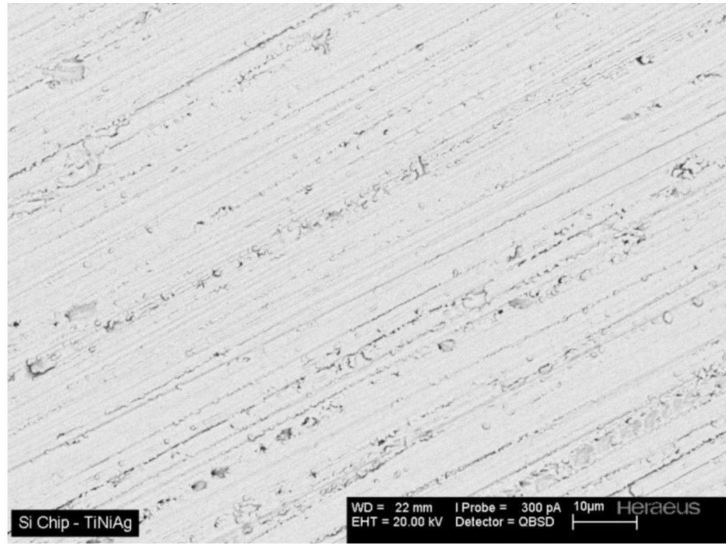


Figure 4.10: SEM images of die BSM (Ag thickness $0.3\mu m$).

Therefore, to prevent this problem and to reach a better smooth die surface, an increment of the thickness of silver metal was considered.
Increasing the thickness of the Ag metallization to $0.6\mu m$, a morphological Energy Dispersive X-Ray (EDX) analysis (see figure 4.11) evidences that the presence of "Ni" and "Cr" was reduced.

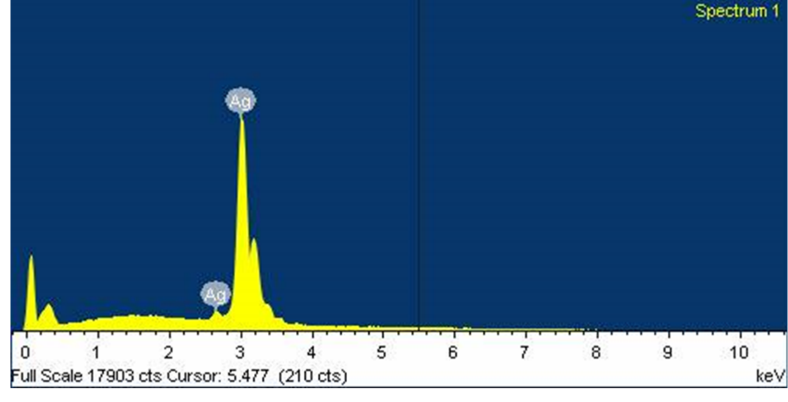


Figure 4.11: EDX analysis of die BSM Ag thickness $0.6\mu m@10KeV$.

Another problem was revealed during the sintering process and this was related to the substrates' materials.
The DBC and Base plate are composed by copper "Cu" metal that could be a relevant obstacle for sintering because, the oxidation of the copper layer, creates a weak silver-to-copper bond. Silver paste requires a noble interface for reliable bonding, as e.g. Ag,

NiAu or Pd [38].
As a consequence, to avoid this phenomenon, two alternatives were taken (Ag and NiAu) and new samples were sintered with following substrates:

MTP (package isolated)
- DBC "A" metallized Ni electroless $3 - 7\mu m$ + Au flash $0,03 - 0,13\mu m$,
- DBC "B" metallized Ag electroless $0,1 - 0,3\mu m$,

ADD-A-PAK (package isolated)
- DBC "A" metallized Ni electroless $3 - 7\mu m$ + Au flash $0,03 - 0,13\mu m$,
- DBC "B" metallized Ag electroless $0,1 - 0,3\mu m$,

TO-244 (package non isolated)
- Base plate "Ag" $2 - 3\mu m$ galvanic silver.

4.3.2 Evaluation of mechanical adhesion

The result of a sintering process can be initially evaluated by a mechanical point of view.

Therefore, to evaluate the adhesion force of the sintered layer, a shear test was leaded on non isolated and isolated samples (TO-244 and MTP packages).
One measure was realized after the sintering process and the second one after a Temperature Cycling Test (TCT) [39].

For the TCT, the thermal system was setting at $T_{min} = -45°C$ to $T_{max} = +150°C$ and $t = 30min$ for each temperature. The following table shows the shear test values obtained before and after the TCT:

	Die Shear Test Results $[N/mm^2]$	
	After sintering process	After TCT (500 cycles)
MTP DBC "A"	> 30	> 60
MTP DBC "B"	> 40	
TO-244 sintered	> 40	

TABLE 4.2: Die shear test results of sintered samples, before and after 500 cycles of TCT.

Table 4.2 shows an increased die shear strength after 500 temperature cycles. That could be possible because, as mentioned in 4.2.2.2, sintering process is positively influenced by temperature.
In some cases, it was impossible to obtain a lecture of shear strength value due to die breakage (see figure 4.12).

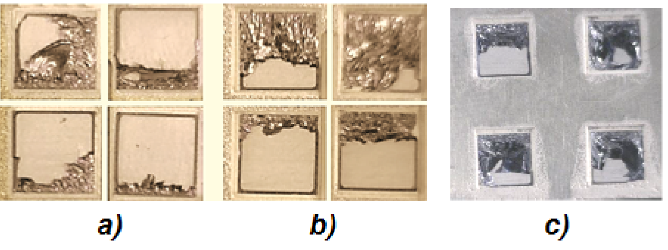


FIGURE 4.12: Some examples of broken dies after shear test at TCT @ $-40/+150°C$, (a) MTP DBC "A" and (b) MTP DBC "B" and (c) TO-244 Base Plate "Ag".

4.3.3 Power Cycling capability

In the industrial production and laboratory studies, PC capability is applied in order to evaluate the reliability of the power module and to observe the morphological ageing of the internal interconnections.

As explained in chapter 3, Long Power Cycling Test (PCT) intends to simulate a real application being a destructive test. Providing a thermal excursion by current, during a long time cycle, a worsening of the module is observed.

In Long PCT (1 to 15min), different from the Short PCT (1 to 15sec), where the thermal stress is localized on the top of the die, the thermal excursion is transferred to the entire power module. Therefore, due to the mismatch of CTE, a thermo-mechanical stress is induced, degrading the joint's interface.

Given that the interest to induce failure mode is centred to obtain "Chip to substrate joint" fatigue, the set-up conditions, following the **International Standard International Norm IEC 60749-34**, were considered in order to define the power module lifetime and to understand their ageing process.

Table 4.3 shows the fixed set-up parameters to obtain a $\Delta T_c \simeq 100°C$ during $t_{cycle} = 10min$. The power module lifetime will be observed comparing the sintered packages (MTP DBC "A", MTP DBC "B", ADD-A-PAK DBC "A", ADD-A-PAK "B" and TO-244 Sintered) with their equivalent soldered packages, called MTP Standard (DBC "Cu" + solder layer) , ADD-A-PAK Standard (DBC "Cu" + solder layer) and TO-244 Standard (Base Plate "Cu" + solder layer).

Packages	I_{test}	t_{on}	t_{off}
MTP	$140A$	$4min$	$6min$
ADD-A-PAK	$70A$	$3min$	$7min$
TO-244	$125A$	$5min$	$5min$

TABLE 4.3: Short Power Cycling Test conditions utilized to evaluates the power modules lifetime.

The different set-up parameters depend on the involved packages structure (their capability to heat and to cooled).
For example: ADD-A-PAK requires less current than the others two (MTP and TO-244) because the DBC is directly in contact with heat-sink; on the other hand, TO-244 and more MTP require higher current, because structure is formed respectively by DBC and DBC + Base Plate between die and heat-sink.

During the test, the thermal resistance junction-case (Rth_{j-c}) was monitored to establish that all devices are being stressed and to detect the lifetime of each single sample (when $\Delta Rth_{j-c} > 100\%$).
Tables 4.4, 4.5 and 4.6 show the number of reached cycles with each kind of package.

	MTP (Isolated)		
	DBC "A"	DBC "B"	Standard
Number of cycles	11300	9500	11280

Table 4.4: Power cycling Test results - MTP results (number of cycles passed before to reach $\Delta Rth_{j-c} > 100\%$).

	ADD-A-PAK (Isolated)		
	DBC "A"	DBC "B"	Standard
Number of cycles	6600	7300	9700

Table 4.5: Power cycling Test - ADD-A-PAK results (number of cycles passed before to reach $\Delta Rth_{j-c} > 100\%$).

	TO-244 (Non Isolated)	
	Sintered	Standard
Number of cycles	4000	5000

Table 4.6: Power cycling Test - TO-244 results (number of cycles passed before to reach $\Delta Rth_{j-c} > 100\%$).

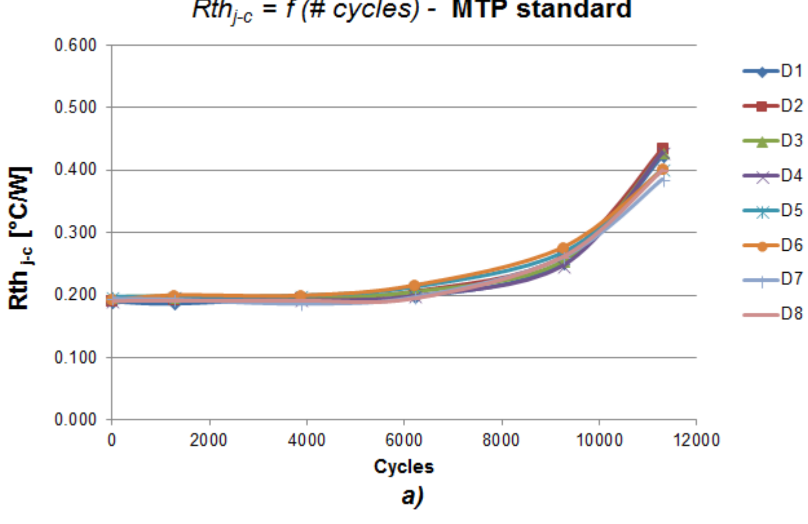
Looking quickly the numbers of reached cycles, a faster conclusion might be realized: sintering seems not improving the reliability of the stressed samples.

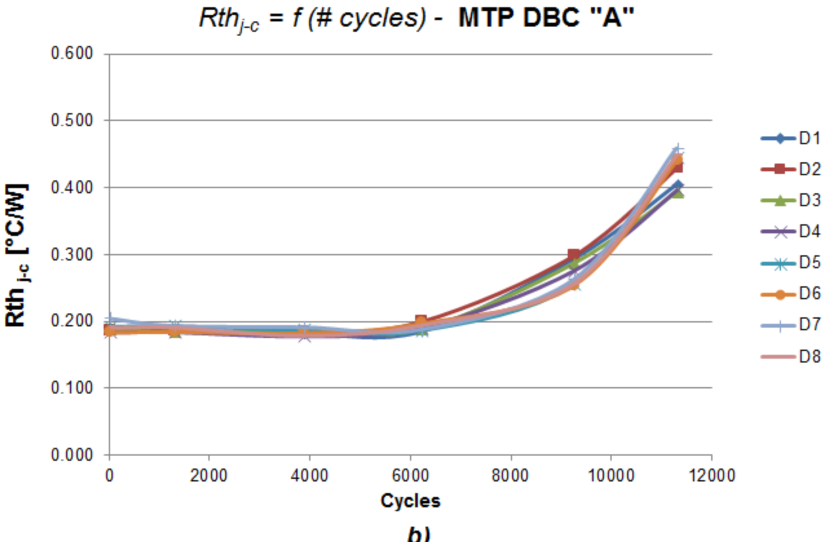
4.3.3.1 Rth_{j-c} measures

Separating isolated and non isolated power modules, the interest is to represents the Rth_{j-c} trend in function of time (or number of cycles).

MTP (Isolated) - Figure 4.13 shows the measured Rth_{j-c} of three different isolated power modules during the time.

Observing the graphs, it is possible to recognize that the thermal resistance remains almost constant up to a large number of cycles (approximately < 6000 cycles). Few cycles





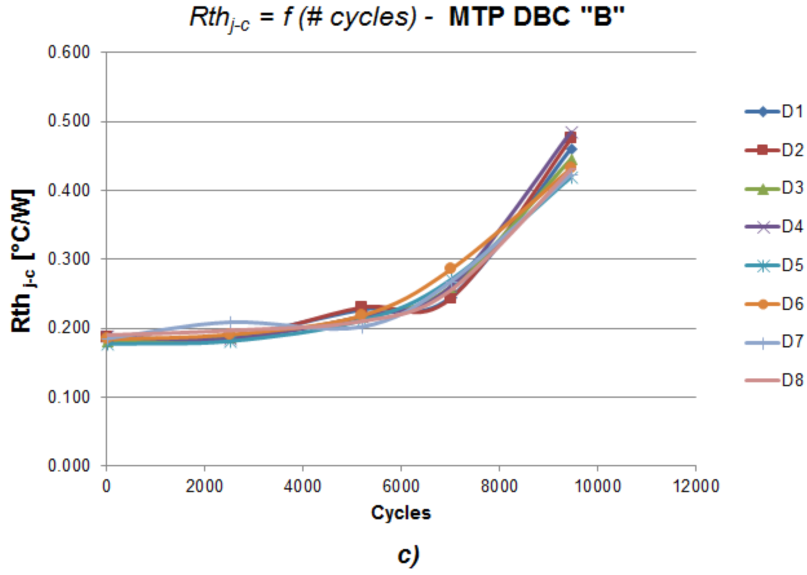


FIGURE 4.13: Rth_{j-c} measures of MTP (a) Standard, (b) DBC “A” and (c) DBC “B”, during Long Power Cycling Test ($@\Delta T_c \cong 100°C$).

after, the MTP DBC "B" case grows up quickly exceeding the 100% at $\simeq$ 10000 cycles. Others two cases (MTP DBC "A" and Standard) Rth_{j-c} grows up later, exceeding the 100% at $\simeq$ 11000 cycles.

TO-244 (Non Isolated) - The figure 4.14 shows the measured Rth_{j-c} on the non isolated power modules proposed.

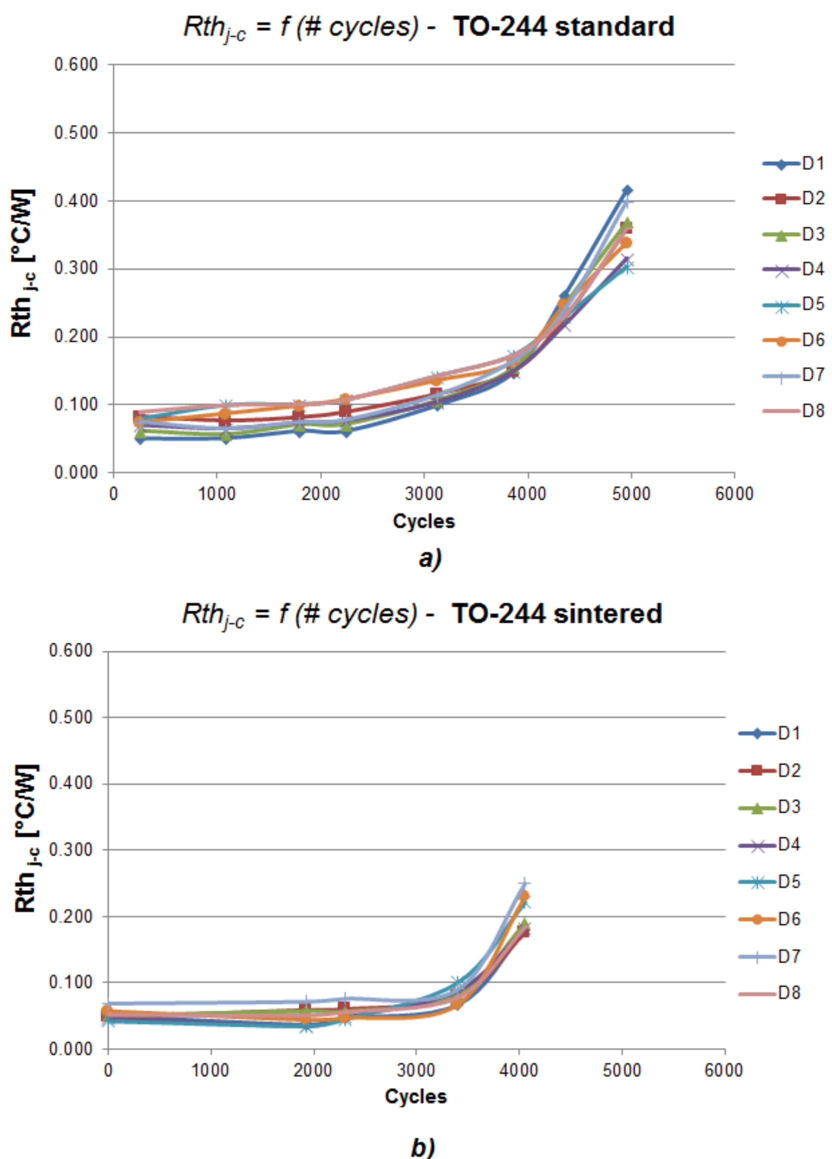


FIGURE 4.14: Rth_{j-c} measures of TO-244 (a) Standard and (b) Sintered during Long Power Cycling Test (@$\Delta T_j \cong 100°C$).

In this comparison the thermal resistance remains almost constant up to approximately 3500 cycles). Few cycles after, in both cases Rth_{j-c} grows up quickly exceeding the 100% at > 4000 cycles.

ADD-A-PAK (Isolated) - The figure 4.15 shows the measured Rth_{j-c} of the others three different isolated power modules during the time.

In this case, the thermal resistance remains almost constant up to approximately < 5000 cycles. Few cycles after, the ADD-A-PAK DBC "A" case grows up quickly exceeding the 100% at $\simeq$ 6000 cycles. The others two cases (ADD-A-PAK DBC "B" and Standard) Rth_{j-c} grows up later, exceeding the 100% at $\simeq$ 7000 and $\simeq$ 9000 cycles respectively.

Summarizing, it is important to note, that sintering improves the thermal characteristics of the power modules. Namely, looking the Tables 4.7, 4.8 and 4.9 it is possible to see that the Rth_{j-c} initial value of sintered modules (measured before to PCT) is lower than the soldered ones. This is clearly evidenced in the TO-244 packages, by the absence of DBC, where the sintered Rth_{j-c} value is nearly a half of soldered.
However, in terms of reliability, sintering technology did not give an improved final result, there is not a significant difference if compared to the standard soldering sample.

	MTP (Isolated)		
	DBC "A"	DBC "B"	Standard
Rth_{j-c} $[°C/W]$	0.189	0.184	0.193

TABLE 4.7: Rth_{j-c} comparison between sintered and soldered MTPs power modules before to PCT.

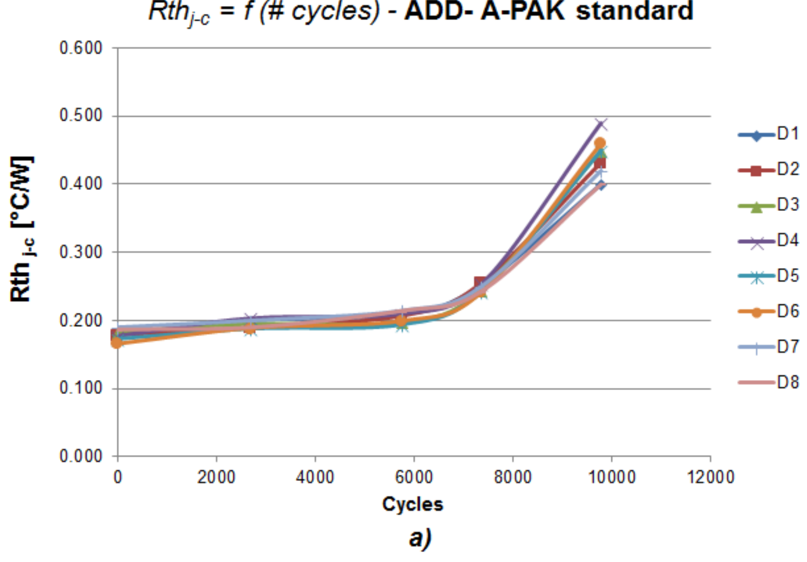
	ADD-A-PAK (Isolated)		
	DBC "A"	DBC "B"	Standard
Rth_{j-c} $[°C/W]$	0.173	0.176	0.179

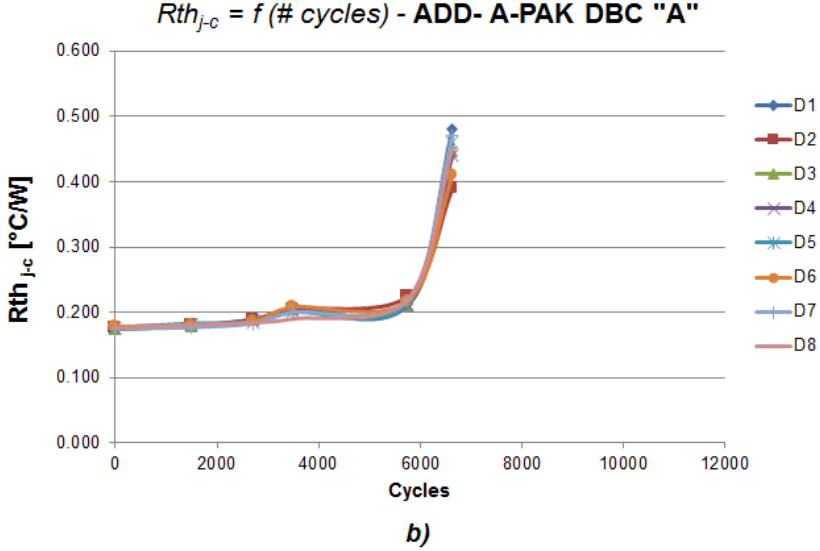
TABLE 4.8: Rth_{j-c} comparison between sintered and soldered ADD-A-PAK's power modules before to PCT.

	TO-244 (Non Isolated)	
	Base Plate "Ag"	Standard
Rth_{j-c} $[°C/W]$	0.049	0.084

TABLE 4.9: Rth_{j-c} comparison between sintered and soldered TO-244's power modules before to PCT.

Next step consists to realize a failure analysis in order to understand, into detail, the internal degradation process during the test.





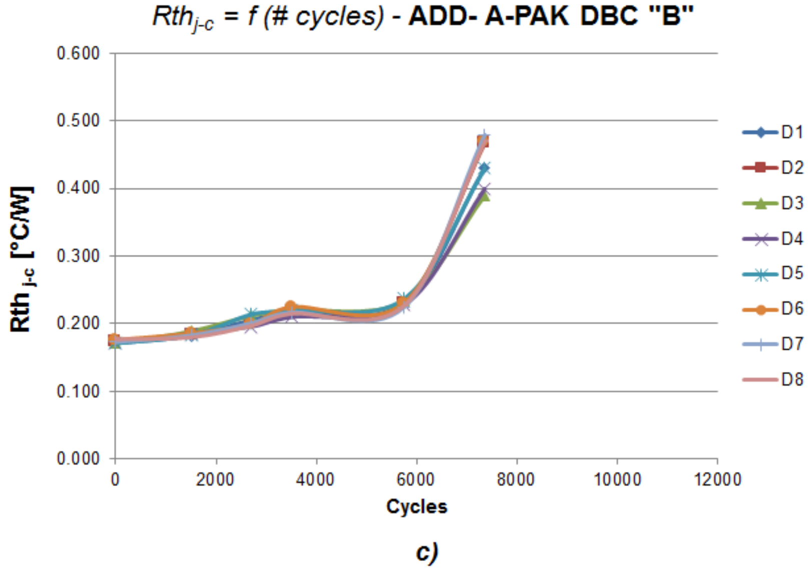


FIGURE 4.15: Rth_{j-c} measures of ADD-A-PAK (a) Standard, (b) DBC “A” and (c) DBC “B”, during Long Power Cycling Test (@$\Delta T_c \cong 100°C$).

4.3.4 Failure Analysis (F.A.)

Due to the interdependency of the failure modes that could happen during PCT, a careful failure analysis[7] was done.

4.3.4.1 MTP (Isolated)

Before opening the power modules, from external visual inspection was observed that some pins were detached from the DBC.
This was noted more frequently on the silver metal finishing samples (DBC type "B").

Continuing the failure description, all the samples were observed with the C-Mode Scanning Acoustic Microscopy (C-SAM) in order to see the states of DBC/Base plate and die/DBC layers.
Figure 4.16 shows that the status of the internal metal layers is critical:
- DBC/Base Plate: all the modules had anomalous morphology of the solder, probably due to solder fatigue or delamination.
- Die/DBC: again all the modules presented a stressed layers, but the morphologies between soldered and sintered were different. While soldered seems "fatigued", sintered seems "detached". Furthermore this was more pronounced on DBC type "A" than DBC type "B" (probably because there are 2000 cycles of differences).

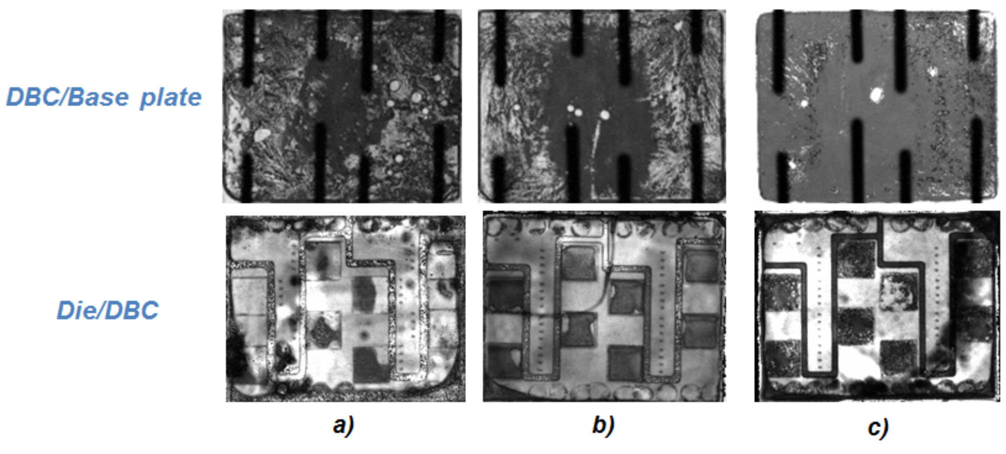


FIGURE 4.16: C-SAM images of DBC/Base plate and Die/DBC joints of (a) DBC type "A", (b) DBC type "B" and (c) Standard.

Therefore, using a stereomicroscope (see figure 4.17) all the structures showed:
- Pin-Out: all of soldered interface between pins/substrate were fractured and fatigued in all of three cases.
- DBC/Base Plate: the anomalous morphology was due to solder fatigue.

[7]For more information about the utilized instrumentation to realize the F.A. please see Appendix B

- Die/DBC: on the soldered samples was confirmed the presence of solder fatigued and in the case DBC type "B" not signal of stress was found. Regarding the DBC type "A", the tilt microscope analysis showed that the sinter was delaminated from diode.
Even if it is not evident from the picture, because of the limited image resolution, some diodes were detached from sinter, due to the device handling during the experimental process; nevertheless sintering remained still attached on the DBC.

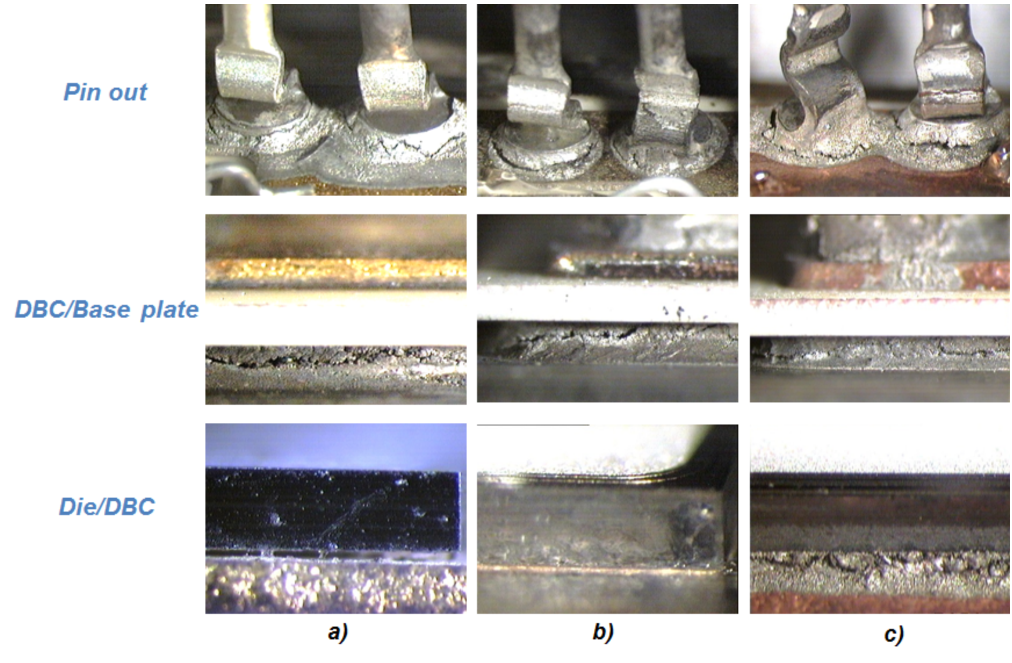


FIGURE 4.17: Tilt microscope analysis of (a) DBC type "A", (b) DBC type "B" and (c) Standard.

Consequently, in order to understand the origin of this detachment SEM images and EDX analysis were done on both interfaces: sintered layer on the substrate and the diode backside.
Figures 4.18 and 4.19, revealed that "Si", "Ni" traces and "Ag" on the sintered were found, but on the diode backside "Ag" remained only on edge of the diode and "Cr", "V" and "Ni" were found in the rest of the area. This explains that the delamination was produced between the "Ni/Ag" BSM of the diodes[8], while the "Ag" metal remained attached on the sintered layer.

The presented delamination could be a consequence of an oxidation of the "Ni" layer, because this phenomenon could be produced at high temperature if sintering process is not under controlled atmosphere (N_2).
Indeed, some researchers published that the inclusion of (N_2) on the process can increase

[8]The die BSM, in this diodes, is composted by Cr/Ni/Ag

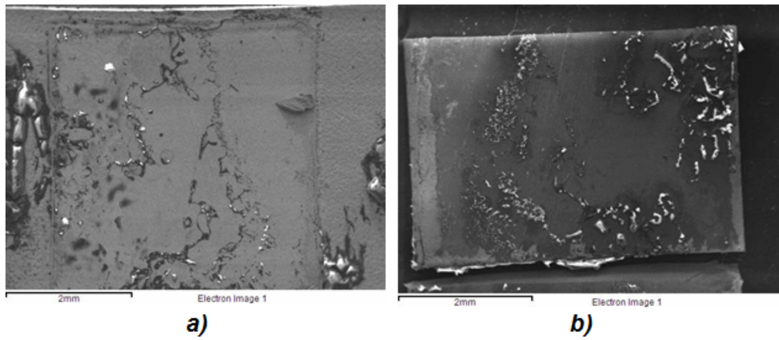


FIGURE 4.18: DBC type "A" - SEM images of (a) Sinter layer on substrate after diode removing and (b) Die backside.

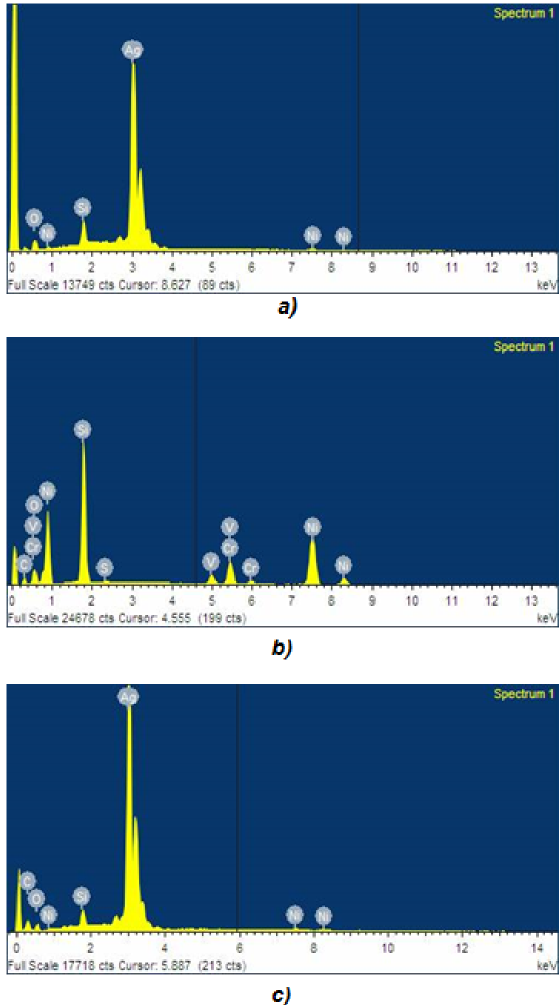


FIGURE 4.19: DBC type "A" - EDX analysis of (a) Sinter layer on substrate after diode removing, where only silver was found and back side die: (b) V, Cr and Ni were found on the centre area and (c) Ag and Ni on the border.

the homogeneity of the sintered layer (if compared with sintering in air); but in terms of reliability this was under test [32].
Hence, a solution proposal could be to realize the sintering process under a controlled atmosphere or study new possibilities to perform news combinations of BSM (as for example Ti/Ni/Ti/Ag), differentiating BSM for soldering and BSM for sintering.

On the other hand, putting together the table 4.4 and the figure 4.16 it is possible to observe that the DBC type "A" was more reliable than "B" and the sinter interfaces were more stressed too. Indeed, the reached number cycle for the DBC type "B" was 2000 cycles less than "A", the DBC type "B" presented an earlier and higher quantity of detached pin-out than "A".
An EDX analysis on the solder residue @5KeV, evidenced a poor presence of silver material on the DBC type "B" surface. Hence, since this type of DBC was finished only with "Ag", id est it did not have a "Ni" blocking layer between "Cu/Ag" as in thee gold case ("Cu/Ni/Au"), it is could be possible assuming the possibility that silver could have migrated/diffused into the copper layer.
In addition, considering that the fatigue propagation in a rectangular area is normally from the corner to centre, the thermal contact under the pins location was affected early by the fatigued DBC/base plate layer.

4.3.4.2 TO-244 (Non isolated) and ADD-A-PAK (Isolated)

Analysing these similar packages (because there is one joint, die/DBC or die/Base plate and the pin-out in not soldered to the substrates) the C-SAM images (see figure 4.20 and 4.21) and a subsequently the de-boxing showed a situation as the MTP case. Namely, on standard samples the solder layer was fatigued, while on the sintered samples die detachment on all the cases was found.

In the case of TO-244 and ADD-A-PAK the delamination (between the diode "Ni/Ag" metallizations, remaining the "Ag" metal attached on the sintered layer), appears on both groups (type "A" and "B"), as in the MTP case.
Therefore it is possible to observe that, for sintering, silver metallization is better and more reliable than gold finishing. In effect, the failure mechanism on MTP type "B" was caused by the early pin out solder fatigued.

Finishing, figures 4.20 and 4.21 evidenced that, with sintering it is possible to control the "Chip to substrate joint" area, while it is not possible with soldering, because an uncontrolled solid-liquid transition intervenes.

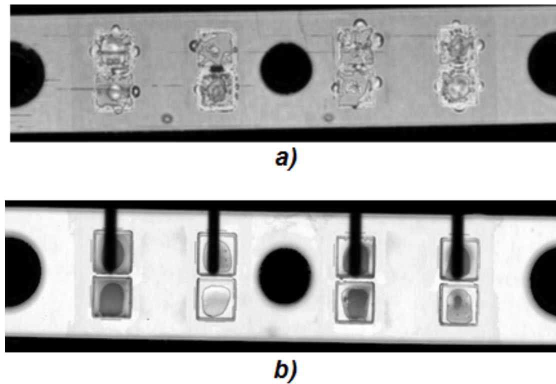


FIGURE 4.20: C-SAM images of die/Base plate joint of (a) TO-244 soldered and (b) TO-244 sintered.

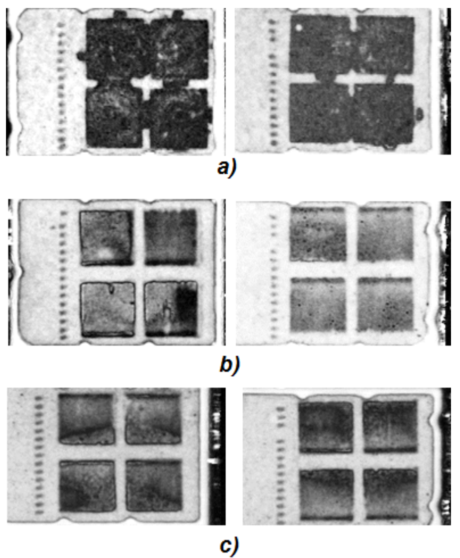


FIGURE 4.21: C-SAM images of die/DBC joint of (a) Standard, (b) DBC type "A" and (c) DBC type "B".

4.4 Evaluation of Electrochemical Migration (ECM)

The introduction of the silver sintering process into high power electronics noticeably improved the characteristics and reliability of power modules [28].

At the same time, the sintering process remains not completely optimized because of the still unclear mechanism that occurs between the material surfaces. Indeed, up to now, most published articles and papers analyze one of the most critical points of silver material: Ag electrochemical migration on sintered silver, focused only on electrodes or dummies [40][41][42][43]. For the first time, this work presents the possibility of detecting silver migration under wet, voltage and low temperature condition into a completed isolated power module.

Furthermore, the solder layer substitution with a pure Ag sintered layer increases the risk of obtaining metal migration. As a consequence, this part evaluates the possibility of generating and avoiding Electro-chemical Migration (ECM), when sintered silver is implemented as a die attach, compared to a standard solder layer SnAg(3.5).

4.4.1 Electrochemical migration phenomenon

This phenomenon is described as the growth of conductive metal filaments (called also dendrites) between two conductors, under the presence of an electrolytic solution (as humidity) and an applied electrical field (DC voltage bias) [40][44][45].

Observing the schematic diagram in Figure 4.22, the ECM can be described in three steps: the electrolytic solution, involving the two electrodes, creates a path and causes metal dissolution on one of the two conductors (with higher electrical potential). It transports the produced metal ions to the opposite bias electrode (lower electrical potential) and the recurring ion deposition forms the so-called dendrites.

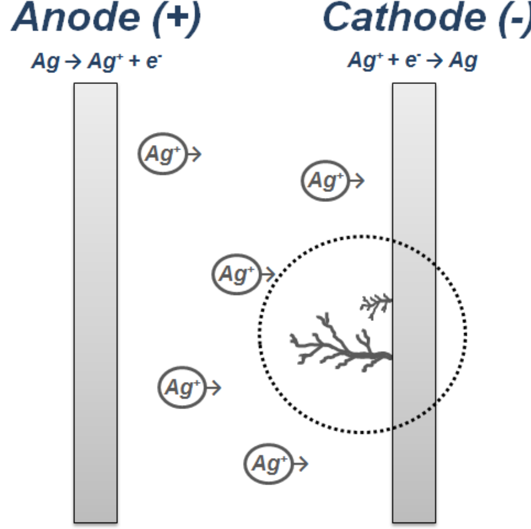


FIGURE 4.22: Silver migration schematic diagram.

The idea behind our work was to study the behavior of a diode, considering the blocking current function, in reverse direction, with a pure silver layer (100% Ag). Under reverse bias and relatively high humidity (HR), a dendrite bridge formation could be induced. Figure 4.23 represents this particular situation, where the Ag ions (from the silver layer) could deposit on the top of die, creating dendrites on the bottom die. Consequently, the leakage current increases until it short circuits the device due to the metallic bridge.

4.4.2 Test without environmental isolation

Firstly, defining time-to-failure (TTF) - the time necessary to create a metallic short circuit, between two conductors [45], it is necessary to study the relationship between TTF with the reverse voltage bias applied without environmental isolation.

Hence, three different structures were defined to compare the behavior of sintered and soldered layers:
- 8 soldered dies on Cu DBC (standard),
- 8 sintered dies on Ag finished DBC,
- 8 sintered dies on Au finished DBC.

Modules were tested and observed under the follow test conditions:
$RH = 98\%$, $T \approx 40°C$ and $V_{Reverse} = 20V$ and $100V$.

In reverse bias, (see Figure 4.22 and 4.23) it is expected that metal ions are removed from the Anode (bottom side of the die) and metal dendrites grow on the Cathode (top die) in the direction of the Anode.

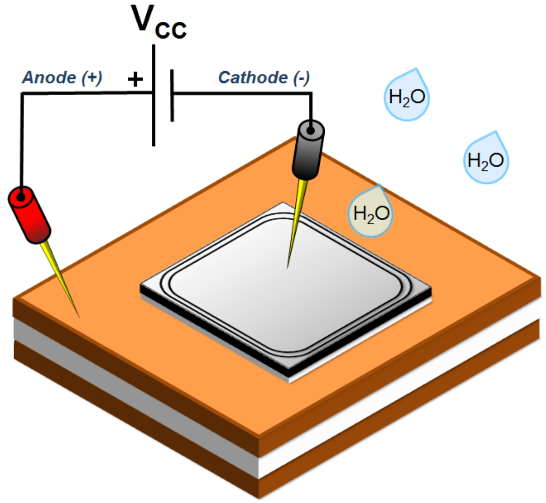


FIGURE 4.23: Scheme of used method to study the dependency of TTF and reverse bias applied on three different structures without gel potting.

On the test, it was observed that when applying $20V$ on the structure, the measured TTF was approximately $2 - 3minutes$. However, when $100V$ were applied, the TTF was drastically reduced ($TTF < 1minute$). Logically, this can be explained by the fact that an increased voltage bias applied on the electrodes causes an increased movement of metal ions (transported through the electrolytic solution). Therefore, the time necessary to create a metal bridge is reduced.

Micro-structural analysis

A micro-structural analysis, employing a SEM-EDX analysis is necessary in order to observe and characterize the founded dendrites.

Figure 4.24 shows the metal bridge created on the die topside. Furthermore, SEM-EDX analysis revealed the metal composition of the dendrites. For example: Cu material due to migration of Cu DBC, Cr from die back metal and some solder material (Sn/Ag) from the backside to the die top-side.

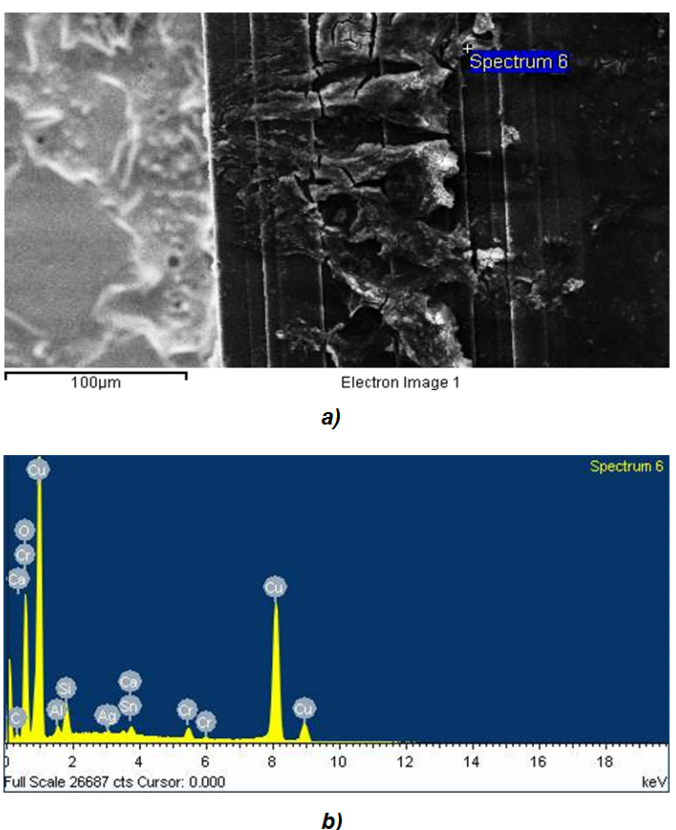


FIGURE 4.24: Standard structure - Copper DBC and solder die attach: (a) SEM images of silver dendrites around the die top, (b) EDX analysis shows dendrites with Cu/C/Ca/Cr/O/Al/Si/Ag/Sn composition.

Figure 4.25 and 4.26, instead, show the metal dendrites considering silver sintering die attach. In this case, all modules had foreign material residue in the termination area. Furthermore, SEM-EDX analysis revealed a high presence of Ag material due to the sintered layer used as die attach.

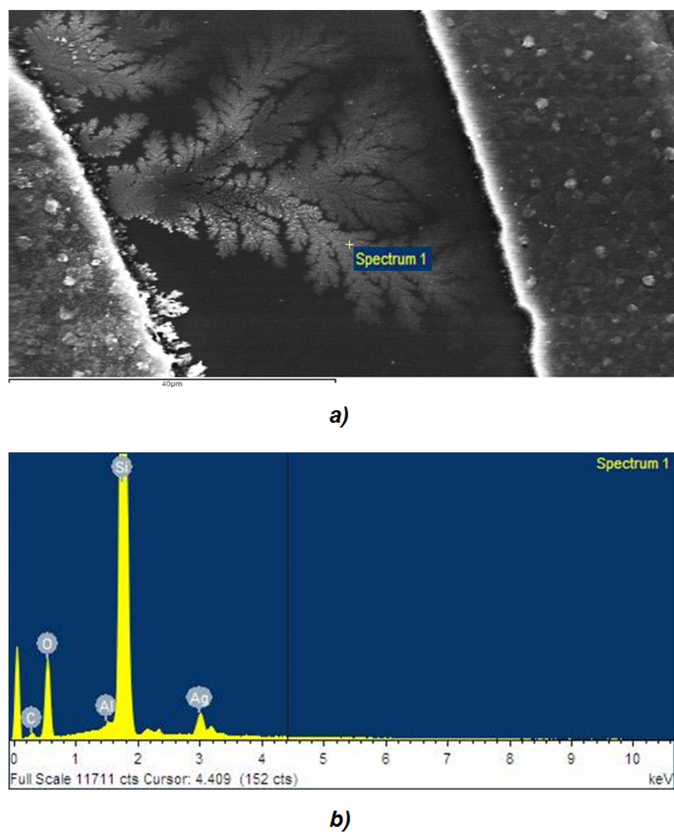


FIGURE 4.25: Sintered structure - DBC Ag finishing and Ag sinter die attach (a) SEM images of silver dendrites around the die top, (b) EDX analysis shows dendrites with Ag/C/O/Al/Si material composition.

4.4.3 Test on performed power module

The second part of the experimental part consisted in studying the isolation capability of the silicone gel, in order to avoid the growth of dendrites. Hence it was necessary to complete the power module (see Figure 4.27), boxing the DBCs and filling in the structure with silicone dielectric gel - SYLGARD 527.

This kind of gel, produced by Dow Corning[9], is a bi-component material, with excellent dielectric properties, low viscosity and adapted to industrial production. In addition, it provides long term sealing against moisture and atmospheric contaminants.
Therefore, all the structures were completed and a new test at the follow conditions was carried out: $RH = 98\%$, $T \approx 40°C$ and $V_{Reverse} = 100V$ for $1000hs$. Unlike the previous test, the $I_{Leakage}$ was monitored over time in order to find the ECM phenomenon and to define TTF.

As a result, after $1000hs$, no leakage current variation was found. Moreover, considering the strong relationship between $I_{Leakage}$ with dendrites growth (as shown in the section

[9]For more information: http://www.dowcorning.com

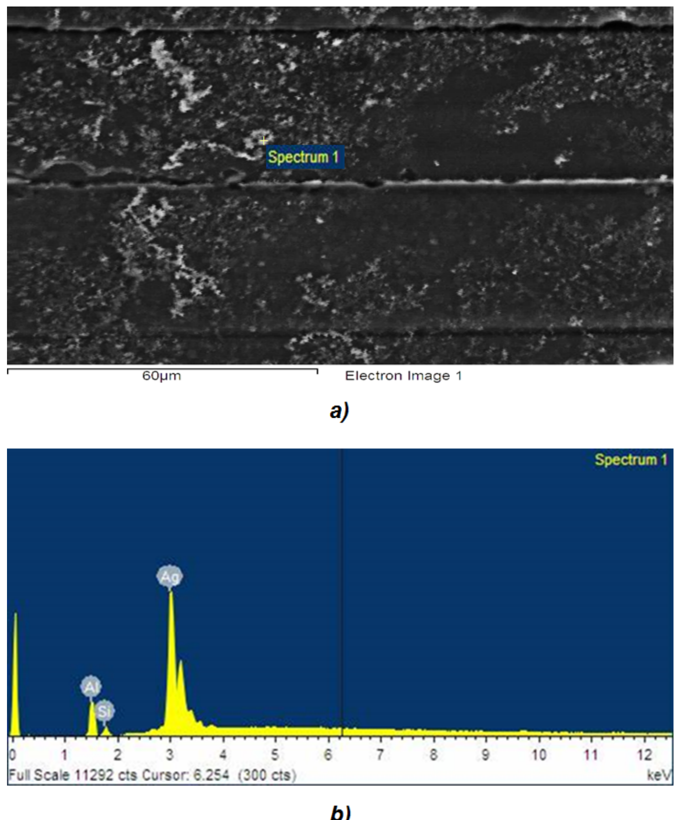


FIGURE 4.26: Sintered structure - DBC Au finishing and Ag sinter die attach (a) SEM images of silver dendrites around the die top, (b) EDX analysis shows dendrites with Ag/Al/Si composition.

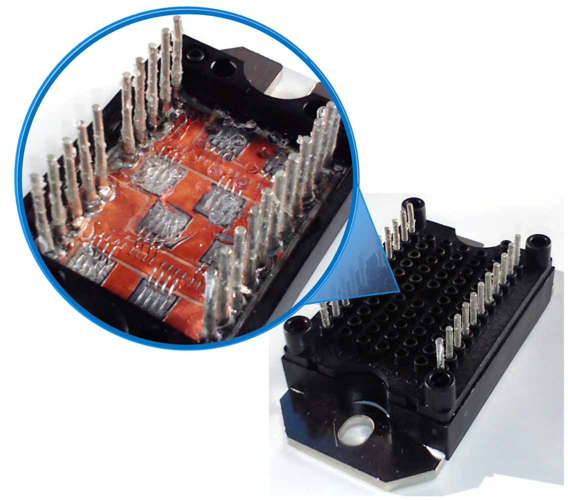


FIGURE 4.27: Completed power module.

4.4.2), it is possible to see that SYLGARD 527 demonstrates an excellent capability to avoid ECM phenomenon on both cases: silver sinter layer die attach and solder layer SnAg(3.5).

Nevertheless, in a complete power module, the possibility to conduct a micro-structural analysis, to guarantee the absence of dendrites on the die level, is still under optimization. Chemical decapsulation by etching process is the most popular technique, but it presents a high risk of dendrites removal. Alternative ways to decapsulate are now under study.

4.5 Conclusion

To summarize, the process sintering adapted to dies (not dummies) has guaranteed an adhesion value $> 40N/mm^2$. This was encouraging because this value reflects data from bibliography, for both sintered and soldered structures. These analysis were supported by shear test, AES spectroscopy, SEM microscopy and EDX.
At the same way, the reached number of cycles of sintered structures is comparable to soldered ones.
On the other hand, a significant point to underline is the decrease thermal resistance value of sintered modules; in particular in the non isolated one (without DBC) a decrease of 50% was measured compared with the soldered one.

Delamination effect, visualized through C-SAM microscopy en EDX, produced on the sintered devices could be explained by an uncontrolled process atmosphere, causing the "Ni" oxidation.

Finally, an other important goal was the silver ECM prevention, detected by EDX, thanks to the introduction of a silicon dielectric gel into the box.

Chapter 5

Bond Connection

Power modules technology is evolving towards higher power densities [46][24]. Longer module lifetimes are required, so the improving of interconnection technologies becomes a focus of study and innovation [47].

Consequently, this thesis work has been focused on the experimental study of power modules **Bond Connection** and first results are presented in this chapter. This process includes the evaluation of possible failure modes, classifying them and finding the appropriate solutions. For instance, one failure mode in these interconnections is the degradation of heavy wire bonding (foot cracks, heel-cracks, lift off and fractures).

In collaboration with HERAEUS Materials Technology[1], various types of wire bonding materials (5N-H11, 5N-H11-CR and CucoreAl) will be employed into an isolated power module and investigated using thermal stress (Short PCT and TCT) and microstructural analyses.

5.1 Heavy wire bonds materials

Considering the interconnection technologies in power electronic devices, the role of heavy wire bonding is very important. They connect different parts within the module, i.e. DBC to DBC, DBC to chip and DBC to frame. Thereby, they play a significant function in order to improve the overall module performance in terms of reliability and power capability.

Today, new combination of materials and technology processes are used to produce better wire bondings, upgrading the mechanical and electrical characteristics.

[1]For more information: http://www.heraeus.com

Therefore, this chapter is oriented to study and compare different materials, in order to improve the wire bonding actually presented on the described power modules.

In power modules packages, wire diameters start from $125\mu m$ ($5mils$), for gate control for example, up to $500\mu m$ ($20mils$) for power control. Furthermore, the selected diameter depends principally to the wire function, the available wire bonding area, etc.
Introducing the wire bonding materials, the two metal more diffused are:
Aluminium (Al) - The most widely material used in the market, thanks to its outstanding properties during the bonding process. Furthermore, Li, Ti, Fe, Mg or Cu are allowed to increase the wire strength and corrosion resistivity [48].

Copper (Cu) - It would be an obvious alternative to aluminium because, thanks to his properties (Table 5.1), allows having a high strength, good bending fatigue and excellent loop stability wire. On the other hand, and unfortunately, it requires a more complex bonding process (high bonding force and ultrasonic power) and special chip metallization to protect the sensitive chips, when compared to Al [48].

	Copper(Cu)	**Aluminium(Al)**	**Units**
Electrical resistivity	0.017	0.027	$\frac{\Omega \cdot mm^2}{m}$
Thermal conductivity	400	220	$\frac{W}{m \cdot K}$
Yield strength	140	29	MPa
Elastic modulus	110-140	50	GPa
CTE	16.5	25	mpm
Melting point	1083	660	°C

TABLE 5.1: Comparison of material properties between Cu and Al [46].

Regarding to Al material, the interest is centred to analyse and compared the following wire typologies:

5N-H11 (Standard) - 15mils of diameter ($380\mu m$)
Al-H11 wires consist of high purity aluminium with selected addition elements homogeneously distributed in defined concentrations. Their benefits are related to defined softness, good bending fatigue properties, excellent loop stability and outstanding bonding properties.

5N-H11-CR - 15mils of diameter ($380\mu m$)
Comparing with 5N-H11, the corrosion resistant Al-H11-CR wire fulfils the increasing requirements made on the reliability of bonded connections in automotive and power electronics. Their benefits are particularly extended to corrosion resistance, modified softening behaviour at increased temperatures and problem-free bonding behaviour.

Figure 5.1 shows a wire cross-section and bring out that with the increasing of the wire diameter (for example at 300μm) the breaking load of 5N-H11-CR is higher compared with the standard 5N-H11.

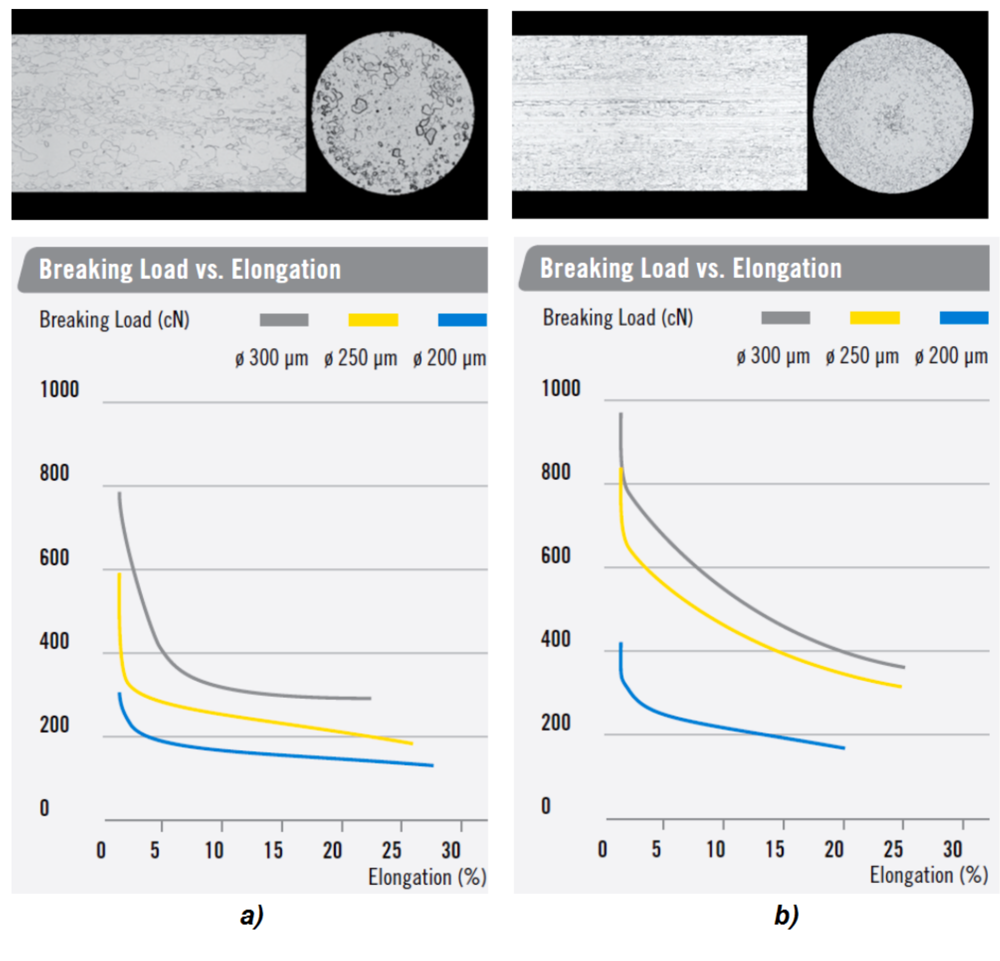


FIGURE 5.1: Perpendicular and parallel cross section, and mechanical behaviour - (a) 5N-H11 wire and (b) 5N-H11-CR wire.

On the other hand, regarding to Cu material, there is a new material generation that mixes the good bondability of pure Al with the optimal mechanical, electrical and thermal properties of Cu (Table 5.1). This is called CucoreAl wire and a cross section is shown in Figure 5.2.

CucorAl

This is a composite wire type with a copper core (60% or 70% of Cu material) and aluminium coating (40% or 30% of Al material). Thereby, this wire structure allows to have a reliable bonding windows, without changing the chip metallization (high compatibility with standard chip technology).
Additionally, it could be used with conventional bonding equipment [49].

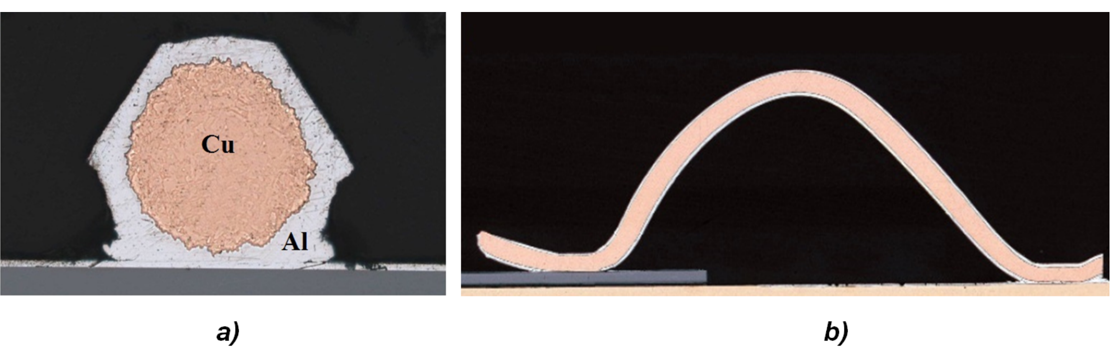


FIGURE 5.2: CucorAl wire bonding: perpendicular (a) and parallel (b) cross section to the bonding direction.

Some research works [24] [49] make evident that, using Cu core, the reliability of DCB Module improves in power cycling test compared to Al wire. This is reflected by the long-term behaviour during active power cycling tests in comparison to pure Al material.

In this chapter the evaluated CucorAl wires are constituted by 60% of Cu, 40% of Al, 15 mils (380μm) and 12 mils (300μm) of diameters.
The selected composition was motivated to avoid the limits of the bonding machine. Namely, since copper is a harder material than the aluminium (see table 5.1 a lower “Cu” composition (60% instead of 70%) was preferred.

5.1.1 Ultrasonic (U/S) bonding process

To perform the wire bonding in the presented power modules packages, a 3600Plus PowerRibbon^{TM} Bonder, made by Orthodyne Electronics[2], was employed.

The machine ultrasonically bonds aluminium wires from 25 to 500μm in diameter (1-20 mils) using the “wedge bonding” technique (see figure 5.3).

Wedge bonding or V-groove wedge is referred to the shape of its bonding tool (see figure 5.3). This kind of tool allows the joint, but it does not press all the wire area [50].

The origin of this technique is the ultrasound energy transfer, creating a durable and reliable connection.
The transfer of energy takes place thanks to the coupling of the tool with the ultrasonic transducer. The elongation of wire metal obtained from the ultrasound irradiation is comparable to that obtained with a substantial increase in temperature, at constant applied pressure.

[2]For more information: http://www.kns.com/

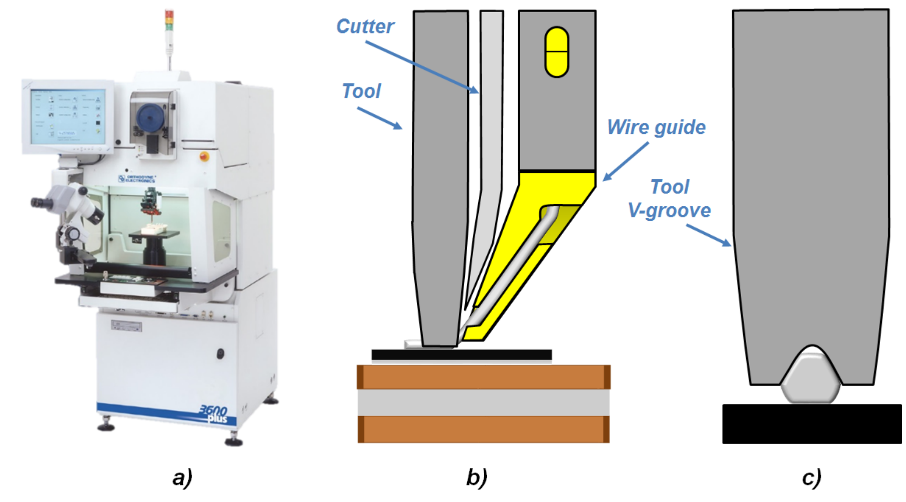


FIGURE 5.3: U/S bonding equipment - (a) Wire bonder machine utilized and description of (b) bonder head "lateral view" and (c) tool "front view".

Furthermore, in this technique the wire is guided, behind the tool, at about $30° - 60°$ from the horizontal bonding surface (see figure 5.3).

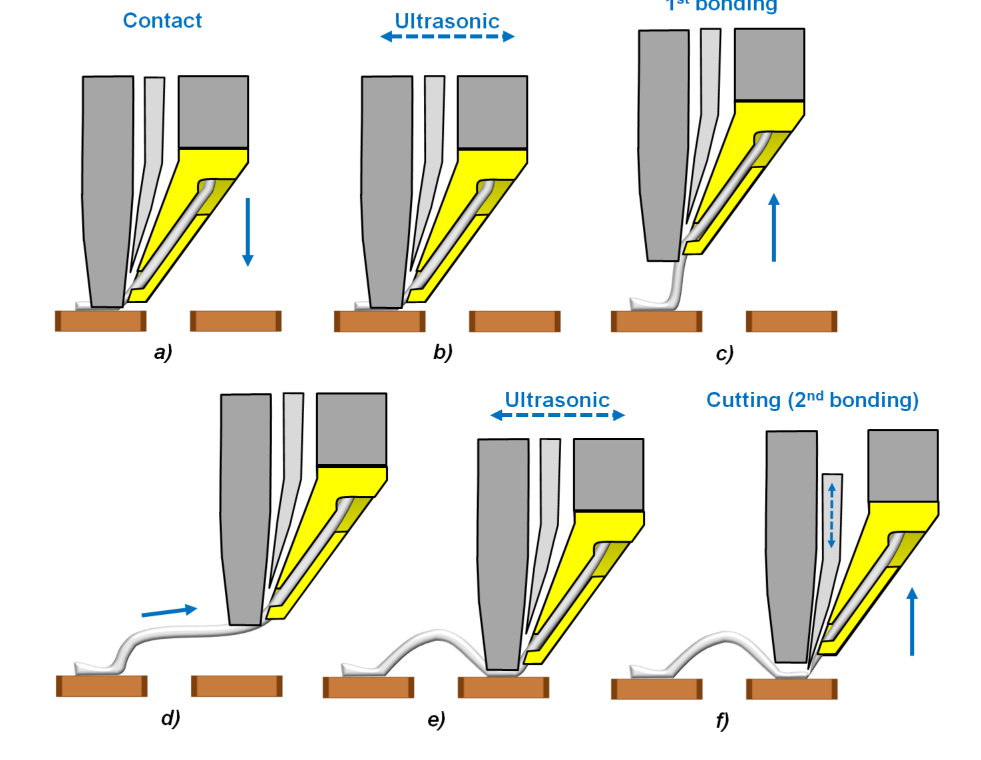


FIGURE 5.4: U/S bonding process description.

The bonding process 5.4 can be explained in six steps: firstly the wedge descends onto the surface (a), the wire is pinned against the pad surface and an U/S bond is performed (b). Next, the wedge rises and executes a motion to create a desired loop shape (c and

d). Finally at the 2nd bond location, the wedge descends, making a second bond (e and f)).

The wire bonding is obtained as a combination of three parameters:
- ultrasound intensity,
- pressure,
- application time.

5.2 Experimental Part

Generally the reliability of a power module can be limited by the electrical and mechanical ageing of interconnections such as "Wire Bonds". Due to the thermal excursion during the operation and the mismatch of CTE, a thermo-mechanical stress is induced, degrading the joint's interface [51][52][22].

As a consequence, the topic of this experimental part is to compare the power module reliability using three different wire bonding materials, individuating the most performing.

5.2.1 Temperature Cycling capability

Temperature Cycling Test became of great interest for the necessity to evaluate the temperature cycling capability and the ageing behaviour of the three different wire bonding materials previously described.

The wires 5N-H11 (standard), 5N-H11-CR and CucoreAl 60/40 with 15mils of diameter, were bonded between the DBC substrate and the metal pad of the pin out (see figure 5.5).

As explained in chapter 3, TCT is a method which provides a thermal excursion during a time cycle, applying the same temperature variation to all constituent layers of the power module [22].

Therefore, the test consists to submit all the different bonding wires under a previously set thermal system from $T_{min} = -55°C$ to $T_{max} = +150°C$, for 30 min at each temperature. During the test, a visual characterization is useful to understand how the wire is stressed.

Visual characterization
The degradation behaviour of the wire bond is observed using an optical microscope.

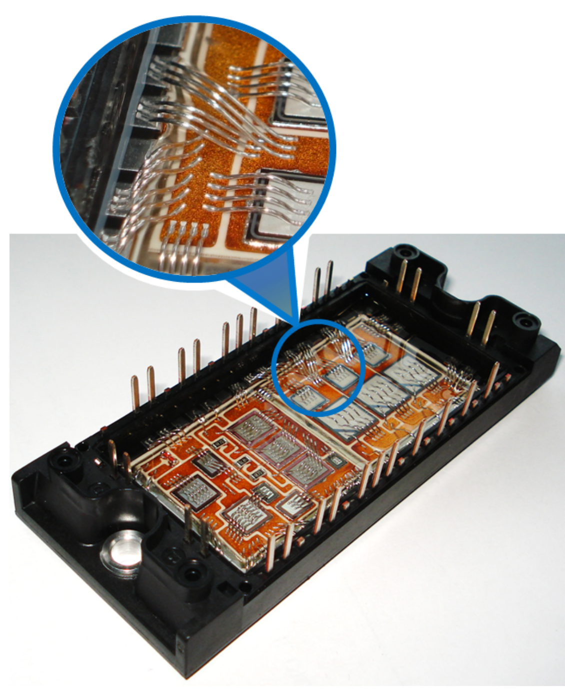


FIGURE 5.5: Wire bonding location into the power module dedicated to TCT analysis.

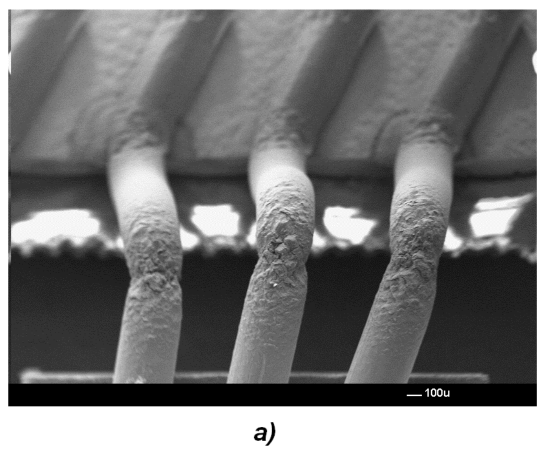
After approximately 300 cycles, the thermal system is stopped and the ageing of the wires is evaluated. During the test two critical points of the wire are considered: the loop and the wedges of the bond.

- The deformation process on the loop starts with an augmentation of the roughness at the surface (modification of the grain structure), then it appears a deformation or reduction of the cross sectional area and finally the fracture of the wire happens, see figure 5.6.
- On the wedge, the deformation process starts with an increase of the roughness, or corrugation at the surface. Corrugation is then followed by a section deformation or reduction and finally a heel-crack in the weakest point of the wedge area (see figure 5.7).

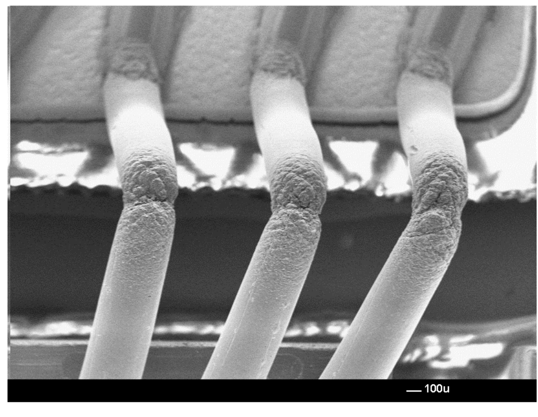
Figures 5.6 and 5.7, using a Scanning Electron Microscopy (SEM), show stressed loops and wedges after 1400 cycles of temperature cycling test and the table 5.2 indicates the number of cycles before the first failures occurred.

ΔT	**5N-H11**	**5N-H11-CR**	**CucoreAl 60/40**
$205°C$	300	1000	> 1400

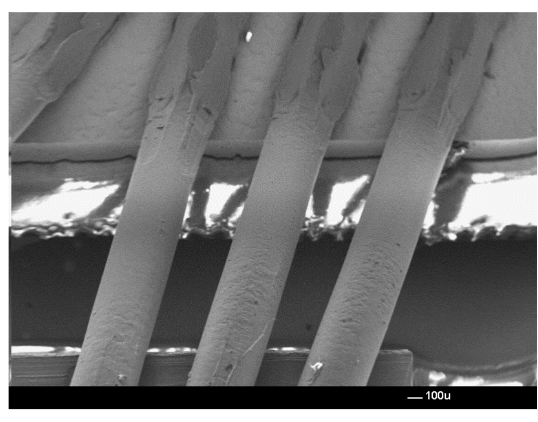
TABLE 5.2: Temperature cycling test results (number of cycles before first failure) for 5N-H11, 5N H11-CR and CucorAl 60/40 wire bonded modules.



a)



b)



c)

FIGURE 5.6: Stressed loops for three different types of wire bonding Al based materials after 1400 cycles of TCT @ $-55°C$ to $+150°C$ - (a) 5N-H11, (b) 5N H11-CR and (c) CucorAl 60/40.

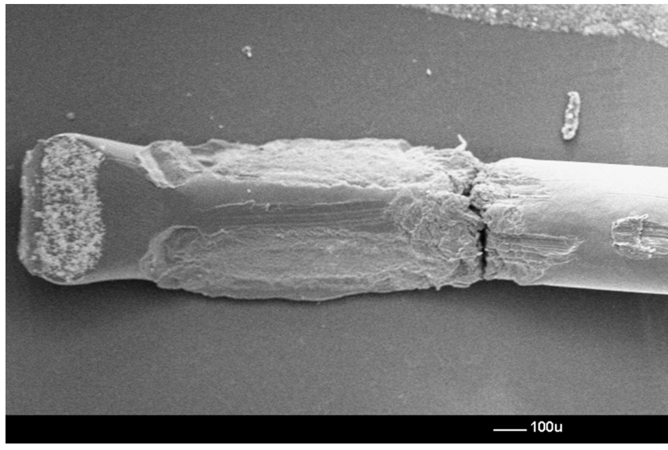


FIGURE 5.7: Bonding point stressed of an 5N-H11-CR wire, as resulting after TCT.

Looking at the figure 5.6 and at the table 5.2 it is possible observing that the CucorAl 60/40 wire has a superior reliability behaviour compared to Al materials. The wire CucorAl 60/40 has a good resistance to the plastic strain up to 1400 cycles and more. Furthermore, the level of damages during the test is low compared to a pure Al wire (5N-H11, 5N H11-CR and Al-PS) and no failure was found.

This could be explained because the high strain hardening of the Cu core leads to an important redistribution of the loading zone. As a consequence, the local stress (on the loop and wedge) is distributed over a wider wire area, reducing the stress [51].

Micro-structural Analysis

A micro-structural analysis, employing a SEM, was necessary to understand into detail processes of degradation during the thermo-mechanical stress.

Modifications of the grain structure at the surface of the Al wire is then followed by a crack development, which starts from nucleation at the surface of the stressed bond wire, due to the plastic deformation at the surface. Applying further loading, cracks could propagate into the material and finally cause the break of the Al bond wire.

Figure 5.8 describes cracks initiation at the surface of an Al wire, caused by the plastic deformation at the surface. Also the figure describes that the crack propagation forms an angle approximately of 45° from the wire direction, this is typical for ductile fatigue.

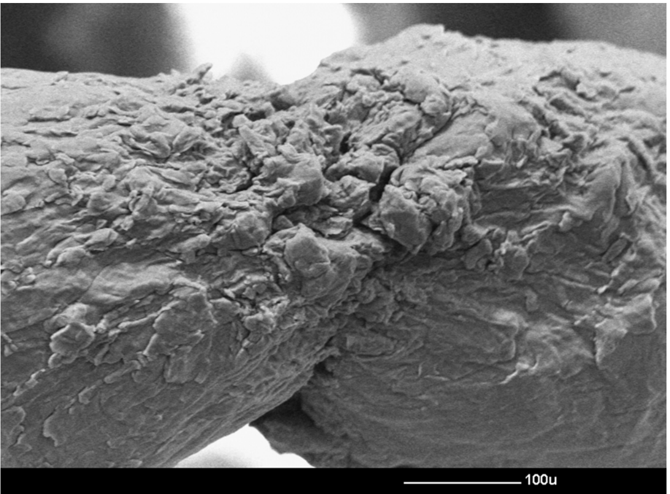


FIGURE 5.8: Crack initiations at the surface of an 5N-H11-CR wire under thermo-mechanical stress.

The figure 5.9, instead, shows a formation of roughness or corrugations at the surface of the CucorAl wire. Again, with an angle approximately of 45° from the wire direction

is visible. In the same way applying further loading, cracks could propagate into the material and finally causes the break of the CucorAl bond wire. First indications taken by microscopy of the surface are that the cracks are not as deep as for Al wire.

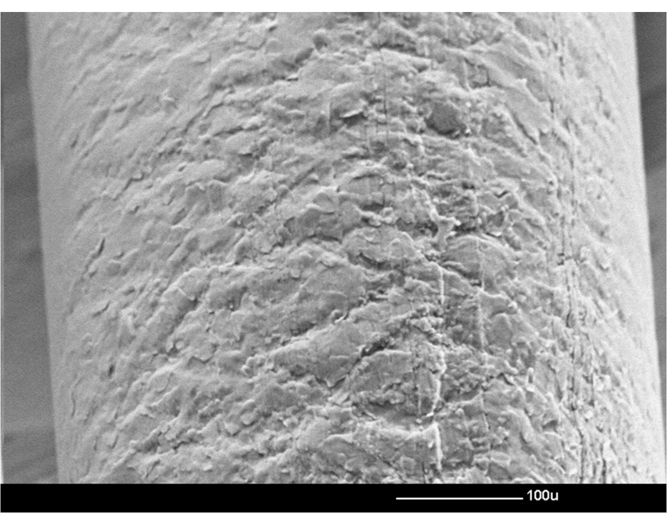


FIGURE 5.9: Crack initiations and corrugation formation at the surface of a CucorAl wire under thermo-mechanical stress.

Corresponding with the last results, the figure 5.10 shows a stressed CucorAl wire bonding cross section. Here it is possible to observe that, in addition to crack nucleation, voids presence is detected in the aluminium coating. This is because, the damage mechanisms are restricted by the Al layer and crack propagation is stopped at the interface with the Cu core (before the rupture of the copper occurs).

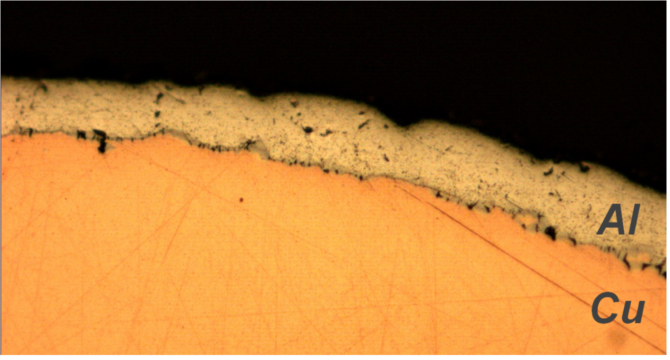


FIGURE 5.10: CucorAl wire bonding cross section under thermomechanical stress.

Because of the better performance of wire CucorAl compared to the aluminium material, the interest was extended to evaluate the power cycling capability, considering, in this case, the isolated power module presented in chapter 2, where the wires are bonded between the die Top-side (susceptible bonding area) and the DBC. Therefore, following the Orthodyne Electronics advices, a smaller wire diameter (12mils $\approx 300\mu$m) was

preferred, in order to avoid friction in the "wire guide" of the U/S bonder machine (see figure 5.3), .

Thereby, the purpose was to define optimum parameter settings required to realize two bonds on the die Top-side and one on the DBC (see figure 5.11), through a Design of Experiments (DOE).

5.2.2 Design of Experiments (DOE) applied to obtain the CucoreAl 60/40 (12mils) bond parameters

DOE or also called experimental design, is the design of a task that aims to describe or explain the variation of information, under conditions hypothesized to reflect the variation. Employing a statistical software called JMP[3], the idea is to study the output response through the variation of the input parameters.

The following model explanation will show as bonding parameter, related to the 1st bond on the die Top-side, were obtained. The same procedure was applied to others two cases (2nd bond on die Top-side and DBC).

Model

As mentioned before, wire bonding is obtained as a combination of three principal parameters: ultrasound intensity, pressure and application time and these parameters must be optimized carefully to achieve high quality bonds.
However, some works haven publicized that ultrasonic power has a major influence on reliability whereas, bonding force and even more the application time have a minor influence [48].

The performed methodology consists of conducting a parameter (screening evaluation) in order to get the preliminary parameter combination. The evaluation criteria were obtained bond yield, bond quality (deformation) and the measured shear value[4].

Subsequently, defined the starting point (central level of each factor) and calculating also ±25% of them, a DOE full-factorial 3^3 was considered: 3 factors (Bond Force, Bond Power and Bond Hold Time) with 3 levels each one (minimum, medium, maximum). See the table 5.3.

[3]For more information: http://www.jmp.com
[4]Shear Test explanation in Apendix A

Input Factors		**Levels**		Units
Bond Force	564	752	940	gr
Bond Power	62	82	103	mW
Bond Hold Time	75	100	125	mseg

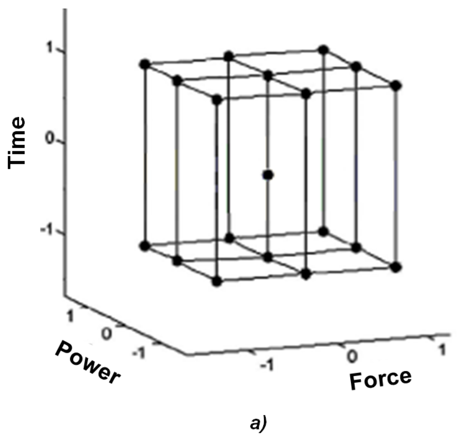
Table 5.3: DOE - Full-factorial.

However, whereas "application time" has a less influence in the bonding process, only 19 were contemplated instead of $3^3 = 27$ combinations (see the table 5.4 and the figure 5.11).

The outputs, or DOE responses, as "Shear Test" value and "Bond Deformation %" were analysed with ANOVA, Interaction Effect, Pareto Plot, Interaction Profiles and Predicted Plot.
Furthermore, in order to avoid random results, 15 bonded wires by parameter combination were considered.

Patern	**Force**	**Power**	**Time**
111	564	62	75
113	564	62	125
121	564	82	75
123	564	82	125
131	564	103	75
133	564	103	125
211	752	62	75
213	752	62	125
221	752	82	75
222	752	82	100
223	752	82	125
231	752	103	75
233	752	103	125
311	940	62	75
313	940	62	125
321	940	82	75
323	940	82	125
331	940	103	75
333	940	103	125

Table 5.4: DOE - Utilized matrix.



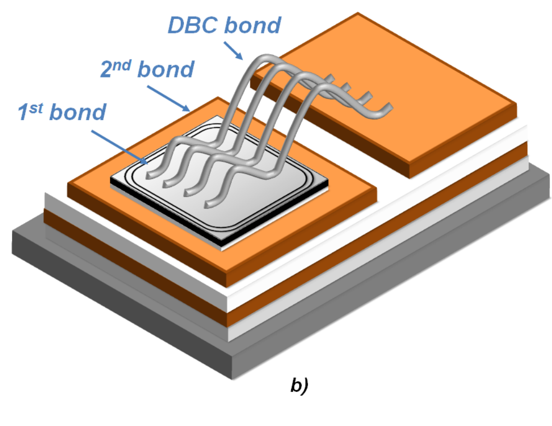


Figure 5.11: DOE wire bonding - (a) Utilized matrix and (b) involved bondings representation.

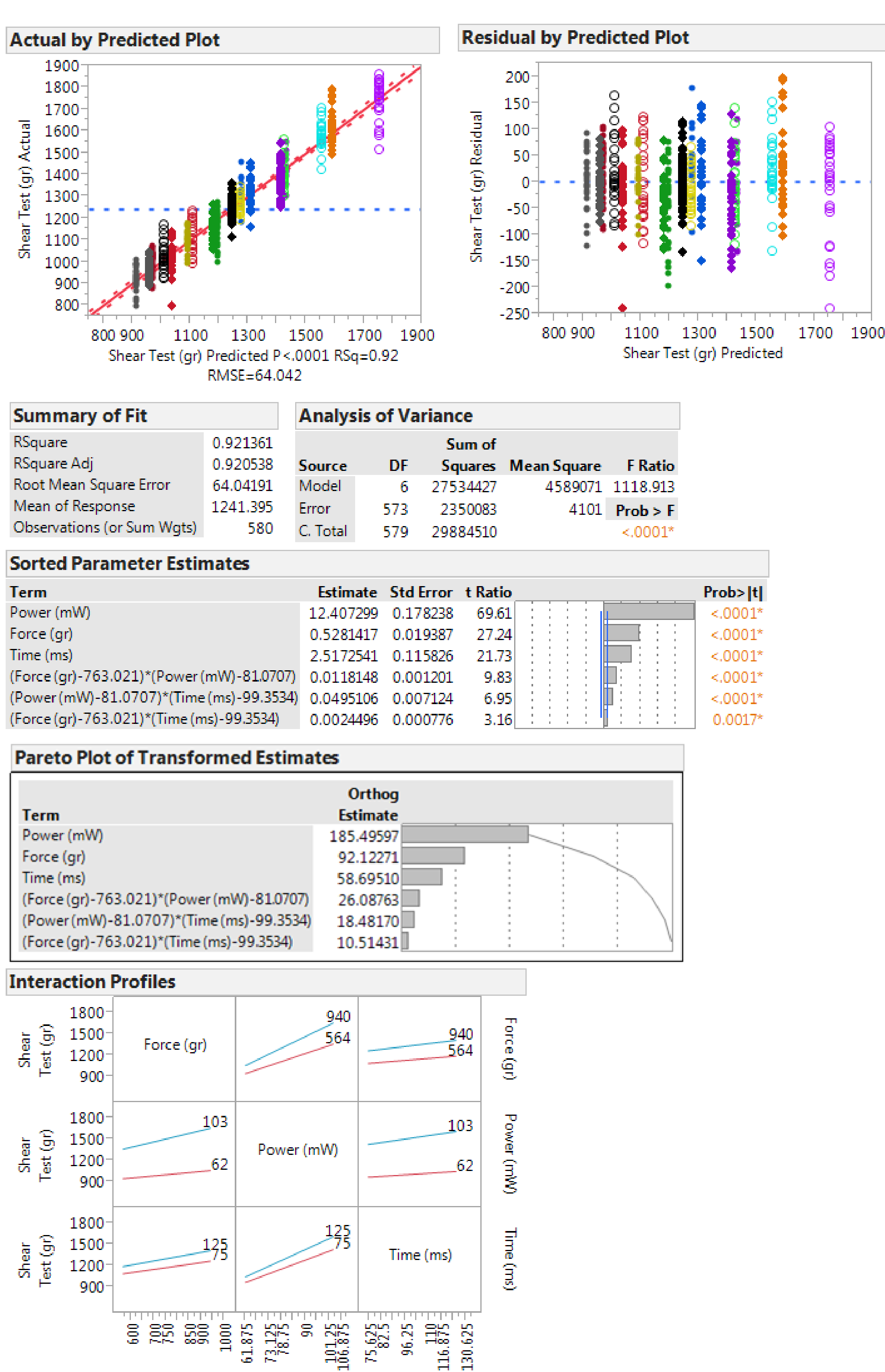
1st **Response: Shear Test**

Observing the figure 5.12 it is possible to see that:
- *ANOVA Analysis of Variance*: the $R^2 \simeq 1$ (which measures the fraction of the total variability in the response that is accounted by the model) suggests that the model correctly fits the data. However, unfortunately is not enough to guarantee that.
Furthermore, on the other hand, the obtained Pvalue (< 0.05) indicates that the importance of the variables is different.
- *Residual Graph*: the randomly behaviour of residuals, with a high R^2, proves that the model can be considered as valid or reliable. Namely, it fits the data appropriately and can give a reliable prediction.
In addition, the random arrangement of the residue indicates the independence of the data.
- *Sorted Parameter Estimates*: it shows that all of the input parameters are significant (Pvalue< 0.05) but there is an important order to consider (1st Power, 2nd Force and 3rd Time).
- *Pareto Plot*: the graph indicates that Power factor, and Force factor, in lesser degree, have significant effect in terms of Bond Shear Test.
- *Interaction Profile*: these graphs confirm that Power is significant in terms of Bond Shear Test. It makes evident that there is only a slight interaction in the combination Power * Time because, the non-intersection of lines (parallelism) indicates low interaction between the input variables.

Based on graphical analysis (Residual Analysis / Interaction Effects / Pareto Chart) the null hypothesis should be rejected.

2nd **Response: Bond Deformation %**

The Bond Deformation percentage is represented in the figure 5.13. Here it is possible observing that:
- *ANOVA*: also in this case $R^2 \simeq 1$ suggests that the model fits the data, but this value is not enough to guarantee that.
- *Residual Graph*: the randomly behaviour of residuals, besides with a high R^2, proves that the model can be considered as valid.
- *Sorted Parameter Estimates*: It shows that all of three input parameters are significant (Pvalue< 0.05) and the same importance order is repeated in this case (Power, Force and Time).
- *Pareto Plot*: The graph indicates that factor Power and Force, in lesser degree, have significant effect in terms of Bond Deformation %.
- *Interaction Profile*: Confirm that Power is significant in terms of Bond Deformation % and, in addition, it makes evident that there is only an interaction in the combination Power * Time.



Summary of Fit

RSquare	0.921361
RSquare Adj	0.920538
Root Mean Square Error	64.04191
Mean of Response	1241.395
Observations (or Sum Wgts)	580

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	6	27534427	4589071	1118.913
Error	573	2350083	4101	Prob > F
C. Total	579	29884510		<.0001*

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Power (mW)	12.407299	0.178238	69.61	<.0001*
Force (gr)	0.5281417	0.019387	27.24	<.0001*
Time (ms)	2.5172541	0.115826	21.73	<.0001*
(Force (gr)-763.021)*(Power (mW)-81.0707)	0.0118148	0.001201	9.83	<.0001*
(Power (mW)-81.0707)*(Time (ms)-99.3534)	0.0495106	0.007124	6.95	<.0001*
(Force (gr)-763.021)*(Time (ms)-99.3534)	0.0024496	0.000776	3.16	0.0017*

Pareto Plot of Transformed Estimates

Term	Orthog Estimate
Power (mW)	185.49597
Force (gr)	92.12271
Time (ms)	58.69510
(Force (gr)-763.021)*(Power (mW)-81.0707)	26.08763
(Power (mW)-81.0707)*(Time (ms)-99.3534)	18.48170
(Force (gr)-763.021)*(Time (ms)-99.3534)	10.51431

FIGURE 5.12: DOE results of 1st Response: Shear Test.

Also in this case the null hypothesis should be rejected.

Since the model can be considered valid, utilizing the Prediction Profiler, it is possible to simulate the output behaviour, in real time, under an input variation. The figure 5.14 shows the chosen 1st bond final parameters.

Therefore, the following table 5.5 summarizes the optimum chosen parameters:

	1st Bond	2nd Bond	DBC	Units
Bond Force	888	894	870	gr
Bond Power	67	68	90	mW
Time Application	75	75	80	mseg

Table 5.5: Final optimum parameters.

Finally, in order to prove the reliability prediction, some samples were bonded with the selected parameters and aspects: Bonging Obtained (%), Electrical Integrity (%), Bond Deformation (%) and Shear Test Measure (gr), were compared.
The table 5.6 shows the comparison between the "Desirable Simulated Outputs" Vs. the "Obtained Outputs" on the 1st Bond.

	Desirable Simulated Outputs	Obtained Outputs	Units
Shear Test Measured	$\cong$ 1058	$\cong$ 1000	gr
Bond Deformation	$\cong$ 17.4	$\cong$ 15.6	%
Electrical Integrity	100	100	%
Good Bonging Obtained	100	100	%

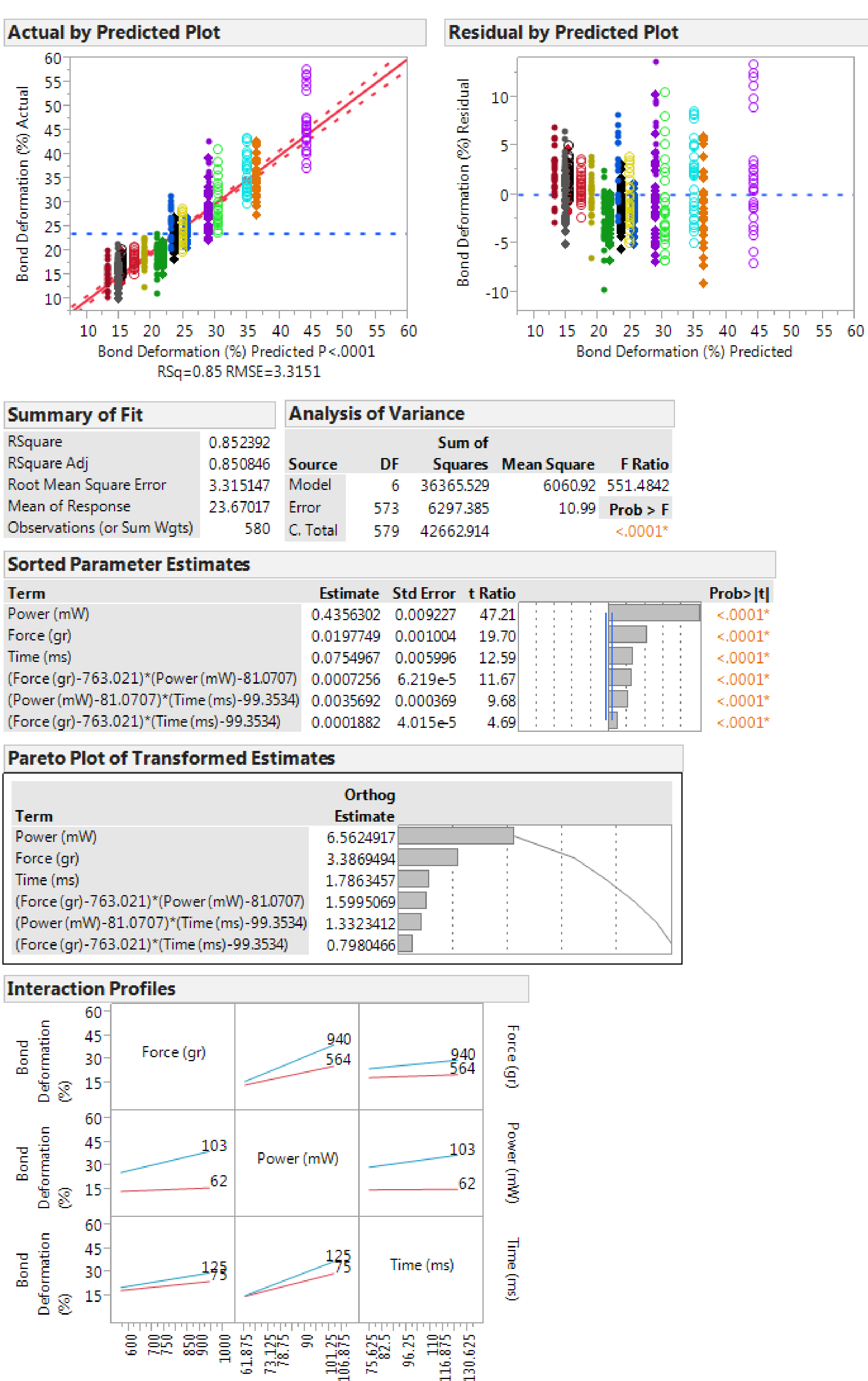
Table 5.6: Measured DOE Outputs after utilized final parameters bonding.

Once obtained the bonding parameters to build the samples, the interest is to evaluate the power cycling capability.

5.2.3 Power Cycling capability

As explained in chapter 3, Short PCT provides thermal and mechanical stress, namely, during the test rapid temperature changes on the devices and interconnections are induced when high current is applied and removed periodically.

Whereas the interested to induce failure mode was centred to obtain wire bond fatigue, the **International Standard International Norm IEC 60749-34** was followed. Two different set-up conditions were considered, in order to define the wire bond lifetime and to understand the ageing process when two ΔT_j are desired:



Summary of Fit

RSquare	0.852392
RSquare Adj	0.850846
Root Mean Square Error	3.315147
Mean of Response	23.67017
Observations (or Sum Wgts)	580

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	6	36365.529	6060.92	551.4842
Error	573	6297.385	10.99	Prob > F
C. Total	579	42662.914		<.0001*

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Power (mW)	0.4356302	0.009227	47.21	<.0001*
Force (gr)	0.0197749	0.001004	19.70	<.0001*
Time (ms)	0.0754967	0.005996	12.59	<.0001*
(Force (gr)-763.021)*(Power (mW)-81.0707)	0.0007256	6.219e-5	11.67	<.0001*
(Power (mW)-81.0707)*(Time (ms)-99.3534)	0.0035692	0.000369	9.68	<.0001*
(Force (gr)-763.021)*(Time (ms)-99.3534)	0.0001882	4.015e-5	4.69	<.0001*

Pareto Plot of Transformed Estimates

Term	Orthog Estimate
Power (mW)	6.5624917
Force (gr)	3.3869494
Time (ms)	1.7863457
(Force (gr)-763.021)*(Power (mW)-81.0707)	1.5995069
(Power (mW)-81.0707)*(Time (ms)-99.3534)	1.3323412
(Force (gr)-763.021)*(Time (ms)-99.3534)	0.7980466

FIGURE 5.13: DOE results of 2nd response: Bond Deformation %.

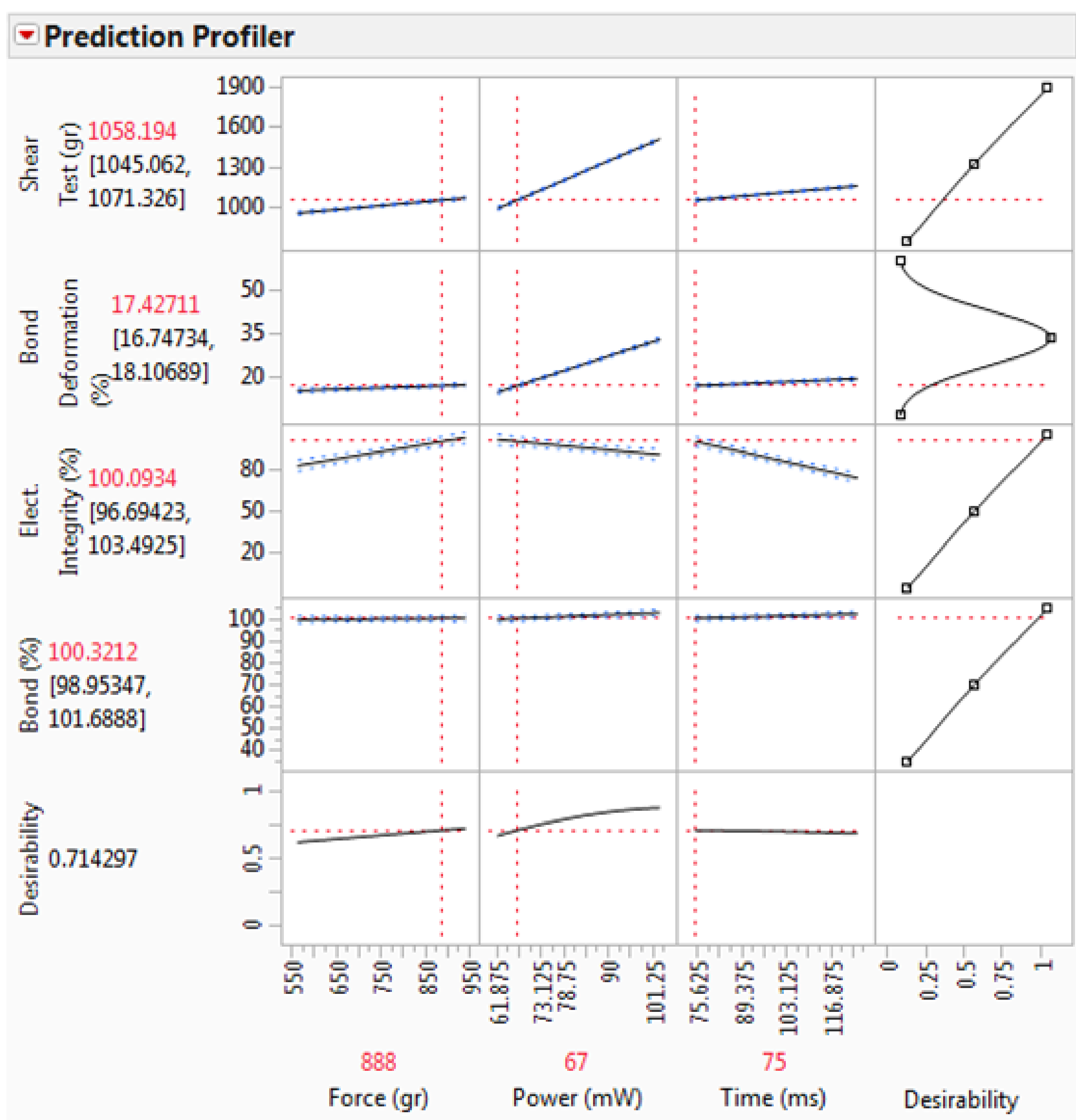


FIGURE 5.14: Final optimised parameters obtained with Prediction Profiler.

	$\Delta T_j \cong 60°C$	$\Delta T_j \cong 90°C$	Units
t_{on}	0.3	1.25	s
t_{off}	12.5	13.7	s
I_{test}	250	300	$A(DC)$

TABLE 5.7: Short Power Cycling Test conditions utilized to evaluates the wire bonding life time.

The test consists on studying the power module lifetime and comparing the CucoreAl 60/40 12mils wire bond to the standard used wire material 5N-H11 15 mils, under two different ΔT_j conditions (see the table 5.7).

Measures $@\Delta T_j \cong 60°C$

During the test two electric parameters (V_f and V_{BR}) and the thermal resistance junction-case were measured in order to monitor the electrical and thermal trends, and to detect the lifetime of each single sample.

Figures 5.15 and 5.17 show the measured voltage drop (V_f), while the figures 5.16 and 5.18 show the measured Rth_{j-c} on all the samples with 5N-H11 "standard" wire and CucoreAl wire.

Observing the graphs 5.15 and 5.16 it is possible to recognize that the voltage drop at the diodes and the thermal resistance remain almost constant up to a large number of cycles (approximately $< 250kcycles$). Few cycles after, there is a smaller, but quick increment of Rth_{j-c} and immediately after the (V_f) grows up to circuit open.

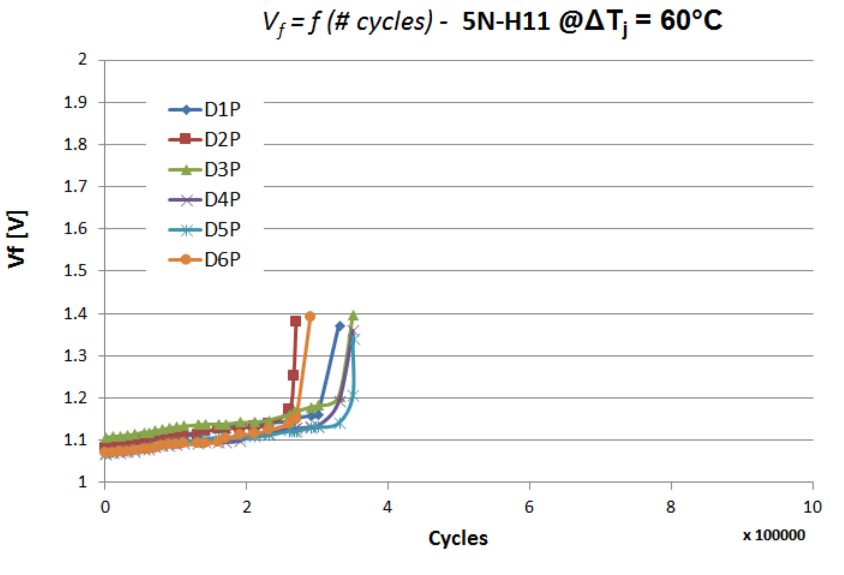


FIGURE 5.15: V_f measures during Short Power Cycling Test ($@\Delta T_j \cong 60°C$) with 5N-H11 wire.

Figures 5.17 and 5.18 describe a flat trend up to $856k$ cycles. As expected in this samples with CucoreAl wire internally, the voltage drop at the diodes and the thermal resistance remained almost constant up to a higher number of cycles, compared to the Al standard wire.

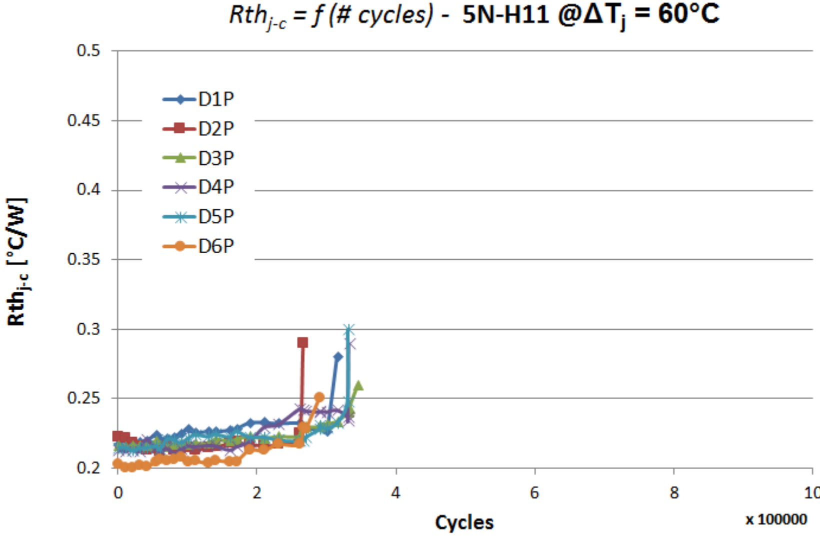


FIGURE 5.16: Rth_{j-c} measures during Short Power Cycling Test (@$\Delta T_j \cong 60°C$) with 5N-H11 wire.

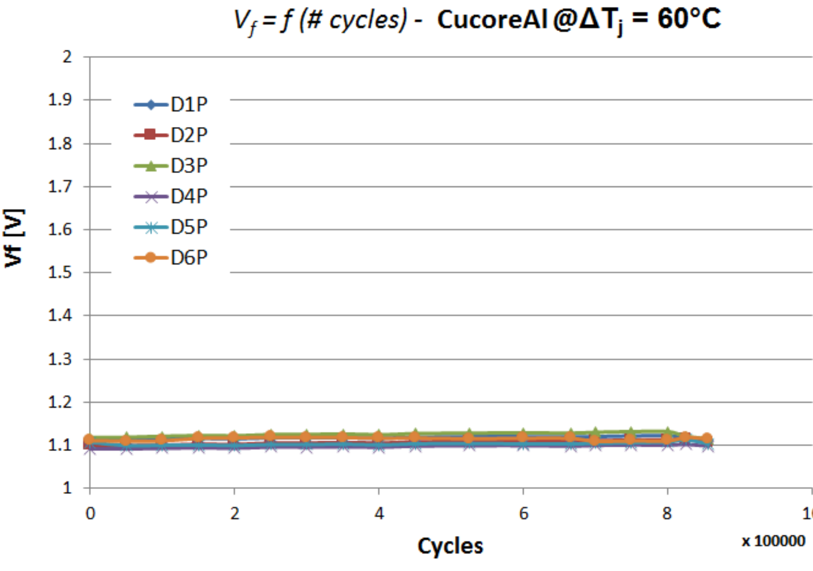


FIGURE 5.17: V_f measures during Short Power Cycling Test (@$\Delta T_j \cong 60°C$) with CucoreAl wire.

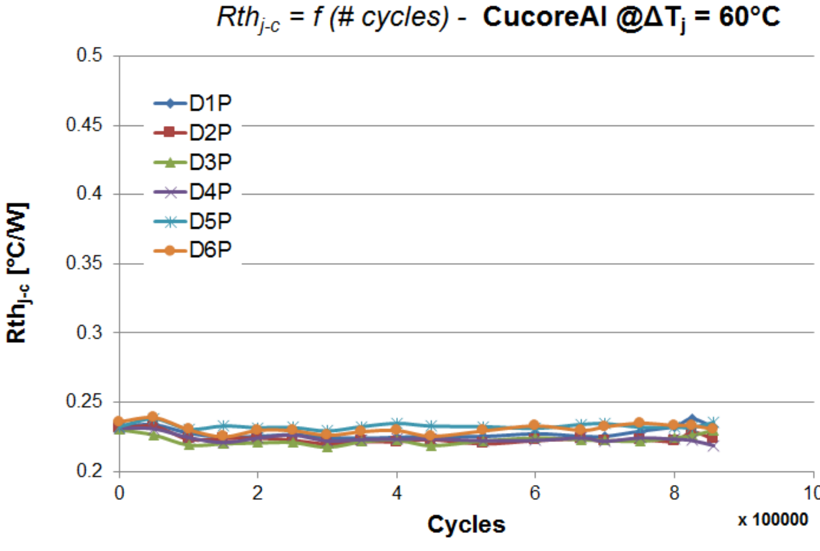


FIGURE 5.18: Rth_{j-c} measures during Short Power Cycling Test ($@\Delta T_j \cong 60°C$) with CucoreAl wire.

In order to directly compare the V_f trend of these power modules, the graph 5.19 resumes clearly that, again, the CucorAl 60/40 wire has a superior reliability behaviour compared to Al material.

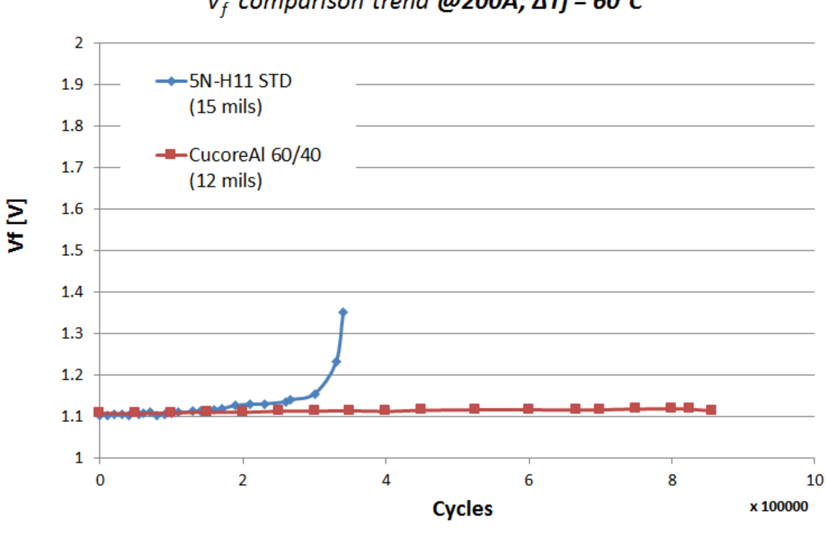


FIGURE 5.19: V_f average trend comparison between 5N-H11 and CucoreAl wire materials ($@\Delta T_j \cong 60°C$).

However, a particular situation was observed measuring the reverse voltage (V_{BR}) during the test: a degrading of V_{BR} of the samples with CucoreAl wire was found. The figure 5.20 shows that after 50kcycles the V_{BR} starts decreasing drastically compared to Al wire.

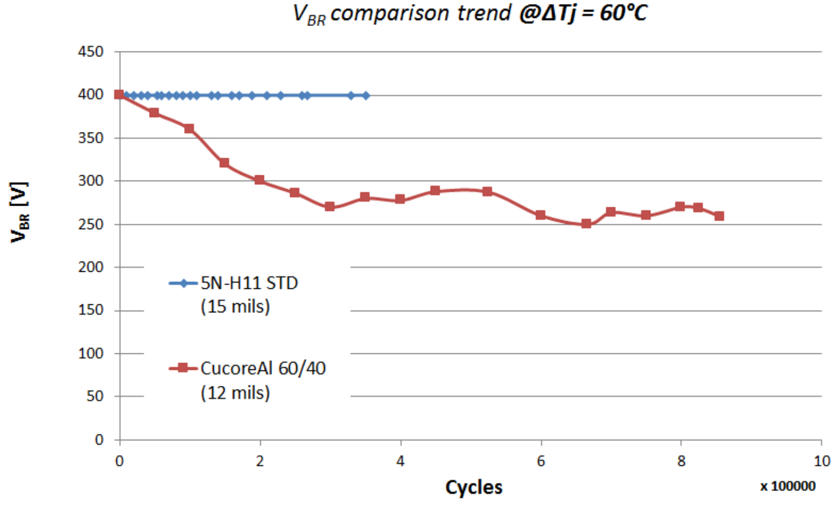


FIGURE 5.20: 5N-H11 vs. CucoreAl wire under Short PCT (@$\Delta T_j \cong 60°C$) - V_{BR} trend.

Measures @$\Delta T_j \cong 90°C$

In this case the same parameters that were described before were monitored, but setting the power cycling test in order to stress with $\Delta T_j \cong 90°C$.

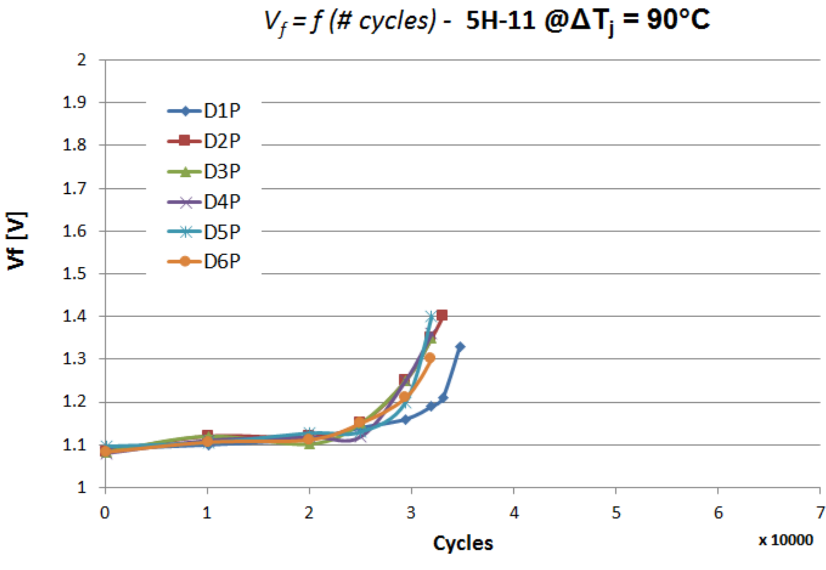


FIGURE 5.21: V_f measures during Short Power Cycling Test (@$\Delta T_j \cong 90°C$) with 5N-H11 wire.

Looking at the graphs 5.21 and 5.22 it is possible to recognize that an increment of applied stress causes an early failure. The voltage drop at the diodes and the thermal resistance remains constant up to approximately $< 25kcycles$.
Few cycles after, Rth_{j-c} and V_f grew up to circuit open and this trend was more pronounced then the previous case.

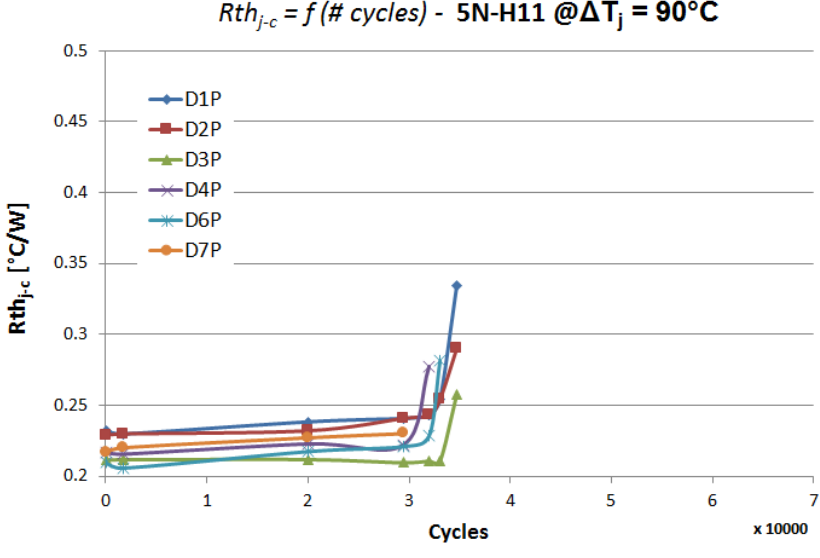


FIGURE 5.22: Rth_{j-c} measures during Short Power Cycling Test (@$\Delta T_j \cong 90°C$) with 5N-H11 wire.

Again, in order to directly compare the V_f trend, the graph 5.23 resumes clearly that, the CucorAl 60/40 wire has a superior reliability behaviour compared to Al material.

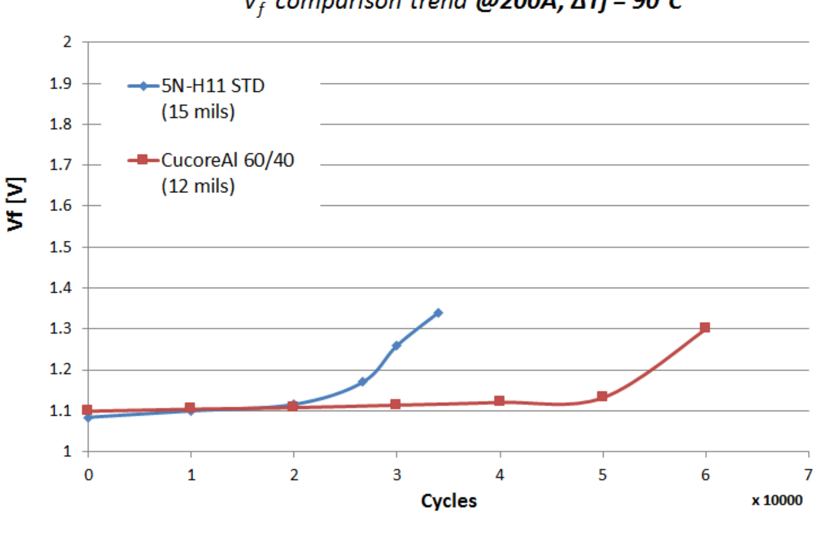


FIGURE 5.23: V_f average trend comparison between 5N-H11 and CucoreAl wire materials (@$\Delta T_j \cong 90°C$).

As happened before, measuring the reverse voltage (V_{BR}), a degrading of CucoreAl wire V_{BR} was found. The figure 5.24 shows that after 1kcycles the V_{BR} starts to decrease drastically.

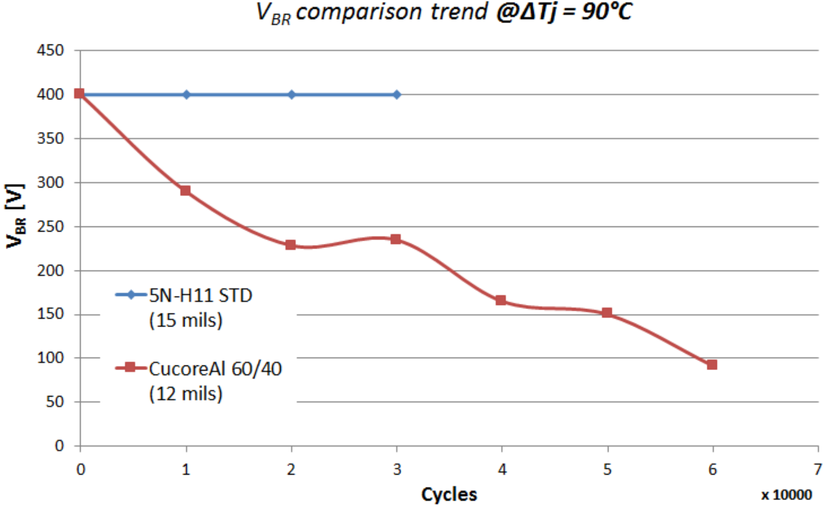


FIGURE 5.24: 5N-H11 vs. CucoreAl wire under Short PCT (@$\Delta T_j \cong 90°C$) - V_{BR} trend.

$\#cycles = f(\Delta T_j)$

To summarize the power modules reliability, regarding wire bonding material, the figure 5.25 and the table 5.8 show (as happened during the Temperature Cycling Test) that the CucorAl 60/40 wire presents a superior reliability behaviour, compared to Al material.

Wire material	$\Delta T_j \cong 60°C$	$\Delta T_j \cong 90°C$
Al 5N-H11 (Standard - 15mils)	308.000 cycles	30.825 cycles
CucoreAl 60/40 (12 mils)	$>$ 856.000 cycles	60.000 cycles

TABLE 5.8: Number of reached cycles during Short Power Cycling Test under two different ΔT_j conditions.

Again, this could be explained because the high strain hardening of the Cu core leads to an important redistribution of the loading zone. As a consequence, the local stress (on the loop and wedge) is distributed over a wider wire area, reducing the stress in critical areas, like the heel at the wedge [51].

Observing the graph 5.8 is clear that there is a strong dependency between the expected $\#cycles$ and the desired ΔT_j. In addition, projecting the straight along the graph, it is possible to estimate what is the $\#cycles$ by each single ΔT_j.

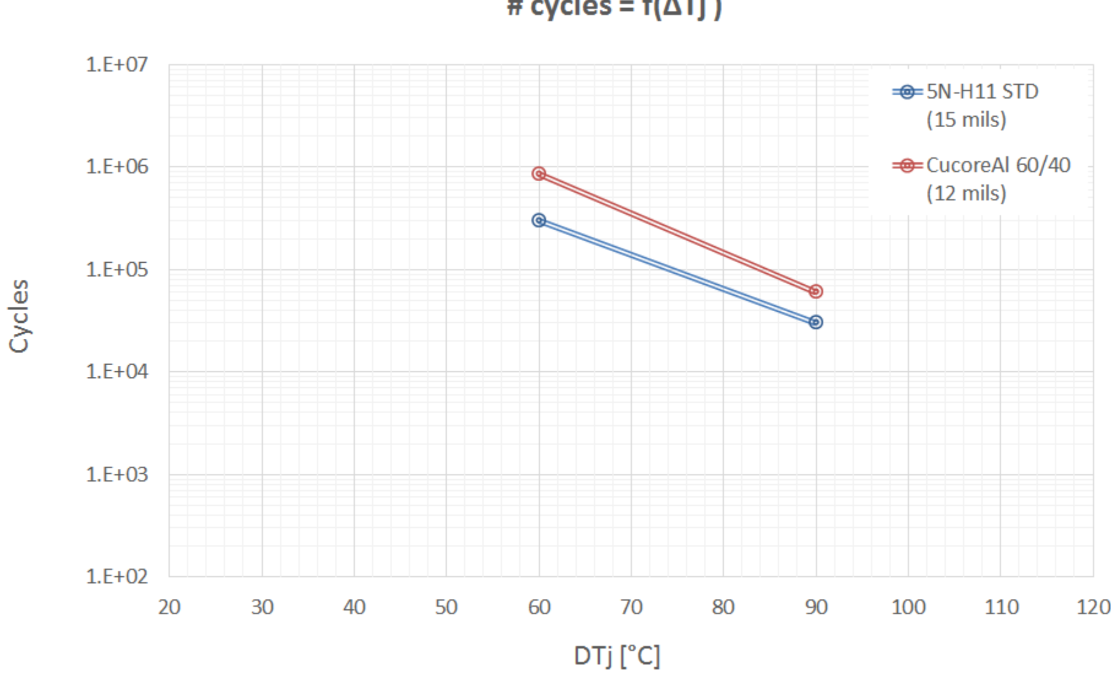


FIGURE 5.25: $\#cycles = f(\Delta T_j)$ under Short Power Cycling Test.

5.2.3.1 Failure Analysis (F.A.)

To understand the particular degrading of power modules with CucoreAl wire in reverse bias, a careful failure analysis[5] was carried out.

Therefore, some tested samples with 5N-H11 and CucoreAl 60/40 wire materials were analysed as follows:

- *C-SAM inspection*

Employing a C-mode Scanning Acoustic Microscope (C-SAM) it was observed that, as expected, the devices did not reveal relevant solder voids between die/DBC and between DBC/base plate.
At $\Delta T_j \cong 60°C$ no solder fatigue or delamination was seen between soldered interfaces (see figure 5.26), while at $\Delta T_j \cong 90°C$ only smaller solder delamination was found. This could confirm that the applied stress was principally focused on the wire interconnections.

In addition, note that the anomalous shape of solder, seen on the edge between base/-substrate, was probably due to a different thickness of solder at the interface edge or to a solder delamination (this will be observed after chemical and mechanical decapsulation).

[5]For more information about the utilized instrumentation to realize the F.A. please see Appendix B

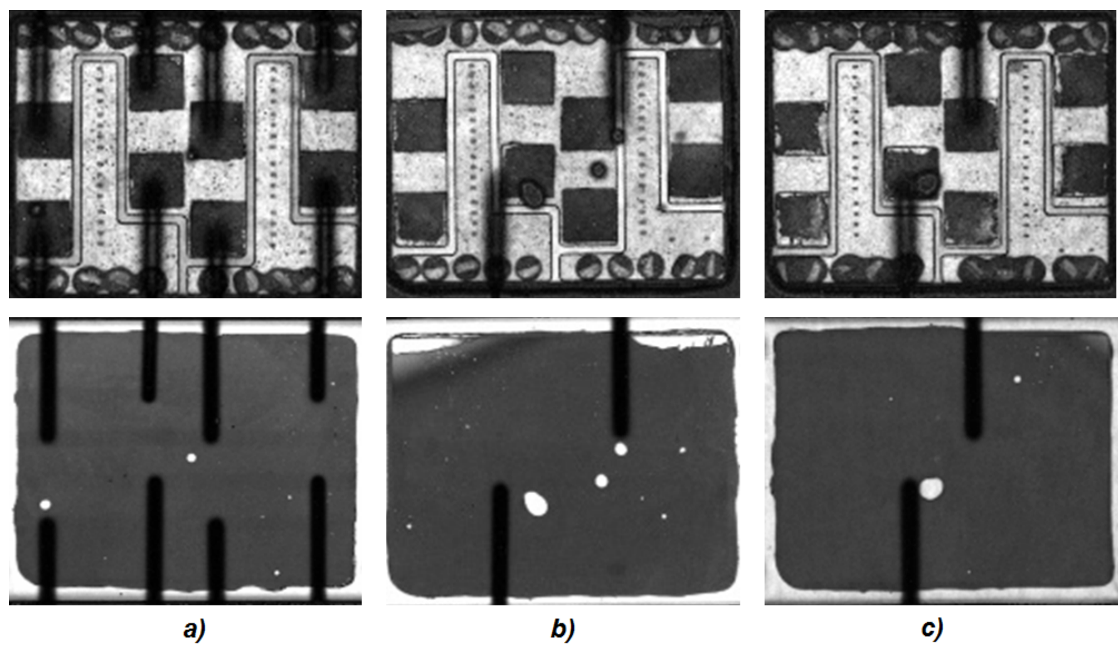


FIGURE 5.26: C-SAM images of die/DBC and between DBC/base plate - (a) 5N-H11 @$\Delta T_j \cong 60°C$, (b) 5N-H11 @$\Delta T_j \cong 90°C$ and (c) CucoreAl @$\Delta T_j \cong 90°C$.

Subsequently, after mechanically removing the plastic cover, it was observed that any analysed sample shows anomalies on the internal silicon gel (see figure 5.27).

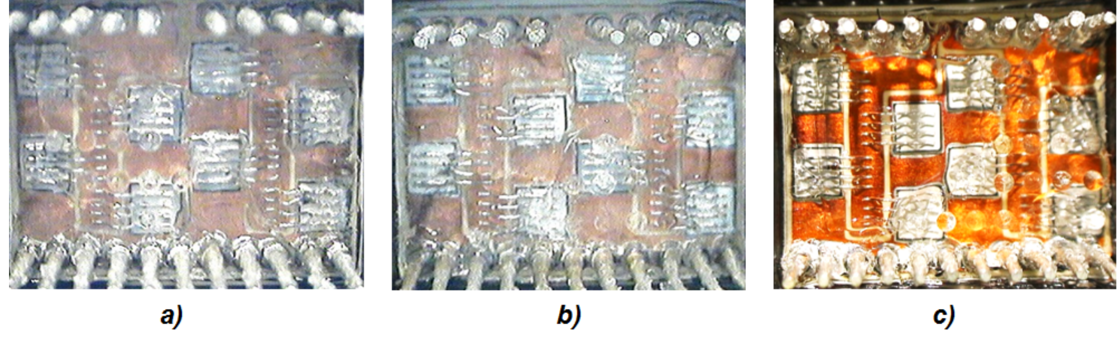


FIGURE 5.27: Silicon gel after Short PCT - (a) 5N-H11 @$\Delta T_j \cong 60°C$, (b) 5N-H11 @$\Delta T_j \cong 90°C$ and (c) CucoreAl @$\Delta T_j \cong 90°C$.

- *Chemical and mechanical decapsulation and sub-assembly internal inspection*

To have a visual access to the internal structure the isolation gel was removed by chemical etching and the plastic box was removed through mechanical action.

As observed in figure 5.28, and previously mentioned with C-SAM instrument, only at $\Delta T_j \cong 90°C$ solder layer between die/DBC showed signals of damage, as delamination (solder fractured). On the other hand, delamination on solder layer between DBC/Base plate did not appear.

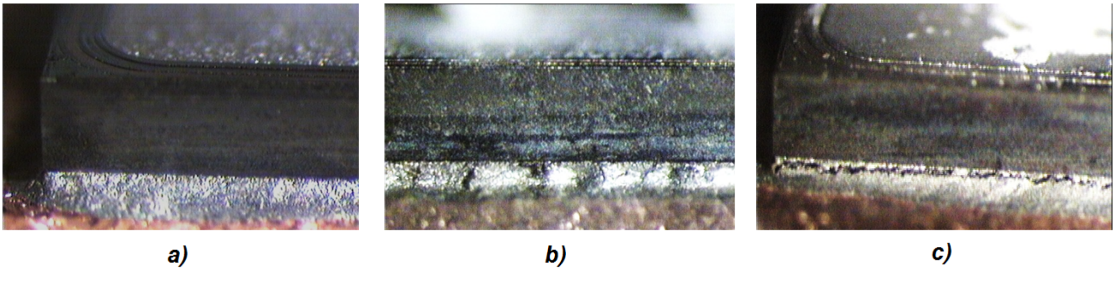


FIGURE 5.28: Tilt magnification view of solder below diode - (a) 5N-H11 @$\Delta T_j \cong 60°C$, (b) 5N-H11 @$\Delta T_j \cong 90°C$ and (c) CucoreAl @$\Delta T_j \cong 90°C$.

- *Micro-structural Analysis*

Employing a SEM, a micro-structural analysis was carried out in order to observe into details the wire materials and to understand the failure mode.

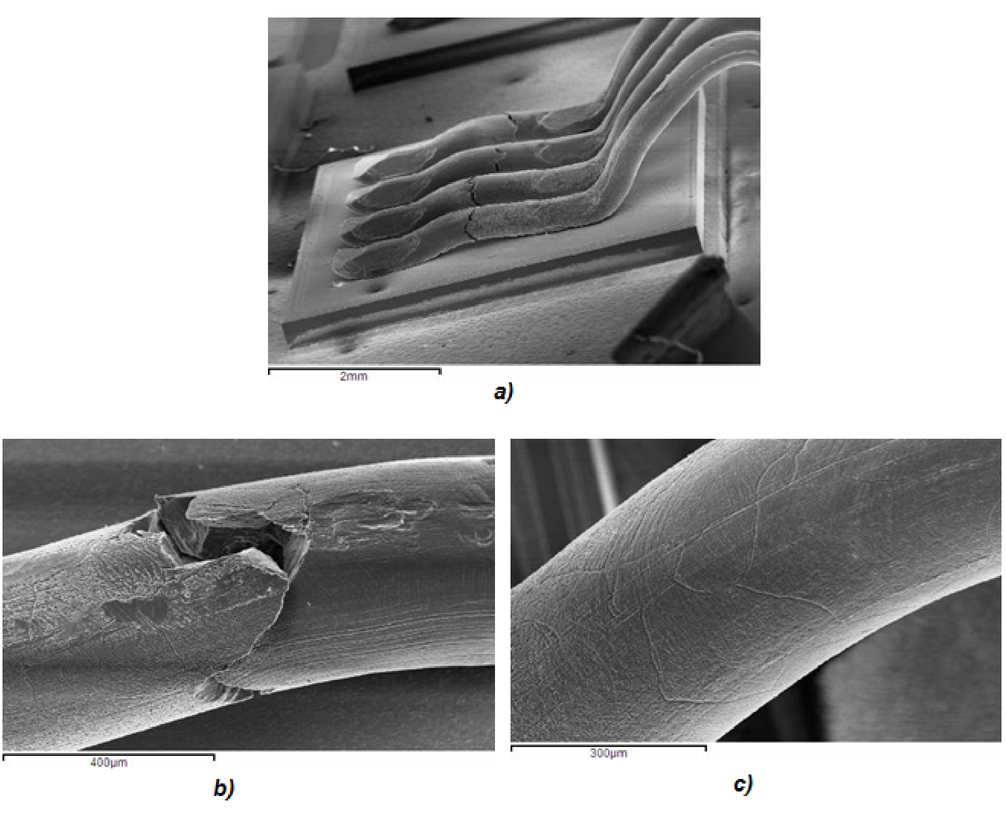


FIGURE 5.29: SEM images of 5N-H11 wires @$\Delta T_j \cong 60°C$ - (a) Analysed wires, (b) Breaks between the 1st and the 2nd bond and (c) Modifications of the grain structure at the surface in the 2nd loop.

As previously exposed in TCT (5.2.1), the Al wire describes more signals of stress then the compared CucorAL wire.

5N-H11 material @$\Delta T_j \cong 60°C$ and @$\Delta T_j \cong 90°C$, shows modifications of the grain structure at the surface in the loop, between 2nd and 3rd bonds, followed by cracks

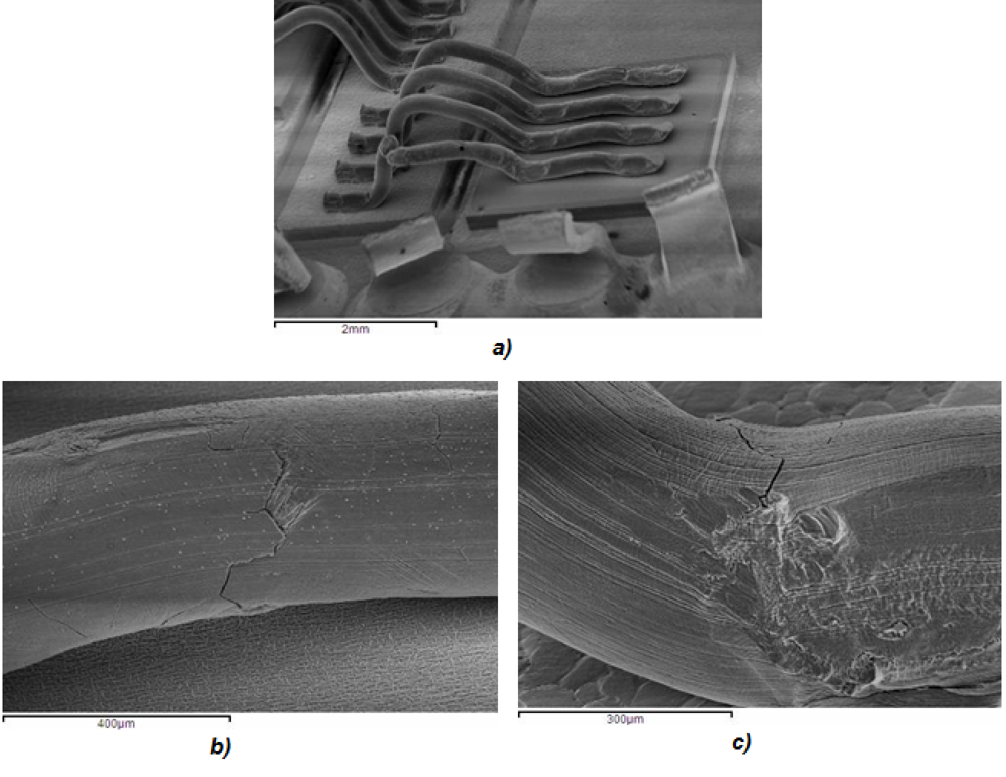


FIGURE 5.30: SEM images of 5N-H11 wires @$\Delta T_j \cong 90°C$ - (a) Analysed wires, (b) Breaks between the 1st and the 2nd bond and (c) Cracks close to the 2nd bond.

initiation founded close to the 2nd bond and breaks in the middle of the 1st and the 2nd bond (caused by the plastic deformation at the surface, see figures 5.29 and 5.30).

Looking at the figure 5.31 it is possible to observe that the CucorAl 60/40 wire has a superior reliability behaviour compared to Al materials. Namely, no fractures and cracks were found at wire level. However, after chemical etching, craters, below the bond wire stitch, were found (the figure 5.32).

Therefore, in order to understand if this craters were induced by the bonding process or if they were consequence of the Short PCT, a non stressed sample was analysed. The figure 5.33 shows a little stress signal that was induced during the bonding process and accentuated during the reliability test.
A cratering formation probably conduced to compromise the electrical characteristics of the device.

Indeed, the V_{BR} degradation observed on the samples with CucoreAl wire during the Short PCT, as is showed in figure 5.33, could be explained as: after the bonding process a smaller stress on the die surface was induced but all the samples were electrically good (measured direct and reverse biased). Subsequently, when the power modules were

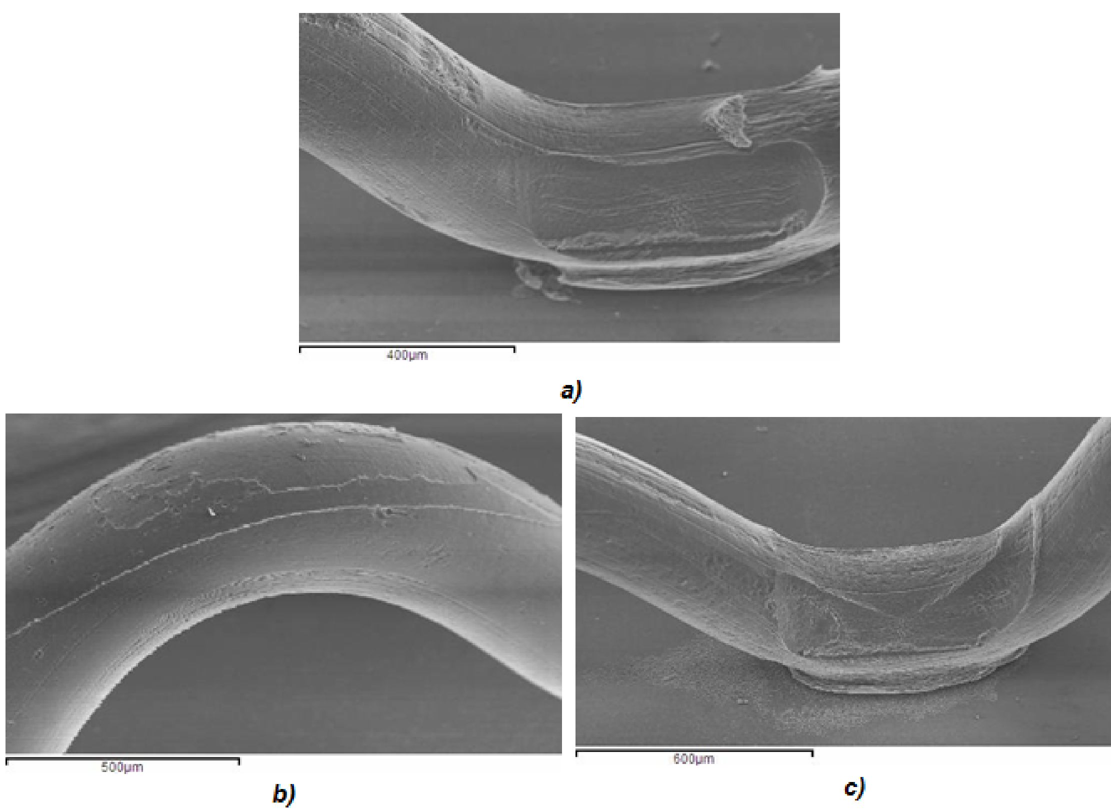


FIGURE 5.31: SEM images of CucoreAl wires @$\Delta T_j \cong 90°C$ - No damages presented on (a) 1st bond, (b) 1st loop and (c) 2nd bond.

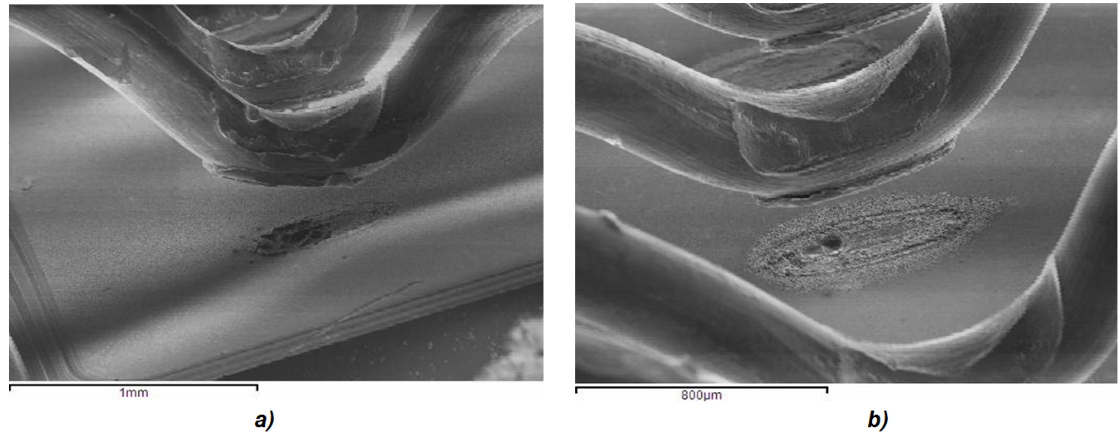


FIGURE 5.32: SEM images of CucorAl wires @$\Delta T_j \cong 90°C$ - (a) Crater produced and (b) Wire lit-off.

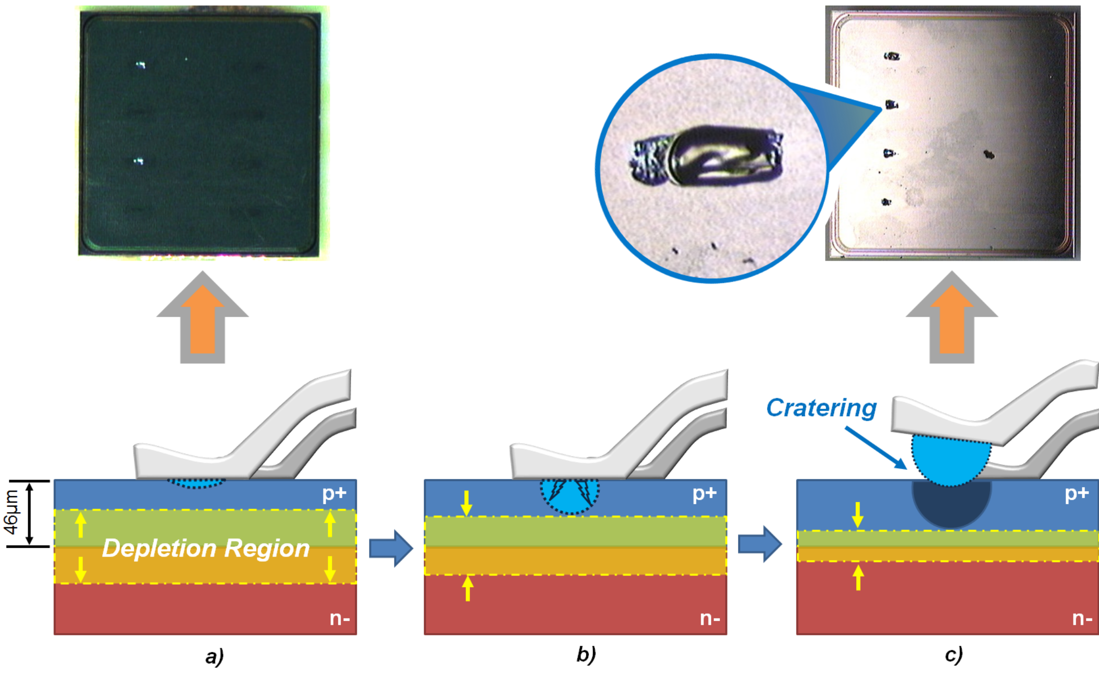


FIGURE 5.33: V_{BR} degradation by cratering formation under CuroreAl bond during Short PCT - (a) Smaller induced stress during bonding process, (b) Stress induced during PCT and (c) Finally cratering formation.

submitted to short but strong current pulses the stitches zones were stressed more and more along the time.

On the other hand, a diode (P-N junction material) in reverse bias, describes a bigger "depletion region" in the P-N junction while is able to block electron passages, blocking the current that passes through of them. The reached blocking voltage depends on the state of this barrier.

Therefore, considering the stressed diodes after bonding process, during Short PCT an additional stress is induced. The depletion region starts to decrease because at small cracks ($< 46\mu m$) and the leakage current finds a way (in the depletion region) where the potential is lower then the others (see figure 5.33). This happens only if the generated cratering does not break the P-N junction.

The P-N junction is not completely broken, but the surface of craters reduces the possibility to have a constant depletion region. This could explain why devices show a stable trend direct biased and not reverse biased.

Therefore, to confirm that the V_{BR} degradation was caused by the cratering, under the stitch wires, a Thermal Emission analysis was made on one diode reverse biased. The figure 5.34 revealed the presence of a hot point under one the bonding wire, which corresponds to a silicon cratering after wire removal by chemical etching.

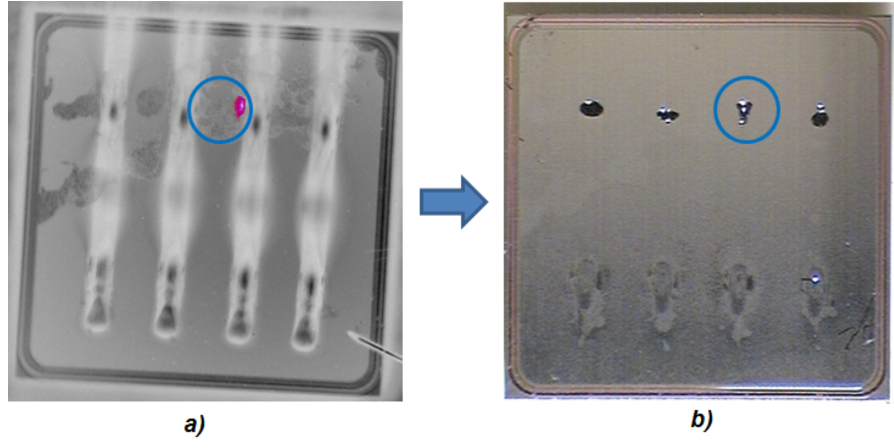


FIGURE 5.34: Thermal emission analysis - (a) Hot spot under CucoreAl wire and (b) Silicon cratering in correspondence of hot point after chemical etching.

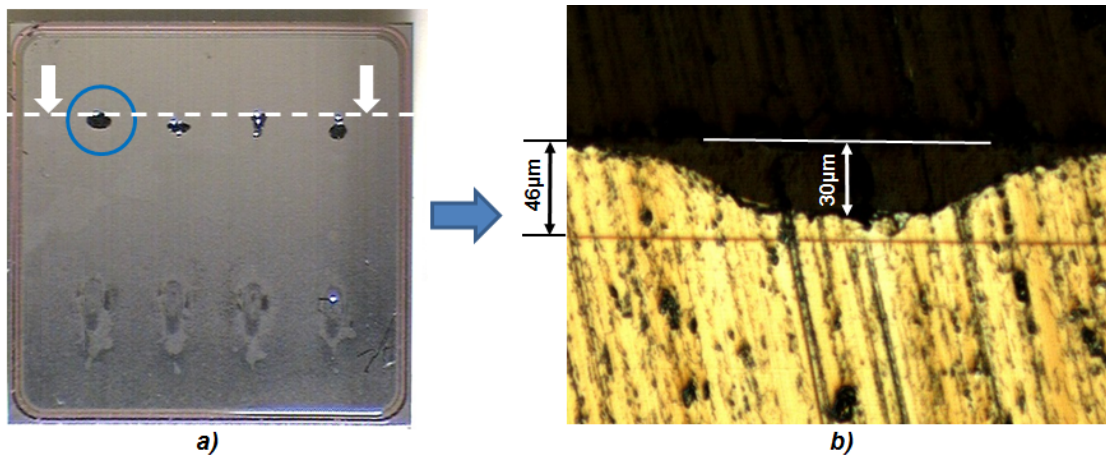


FIGURE 5.35: Cross-section analysis - (a) Indication of sectioned area and (b) Crater magnification with measurements.

In addition, a die cross-section analysis at cratering level was realised in order to assess the craters depth. The figure 5.35 shows that the damage caused by the craters was close to the epilayer or P-N junction ($< 46\mu m$).

Summarizing, the experimental part demonstrates that **CucoreAl 60/40 12mils** could be a better solution in the way to increase the power module life time.
However a readjustment on the bonding parameters will be necessary in order to avoid the initial induced stress.

5.3 Conclusion

To summarize the CucoreAl 60/40 wire was selected to take advantage of copper properties combined to aluminium bondability.
A TCT analysis confirmed that the copper core of the wire reduces the stress in the critical points of the wire. The result was supported by SEM analysis.

A DOE experimental design was useful to determine the optimal bonding parameters (wire on die), verified by a shear test and electrical measures.
Subsequently, after bonding, a PCT test was important to reveal that power module reliability (with internal CucoreAl wire) was doubled compared to a standard structure (with internal Al wire).

Finally, failure analysis, demonstrated again the CucoreAl was less stressed then the Al wire.

Chapter 6

Conclusive Remarks

The framework of this thesis was the study of new materials and production processes, focused on “heavy wire bonding” and “die attach layer” applies in Power Electronics (power modules).

Heavy wires bonding plays a significant role in order to improve the overall module performance in terms of reliability and power capability.
Consequently, new combinations of materials and technologies are used to produce a better heavy wire bonding, upgrading their mechanical and electrical properties.
In this thesis, the research is centred on “sintering process of silver powder”, applied into a power module as die attach process. The advantages and disadvantages of this particular and innovative technology, when is included into an isolated and non-isolated standard power module (a non-laboratory samples), were analysed. Their reliability and characteristics were compared with “standard soldering process”.

- *Process* - Sintering offers the possibility to avoid the costly cleaning step and allows the possibility to control the obtained sintered area (it exactly corresponds to the chip area without voids formation).
- *Mechanical Adhesion die/substrate* - it requires specific metal surfaces, but the obtained value of shear test is very high and according with the bibliographic search ($> 30 - 40MPa$). In addition it is comparable with the SnAg(3.5) shear strength value ($\cong 40MPa$).
- *Reliability* - Concerning the presented samples, sintering and soldering technology showed the same reliability performance.
- *Thermal Characteristics* - Sintering improves the thermal characteristics of power modules. Namely, the Rth_{j-c} initial value of sintered modules (measured before

to Power Cycling Test) is lower than the soldered ones.
This is clearly evidenced in the case of non-isolated package (without DBC), where the sintered Rth_{j-c} value is nearly a half of soldered.

Furthermore, this thesis work evaluates the possibility of generating and avoiding Electrochemical Migration (ECM) when sintered silver is implemented into power modules.

- *Without Silicone Gel* - In absence of internal module environmental isolation (gel potting), dendrite growth occurs easily and swiftly in Ag sintered and standard solder parts. Moreover, there is a direct relationship between the applied voltage bias and time-to-fail (TTF).
- *With Silicone Gel* - The second test showed that silicone dielectric gel is a good candidate to avoid electro-chemical migration phenomenon. Up to $1000hrs$, low current leakage and zero presence of dendrites were found.
  Therefore, the Ag ECM can be drastically reduced and also managed in sintered modules as a low content silver metal standard structure.

On the other hand, the implementation of a new material called CucorAl 40/60 ("Cu" core and "Al" coated), the evaluation of the power module reliability and comparison with standards Al wires were studied and discussed.

- *Process* - This wire offers the possibility to exploit the excellent mechanical, electrical and thermal properties of Cu, without changing the chip metallization (high compatibility with standard chip technology).
- *Reliability* - CucorAl 60/40 presents a superior behaviour compared with "Al" standard wires.
  Higher temperature cycling capability and higher power cycling capability can be obtained. In addition, during the test the level of ageing or damages in the wire are lower during the test, if compared with a pure Al wire. Namely, no fractures and cracks were found at wire level.

This kind of heavy wire could be a good improvement in terms of increasing power module lifetime.

Future works

Silver powder sintering process

Because of the fact that the presented delamination, after Long PCT, could be a consequence of an oxidation of the “Ni” layer produced at high temperature through an uncontrolled atmosphere process (N_2) [32], a future work could be oriented to realize the sintering process under a controlled atmosphere. Furthermore it will be interesting to study possibilities to perform new combinations of BSM, differentiating BSM for soldering and BSM for sintering processes.

Electrochemical migration (ECM) evaluation

A future approach could consider in account the study of other environmental isolation materials, combined with other sintering materials, such as silver nano-powder (up to day not applied in industry).
In addition, the temperature could be included as a conditioning parameter to study how the ECM could be influenced by a temperature increment.

CucorAl 40/60 heavy wire

A future approach could be performing a readjustment on the bonding parameters, considering also a loop reduction, in order to avoid the initial induced stress (verifying by chemical etching). Consequently another round of Short PCT could be carried on to observe if an improved power module lifetime could be obtained.

Summarizing, these studies gave to **VISHAY Semiconductor Italiana S.p.a.**, the possibility to include a new reliability test (Short Power Cycling Test) in their Reliability Lab., in order to analyse the relation between the heavy wires bonding materials and the power module lifetime of their products. In addition, the possibility to include a new wire bonding material into their packages could be evaluated.

Finally, this thesis work allows the possibility to explore and to realise first steps pointed towards the inclusion of a new die attach technical process (sintering), enhancing first studies demonstrating good thermal and mechanical properties.

Appendix A

Shear Test

Die Shear Test

The purpose of this test is to measure bond strengths, to evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test is applied to internal bonds between die and substrate, called also “Chip to Substrate Joint”.

Traditional die shear testing involves the accurate landing of the load tool and positioning of the tool above the substrate. Testing is similar to standard ball shear tests and is performed in accordance with the scheme A.1.

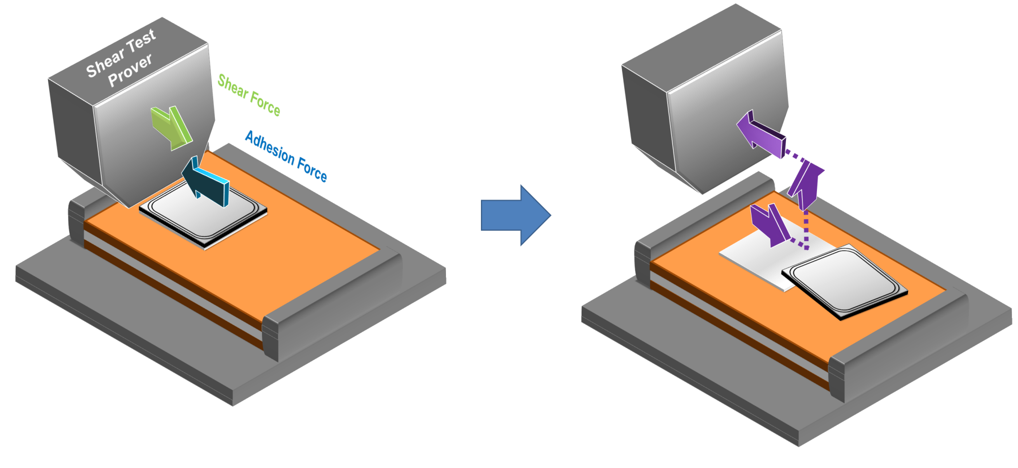


Figure A.1: Shear test scheme.

Test process: A suitable tool or wedge shall be brought in contact with the die (or carrier) just above the primary substrate (DBC). A force is applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond

failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

A.1 4000 Multipurpose Bondtester

Fabricated by Nordson DAGE, this tester is a multipurpose device, capable of performing all pull and shear applications. Ball Shear, Solder Ball Shear, Wire Pull Terser or Die Shear dependent on the system configuration, namely, this tester can be configured as a simple bond wire pull tester or upgraded for ball shear, die shear, bump pull, vectored-pull, or tweezer pull tests (see figure A.2).

FIGURE A.2: Nordson DAGE Shear tester - utilized instrument.

4000 Bondtester key features: - it uses patented frictionless load cartridges and air bearing technologies to ensure maximum accuracy, repeatability and reproducibility.
- Cartridges for different applications are readily exchanged.
- Many functions are automated with sophisticated electronic and software controls.
- Internal SPC software to provide basic analysis.
- System control is provided through an external PC running Windows.

For more information:
$http://www.nordson.com/en/divisions/dage/products/bondtesters$

Appendix B

Failure Analysis Instrumentation

On this part instruments utilized in the Failure Analysis will be described.

B.1 Curve Tracer

Created by Tektronics, the High Power Curve Tracer 371A (see figure B.1) is an electronic instrument applied on parametric characterization of semiconductors, failure analysis, manufacturing test, data sheet generation, process monitoring and quality control, incoming inspection, etc.

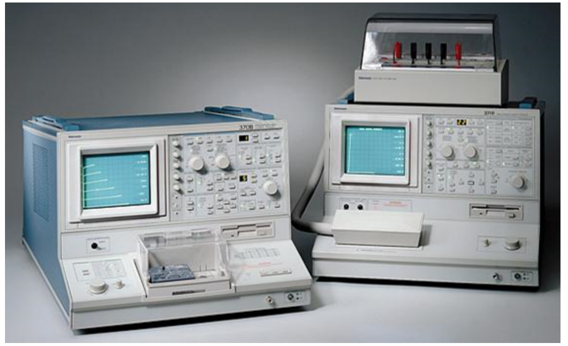


FIGURE B.1: Curve Tracer (photo from www.tek.com).

This instrument was utilized to measure the electrical static characteristics of the semiconductor devices (as for example V_{BR}, $I_{leackage}$, V_f, etc). On each case, depending to the necessary measure to realize, the tester was imposed to work on current or voltage mode.

Features, benefits and more information could be found at:
$http://www3.nd.edu/~nano/facilities/at_Tektronix370A_StorageCurveTracer.pdf$

B.2 Microscopes

B.2.1 Nikon Eclipse LV150

Fabricated by Nikon Corporation the Nikon Eclipse LV150, showed in figure B.2 the instrument is a digital imaging combined with advanced optical system.

FIGURE B.2: Nikon Eclipse LV150 Microscope (photo from www.nikonmetrology.com).

Some characteristics:
- it is a manual nose-piece type microscope, which meets the various needs of observation, inspection, research and analysis across a wide range of industrial fields (as optoelectronics, microelectronics, metal manufacturing, wafers, surface examination, etc),
- higher NA and a longer working distance,
- efficient digital imaging,
- max. sample size: $150x150mm$,
- is compatible with a wide range of observation methods: brightfield, darkfield, polarizing, differential interference, epi-fluorescence, and two-beam interferometry.

For more information:
$http://www.nikonmetrology.com/en_EU/Products/Microscope-Systems/Upright-Microscopes/Eclipse-LV150N$

B.2.2 Tagarno

Fabricated by Tagarno, the Magnus HD Trend (see figure B.3) is a digital microscope able to realise measurements easily and drawings on high-resolution images.

This digital microscope provides sufficient space for moving even large objects around under the camera and thereby creates good conditions when performing quality control procedures.
It combines high-definition image quality, magnification up to $320X$, live imaging at $60fps$ and built-in autofocus ensures a sharp image regardless of magnification size.

FIGURE B.3: Tagarno microscope (photo from www.tagarno.com).

Application: it can be applied on quality control or in developing a well functioning quality management system, failure analysis, etc.

For more information:
$http://www.tagarno.com/tagarno-magnus-hd-trend$

B.2.3 Leica Wild MZ8

Fabricated by Leica Microsystems, the Leica MZ8 stereomicroscope is a stereo light optical microscope, suitable for flat specimens investigation and utilized for the study of fracture surfaces, corroded surfaces, etc. As is showed in figure B.4 it is mounted on a stand and a gliding stage that can be quickly moved in any direction or rotated.

Some characteristics:
- Lamps: Reflection - bright field - polarisation.
- Objective lenses: Plan $1x$.
- Zoom: continuous with marked positions.
- Maximum magnification: $50x$.

Figure B.4: Leica MZ8 stereomicroscope.

B.2.4 C-Mode Scanning Acoustic Microscopy (C-SAM)

Fabricated by Hitachi, the FineSAT FS100 II Series is a High speed Scanning Acoustic Tomograph (SAT).

This instrument (see figure B.5) is able to evaluate in internal layers, the presence of delamination, voiding, and cracking non-destructively, utilizing ultrasonic waves[1].

Figure B.5: Scanning Acoustic Microscopy utilized.

[1]Ultrasonic waves are sound waves above $20KHz$ that cannot be heard by the human ear

Applications:
it is a non-destructive method of examining the inside of industrial parts using ultrasonic waves and is called an ultrasonic examination method. It has higher ability to detect cracks and dis-boding, and it is widely used for evaluating the reliability of electronic parts and performing breakdown analysis, stacked die, system-in-package, MEMS, etc.

Highlights:
- Maximum Scanning Speed: $1000 mm/sec$.
- High Definition Imaging: $67 Mega - pixel$ ($8192x8192 pixels$) and $0.5mm$ resolution.
- System Bandwidth: matches up to $500MHz$.
- Conventional and focused transmission probes, $10 - 25MHz$

Scanning Electron Microscope (SEM)

Fabricated also by Hitachi, the S-4500 Ultra High Resolution Scanning Electron Microscope (SEM) is a field emission scanning electron microscopy.

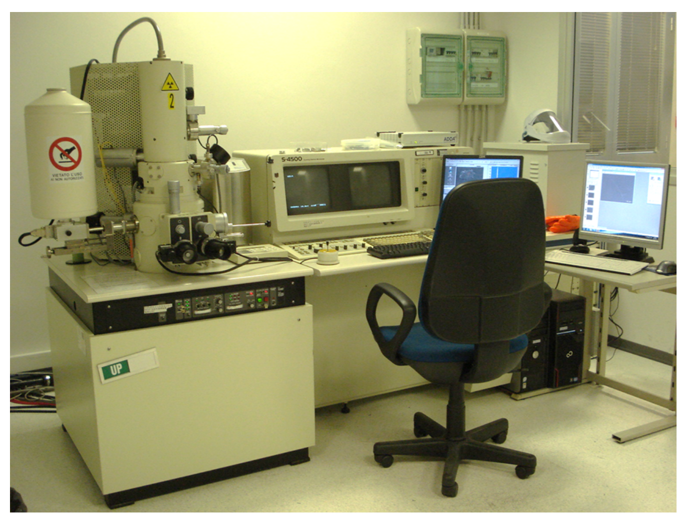


FIGURE B.6: Scanning Electron Microscope utilized.

This microscope (see figure B.6) provides high quality three dimensional images of the surface of a sample with a resolution of $1nm$. This is done by bombarding the sample with a beam of electrons, which interacts with the atoms of the sample to emit signals about the surface of the sample, i.e., the generation of secondary electron from the sample surface.

Furthermore, the S-4500 Hitachi Ultra High Resolution SEM is equipped with an energy dispersive X-Ray fluorescence detection system for Elemental Analysis.

B.2.5 Thermal Emission

Fabricated by Quantum Focus Instruments Corporation (QFI), it is an advanced microscope able to accept multiple sensors, covering a broad range of analytical techniques for failure analysis requirements and semiconductor industry (see figure B.7).

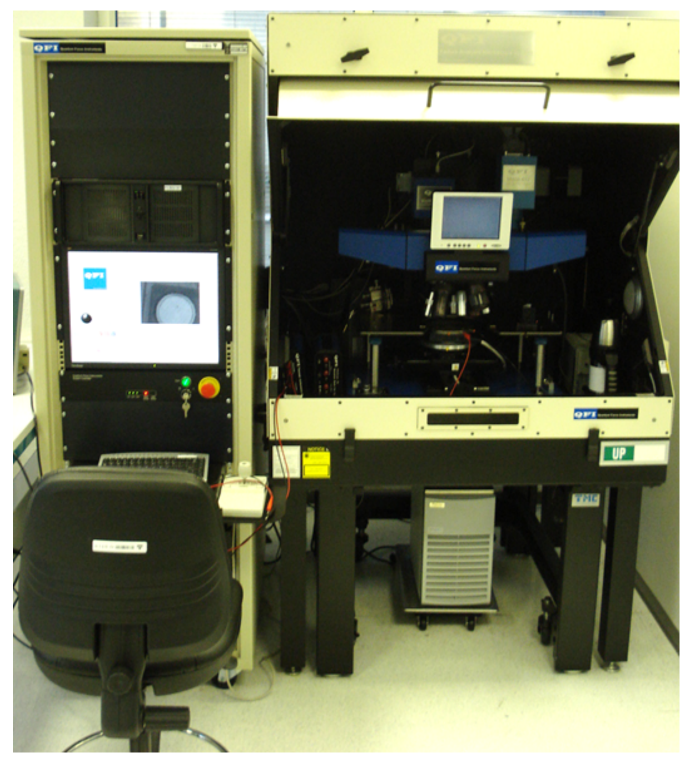


FIGURE B.7: QuantumScopeTM microscope utilized.

A single QuantumScopeTM configured with a multiple sensor microscope head can locate open lines, ohmic shorts, impedance issues, leakage currents, leaky capacitors, timing errors, oxide defects, resistive vias, latchup, ESD damage, and dynamic failures.

Failure analysis microscopy solutions:
- emmiTM Photoemission Microscopy
- XIVATM LSIM Laser Signal Injection Microscopy
- Thermal-HS MWIR Hot Spot Detection Microscopy

For more information:
http://www.quantumfocus.com

B.3 Polishing System

Figure B.8 shows this semi-automatic system, fabricated by MultiPrep. It is utilized for the sample preparation of a wide range of materials for microscopic (optical, SEM, EBSD, FIB, TEM, AFM, etc.) evaluation, cross-sectioning, serial/3-D preparation, wedge polishing, EBSD polishing, etc.

FIGURE B.8: Polishing System utilized (photo from: www.alliedhightech.com).

Some characteristics:
- it includes parallel polishing, angle polishing, site-specific polishing or any combination thereof.
- Dual micrometers (pitch and roll) allow precise sample tilt adjustments relative to the abrasive plane.
- A rigid Z-indexing spindle maintains the pre-defined geometric orientation throughout the grinding/polishing process.
- Digital indicators enable quantifiable material removal.
- Variable speed rotation and oscillation maximize use of the entire abrasive/polishing disc. - Adjustable load control to handle a range of small (delicate) to large samples.

For more information:
$http://www.alliedhightech.com/Equipment/multiprep-polishing-system-8$

B.4 Chemical Fume Hood

The last utilized instruments was a Chemical Fume Hood (see figure B.9).
A fume hood is typically a large piece of equipment enclosing five sides of a work area, the bottom of which is most commonly located at a standing work height.

FIGURE B.9: Leica MZ8 stereomicroscope.

This is a type of local ventilation device that is designed to:
- protect the user from inhaling this toxic gases, limiting the exposure to hazardous or toxic fumes, vapours or dusts.
- protect the product or experiment (biosafety cabinets, glove boxes);
- protect the environment (recirculating fume hoods, certain biosafety cabinets, and any other type when fitted with appropriate filters in the exhaust airstream).

Secondary functions of these devices may include explosion protection, spill containment, and other functions necessary to the work being done within the device.

During this thesis work, the Chemical Fume Hood was used to realize all the necessaries chemical etchings, and cleaning processes to failures analysis.

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