Assessment of surge current capabilities of SiC-based high-power diodes through physics-based mixed-mode electro-thermal simulations

Assessment of Surge Current Capabilities of SiC-based High-Power Diodes Through Physics-Based Mixed-Mode Electro-Thermal Simulations

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SiC-based Schottky diodes largely outperform Si *pin* diodes in terms of switching loss; however, they show a comparatively limited ruggedness to power stress conditions, such as current overloads in high-power switching-mode power supplies (SMPS). In fact, high-current short pulses significantly increase the device temperature, resulting into a large degradation of the carriers' mobility. As a consequence, the slope of the *I* - *V* characteristic tends to zero, leading to thermal runaway and device failure. Improved surge current capabilities are being pursued either at the electrical level, by exploiting, e.g., more advanced structures such as Junction Barrier Schottky (JBS) diodes [1], or at the thermal level, through innovative solutions to heat dissipation, exploiting advanced package technologies and materials. The successful development of such approaches requires the availability of reliable simulations, able to accurately describe the interplay between the device (described at a physical level, including heat diffusion), the driving electric circuit, and the package thermal impedance. In this paper we apply such coupled methodology to the analysis of 4H-SiC based Schottky and JBS diodes, with the aim to assess the impact of device design and of thermal dynamics on the device ruggedness to current overloads.

The analyzed devices are fabricated on 4H-SiC epitaxial layers grown on heavily *n*-doped 4H-SiC substrates [2] and assembled in standard TO-220 packages. 4H-SiC electrical and thermal properties were modeled on the basis of recent experimental data [3], whereas Schottky barrier height and epilayer doping concentration were extracted from *I*-*V* and *C*-*V* measurements [2]. The physics-based model includes incomplete dopant ionization, temperature- and doping-dependent mobility, and bandgap narrowing [3]. The package equivalent thermal circuit, a single-pole RC circuit with 3.3 K/W thermal resistance and 10 ms time constant, has been extracted from thermal impedance measurements of packaged devices and FEM based thermal simulation of unpackaged devices.

First, we have validated the model against experiments concerning Schottky diodes (4 A rated current) driven by current pulses with pulse widths ranging from 0.5 ms to 6 ms, as reported in Fig. 1. Then, we moved to the analysis of JBS diodes (6 A rated current). Fig. 2 compares the results of the numerical analysis (left) and the experimental characterization (right) of prototype devices, with increasing ratio of *pin* to Schottky area, under short current pulses. Measured on-state voltage drop is larger than what expected from the theoretical model, probably due to an unexpected high contact resistance (about 2.3 10^{-4} Ω cm^2, as estimated from the low-voltage part of the measured *I*-*V* curve). Interestingly, such parasitic resistance, because of device self-heating, has a significant impact also on the high-current regime, as shown in Fig. 3 (left). Concerning the evaluation of surge current capability, Fig. 3 (right) reports a comparison between Schottky and 60% JBS diodes, both rated for 6 A operation, under 6 ms current pulse. Sustainable overload currents are expected to be about 25 A for the Schottky diodes and 40 A for the JBS ones. Such values are in good agreement with preliminary characterizations which have shown current surges of about 26 A for the Schottky diode and 46 A for the JBS. The improvement achieved by the JBS design hinges on the ability to induce a bipolar current path during surge condition. This is exemplified in Fig. 4 (left)

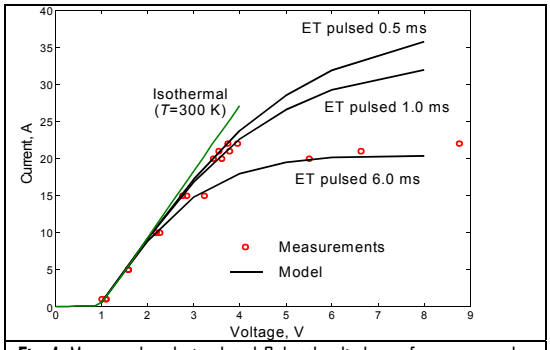

Fig. 1: Measured and simulated Schottky diode performance under pulsed current driving.

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showing the hole density distribution after 35 A, 6 ms current pulse: the injection of minority carriers into the low doped *n*-type epilayer is clearly visible. Finally, the time evolution of temperature, voltage, and *pin*/Schottky currents during 6 ms 35 A peak current pulses are shown in Fig. 4 (right) .

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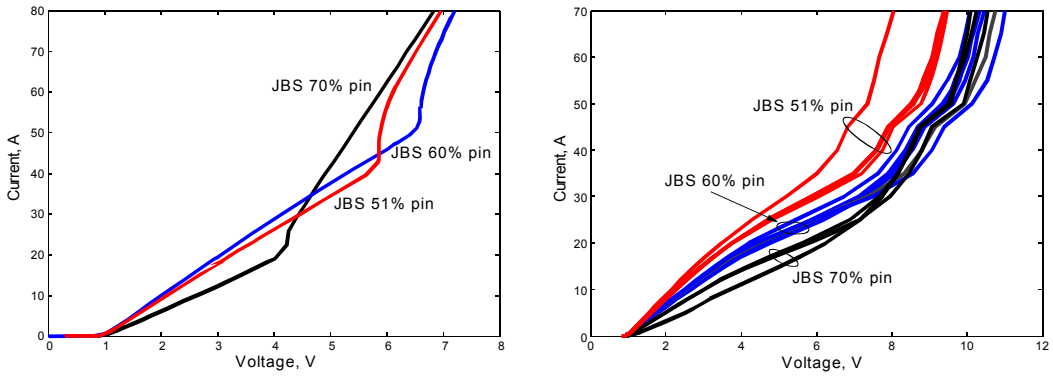

Fig. 2: Simulated (left) and measured (right) JBS diodes performance under pulsed current driving.

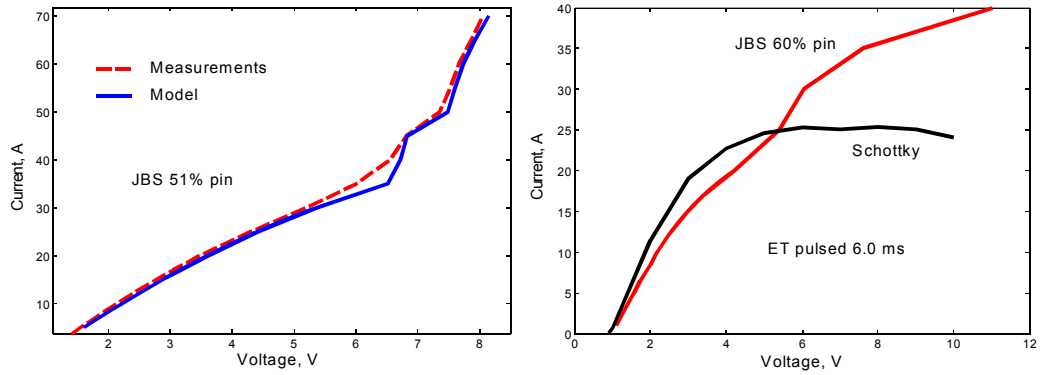

Fig. 3: Left: Effect of parasitic contact resistance on pulsed forward characteristic of 51 % JBS diode. Right: Simulated surge current test of Schottky and JBS diodes.

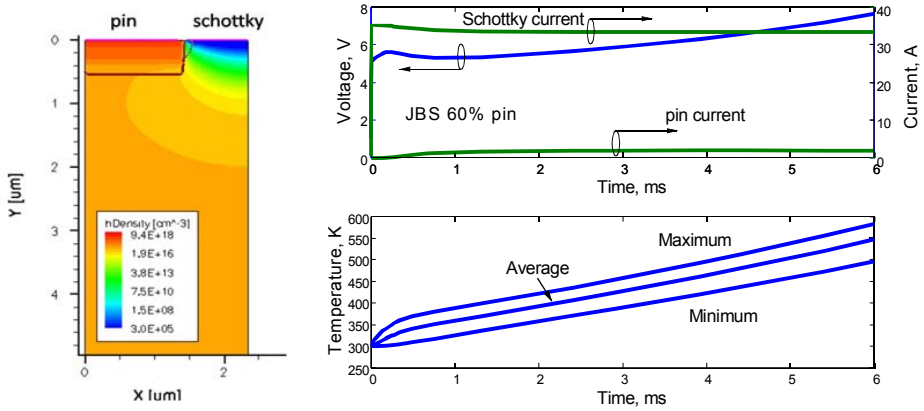

Fig. 4: Left: Hole density distribution after 35 A, 6 ms current pulse. Right: Voltage, current, and temperature time waveforms during 35 A current pulse.