Behavioural Model of Integrated Circuits for EMC Prediction

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Franco Fiori

Eln. Dept., Politecnico di Torino
Corso Duca degli Abruzzi, 24, Torino, Italy
franco.fiori@polito.it

Abstract— **This paper deals with the modeling of integrated circuits for electromagnetic compatibility (EMC) analysis.**
With reference to complex integrated circuits that usually include huge core logic blocks, analog and mixed signal circuits as well as power sections (smart-power system-on-chip), the paper shows a new behavioral model whose parameters can be derived on the basis of scattering parameters and switching noise measurements.
Through this new model, the electromagnetic emissions arising from such system-on-chip in application boards can be evaluated and mitigated before fabrication.

Key words: Electromagnetic Emissions, Integrated Circuits, System-on-Chip, Behavioral model, Parasitic Coupling.

I. INTRODUCTION

The strong development of semiconductor technology processes have brought about more and more complex integrated systems, which include an always rising number of logic switching gates as well as analog and digital front-end circuits.

In general, switching integrated circuits make steep currents to flow on-chip but also off-chip through the IC package lead frame, printed circuit board (PCB) traces and cables which behave as emitting antennas.

The electromagnetic emission originating from switching integrated circuits have been the subject of several investigations which has regarded the propagation of switching noise (both conducted and radiated) as well as the modeling of integrated circuits as primary sources of interference.

In the last decades, several circuital models like ICEM [1] have been developed to support engineers in the design and development of application boards with electromagnetic emissions constraints [2, 3].

Such models include an equivalent circuit of each block composing the overall integrated system, so that the IC package is modeled by a passive lumped network, which connects IC pins and IC pads at silicon level, the power supply network on silicon and the substrate parasitic coupling is also described by lumped elements, while each switching building block is modeled by a current source sinking pulse-shaped current and an equivalent on-chip capacitor.

While the model parameters of the power supply network and that of the substrate coupling are derived from scattering parameters measurements, those of core switching gates come out from computer aided analysis: the power supply switching current of analog and mixed signal circuits is obtained by transistor level simulations, while that of huge core blocks is evaluated by means of proper logic simulators [4].

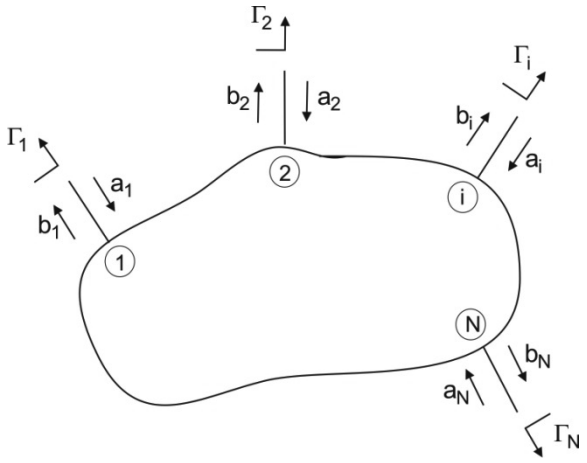

Fig. 1 A System on Chip is described here as a multiport time-variant nonlinear network. Electric power flows through the ports depending on coupling among ports and external loading.

Furthermore, the switching current of I/Os is usually described referring to behavioral models like those described in [5, 6].

The identification of model parameters as well as the waveform of current sources describing internal system activity are difficult to be performed especially for application designers who are not familiar with tools for IC analysis and design.

Based on that, the paper proposes a simple and effective method to build up the behavioral model of complex SoCs for EMC analysis, whose parameters are derived on the basis of experimental test results.

The paper has the following structure: in Section II the new behavioral model and how its parameters can be extracted is discussed, while a case study including the EMC model extraction and its validation for a smart-power SoC is shown in Section III. Some concluding remarks are drawn in Section IV.

II. THE BEHAVIORAL MODEL

Common System-on-Chips like microcontrollers or smart-power integrated systems include at least one huge logic core block as well as analog and mixed-signal circuits, which share the same silicon substrate. Such components are usually encapsulated in plastic packages, which allow integrated circuits communicating with off-chip components through metallic interconnects (lead frame and bonding wires). From the electrical point of view, an integrated system behaves as a nonlinear time-varying passive system, whose operation draws and delivers electric power at its ports from/to the external (off-chip) components. Each port is loaded by a certain circuit having frequency-dependent power reflection coefficient (Γ_i) so that, interference originating from the switching of internal circuits is spread among these ports depending on external loading and on wanted/unwanted coupling with the primary sources of switching noise.

Basically, a SoC behaves like a multiport source of switching noise, which feeds PCB traces and cables that radiates electromagnetic emissions.

This paper shows a new macro-model of such interference sources, which includes the parasitic coupling among the IC terminals, a set of noise equivalent source which models the switching noise of core blocks, and the equivalent circuit for each switching output driver.

All model parameters can be derived from experimental results, ignoring any information about the IC physical design, technology-related parameters as well as package parasitic elements.

A. Parasitic Coupling

Let's now consider a generic SoC encapsulated in a plastic package, having N terminals (pins) and m power supply couple of pins. The IC to be modeled is assumed to be mounted on a test board just above a complete PCB ground layer.

Each pin of the IC and the PCB ground will be referred to as IC port except for the IC ground pins, which will be assumed shorted to the PCB ground. Furthermore, the system is assumed to be properly biased through its power supply pins by means of bias tees.

Assuming now to stop completely any system operation (including clock tree), a small signal model of the parasitic coupling among IC ports, i.e. a time-invariant linear equivalent circuit can be extracted, on the basis of two-ports scattering parameters measurements. In principle, the measurement of a multiport scattering parameter matrix, by means of a two-port Network Analyzer (NA) would be cumbersome because each IC port, that is not connected to the NA should be loaded by the port reference resistance (R_0). Actually, the elements of this $N \times N$ S-parameter matrix can be derived from a set of two-ports scattering measurements, to be performed with the remaining $(N-2)$ ports of the system loaded with a set of known impedances of arbitrary value (for instance, the $(N-2)$ ports can be left open) [7].

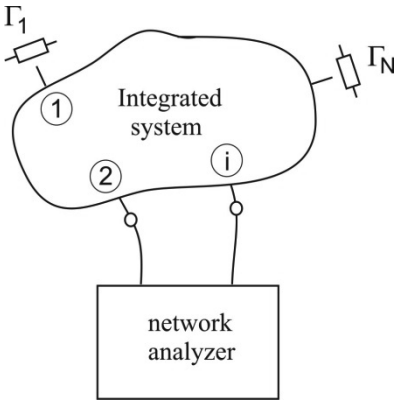

Fig. 2 Measurement of the scattering parameters measurement by means of a two-ports network analyzer.

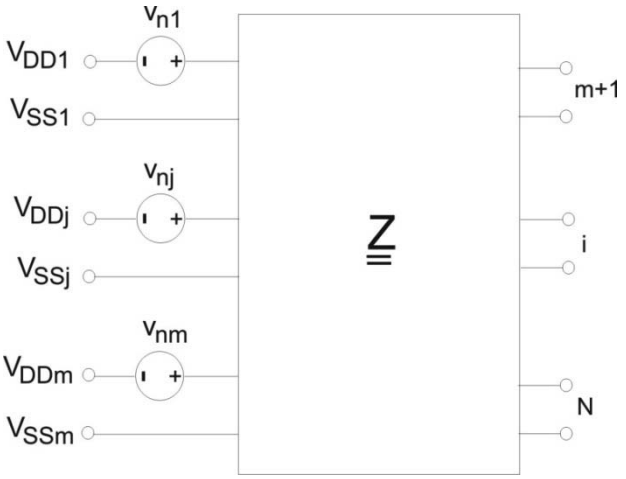

Fig. 3 Schematic description of the proposed behavioral model.

In particular, the N-ports scattering matrix can be derived as follows:

- Measure the $\frac{N(N-1)}{2}$ two ports matrix $(\boldsymbol{S_2})$. Create each two-port by connecting $N-2$ of the N terminations to the N-port.
- Convert each of the two-port S-parameters to Gamma-R parameters as follows:

$$\boldsymbol{R_2} = (\boldsymbol{\Gamma_2}^* + \boldsymbol{S_2})(\boldsymbol{1} - \boldsymbol{\Gamma_2 S_2})^{-1} \qquad (1)$$

  where $\boldsymbol{\Gamma_2}$ is the diagonal matrix which includes the reflection coefficient (Γ_i) of port loads with all $(N-2)$ rows and columns corresponding to the terminated ports eliminated.
- Fill the $N \times N$ Gamma-R matrix ($\boldsymbol{R}$) with the Gamma-R parameters derived from the two-port measurements.
- Convert the final $N \times N$ Gamma-R matrix back to S-parameters as follows:

$$\boldsymbol{S} = (\boldsymbol{1} + \boldsymbol{R\Gamma})^{-1}(\boldsymbol{R} - \boldsymbol{\Gamma}^*). \qquad (2)$$

Once we get the overall S-parameter matrix, it can be further worked out to describe the system through the impedance or the admittance matrix.

B. Switching noise equivalent sources

Let's now consider the same integrated circuit, whose core logic gates are now made executing a certain code, so that they generate switching noise, which propagates throughout the chip, affecting the nominal signal at each pin.

Actually, such disturbances are related to the voltage bounce at the inner power supply pads of core logic gates [8], so that the model of the overall integrated system is made of the small-signal noiseless admittance matrix fed at the power supply ports by equivalent voltage sources (one for each independent power supply pin) as it is sketched in Fig. 3. Each voltage source in the model describes the switching noise of circuits drawing current from that power supply pins (V_{DDj}, V_{SSj}).

The waveform of such equivalent voltage source can be derived from the voltage measurement at i-th port, which is loaded by the reference resistance R_0, the power supply pin of the switching core blocks (V_{DDj}) loaded by a bypass capacitor and all the other ports left open.

In this framework, the j-th equivalent source can be expressed as

$$v_{nj} = \left[\frac{Z_{jj}}{Z_{ij}}\left(1+\frac{Z_{ii}}{R_0}\right)-\frac{Z_{ji}}{R_0}\right]v_{im} \qquad (3)$$

where Z_{jj}, Z_{ij}, Z_{ji} are elements of the impedance matrix, v_{nj} is the equivalent switching noise source at the j-th port and v_{im} is the voltage, which has been measured at the i-th port of the noisy integrated system. This expression is valid for SoCs having one pair of power-supply pin, which is loaded with a bypass capacitor. Similar expression can be found for devices having an higher number of independent power supply.

In the proposed model, the noise equivalent sources show waveforms which drive the noiseless admittance matrix, so that voltages resulting at the IC ports equal disturbances, which can be observed at the same ports of the noisy integrated system.

Finally, the disturbances originating from switching output buffers are described in this new model by means of common behavioral models like those described in the literature [5,6], which has to be connected in parallel to corresponding ports of the above mentioned impedance matrix.

III. Experimental results

The above described model has been extracted for a smart power SoC, which include a huge core logic block, analog and mixed-signal circuits as well as several power transistors. It shows three power supply pins: one for the core logic gates, another for the analog blocks and an high voltage supply (car battery voltage) for output buffers and power transistors. The IC is encapsulated in a 80 pin quad flat package.

The new model has been extracted for a reduced number of pins. In fact, power supply and ground pins as well as pins of circuits usually connected to long PCB traces or cables (unit connector) has been considered, while the remaining pins have been connected to circuits and loads as suggested by the silicon-maker application notes.

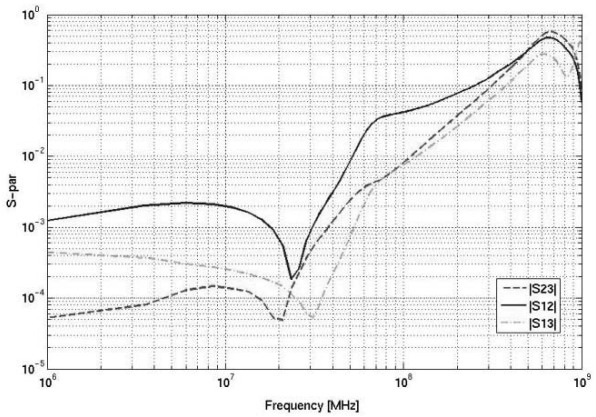

Fig. 4 Transmission scattering parameter between the power supply of core logic (port #1) and a power the drain of two different power transistors (ports #2 and #3) integrated in the same chip.

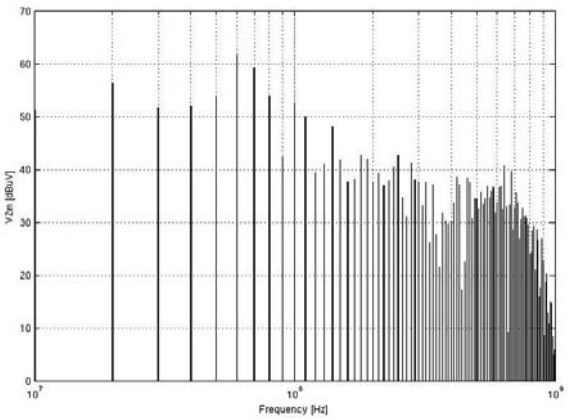

Fig. 5 Spectrum of the disturbance at the drain of a switched-off power transistor (port #2) of a smart power System on Chip due to the switching noise of core logic gates. The spectrum has been measured with reference to 50Ω.

The IC has been properly biased at its power supply pins through three bias tees and the S-parameter matrix has been extracted on the basis of two-ports S-parameter measurements with the remaining ports left open [7]. To this purpose, Fig. 4 shows the parasitic coupling among blocks of the same SoC, which are not connected each other by metal interconnects but they share the same package and the same silicon substrate. Being port #1 the power supply of the core logic block and port #2 and #3 the drain terminals of two switched-off independent power transistors, the scattering parameters shown in Fig. 4 highlights that over 60 MHz, such a parasitic coupling becomes significant.

Afterwards, the test setup has been modified adding a 100nF bypass capacitor and connecting a 50Ω spectrum analyzer to port #2. The IC under test has been made executing a code repeatedly and the power spectral density resulting at port #2 has been measured (see Fig. 5).

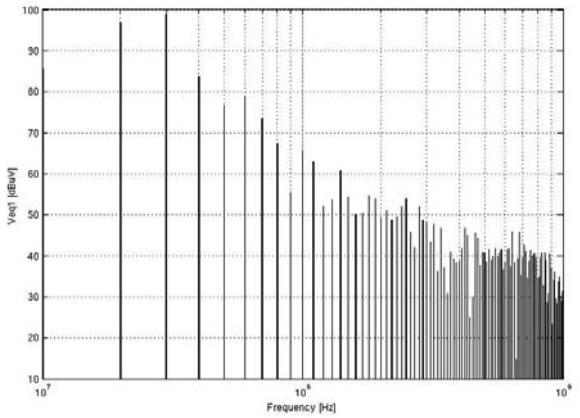

Fig. 6 Spectrum of the equivalent voltage source at the power supply port of logic switching gates, which has been obtained by the SoC S-parameters matrix and the voltage spectrum measured at port #2 through the method described in this paper.

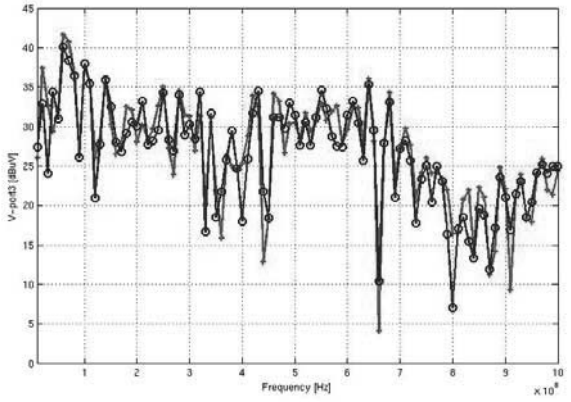

Fig. 7 Spectrum envelope of the disturbance at port #3 due the switching noise of core logic gates. Circles in blue have been obtained by experimental tests while red crosses have been derived with the new model.

Finally the equivalent voltage source at the core power supply has been evaluated using expression (3) and the result is reported in Fig. 6.

Additional measurements have been performed aiming at the validation of the new model. To this purpose, the switching noise resulting at port #3 has been measured with a spectrum analyzer and the remaining ports has been left open.

Finally, Fig. 7 shows with blue circles linked by the dashed line, the peak value of spectral harmonics, which have been obtained from measurements while crosses in red, linked by the solid line have been obtained using the above described model.

IV. CONCLUSION

In this paper a new model of complex integrated circuits for EMC analysis has been presented. It includes an N-ports scattering parameter matrix, which is fed at the power supply pin by voltage equivalent source. Unlike common IC model for EMC, the parameters of the proposed model can be evaluated on the basis of S-parameter measurements and switching-noise measurements.

Finally, the model has been extracted and validated for a smart power SoC, which is encapsulated in an 80 pin plastic package.

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