SOI versus Bulk Performance in Future CMOS Technologies for Low-Power Applications

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1. Abstract

The main field where Silicon-on-Insulator (SOI) is nowadays in use for high-volume production is that of high-performance high-speed devices. We show that using SOI in future technologies can be extremely beneficial not only for high-speed but most importantly to get a significant power reduction.

2. Introduction

SOI technology is currently used for high-volume high-performance devices, especially microprocessors (by companies like IBM and AMD), even if the low-power features of this technology, which might be exploited in other market segments, are well understood [1]. We show in this paper that using SOI in future CMOS technologies could be beneficial to get a significant power reduction while not sacrificing performance. To this aim, we used a physical charge-based MOSFET model, UFSOI [2][3]. Its most important feature for this work was the possibility to model both Bulk and SOI FET's sharing many process parameters, thus enabling a fair comparison of the two technologies with the same features, like gate length and oxide thickness.

We used the ITRS roadmap specifications for CMOS [4] and fit them in the UFSOI Bulk model in order to build a reference for technology nodes from 90 to 35 nm gate length. Then, the so built I/V characteristics were used to fit the SOI model, both Partially Depleted (PD) and Fully Depleted (FD), aiming at achieving the same ON-state current as in Bulk. DC results show that the OFF-state current is much lower in FD-SOI (with slightly improved ON current as well), while PD is not dissimilar from Bulk.

In AC, at the same power supply voltage of Bulk, the reduced capacitance contributes for a power reduction and an increase in speed for PD and more pronounced for FD. By decreasing the power supply in SOI and targeting the same speed as Bulk, the energy reduction for SOI devices becomes particularly significant.

3. ITRS Specifications and model fitting

The ITRS roadmap forecasts the characteristics of future CMOS devices and specifies gate length, voltage supply, gate oxide thickness, ON-state (saturation) current, OFF-state (subthreshold) leakage current, subthreshold swing (inverse of the slope of the IdVg characteristics in subthreshold) and parasitic source/drain resistance [4]. Using these inputs, it is possible to build the I/V characteristics of future MOS devices and to fit them in a suitable model like UFSOI [3]. The geometrical parameters can be taken from the roadmap while doping levels, mobility, DIBL, GIDL and gate oxide tunneling parameters have to be fitted. The procedure has been repeated for all roadmap technology nodes from 90 to 35 nm gate length. The model cards derived for Bulk transistors can been used as a reference for fitting PD and FD SOI models, according to the UFSOI manual. Many of the parameters do not change, like gate length and oxide thickness. We matched all lithographic parameters so as to make a fair comparison. There are a few SOI specific parameters to define or to fit. Some of them have been left at their UFSOI default value because of their unsubstantial impact or because the need of measurements on fabricated devices. We thus concentrated on doping levels, silicon film and buried oxide thickness that are (potentially) under control of the transistor architects. The usual procedure SOI technologists implement for high-speed devices consists in fixing the Ioff specification for both Bulk and SOI wafers and then exploit the larger Ion current [5]. Since our intent is mainly to prove the effectiveness of SOI for low power applications, we tried to keep instead the same Ion current and to exploit the reduced Ioff. The speed improvement at the same supply voltage is then only due to the reduced S/D capacitance and the current overshoot due to the floating body effects [1][2].

The thickness of the silicon film (Tsi) and buried silicon dioxide (BOX) have marginal impact on the performance of PD devices. On the contrary, in FD such parameters control both threshold voltage and subthreshold swing, due to the fringing field effect that couples drain and channel [1]. We thus derived an optimal value so as to meet the roadmap specs. Other works confirm our trend for optimal Tsi and BOX [6].

In Fig. 1 the 90 nm IdVg characteristics of Bulk, PD and FD devices are reported in a semilogarithmic graph, together with the Ion/Ioff constraints set by the roadmap specifications. Similar curves can be plotted for the more advanced devices up to the 35 nm gate length transistors.

Table 1 summarizes the DC characteristics of SOI devices compared to Bulk. For FD, silicon film and BOX thickness are also reported.

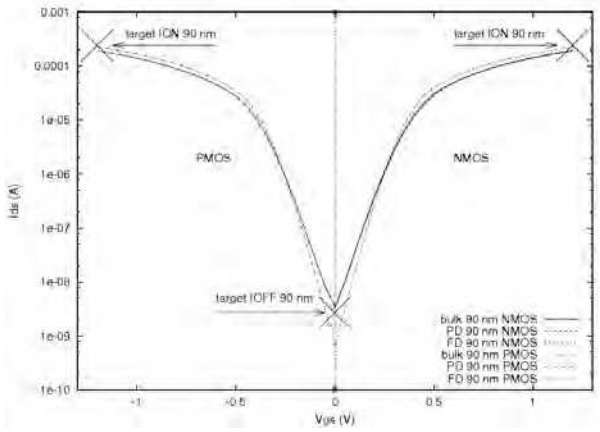

Fig.1: *90 nm devices IdVg characteristics.*

Tab.1: *PD and FD SOI vs. Bulk in terms of Ion and Ioff.*

Lg (nm)	Δ Ioff PD	Δ Ioff FD	Δ Ion PD	Δ Ion FD	TSi (nm)	BOX FD (nm)
90	-4.1%	-80%	3.8%	17%	16	200
75	-2.4%	-59%	2.8%	11%	15.5	200
65	-10%	-70%	3.9%	13%	14.5	100
53	-6.6%	-26%	2.4%	11%	14	100
45	-9.1%	-32%	2.2%	11%	12.5	100
40	-3.7%	-44%	7.1%	12%	12	50
35	-10%	-35%	1.2%	14%	11.5	50

In each technology, the SOI devices outperform the Bulk ones. The PD improvement is slight compared to FD that also shows a superior behavior in subthreshold.

4. Bulk, PD and FD AC comparison

We measured the fanout-of-four delay (FO4) in inverter chains (device under test loaded with 4 equal inverters), a test usually conducted to evaluate the technology speed [4]. The switching energy has been measured as well. In Fig. 2 the three technologies are compared in the energy-delay plane. For a given technology from 90 to 35 nm, PD devices are always better than Bulk both for delay and energy, while in turns FD is always better than PD. The PD delay improvement is in the range 9÷13% across all the roadmap nodes (average improvement 11%) while the FD one is 28÷37% (average 33%). The speed increase is due to the slight improvement in Ion and to the reduction of S/D parasitic capacitance (the gate capacitance is approximately the same). The superior delay performance in SOI is due to the fact that the S/D capacitance accounts for a smaller fraction of the total load. In fact, by using FO1 inverters instead of FO4 in ring oscillators, and so reducing the impact of gate capacitance over S/D parasitics, we obtained a 30% improvement in PD and record +135% in FD devices. The energy reduction, due to the reduced switched capacitance, is 11÷14% (average 13%) in PD and 14÷27% (average 23%) in FD.

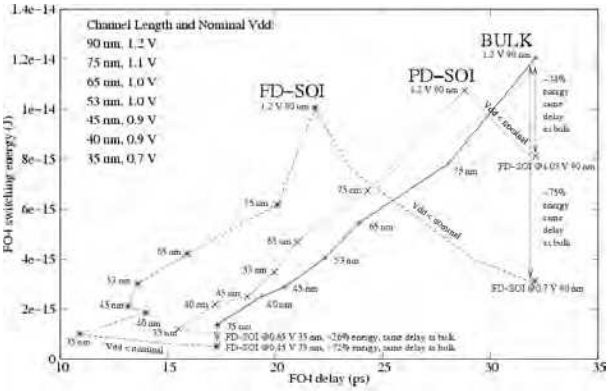

Fig.2: *Bulk, PD-SOI and FD-SOI delay and energy comparison.*

5. Voltage scaling for power reduction

One can decide to exchange the higher SOI speed with smaller energy consumption, by lowering the SOI supply voltage and targeting the same speed as Bulk devices. Fig. 2 shows that for the 90 nm technology, lowering Vdd from nominal 1.2V to 1.05V in PD allows a 34% energy saving at the same Bulk speed. For FD, at 0.7V, the energy saving is 75%. Similar results are obtained for all technologies. We reported only the 35 nm results varying Vdd in Fig. 2 for sake of clarity. The PD energy saving is 26% from 0.7V to 0.65V while the FD one is 72% at 0.45V, again at the same speed of Bulk devices with 0.7V supply voltage.

6. Conclusions

We compared the delay-energy figures of future CMOS devices in Bulk, PD and FD SOI technologies. SOI devices are shown to be suitable candidates for low-power applications. Best results are obtained for FD devices. The improvement is clear at the nominal supply voltage indicated by the ITRS roadmap. Moreover in SOI, a lower Vdd designed for having the same Bulk speed, helps reduce greatly the power consumption.

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