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Abstract

This paper addresses the modeling of output and power supply ports of digital drivers for accurate and efficient SSN simulations. The proposed macromodels are defined by parametric relations, whose parameters are estimated from measured or simulated port transient responses, and are implemented as SPICE subcircuits. The modeling technique is applied to commercial high-speed devices and a realistic simulation example is shown.

1 INTRODUCTION

The system level simulation of high performance digital circuits for signal integrity (SI) and electromagnetic compatibility (EMC) effects requires effective models of the Integrated Circuits (ICs) ports driving and loading interconnect structures.

Recently, a macromodeling methodology based on the estimation of parametric models from port transient responses has been proposed and successfully applied to real modeling problems [1, 2, 3]. This approach has specific advantages, making it a useful complement to the traditional modeling approach based on simplified equivalent circuits of the device ports [4].

In this paper, the parametric modeling approach is applied to the modeling of output and power supply ports of IC drivers. Different parametric relations based on Gaussian Radial Basis Functions (RBF) and sigmoidal (SIG) functions as well as different parameter estimation algorithms are tested. Accurate and efficient models are demonstrated for high-speed commercial drivers and a realistic SSN simulation example is developed.

2 PARAMETRIC MACROMODELING OVERVIEW

The modeling of ICs for SI and EMC simulations amounts to finding suitable port relationships (which we refer to as "constitutive"), for a known logical activity of the ICs. As an example, Fig. 1 shows the typical structure of an IC output buffer (driver in the following) that can be considered as a three-port element, whose input port is connected to the IC internal logic and the other two ports are the output and the power supply ports connected to the external interconnects. The electrical behavior of output and power supply ports for such element can be described by the following constitutive relations

$$\begin{cases} i &= F_o(v, v_{dd}) \\ i_{dd} &= F_d(v, v_{dd}) \end{cases} \tag{1}$$

where F_o and F_d are suitable nonlinear dynamic operators.

For parametric macromodeling, the above constitutive relations are sought as dynamic nonlinear parametric equations. The use of parametric equations to model physical systems is conceptually simple and can be described by the three steps: (1) *model selection, i.e.,* the selection of the parametric relation defining the model (model representation hereafter); (2) *parameter estimation, i.e.,* the computation of the model parameter values so that the model responses

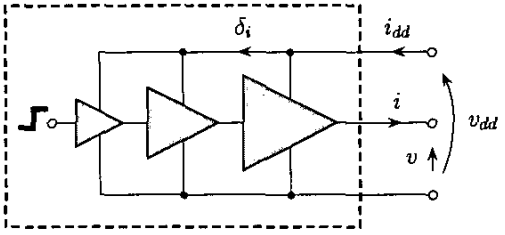

Figure 1: General structure of a driver circuit and its relevant (output and power supply) port electric variables.

mimic well those of the device under modeling; (3) *model implementation, i.e.,* the translation of the model in a circuit simulation environment by representing its equations with equivalent circuits.

Model selection is the most critical step of the modeling process, since a model representation far from the functional form of the real system can hardly reproduce its behavior. The model representation suitable for buffer circuits is searched for within the class of discrete-time parametric models. This is mainly due to the large availability of methods for the estimation of this class of models [5, 6]. Besides, this is the natural choice when the raw data, *i.e.,* the external responses of the system, are known as sampled waveforms. An additional back conversion to continuous-time is needed for the implementation of the model as a subcircuit, yet this is easily carried out via standard methods in step three of the modeling procedure [1].

A general discrete-time input/output parametric relation can be obtained by a nonlinear mapping defined by a sum of basis functions [6]. For a single input (extension to multiple input is straightforward) this writes

$$y(k) = g(\mathbf{x}(k), \Theta) \tag{2}$$

where y is the output, vector Θ collects the model parameters and the scalar function g maps the present and past samples of the input u and the past samples of the output into the present sample of the output. The mapped input/output samples are collected in the regressor vector

$$\begin{aligned} \mathbf{x}(k) = [&u(k), u(k-1), \ldots, u(k-r), \\ &y(k-1), \ldots, y(k-r)]^T \end{aligned} \tag{3}$$

where index r is referred to as the dynamic order of the model. Function g is defined by

$$g(\varphi, \Theta) = \sum_{n=1}^{p} \alpha_n \phi_n(\eta(\mathbf{x})) \tag{4}$$

where ϕ_n is the n-th basis function, obtained from a single mother generating function $\phi(\eta)$ by changing its spreading and its position

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(nonlinear parameters), α_n is a linear coefficient (linear parameter) and p is the total number of components (model size). Many different basis functions can be used in (4), giving rise to model representations with significantly different properties.

Parameter estimation relies on the information contained in a set of transient responses (*identification signals* hereafter) of the system under modeling $\{u(k), y(k)\}$, $k = 1 \dots N$, where N is the length of the sequences. For given values of the model size p and of the dynamic order r, model parameters are computed as solution of the following nonlinear approximation problem, usually cast as a least square problem

$$\mathbf{U} = \begin{bmatrix} u(1) \\ \vdots \\ u(N) \end{bmatrix} \approx \mathbf{g}(\mathbf{X}, \Theta) = \begin{bmatrix} g(\mathbf{x}(1), \Theta) \\ \vdots \\ g(\mathbf{x}(N), \Theta) \end{bmatrix} \quad (5)$$

Specific algorithms are available to solve this problem, that depends on the specific choice of the family of basis functions [6].

3 BASIS FUNCTIONS AND ESTIMATION ALGORITHMS

Presently, parametric macromodels based on Gaussian RBF expansions have been successfully applied so far to the macromodeling of the ports of digital ICs [1, 2, 3]. Gaussian RBF models belong to the generic class defined by (4), where the mother generating function is $\phi(\eta) = \exp(-\eta^2/2)$ and the n-th basis function ϕ_n is defined by the argument

$$\eta(\mathbf{x}) = |\mathbf{x}(k) - \mathbf{c}_n| / \beta_n \quad (6)$$

where $|\cdot|$ denotes the Euclidean norm and $\mathbf{c}_n$ and β_n are the nonlinear parameters defining the shape factor of the n-th basis function.

Gaussian RBF models offer remarkable advantages. Mainly, they are robust and have a regular and smooth behavior outside the fitting domain. The estimation of model parameters relies on simple and efficient algorithms [7, 8] in which the nonlinear least squares problem (5) is cast as an equivalent linear problem. This can be done since RBF models are weakly sensitive to the position of center and spreading parameters. In such a way, the set of possible center and spreading parameters are selected *a priori* and the nonlinear problem (5) is reduced to the estimation of the linear parameters only.

However, this is not the only choice of basis functions leading to models suitable for the approximation of a wide class of nonlinear dynamic systems. A complete overview of possible choices can be found in [6]. An alternate choice considered in this paper is the widely used class of SIG basis functions that are defined by a mother function $\phi(\eta) = \tanh(\eta)$ and by

$$\eta(\mathbf{x}) = \mathbf{v}_n^T \mathbf{x}(k) + b_n \quad (7)$$

where $\mathbf{v}_n$ and b_n are the nonlinear parameters of the basis function ϕ_n.

It is worth noting that, Gaussian RBF have spherical symmetry and finite spreading, whereas sigmoidal functions defined by (7) have planar symmetry and unbounded support. The planar symmetry is more suitable for fitting the actual constitutive relations of output and power supply ports of IC drivers. Thereby, (7) is a good alternative to Gaussian RBF for the problem at hand, leading to models with improved efficiency (less basis functions). Besides, for the approximation of mappings that exhibit a regular (*e.g.*, weakly nonlinear) behavior, Gaussian RBF representations can lead to models with a large number of basis functions. As an example, Fig. 2 shows the approximation of a one dimensional static mapping by the superposition of Gaussian bell shaped functions and of sigmoid functions within a specific domain.

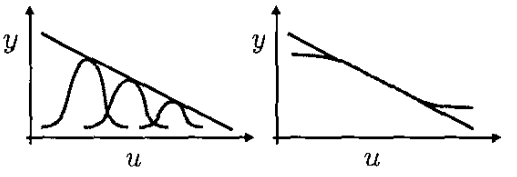

Figure 2: Approximation of a simple linear static $u - y$ relation by the superposition of different scalar basis functions (left panel: Gaussian bells; right panel: sigmoid)

Unfortunately, SIG-type models do not exhibit the nice property of weak sensitivity to the nonlinear parameters and therefore a fully nonlinear estimation algorithm is required to solve problem (5). Within the many possible estimation algorithms we found good results with the Levenberg-Marquardt method [10] and the procedure for the selection of the initial guess of parameters in [9].

As a final remark, supplemental information on the device being modeled, like its static characteristic $\{u_{sc}, y_{sc}\}$, when available, can be included in the model. This can be done by modifying the least squares problem (5) by stacking additional rows as follows,

$$\begin{bmatrix} \mathbf{U} \\ \mathbf{U}_{sc} \end{bmatrix} \begin{bmatrix} \mathbf{g}(\mathbf{X}, \Theta) \\ \mathbf{g}(\mathbf{X}_{sc}, \Theta) \end{bmatrix} \quad (8)$$

where $\mathbf{U}_{sc}$ is a column vector collecting the static values of the input variable $[u_{sc}(1), u_{sc}(2), \dots]$, and $\mathbf{X}_{sc}$ collects the regressor vectors built on the static characteristic (the present and past values of u and the past values of y in the regressor vector (3) are set to the same static values in $\{u_{sc}, y_{sc}\}$). The range of the static characteristic is usually chosen larger than the range explored by the transient input identification sequence stored in $\mathbf{U}$, ensuring the right static behavior over a wide domain.

4 OUTPUT AND POWER SUPPLY PORT MACROMODELS

This Section shortly reviews macromodels for output and power supply ports of driver circuits. The key problem for the development of a driver model is that the internal (logic) signal feeding the buffer is not a measurable quantity. In spite of this, the port model must allow for variation of the logic state. For constant values of the power supply port voltage, a parametric macromodel of the output port has been presented and thoroughly discussed in [1]. It approximates the output port constitutive relation with a two-piece model

$$i(k) = w_1(k) f_1(\Theta_1, v) + w_2(k) f_2(\Theta_2, v) \quad (9)$$

where f_1 and f_2 are nonlinear parametric models accounting for the port behavior in a fixed High or Low logic state, respectively and w_1 and w_2 are time-varying weighting coefficients for state switchings.

In order to include the effects of the power supply voltage v_{dd} in the macromodel (9), taking into account supply voltage fluctuations on the switching of logic devices, the v_{dd} variable is added as an additional input in the parametric models f_1 and f_2. The output port macromodel then writes

$$i(k) = w_1(k) f_1(\Theta_1, v, v_{dd}) + w_2(k) f_2(\Theta_2, v, v_{dd}) \quad (10)$$

The weighting coefficients describing state switching, instead, are constant with respect to v_{dd} owing to the properties of model representation (9) [1]. The transient responses for the estimation of the model parameters are obtained by driving the model devices with $v(k)$ and $v_{dd}(k)$ signals that are multilevel noisy waveforms [5].

The models of the power supply ports are needed for the simulation of switching noise effects and yield the driver supply current i_{dd} as a function of the supply port voltage v_{dd} and of the output port voltage v (see Fig. 1). The model representation exploited for the power supply port of drivers is

$$\begin{aligned} i_{dd}(k) &= w_{d1}(k) f_{d1}(\Theta_{d1}, v, v_{dd}) + \\ &\quad + w_{d2}(k) f_{d2}(\Theta_{d2}, v, v_{dd}) + \delta_i(k) \end{aligned} \tag{11}$$

where $\delta_i(k)$ takes into account the supply current drawn by the driver stages that precede the last one, and f_{d1} and f_{d2} are the parametric submodels of the current of the last driver stage when it operates in the LOW and HIGH logic states, respectively, and w_{d1} and w_{d2} are the usual weighting coefficients describing state switchings.

5 NUMERICAL EXAMPLES

In this Section, the parametric models of Section 4 with the basis functions described in Section 3 are applied to the modeling of commercial drivers. In the following, RBF and SIG indicate models composed of Gaussian RBF and of sigmoid functions, respectively, whereas SIG-SC denote models composed by sigmoid functions whose parameters are estimated by including information on the static characteristics, as shown in Section 3. All models are obtained from transient responses of detailed transistor-level model of the devices under modeling (hereafter references) and implemented as SPICE subcircuits. Reference and models are compared by simulating realistic test circuits.

Example #1. The first modeled device is the output port of a high-speed IBM CMOS driver ($V_{dd} = 1.8$ V) for servers operating at 250 MHz. For this device, both the complete RBF and the SIG type macromodels are estimated. For this example, we concentrate on the characterization of the output port only and assume constant power supply voltage equal to the nominal value V_{dd}.

As a first comparison, devised to highlight the differences among the possible choices of basis functions, both the RBF and the SIG parametric models are estimated for submodel f_1 of (10), *i.e.*, the dynamic $i - v$ port relation when the driver is forced in the fixed High output state. In this example, the dynamic order of submodels is $r = 1$. As an example, Fig. 3 shows the set of transient identification signals for submodel f_1. The identification sequences feeding the estimation algorithms are obtained by sampling the transient waveforms with a sampling period of 10 ps.

Table 1 shows the Mean Square Errors (MSE) computed during the estimation procedure for submodel f_1 and different values of the number of basis functions p included in the model. MSE values on the order of 1E-6 lead to macromodels reproducing the behavior of the device very well and make the predicted responses almost indistinguishable from the reference ones. It is worth noting that the same good accuracy obtained with RBF models for $p = 7$ is achieved with SIG-type models for $p = 1$, only.

For the same comparison, Table 2 lists the Mean sum of the Squares of the linear Parameters (MSP) in (4). The values in the table highlight the trend of the linear coefficients of a parametric model to grow up with p for the case RBF. Roughly speaking, this behavior is due to the numerical problem in approximation a mapping by means of the sum of a number of asymptotically vanishing functions larger than the number necessary to obtain a good fit. On the other hand, the choice of SIG-type functions and of the estimation algorithm [10] lead to models with always the same order of magnitude of the MSP.

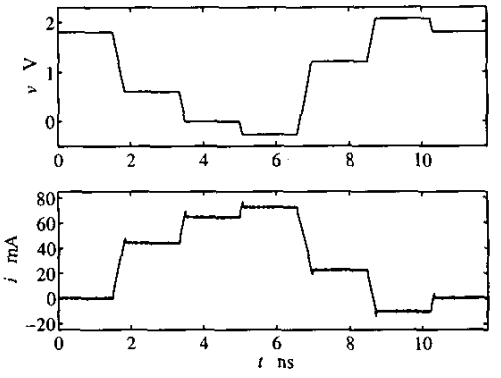

Figure 3: Port voltage waveform applied to the output port of the example device #1 forced in the High state and its port current response (identification signals for submodel f_1).

Table 1: Mean Square Error (MSE) between the output identification sequence and the model response to the identification sequences (approximation error). Both the RBF and the SIG type models are considered. The total number of basis functions p included in the models is in the range $[1, 10]$.

p	MSE(RBF)	MSE(SIG)
1	4.12e-1	**2.07e-6**
2	7.22e-2	8.30e-7
3	3.25e-4	8.28e-7
4	3.14e-4	8.11e-7
5	1.40e-4	8.78e-7
6	2.40e-5	8.48e-7
7	**1.63e-6**	8.87e-7
8	1.59e-6	8.82e-7
9	1.44e-6	8.88e-7
10	1.34e-6	8.65e-7

The complete macromodel (10) is estimated using the procedure detailed in [1] and Table 3 summarizes some results on the complexity and efficiency of possible macromodels. For this comparison, the RBF, SIG and SIG-SC type of parametric models are used. The table lists the number of basis functions p_1 and p_2, for the submodels f_1 and f_2, respectivey, and the CPU time required to compute a simple transient simulation test using the reference transistor-level models and two SPICE-like implementations of the macromodels. The test setup consists of the driver being modeled connected to a 100 Ω load resistor and producing a logic high pulse (bit pattern `"010"`). The speed-up factor introduced by the macromodels can be clearly appreciated.

As a realistic validation setup, the example driver #1 applying a logic high pulse on an open-ended ideal transmission line ($Z_0 = 100\,\Omega$, $T_d = 100\,ns$) is considered. Fig. 4 shows the near-end tran-

Table 2: Comparison between the Mean sum of Squares of the linear Parameters (MSP) of the RBF and of the SIG type models. The total number of basis functions p included in the models is in the range $[1, 10]$.

p	MSP(RBF)	MSP(SIG)
1	1.10	**3.30**
2	1.25	1.05e+1
3	8.22e-1	3.31e+0
4	3.56e+1	1.81e+0
5	1.26e+3	1.52e+0
6	8.97e+3	1.44e+0
7	**7.88e+3**	1.15e+0
8	6.57e+3	9.38e-1
9	4.85e+3	7.68e-1
10	3.05e+4	7.60e-1

Table 3: Number of basis functions of the possible macromodels of the example driver #1 and CPU time comparison for a simple transient simulation test (see text).

Macromodel	p_1	p_2	CPU time (PowerSPICE)	CPU time (Pspice)
reference	-	-	27 s	-
RBF	7	8	0.42 s	1.77 s
SIG	1	2	0.22 s	0.50 s
SIG-SC	3	3	0.30 s	0.80 s

sient voltage waveform computed through PowerSPICE and using the reference transistor-level model and the SIG-SC type macromodel. Curves obtained using the RBF and the SIG type of models are not reported since they are indistinguishable from that of the SIG-SC type.

An additional index on the model quality is obtained by computing the timing error, that is expressed as the maximum delay between the reference and the macromodel responses measured for a suitable voltage crossing (*e.g.*, 50 % of the voltage swing). As an example, for the curves of Fig. 4 the timing error is 7 ps (0.35 % of the bit time).

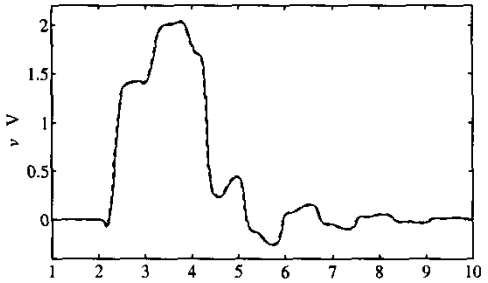

Figure 4: Near-end voltage waveform on an ideal transmission line driven by the example driver #1 (see text). Solid line: reference; dashed line: SIG-SC macromodel.

Example #2. The modeled device is a high-speed IBM CMOS driver ($V_{dd} = 1.32$ V) for servers operating at 500 MHz. For this device, both the output and the power supply port macromodels are estimated. In this example, only the SIG-SC type parametric models are considered.

The obtained output port macromodel (10) turns out to have submodels f_1 and f_2 composed of 8 and 11 basis functions, respectively. Whereas, the power supply port macromodel (11) has submodels f_{d1} and f_{d2} composed of 9 and 5 functions, respectively. All the submodels have dynamic order $r = 2$. As an example of the identification curves used in the estimation process, Fig. 5 shows the identification signals for submodels f_1 and f_{d1} that are recorded while the driver is forced in the fixed High state and the output and power supply pin are connected to ideal voltage sources producing the v and v_{dd} curves in figure. The identification sequences feeding the estimation algorithms are obtained by sampling the transient waveforms with a sampling period of 5 ps.

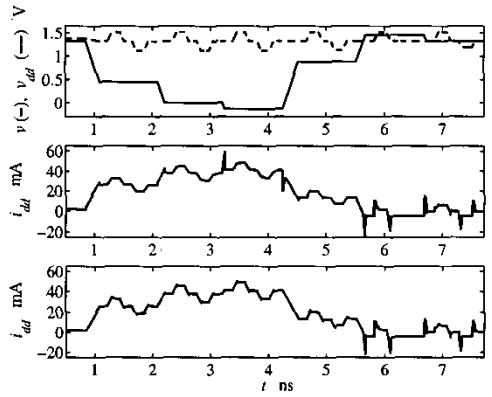

Figure 5: Identification signals for submodels f_1 (v, v_{dd} and i) and f_{d1} (v, v_{dd} and i_{dd})

As a validation test, Fig. 6 shows the driver port waveforms predicted by the reference transistor-level model of the device and by the macromodels while the driver applies a bit stream `"0100110010"` on a dynamic load (ideal transmission line with $Z_0 = 50\,\Omega$ and 0.3 ns) and the power supply pin is connected to a V_{dd} battery. The timing error for this test is 11 ps (1.1 % of the bit time).

6 SSN APPLICATION

In this Section, the proposed macromodels are applied to the simulation of SSN effects. The example test circuit is composed of M identical open-ended transmission lines driven by M replicas of the device modeled in Example #2 of Section 5. The power supply port of every driver is connected to a common power supply structure that is modeled by R_s, L_d and by the battery V_{dd} (see Fig. 7). The parameter values are: transmission line characteristic impedance $Z_0 = 50\,\Omega$, time delay $T_d = 0.3$ ns; $R_s = 1\,\text{m}\Omega$, $L_d = 0.1$ nH and $V_{dd} = 1.32$ V. All drivers switch simultaneously (bit stream `"0100110010"`) and the circuit waveforms are computed.

Figure 8 shows the reference and the predicted voltage and current waveforms at the output of a driver and the total power supply voltage and current waveforms for $M = 11$ simultaneous switchings. The model predictions and the reference responses are in good agreement. The parametric model involved in this test has been estimated for v_{dd} variations in the range $V_{dd} \pm 15\%$, whereas the v_{dd}

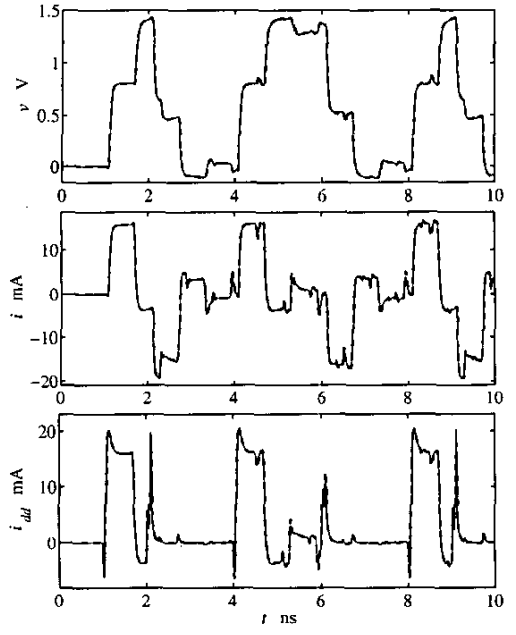

Figure 6: Near-end voltage waveform on an ideal transmission line driven by the example driver #2 whose power supply pin is connected to a V_{dd} battery (see text). Solid line: reference; dashed line: SIG-SC macromodel.

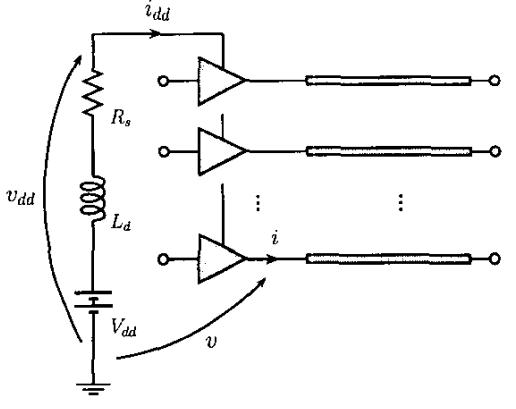

Figure 7: Test setup consisting of several identical drivers connected to transmission line loads.

variations for this case exceeds the modeling range. This means that the accuracy of the obtained model remains acceptable also on the boundaries of the v_{dd} modeling range. The timing error computed from the previous curves is 31 ps (3.1 % of the bit time).

A second example is defined by the previous test circuit with $M = 20$ asynchronous switching of drivers. The involved devices are the high-speed IBM CMOS driver with $V_{dd} = 1.8$ V considered in the example #1 of Section 5. For these devices, the estimated submodels f_1, f_2, f_{d1} and f_{d2} turns out to be composed of 3, 4, 3 and 5 basis functions, respectively, whereas the dynamic order of all submodels is $r = 2$. Each driver is assumed to switch with a Gaussian random delay with respect to a reference switching time. The variance of the delay is set to 100 ps and the circuit

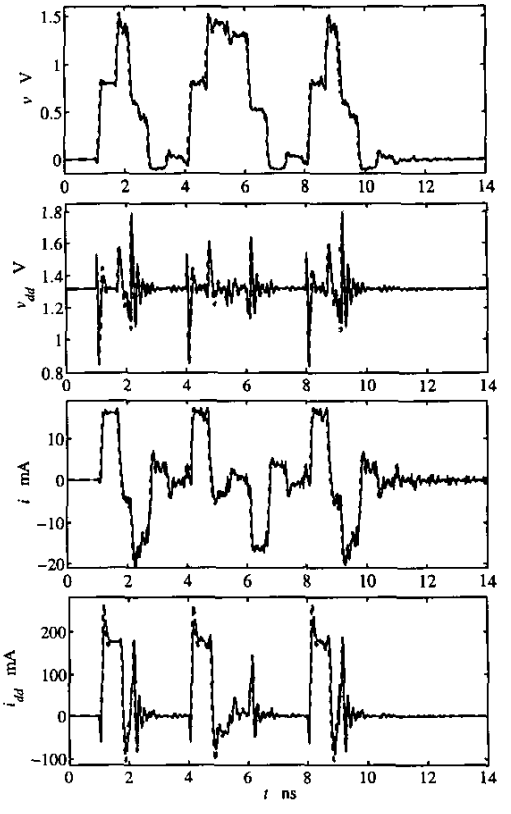

Figure 8: Voltage and current waveforms at the output of a driver and the total power supply voltage and current waveforms for $M = 11$ simultaneous switchings.

response is simulated for ten different realization of the distribution of switching delays. Figure 9 compares the predicted output port voltage waveforms (driver on top of Fig. 7) for the different switching delay realizations with the waveform computed when all drivers switch simultaneously. Similarly, Fig. 10 shows the same comparison for the power supply voltage waveforms.

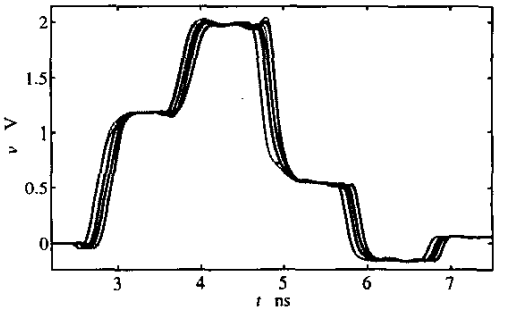

Figure 9: Comparison between the predicted voltage waveforms at the output of a driver $v(t)$ recorded for the ten different realizations of the random switching delays (gray lines) and the waveform obtained in the *worst-case* simultaneous switching situation (dark line).

The curves of Fig. 9 and 10 are computed for PowerSPICE. The

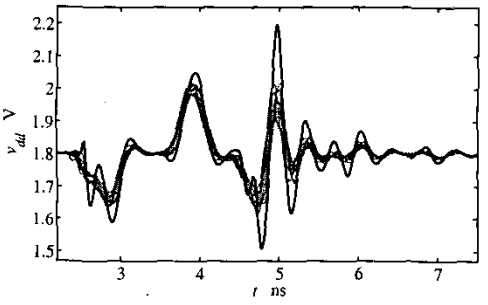

Figure 10: Comparison between the predicted power supply voltage waveform $v_{dd}(t)$ recorded for the ten different realizations of the random switching delays (gray lines) and the waveform obtained in the *worst-case* simultaneous switching situation (dark line).

CPU time required by the transient simulation is on the order of some ten seconds (50 s for this specific example) and confirms the efficiency of the proposed macromodels in handling the complexity of real simulations. It should be remarked that to carry out the simulation of the above example by means of device transistor level models would be a demanding task for both memory and CPU time requirements. Besides, Fig. 10 shows that simulation with randomly distributed switching times help better estimation of the power supply voltage fluctuations, because the peak fluctuation predicted for simultaneous switching is much larger than that predicted for nearly simultaneous switching.

7 CONCLUSIONS

The parametric modeling of the output and power supply ports of IC drivers is addressed, taking into account the influence of the model representation and parameter estimation algorithm. Parametric models defined by sigmoidal basis function of ridge type turn out to be particularly effective for the problem at hand. The proposed approach is applied to the modeling of commercial high-speed devices and its capabilities to handle the complexity of real simulation problem is demonstrated in a complete SSN example.

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