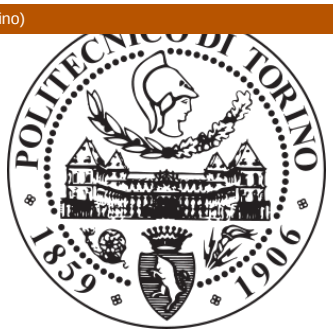

Reliable Eye-Diagram Analysis of Data Links via Device Macromodels

Reliable Eye-Diagram Analysis of Data Links via Device Macromodels

Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, Flavio G. Canavero, *Senior Member, IEEE*, and Claudio Siviero

***Abstract*—This paper addresses the impact of device macromodels on the accuracy of signal integrity and performance predictions for critical digital interconnecting systems. It exploits nonlinear parametric models for both single-ended and differential devices, including the effects of power supply fluctuations and receiver bit detection. The analysis demonstrates that the use of well-designed macromodels dramatically speeds up the simulation as well it preserves timing accuracy even for long bit sequences.**

***Index Terms*—Circuit modeling, digital integrated circuits, electromagnetic compatibility, macromodeling, signal integrity, system identification.**

I. Introduction

DATA transmission in modern information and communications technology (ICT) devices requires higher and higher bit rates, and the analog nature of transmitting digital data on interconnects becomes increasingly important. This trend involves interconnects and links at any scale, from chip to system level, and reproduces also at smaller scales the transmission problems that are typical of traditional data links. Thus, the designers need to worry more and more of the analog signals reaching the receiver input and the corresponding eye diagrams, from which information on the data link reliability and bit error rate can be extrapolated.

In the design phase, the prediction of received signals and the generation of eye diagrams is currently done by means of analog simulation. In order to highlight those critical effects like jitter, intersymbol interference, crosstalk, etc., simulations must be able to handle very long bit streams on transmission structures that are realistically modeled. This requirement inevitably calls for a simulation power that might exceed the capacity of available computers. Efficient models are, therefore, imperative, and a combination of driver and receiver macromodels with a clever solution method of long interconnects, and a reduced-order representation of connectors and junctions has been demonstrated to potentially enable the simulation of data link operation during the transmission of long bit sequences [1]. Of course, questions may arise about the accuracy of data link performances assessed by using device macromodels, that are approximations of reality. In particular, the accumulation of errors during the simulation of a very long bit-stream transmission might raise concerns about the validity of simulation results.

This paper is aimed at the discussion of the impact of device macromodels on the accuracy of signal integrity and performance predictions for critical data link of ICT devices and extends the preliminary study published in [2]. Fig. 1 shows the structures of typical single-ended and differential data links, that are composed of drivers (left side) and receivers (right side) communicating via an interconnect, and energized by a common power supply network. For these structures, the performance assessment requires the simulation of signals $v_2(t)$, $v_{12}(t)$, and $v_{22}(t)$ for checking timing and distortion effects, as well as of the eye diagram at the receiver level, essential for the prediction of the bit error rate of the link.

Both schemes of Fig. 1 define also $v_3(t)$, that is the analog output of the first receiver stage, where the input port receiver signal is compared with a threshold value. This signal v_3 is presently not considered by the designers, since it is not readily accessible in analog input-port models of the receivers. However, v_3 has two great advantages, i.e., it includes the threshold detection carried out by the receiver, and it carries additional information on the effects of the power supply noise and of electromagnetic interferences as they reach the logic core of the receivers. Later in this paper, we discuss the value of including v_3 in the receiver model and of using it for the performance estimation of an entire data link.

This paper is organized as follows. Section II briefly reviews the basic macromodels for single-ended and differential drivers and receivers and discusses the extension of the basic receiver models and the inclusion of the power supply fluctuations in differential driver macromodels. Section III discusses the impact of device macromodels for realistic application test cases. Finally, Section IV summarizes the results obtained.

II. Device Macromodels

A common approach to the modeling of devices is via simplified equivalent circuit representations, in which the information on the internal structure of the device is used to devise a simplified equivalent circuit. The equivalent circuit is composed of various blocks, accounting for a specific static or dynamic effect. A well-known example is provided by the input/output buffer information specification (IBIS) [3], that has been established as a standard for the description of the ports of a digital integrated circuit (IC), leading to a large availability of device descriptions and commercial tools handling models based on IBIS. When properly designed and estimated, IBIS models for regular devices have been proven to be accurate enough for the

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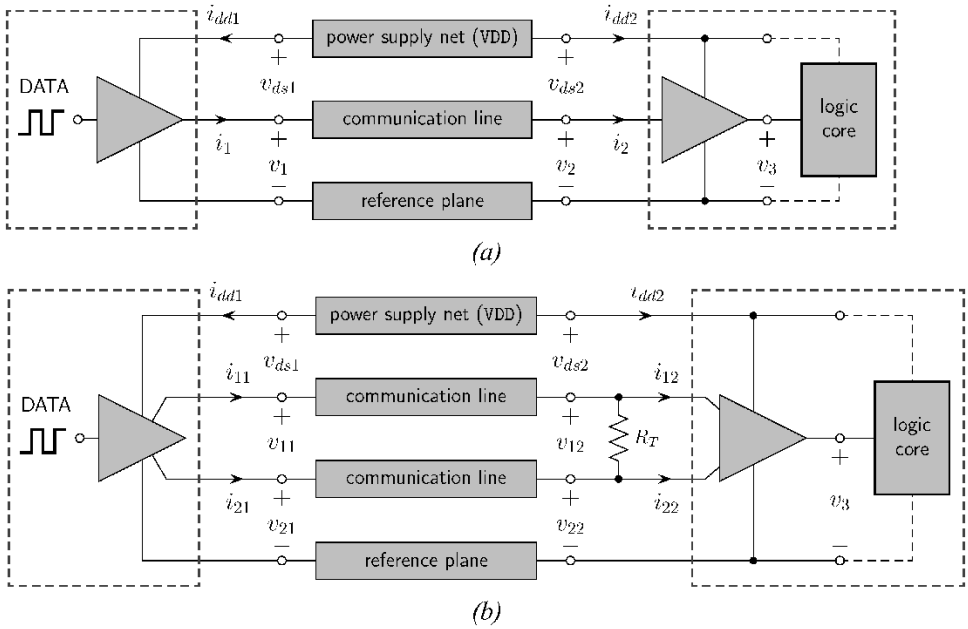

Fig. 1. Structure of a generic high-speed data communication link with the relevant blocks and electrical variables of interest. (a) Single-ended link. (b) Differential link.

simulation problems at hand. However, the growing complexity of recent devices, their enhanced features, and the possible inclusion of specific control circuitry, demand for greater refinements of the basic equivalent circuits, and call for the present version of IBIS to include external models. Such an extension, known as the *IBIS multilingual extension*, allows for the inclusion of models in different possible languages like SPICE or VHDL-AMS.

Within the extended IBIS framework, this paper proposes a possible modeling approach based on mathematical relations and circuit theory, with the aim of reproducing the electrical behavior of device ports, without use of physical details of the device structure or any circuit extraction. The advantage of this approach relies in the flexibility of the equations descriptions with respect to the circuit representation. In fact, the parasitic effects and some of the exotic effects inherent to the nonlinearity of devices are clearly more difficult to capture if we have at our disposal only capacitors, inductors, and resistors (even if nonlinear), while equations allow us to better fit the complex behavior of components. Besides, the proposed macromodels can be easily implemented in any simulation tool.

This section shortly reviews the basic macromodels of CMOS drivers and receivers. For drivers, we use the state-of-the-art $M\pi\log$ approach already detailed in [5] and [6]; a brief summary of the methodology is postponed at the end of this section. For receivers, we propose in Section II-A a three-port extension of conventional models, as anticipated in [6] and [8].

A. Receivers

The right side of Fig. 1 shows the basic structure of receiver circuits with their relevant electrical variables. For the sake of simplicity, the following discussion addresses first single-ended devices, then specific comments are presented for the case of differential devices.

Today's receiver macromodels usually consist of a single port, relating v_2 and i_2 variables, whereas a complete behavioral model of a receiver must relate the electrical variables of all ports, i.e., input, supply, and output ports of the device [7]. However, the knowledge of the activity performed by a receiver allows us to make simplifications of the functional relationships of the device. In fact, the strong nonlinear nature of the $(v_3,\ v_2)$ static characteristic, the possible enhanced detection mechanisms of the receiver input stages, and the fact that the activity of the logic core weakly reacts on the input port, suggest to represent the receiver as a nonlinear dynamic load acting at the input port and a controlled source delivering the detected "digital" signal at the output port. In addition, both input and output ports are affected and do influence the power supply port. The following equation set summarizes the above facts, in a more formal language, making use of the variables defined in Fig. 1:

$$\begin{cases} i_2(t) = F_2\left(v_2, v_{ds2}, \frac{d}{dt}\right) & \text{(a)} \\ v_3(t) = F_3(v_2, v_{ds2}) & \text{(b)}\ . \\ i_{\mathrm{dd2}}(t) = F_{dd}\left(v_2, v_{ds2}, v_3, \frac{d}{dt}\right) & \text{(c)} \end{cases} \tag{1}$$

A separate discussion with more details of the three equations above follows.

The receiver analog port relationship (1a) is conveniently expressed as a sum of a static and a dynamic part, as follows:

$$i_2(t) = F_2\left(v_2, v_{ds2}, \frac{d}{dt}\right) = f_s(v_2, v_{ds2}) + f_d\left(v_2, v_{ds2}, \frac{d}{dt}\right) \tag{2}$$

where f_s is the two-dimensional static characteristic of the input port of the receiver, and f_d is a general nonlinear dynamic model. The splitting of static and dynamic contributions is justified in the Appendix.

In (2), the static part f_s is approximated via a linear interpolation of the device port static characteristics computed for two different values of the power supply, as follows:

$$f_s(v_2, v_{ds2}) \approx \left(\frac{v_{ds2} - V_{\rm DD2}}{V_{\rm DD1} - V_{\rm DD2}}\right) f_s(v_2, V_{\rm DD1}) + \left(\frac{v_{ds2} - V_{\rm DD1}}{V_{\rm DD2} - V_{\rm DD1}}\right) f_s(v_2, V_{\rm DD2}) \quad (3)$$

where $f_s(v_2, V_{\rm DD1})$ and $f_s(v_2, V_{\rm DD2})$ are the static characteristics of the receiver current i_2 computed while the power supply terminals of the device are connected to a $V_{\rm DD1}$ and to a $V_{\rm DD2}$ battery, respectively. The two values of the power supply are set to 100% and 90% of the nominal value of the power supply. This choice leads to a static approximation (3), accurately reproducing the complete static surface for realistic values of power supply observed during normal operation of devices.

For the dynamic part f_d, (15) of the Appendix provides a general input–output discrete-time relation. Our recent studies [5] have shown that sigmoidal expansions can be effectively used for the parameterized nonlinear mapping F in (15), i.e.,

$$F(\cdot) = \sum_n \alpha_n \tanh\left(\frac{|(\cdot) - \mathbf{v}_n|}{b_n}\right) \quad (4)$$

where α_n is a linear parameter, and $\mathbf{v}_n$ and b_n are the nonlinear parameters defining the position and dilation, respectively, of the nth sigmoidal function. For the particular cases of devices showing a dynamic behavior dominated by linear effects, the general relation (15) reduces to an autoregressive equation (cfr. [13])

$$f_d(k) = \alpha_{01} f_d(k-1) + \cdots + \alpha_{10} v_2(k) + \alpha_{11} v_2(k-1) + \cdots + \alpha_{20} v_{ds2}(k) + \cdots \quad (5)$$

where α_{ij} are the model parameters. It is worth noting that simpler linear parametric models can hardly reproduce the nonlinear dynamic behavior within the region where the effects of receiver clamps are dominant.

A detailed discussion on the procedure for the generation of estimation signals and on the parameter estimation is out of the scope of this paper and readers should refer to [4]–[6], [8], where a similar procedure is discussed in details and applied to the modeling of IC drivers and receivers. Additional information and a demo tool for the modeling of nonlinear circuit elements are freely available from the Authors' web site http://www.emc.polito.it/.

For the modeling of differential receivers, the above procedure is extended, in the sense that two different relations must be used in place of (2) for the two port currents, as follows:

$$\begin{cases} i_{12}(t) = f_{s1}(v_{12}, v_{22}, v_{ds2}) + f_{d1}\left(v_{12}, v_{22}, v_{ds2}, \frac{d}{dt}\right) \\ i_{22}(t) = f_{s2}(v_{12}, v_{22}, v_{ds2}) + f_{d2}\left(v_{12}, v_{22}, v_{ds2}, \frac{d}{dt}\right) \end{cases}. \quad (6)$$

The receiver "digital" port relationship (1b) is conveniently expressed as a controlled voltage source, since the logic core behaves as a fixed load for the receiver output port. The advocated expression is

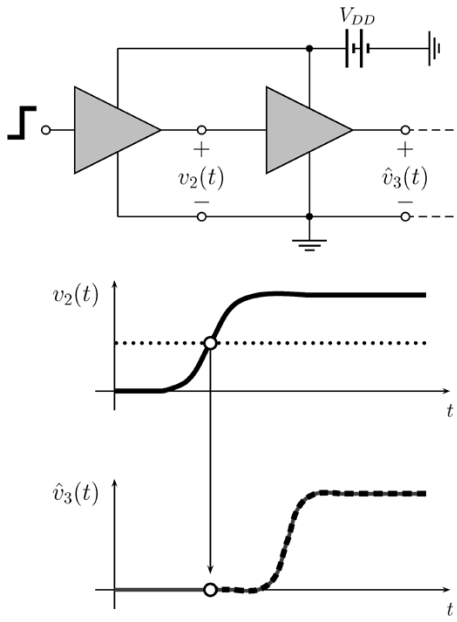

Fig. 2. Ideal setup for recording the basic up state transition of $\hat{v}_3(t)$ (the dashed-black curve in figure) that is triggered by a suitable voltage crossing of receiver input voltage $v_2(t)$.

$$v_3(t) = \hat{v}_3(t)\left(\frac{v_{ds2}(t)}{V_{\rm DD}}\right) \quad (7)$$

where $\hat{v}_3$ models the transmission between the receiver input and output ports, and the second term (in parenthesis) represents a linear correction due to the supply effects. This model is adopted to both single-ended and differential devices, to which the following considerations apply indistinctly. The basic element of expression (7) is $\hat{v}_3$, that is obtained by juxtaposing in time the elementary up and down state transitions of voltage v_3, consequent to up (or down) state transitions of the receiver input voltage v_2. As an example, Fig. 2 schematically shows the ideal setup for the generation of the basic up state transition of voltage v_3, for constant supply voltage. The state transitions of $v_3(t)$ are triggered when v_2 crosses a suitable threshold value (or more than one for a receiver with hysteresis) and the shape of the $v_3(t)$ edges is independent of the shape of $v_2(t)$, due to the internal structure of the receiver. It is worth noting that each elementary transition includes the delay between the v_2 and the v_3 state transitions. If necessary, the dependency of the delay on external parameters like the temperature or the v_2 slope in the threshold region, can be readily included. The linear correction factor of expression (7) is adopted on the assumption (confirmed by our experience of several devices) that $v_3(t)$ is roughly proportional to the power supply voltage $v_{ds2}(t)$.

A final comment on possible alternatives to model (7) is in order here. A simplified model consisting of a cascade of a static mapping and a linear dynamic system, as one might suggest at first sight, is inadequate, since it may generate misalignments of the juxtaposition of up and down transitions; thus, in turn, violating causality. On the other hand, more complex neural-network type of models trying to capture the entire detection

process of the receiver, are heavy in terms of simulation time, without significantly improving the accuracy of the advocated model (7), which already provides good results, as demonstrated in Section III.

The receiver power supply port relationship (1c) is conveniently expressed as a sum of a static (ϕ_{dd}, in the following) and a dynamic (ψ_{dd}) part, as suggested for the analog input port. For single-ended devices, (1c) takes the form

$$\begin{aligned} i_{dd2}(t) &= F_{dd}\left(v_2, v_{ds2}, \frac{d}{dt}\right) \\ &= \phi_{dd}(v_2, v_{ds2}) + \psi_{dd}\left(v_2, v_{ds2}, \frac{d}{dt}\right) \end{aligned} \tag{8}$$

while the relation for differential receivers is

$$\begin{aligned} i_{dd2}(t) &= F_{dd}\left(v_{12}, v_{22}, v_{ds2}, v_3, \frac{d}{dt}\right) \\ &= \phi_{dd}(v_{12}, v_{22}, v_{ds2}) \\ &\quad + \psi_{dd}\left(v_{12}, v_{22}, v_3, v_{ds2}, \frac{d}{dt}\right). \end{aligned} \tag{9}$$

All considerations expressed above for the case of the analog input port apply in this case as well, and are omitted for brevity.

B. Drivers

The driver macromodels employed for the simulations of the following section refer to a modeling procedure that is already well established and discussed in several publications. Only a short overview is provided here.

In essence, behavioral macromodeling of both single-ended and differential drivers amounts to devising a mathematical relationship between the analog port voltage and current variables, controlled by a bit stream. The experience of the IBIS standard and of our subsequent handling of real devices indicates that a two-piece model representation, driven by an externally-supplied bit stream, is the best way to create a driver macromodel.

For the single-ended driver of Fig. 1(a), this translates into the following relationship

$$i_1(t) = w_H(t) i_H\left(v_1, \frac{d}{dt}\right) + w_L(t) i_L\left(v_1, \frac{d}{dt}\right) \tag{10}$$

where i_H and i_L are dynamic submodels accounting for the port behavior at fixed logic high or low state, respectively, and w_H and w_L are weighting coefficients playing the role of the input signal and accounting for logic state transitions. A detailed discussion of possible representations for (10) can be found in [9], and a model extension, that includes the variation of power supply terminals (as used in this paper), as well as the inclusion of temperature parameter and the tri-state operation is discussed in [5]. Once the parameters defining (10) are estimated by means of the procedure outlined in the Appendix and discussed in [5] and [8], the above equation must be interpreted or synthesized in order to be included in standard circuit simulation environments. Such a synthesis enables standard analog mixed-signal simulators or circuit simulators, like SPICE, to solve signal integrity (SI) and electromagnetic compatibility (EMC) problems involving the real behavior of IC ports. The synthesis is carried out by converting (10) into a continuous-time state space realization, that can be directly described in metalanguages like VHDL-AMS or effectively implemented in any circuit simulation environment by its equivalent circuit representation. For the latter case, the output port current $i_1(t)$ can be implemented by a simple current controlled source, whose submodels i_H and i_L are represented by equivalent circuits consisting of standard circuit elements and controlled sources, and the weighting coefficients w_H and w_L as time varying ideal voltage sources. For more information, readers should refer to [8], where the above process is described in details, and an example SPICE script is also provided.

In a similar way, for the differential driver of Fig. 1(b), (10) translates into the following coupled relationship:

$$\begin{cases} i_{11}(t) = w_{H1}(t) i_{H1}\left(v_{11}, v_{21}, \frac{d}{dt}\right) + w_{L1}(t) i_{L1}\left(v_{11}, v_{21}, \frac{d}{dt}\right) \\ i_{21}(t) = w_{H2}(t) i_{H2}\left(v_{11}, v_{21}, \frac{d}{dt}\right) + w_{L2}(t) i_{L2}\left(v_{11}, v_{21}, \frac{d}{dt}\right) \end{cases}. \tag{11}$$

A detailed discussion of the above macromodel representation can be found in [6].

III. Discussion of Test Cases

In order to study the influence of device macromodels on data links performance assessment, we simulate the operation of the typical data links shown in Fig. 1 by using different combinations of driver and receiver models. The power supply networks are considered either ideal or modeled by a lumped equivalent (see next section), and no transitions or junctions are included in the transmission path, for the sake of simplicity. For all tests, transistor-level models of devices are used as reference, and specialized macromodels for drivers and receivers are derived from the responses of such transistor-level models, and are implemented as SPICE-like subcircuits. All the simulations are carried out by means of PowerSPICE (the IBM circuit solver tool, described in [18]) for the single-ended data link and HSPICE for the differential link. Two test cases are also considered, including or not the effects of the power supply network.

A. Single-Ended Data Link

In this case, the same high-speed IBM CMOS transceiver ($V_{\mathrm{DD}} = 1.8$ V) is employed as a driver and a receiver in the scheme of Fig. 1(a). The driver and receiver macromodels are the ones illustrated in Section II. Additional details of the transceiver utilized in this study and on the generation of its macromodels can be found in [2] and [8]. The interconnect between driver and receiver is an 8-cm-long multichip module (MCM) trace, that is modeled as a lossy dispersive transmission line (phase velocity $1.1765\ 10^8$ m/s, lossless characteristic impedance 55.3 Ω, dc resistance 24.4 Ω/m, skin effect coefficient $11.7\ 10^{-6}\ \Omega \cdot \mathrm{s}^{-1/2}$/m, dielectric loss factor $2.5\ 10^{-3}$). The data pattern used for this study is a 2048-bit-long sequence with 1-ns bit time and jitter error uniformly distributed in the range [−50, 50] ps.

The following simulation strategy has been adopted. A set of reference waveforms is computed by using transistor-level models for both the driver and the receiver. Then, two sets of

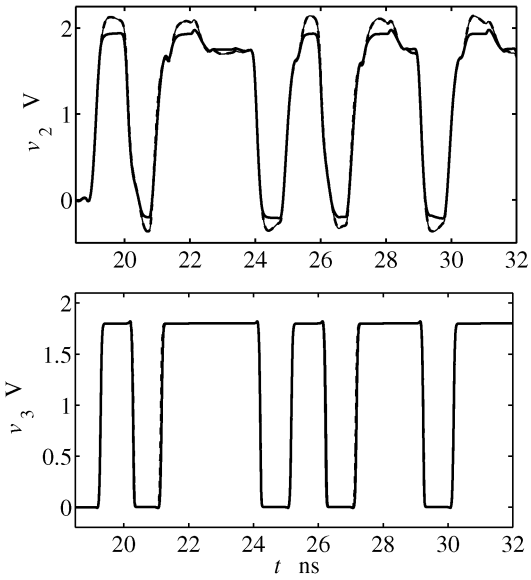

Fig. 3. Voltage waveform $v_2(t)$ for the test case #1. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

approximate waveforms are generated by using 1) a fully nonlinear macromodel for the driver, and a simplified linear parametric model for the dynamic term of the receiver (this set is labeled with **M1**) and 2) a fully nonlinear macromodels for both devices (labeled with **M2**). The goal is to provide comparisons between the reference and approximate waveforms, and to generate their corresponding eye diagrams, in order to estimate the impact of possible errors introduced by macromodels.

Test Case 1: As a first test case, we consider a simplified data link with an ideal power supply network modeled by a simple $V_{\rm DD}$ battery and a perfectly conducting reference plane, in order to exclude all possible power supply disturbances.

Fig. 3 shows the reference and approximate waveforms of the $v_2(t)$ and $v_3(t)$ voltages, for a duration of 14 ns, picked at random along the simulation of the entire bit pattern. A very good correlation among the different curves, especially during the transitions, indicates that the macromodels are capable of providing accurate timing information. In fact, the timing error on v_2 and v_3, computed as the maximum delay between the reference and the approximate waveforms at 0.9-V level, turns out to be always less than 1% of the bit time over the entire bit sequence for both set of approximate waveforms. The sole deviation of the **M1** curve from the reference is in the overshoots and undershoots regions, where the v_2 shape is mainly decided by the receiver clamps, and the corresponding macromodels implementing a simple linear dynamic part demonstrate (as expected) their inadequacy in the clamp regions. In spite of this, for both sets of macromodels, the accuracy of predicted voltage v_3 is very good since the receiver detection mechanism hardly suffers from fluctuation of voltage v_2 in the region of the power supply rails.

In order to quantify the maximum errors in the predicted waveforms, the complete eye diagrams derived from both the reference and predicted waveforms of $v_2(t)$ and of $v_3(t)$ are compared. Such a comparison is done by computing the eye

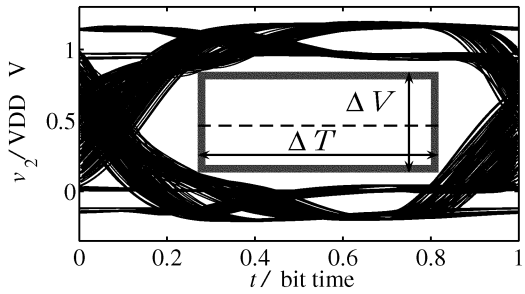

Fig. 4. Eye diagram arising from the reference waveform $v_2(t)$ of test case #1 and the definition of the eye opening parameters ΔV and ΔT.

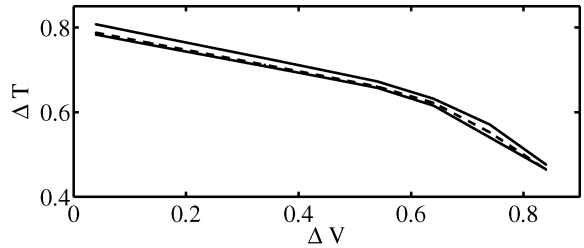

Fig. 5. Eye opening parameter values (defined in Fig. 4) for the eye diagrams of waveforms v_2 computed in test case #1. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

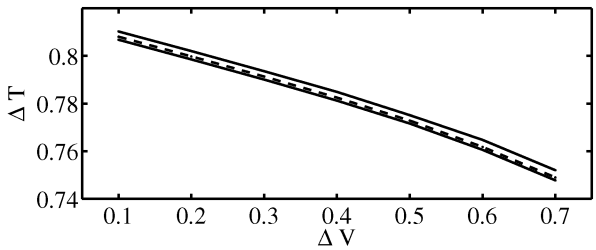

Fig. 6. Eye opening parameter values (defined in Fig. 4) for the eye diagrams of waveforms v_3 computed in test case #1. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

apertures ΔT and ΔV defined as in Fig. 4. Plots of ΔT versus ΔV are shown in Figs. 5 and 6, where, for every value of ΔV, the difference of the corresponding ΔT's quantifies the error in the eye opening caused by the use of approximate waveforms. The above comparison highlights that the openings of eye diagrams obtained from simulations with macromodels are within 2% of openings from reference simulations for the entire 2048-bit-long sequence.

Test Case 2: The aim of this second test case is to examine the switching noise effects. For this purpose, the power supply network and the reference plane are modeled by realistic lumped equivalent circuits.

Fig. 7 shows the reference and approximate waveforms for $v_{ds2}(t)$, $v_2(t)$, and $v_3(t)$. As for the first test case, the accuracy of the approximate models is confirmed, and the timing error on v_2 turns out to be less than 3% of the bit time over the entire bit sequence for both the **M1** and **M2** waveforms. The accuracy of the receiver macromodel in reproducing the power supply effects on v_3 can be clearly appreciated.

Figs. 8 and 9 show the reference and approximate ΔT versus ΔV curves, computed from the eye diagrams of $v_2(t)$ and $v_3(t)$ (not shown), thus confirming, for a realistic test case, errors

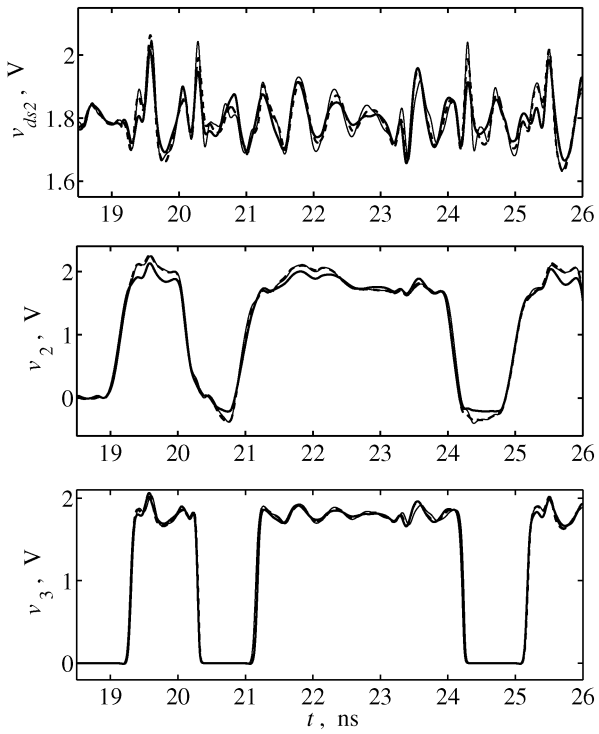

Fig. 7. Voltage waveforms $v_{ds2}(t)$, $v_2(t)$, and $v_3(t)$ for the test case #2. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

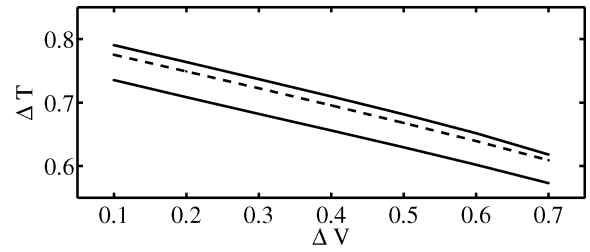

Fig. 8. Eye opening parameter values (defined in Fig. 4) for the eye diagrams of waveforms v_2 computed in test case #2. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

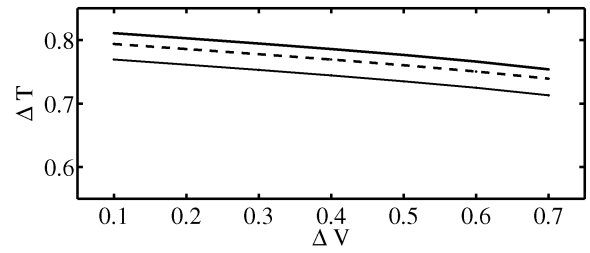

Fig. 9. Eye opening parameter values (defined in Fig. 4) for the eye diagrams of waveforms v_3 computed in test case #2. Solid thin line: reference; solid thick line: macromodels (**M1** set); dashed thick line: macromodels (**M2** set).

less than 4% in the eye opening diagrams caused by the use of macromodels.

Finally, Table I shows a comparison of the CPU time required by the PowerSPICE simulation of the reference 2048-bit-long transmission of test case #2 and the corresponding time of the simulation using macromodels; the speed-up factor is on the order of 34 for the set **M1** and 22 for the set **M2**.

TABLE I
EFFICIENCY COMPARISON [PowerSPICE SIMULATION OF A 2048-bit PATTERN APPLIED TO THE STRUCTURE OF FIG. 1(a)]

Device models	CPU time
reference transistor-level	10 h
macromodels (**M1** set)	19 min
macromodels (**M2** set)	29 min

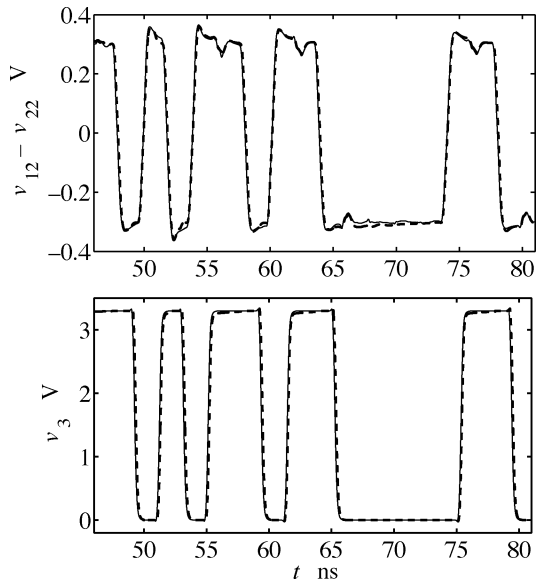

Fig. 10. Differential voltage waveform $v_{12}(t) - v_{22}(t)$ for the test case #3. Solid thin line: reference; dashed thick line: macromodels.

B. Differential Data Link

In this case, the Fairchild FIN1019 ($V_{dd} = 3.3$. V) LVDS High Speed Differential Transceiver is used in place of the driver and the receiver in the scheme of Fig. 1(b). The HSPICE encrypted transistor-level model of this transceiver is available from the website www.fairchildsemi.com. Additional details of the transceiver utilized in this study and on the generation of its macromodels can be found in [6]. The interconnect between driver and receiver is a lossless transmission line (odd mode impedance $Z_o = 50\,\Omega$, even mode impedance $Z_e = 90\,\Omega$, line length 0.15 m) loaded by a 100-Ω differential resistor. The data pattern used for this study is a 2048-bit-long sequence with 2-ns bit time and jitter error uniformly distributed in the range [−100, 100] ps. As in the previous section, a set of reference waveforms is computed by using transistor-level models for both the driver and the receiver; then, the approximate waveforms are generated by using the differential driver and receiver macromodel discussed in Section II. Again, the goal is to provide comparisons between the reference and approximate waveforms, and to generate their corresponding eye diagrams, in order to estimate the impact of possible errors introduced by differential macromodels.

Test Case 3: This test case is defined by the data link described above with an ideal power supply network modeled by a $V_{\rm DD}$ battery and a perfectly conducting reference plane, in order to exclude all possible power supply disturbances.

Fig. 10 shows the reference and approximate waveforms of the differential voltage $v_{12}(t) - v_{22}(t)$ and of the detected signal

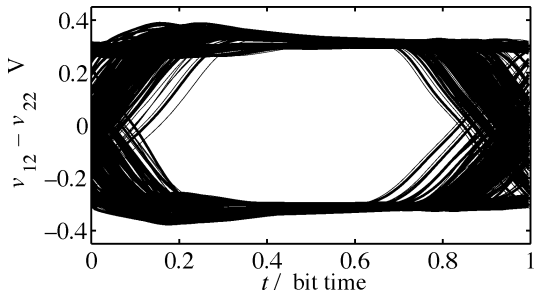

Fig. 11. Eye diagram arising from the reference waveform $v_{12}(t) - v_{22}(t)$ of test case #3.

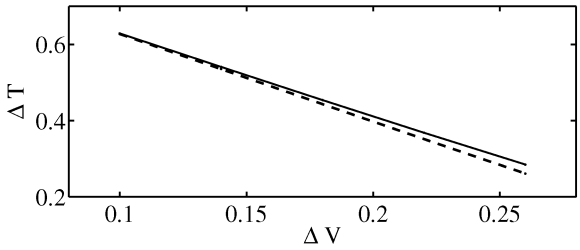

Fig. 12. Eye opening parameter values (defined in Fig. 4) for the eye diagrams of waveforms $v_{12} - v_{22}(t)$ computed in test case #3 (see Fig. 11). Solid thin line: reference; dashed thick line: macromodels.

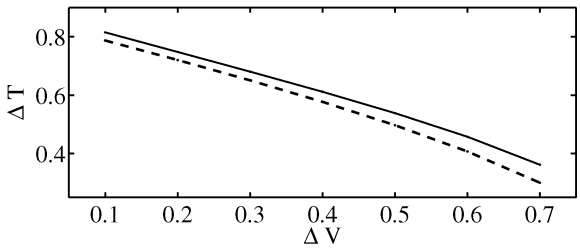

Fig. 13. Eye opening parameter values (like those defined in Fig. 4) for the eye diagrams of waveforms v_3 computed in test case #3 (see Fig. 11). Solid thin line: reference; dashed thick line: macromodels.

$v_3(t)$, for a duration of 35 ns, picked at random along the simulation of the entire bit pattern. A very good agreement between the reference and macromodel responses is achieved for the differential case as well. As in the test cases of the single-ended link, Fig. 11 shows the eye diagram computed from the differential voltage waveform $v_{12}(t) - v_{22}(t)$, and Figs. 12 and 13 compare the eye opening curves for the differential signal and for the detected signal $v_3(t)$, thus confirming timing errors less than 1% of the bit time.

IV. Conclusion

This paper deals with the impact of device macromodels on eye prediction and data links performance assessment in high-speed interconnection systems. An effective macromodel of drivers and an extended receiver macromodel including the power supply pin and the threshold decision of received signals are adopted for both single-ended and differential devices.

Two realistic data links are considered, and the analysis demonstrates that the use of well-designed macromodels dramatically speeds up the simulation. Also, a thorough analysis of simulated eye diagrams shows that macromodels are accurate enough for the simulation problem at hand and guarantee timing accuracy even for long bit sequences.

Appendix

This Appendix justifies the splitting of a device port equation like (2) into the sum of a static and a dynamic contribution, and the representation of the latter in terms of a nonlinear parametric equation.

In general, a constitutive relation of a nonlinear dynamic system can be described by an arbitrary state-space representation involving external measurable variables and internal nonmeasurable state variables, as follows:

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{g}\left(\mathbf{x}(t), \mathbf{u}(t)\right) \\ y(t) = f\left(\mathbf{x}(t), \mathbf{u}(t)\right) \end{cases} \tag{12}$$

where y is the output variable, $\mathbf{x}$ is the vector of internal state variables, $\mathbf{u}$ is the vector of input variables, and $\mathbf{g}$ and f are multivariate nonlinear mappings. If we designate by $f_s(\mathbf{u})$ the above nonlinear mapping in static conditions, (12) can be recast in the following form:

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{g}\left(\mathbf{x}(t), \mathbf{u}(t)\right) \\ y(t) = f_s\left(\mathbf{u}(t)\right) + \left[f\left(\mathbf{x}(t), \mathbf{u}(t)\right) - f_s\left(\mathbf{u}(t)\right)\right] \end{cases} \tag{13}$$

where the output equation turns out to be interpreted as the sum of a static and a dynamic part, i.e.,

$$y(t) = f_s\left(\mathbf{u}(t)\right) + f_d\left(\mathbf{x}(t), \mathbf{u}(t)\right) \tag{14}$$

where $f_d(\mathbf{x}, \mathbf{u}) = [f(\mathbf{x}, \mathbf{u}) - f_s(\mathbf{u})]$ is a new mapping such that $f_d(\mathbf{x}, \mathbf{u}) = 0$ for constant $\mathbf{u}(t)$.

In addition, owing to a result published in [11], for *almost any* nonlinear dynamic system, the external system behavior defined by the dynamic term f_d in (14) can be effectively approximated by parametric input–output discrete-time models involving the present and past samples of input and output variables. Thus, the general parametric relation for the dynamic part $f_d(\mathbf{x}, \mathbf{u})$ in (14) writes

$$f_d(k) = F\left(\left[f_d(k-1), \ldots, \mathbf{u}(k), \mathbf{u}(k-1), \ldots\right]^T\right) \tag{15}$$

where k is discrete-time and F is a parametrized nonlinear mapping. It is worth noting that, for the case of the input port of a single-ended receiver, for which $y = i_2(t)$, $\mathbf{u} = [v_2(t), v_{ds2}(t)]^T$, and f_s is the actual static characteristic of the receiver input port, (14) corresponds to (2), and (15) represents the model relationship for the dynamic part. A complete review of possible input–output discrete-time models as well as of the methods for estimating their parameters can be found in [12] and [13]. The estimation of model parameters can be obtained by fitting the model responses to so-called estimation signals, that are the responses of the device to be modeled to specific excitations (voltage waveforms) applied to the device output terminals. Sampled estimation signals (e.g., $i_2(k) = i_2(kT)$, T being the sampling period) are used, and the algorithms and tools for this fitting are borrowed from the *System Identification* literature (e.g., see [14] for the estimation of linear dynamic models and [15]–[17] for the estimation of

nonlinear dynamic models). It is worth noting that the major difficulty of the above process is that, due to the nonlinear nature of the problem, there are no general rules for the choice of the estimation waveform and of the modeling setup (e.g., number of samples, sampling time, estimation algorithm, model representation, etc.). Usually these choices are carried out via empirical guidelines [13] and the model estimation is rather easy. However, a systematic study of the effects of the modeling setup can help to improve the model quality and can facilitate the model generation for those devices that exhibit nonlinear or dynamic behaviors difficult to reproduce. The effects of the modeling setup on the final model have been recently addressed in [10].

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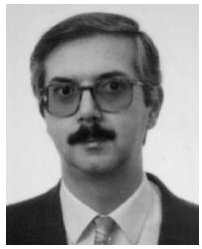

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