TOKYO CITY UNIVERSITY

DOCTORAL THESIS

Study on Design Technique of High Resolution ADC Using Dynamic Analog Components

---

Chunhui PAN

A thesis submitted in fulfillment of the requirements

for the degree of Doctor of Engineering

in the

Graduate School of Engineering

Department of Information Engineering

March 16, 2019

Abstract

Chunhui PAN

Study on Design Technique of High Resolution ADC Using

Dynamic Analog Components

The digital signal processing is performed widely on the computer system and communication system. Benefit from digital circuits are robust and can be realized by extremely small and simple structures, the fast, and very complex accurate systems can be implemented. As time goes by, the speed and density of digital integrated circuits is increasing, the dominance of digital system in almost all areas of communications system and consumer products is increasingly obvious. However, humans live in the physical world of analog signals, the data converters are needed to interface with the digital signal processing (DSP) system. As the speed and capability of DSP cores increases, the speed and accuracy of the converters associated with DSP have to increases, which led to unprecedented challenges.

Low voltage, high signal-to-noise and distortion ratio (SNDR) ADC analog-to-digital converters (ADCs) are widely used in the mixed-signal system on chip (SoC) in the fields of the wireless sensor network such as human body information measurement, environmental information monitor, interactive multimedia system, consumer device and industrial applications. In recent years, with the feature size of CMOS (Complementary Metal Oxide Semiconductor) devices scaled down, the increasing speed of devices has enabled the ADCs to achieve several tens of MS/s to low GS/s sampling rates. However, the degradation of the transistor is influencing the performance of the integrated circuit, such as the increase of threshold-voltage mismatch, and the reduction of the intrinsic gain. Moreover, the dynamic range of analog signal

is limited by the low supply voltage. Due to the degradation of the analog circuit linearity, the realization of the high-gain amplifier and high-resolution ADC is difficult. In order to achieve the high energy efficiency of ADC.

In this thesis, the design technique of delta sigma modulator using dynamic analog components is proposed to improve the performance of AD convertor. The dynamic amplifier (ring amplifier) is used to realize the integrator in the proposed delta sigma modulator. Benefit from the bias circuit not requited in the dynamic amplifier, the energy efficiency of delta sigma modulator can be improved. The SAR quantizer with dynamic comparator is used to realize the internal multi-bit quantizer, which not only can relax the slew-rate requirement on the amplifier in the integrator, but also can maintain the high energy efficiency for delta sigma modulator. Moreover, several techniques are proposed for enhance the performance of delta sigma modulator using dynamic analog component. The passive adder embedded noise coupling (NC) SAR quantizer is proposed to realize the summation of analog signals, and the quantization error feedback (It can feed the shaped the quantizer noise to the loop filter without the active amplifier) which achieve an addition 1st-order noise shaping without the extra integrator. As a result, a 3rd-order noise coupled delta sigma modulator is realized by two integrators using dynamic amplifier and the proposed noise coupling SAR quantizer, it achieved the greater bandwidth and the better performance (eg. better FOMW and FOMS). Furthermore, a novel implementation of complex integrator circuit is proposed to improve the energy efficiency and to reduce the circuit area of quadrature bandpass delta sigma modulator. The digitized noise coupling SAR quantizer is used to realize high order noise shaping and image rejection for the quadrature bandpass delta sigma modulator. By applying the above proposed techniques, a 6th-order QBPDSM with 2nd-order image rejection is realized by two dynamic analog components based complex integrators and the digital domain noise coupling SAR quantizer embedded by passive adder, which achieved the better performance.

Acknowledgements

Three years of doctoral candidate career is coming to an end, looking back to the past along the way, it is really hard to describe this feeling with words. Although most of the time were spent in a busy environment, I have made great progress in learning and growing during this period, both in problem solving and in dealing with people. Now I have successfully obtained my doctor's degree. I am so grateful to all the people who have helped and cared for me in this period.

First, I would like to thank my supervisor, Professor San, thank you for your invaluable guidance, technical knowledge and support during the study. From master's program to doctoral program, a total of five years of time, not only he provided me with good study environment, learning resources, and detailed guidance for this research, but also cultivated my professional objective research spirit and taught me the way of doing things. I would also like to acknowledge Prof. T. Shibata, Prof. M. Sawahashi, Prof. K. Sawano and Prof. A. Hyogo for their invaluable advice. Sincere thanks are also extended to my colleagues in the Integrated System Laboratory.

Finally, I would like to thank my parents for their care, support and encouragement during my PhD program. Thank you for your efforts to let me pursue my ideal without any worries, so that I can successfully complete my study. I would also like to dedicate this paper to all those who have helped and cared for me. I hope you can share this honor and happiness with me. In the future, I will try my best to enrich myself and push the limits my strengths so as not to fall short of everyone's expectations of me.

<div style="text-align: right">

Chunhui Pan

Tokyo City University

March 2019

</div>

Contents

List of Figures

List of Tables

List of Abbreviations

DSP	Digital Signal Processing
ADC	Analog-to-Digital Converter
SNDR	Signal-to-Noise and Distortion Ratio
SoC	System on Chip
CMOS	Complementary Metal Oxide Semiconductor
SAR	Successive Approximation Register
OTA	Operational Transconductance Amplifier
INL	Integral-Non-Linearity
LSB	Least-Significant-Bit
DAC	Digital-to-Analog Converter
PSD	Power-Spectral-Density
FS	Full Scale
NTF	Noise Transfer Function
STF	Signal Transfer Function
OSR	Over Sampling Rate
SQNR	Signal-to-Quantization-Noise Ratio
ENOB	Effective-Number-Of-Bits
DWA	Data-Weighted-Averaging
MDAC	Multiplying Digital-to-Analog Converter
CMFB	Common-Mode-Feed Back
SFDR	Spurious Free Dynamic Range
THD	Total Harmonic Distortion
MSB	Most Significant Bit
PSS	Periodic Steady-State analysis
PNOISE	Periodic Noise analysis
RAMP	Ring Amplifier
DFF	D Flip-Flop
QNS	Quantization Noise Shaping
CMRR	Common Mode Rejection Ratio
CBPDSM	Complex Bandpass Delta Sigma Modulator
QBPDSM	Quadrature Bandpass Delta Sigma Modulator
NC	Noise Coupling
QDWA	Quadrature Data-Weighted-Averaging

Physical Constants

Boltzmann's constant $k = 1.38 \times 10^{-23}\,\text{J/K}$

List of Symbols

V	voltage	V
P	power	W ($\mathrm{J\,s^{-1}}$)
U	sampled input signal	
E	quantization noise	
Q	shaped quantization noise	
T	sampling periodic	s
S	power spectral density	
f	frequency	
ω	angular frequency	rad
γ	content associated with CMOS technology	
Δ	quantization error	
μ	mean value	
σ	mean-square value	

Chapter 1

Introduction

1.1 Background

The digital signal processing techniques is performed widely on the computer systems and communication systems. Benefit from digital circuits are robust and can be realized by extremely small and simple structures, the fast, and very complex accurate systems can be implemented. As time goes by, the speed and density of digital integrated circuits is increasing, the dominance of digital system in almost all areas of communications system and consumer products is increasingly obvious. However, humans live in the physical world of analog signals, the analog-to-digital data converters (ADCs) are required to interface with the digital signal processing (DSP) system. As the speed and capability of DSP cores increases, the speed and accuracy of the converters associated with DSP have to increases, which led to unprecedented challenges. The performance of ADC is often limited by the available device technology. While recent designs may benefit from scaled device geometries and higher bandwidth, there is a loss in dynamic range and sampling linearity due to reduced supply voltages and available swing.

In recent years, low voltage, high signal-to-noise and distortion ratio (SNDR) ADC analog-to-digital converters are widely used in the mixed-signal system on chip (SoC) in the fields of the wireless sensor network such as human body information measurement, environmental information monitor, interactive multimedia system, consumer device and industrial applications. With the feature size of CMOS (Complementary Metal Oxide Semiconductor) devices scaled down, the increasing
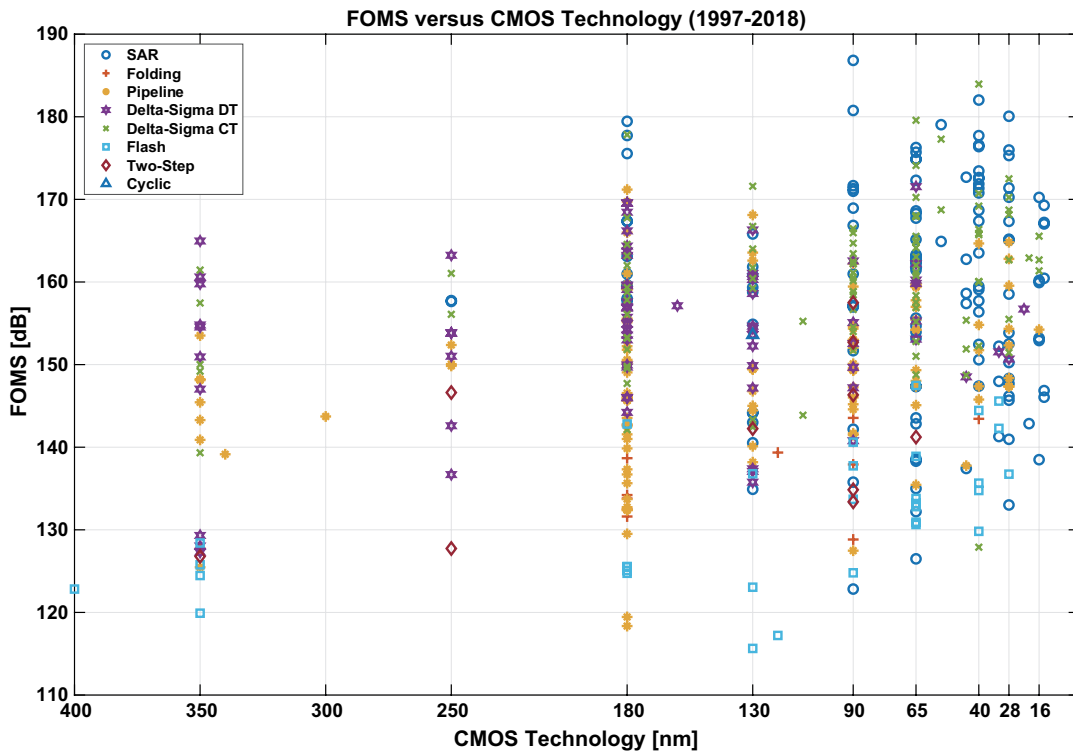
FIGURE 1.1: FOMS versus CMOS Technology
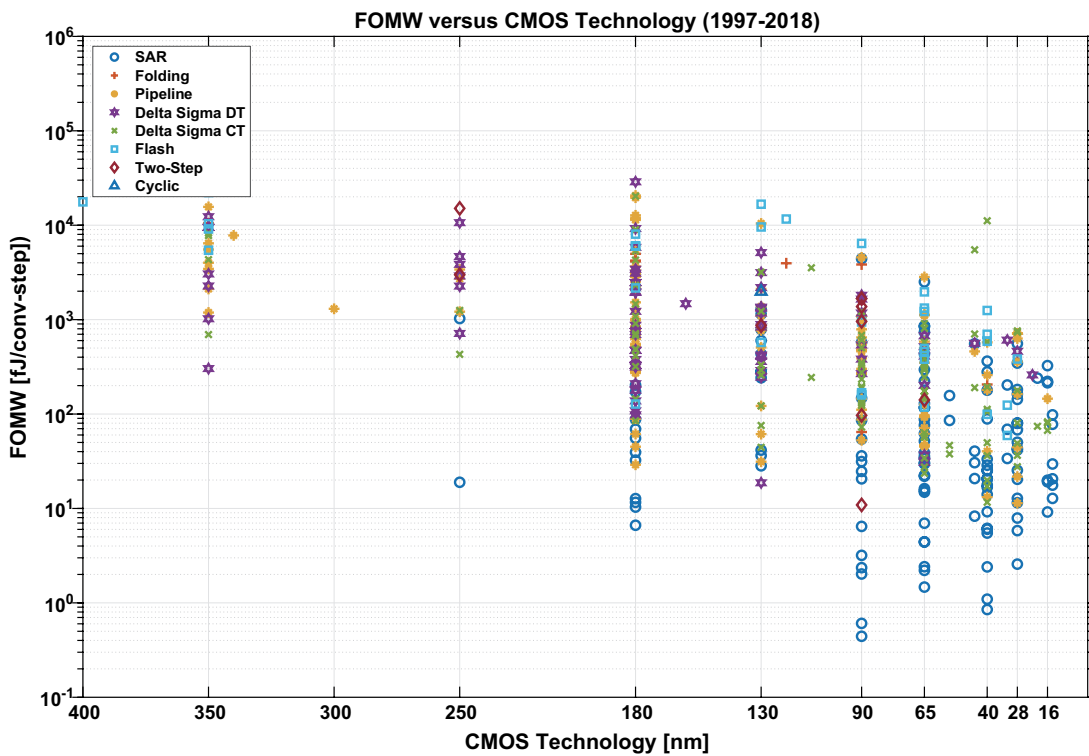
FIGURE 1.2: FOMW versus CMOS Technology

speed of devices has enabled the ADCs to achieve several tens of MS/s to low GS/s sampling rates. However, the degradation of the transistor is influencing the performance of integrated circuits, such as the increase of threshold-voltage mismatch, and the reduction of the intrinsic gain. Besides, the dynamic range of analog signal is limited by low supply voltage. Due to the linearity of analog circuit deteriorate, the realization of the high-gain amplifier and high-resolution ADC is difficult. The effects of technology scaling made that to implement accurate, efficient amplifiers is increasingly difficult under the low supply voltage, and the intrinsic properties of transistors were quite different from that of the large size transistor [1].
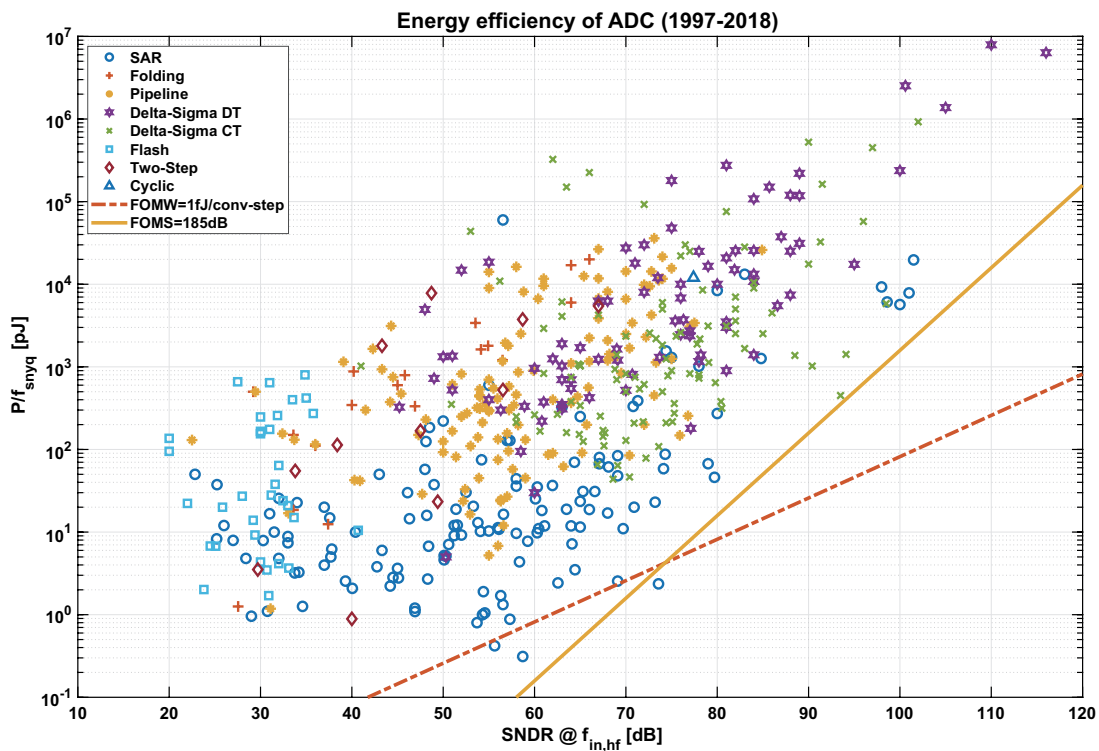
FIGURE 1.3: Energy efficiency of ADC

In order to solve the each scaling challenge, a lot of techniques are proposed as gain enhancement of amplifier, output swing enhancement techniques and many highly effective digital correction. But, the ability of these techniques to deliver favourable amplifier scaling characteristics in actual fabricated designs does not achieve the expectation. As shown in Fig. 1.1 and Fig. 1.2, the ADC performance surveys conducted in [2] and[3] show that the high-resolution ADCs implemented in nanoscale CMOS is very few, and its energy efficiency is declining gradually. The Walden FOM

(FOMW) [4] is the respective energy/conversion-step value, it is defined as:

$$FOMW = \frac{P}{2 \times BW \times 2^{SNDR-1.76}/6.02} \ [J/conv. - step], \qquad (1.1)$$

where, P is the power consumption of AD convertor, BW is the band width of signal. The Schreier FOM (FOMS) is the figure of merit that assumes that the ADC power is set by thermal noise, and hence quadruples per 6dB in precision. Schreier originally defined this FOM using DR [5] as:

$$FOMS = DR + 10 \times log_{10}(BW/P) \ [dB], \qquad (1.2)$$

where, DR is the dynamic rang of AD convertor. but it has become common to also account for distortion, i.e.

$$FOMS = SNDR + 10 \times log_{10}(f_{snyq}/2/P) \ [dB], \qquad (1.3)$$

where, f_{snyq} is defined as f_{snyq} = Sampling-Rate(FS)/Oversampling-rate(OSR) (it is given by 2FS/OSR for a complex delta-sigma modulator), it equal to the double BW. (e.g. [6]). It is clear from the energy plot shown in Fig. 1.3 that FOMS is a better metric for high-resolution designs. Because, the amplification is used for almost all high resolution ADC circuits, these observations reflect the effect of operation amplifier scaling challenges on the performance of the system level. By contrast, the low and medium resolution ADC architectures which do not use operating amplifier such as SAR (Successive Approximation Register) ADCs can deliver the transistor scaling characteristics very well. SAR ADCs are well known as an energy efficiency architecture for low power, low and medium speed, medium resolution applications [7], [8]. Because the resolution of SAR ADC depends on the accuracy of capacitor matching and the offset of comparator, it is difficult to realize a high resolution SAR ADC in nanoscale CMOS technology. For medium-to-high speed applications, the flash ADC and pipelined ADC have been the popular architectures.

In the most case which the operating amplifier is used, the transistor scaling characteristics can not be delivered favourably, since the operation amplifier ill-suited fundamentally to scaling is included in the underlying circuits of ADC. the high
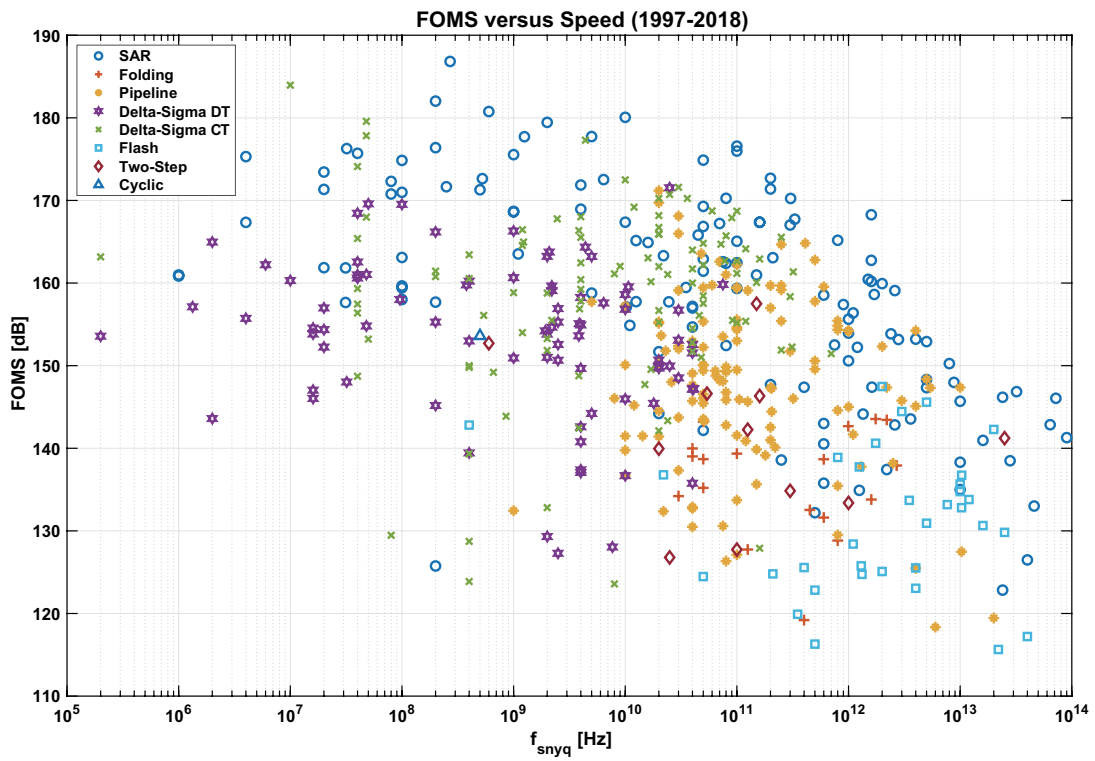
FIGURE 1.4: FOMS versus Speed
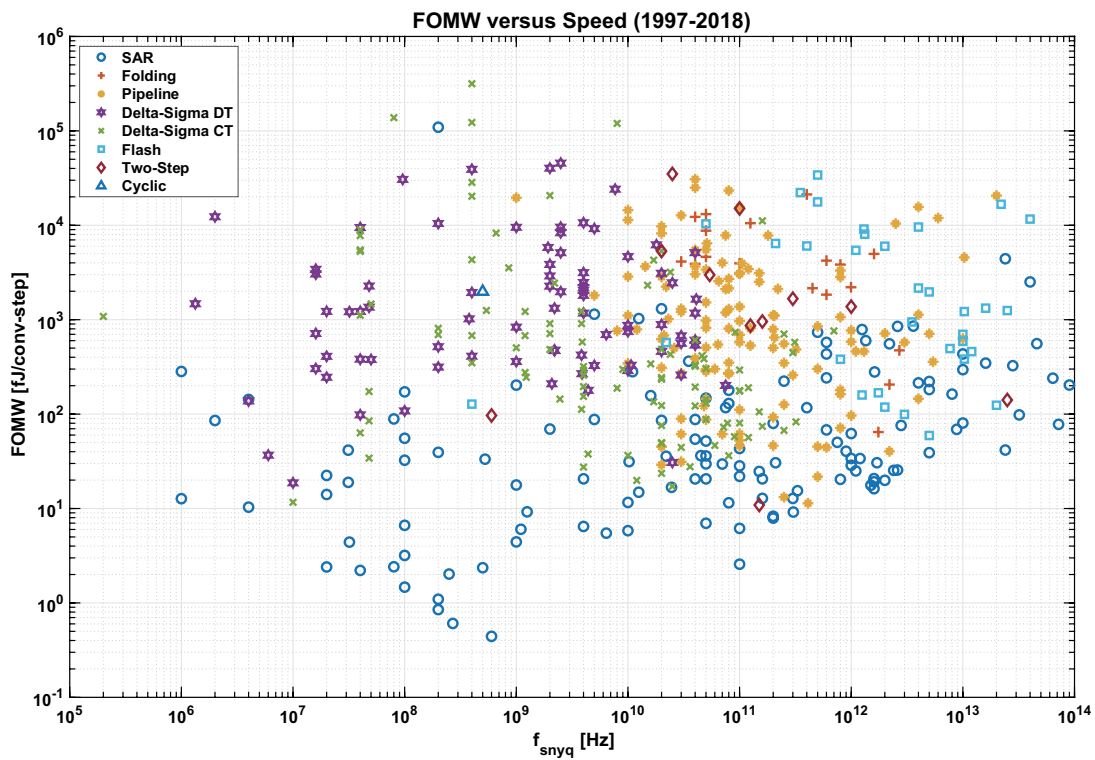
FIGURE 1.5: FOMW versus Speed

performance operating amplifier in nanoscale technology may be realized by employing the additional techniques, but the ability to scale at the same pace as digital performance improvements can not be achieved. A truly scalable amplifier must be consist of the circuit components which include the characteristics of scaled CMOS. The technology scaling is deliberately designed to favor the time domain world of high-speed digital, thus the scalable analog techniques will likely be found by using the same method as well. In order to fully exploit the abilities of a transistor, the biasing and small signal properties of the device must be viewed as highly coupled, time dependent variables which can be applied as feedback to each other with respect to time [1]. The ring amplification technique is proposed for solving the above problem. The ring amplifier is a small modular amplifier derived from a ring oscillator which naturally embodies all the essential elements of scalability. The ring amplifier not only can realize the amplification with rail-to-rail output swing, but also can efficiently charge for the large capacitive loads by using slew-based charging. The ring amplifier is simple enough to be quickly constructed from only capacitors, switches consist of transistors and inverters in series and according to process trends it can be scale well in performance.

On the other hand, since the delta sigma AD modulator reduces the quantization noise in the desired signal band by oversampling and noise shaping technique, it is a digital rich architecture, and it is suitable to realize the high SNDR ADC in nanometer CMOS technology as shown in Fig 1.4 and 1.5. Normally, high SNDR modulator is realized by the techniques of high-order noise-shaping and/or higher OSR (Over Sampling Ratio). However, high OSR needs high speed operation and increases the total power consumption of the modulator. High-order noise-shaping needs several numbers of integrators with power hungry amplifier. Several techniques have been proposed to improve the SNDR and reduce the power consumption of the delta sigma AD modulator. The feed-forward structure is a preferred architecture for delta sigma AD modulator to tolerate the distortion of the internal amplifier [9]. Moreover, the feed-forward structure can also reduce the output swing of the integrator, which can relax the linearity requirements on the amplifier in the integrator, and hence to reduce the power consumption of the delta sigma modulator. Multi-bit

quantizer can also be chosen to relax the slew-rate requirement on the amplifier to reduce the power of the modulator [5]. Error feedback technique (noise coupling) also has been proposed to aggressive the noise shaping characteristic of the delta sigma AD modulator [10]. However, in nano CMOS technology, that it is difficult to realize a high gain, low distortion, wide band-width amplifier lead to the non-linearity of the amplifier. The variation of the noise transfer function coefficient caused by the non-linearity of the amplifier weakens the delta sigma modulator's ability for suppressing the in-band quantization noise, thus, the performance of delta sigma modulator is not affected.

1.2 Objectives

(Example Integrator using ring amplifier)
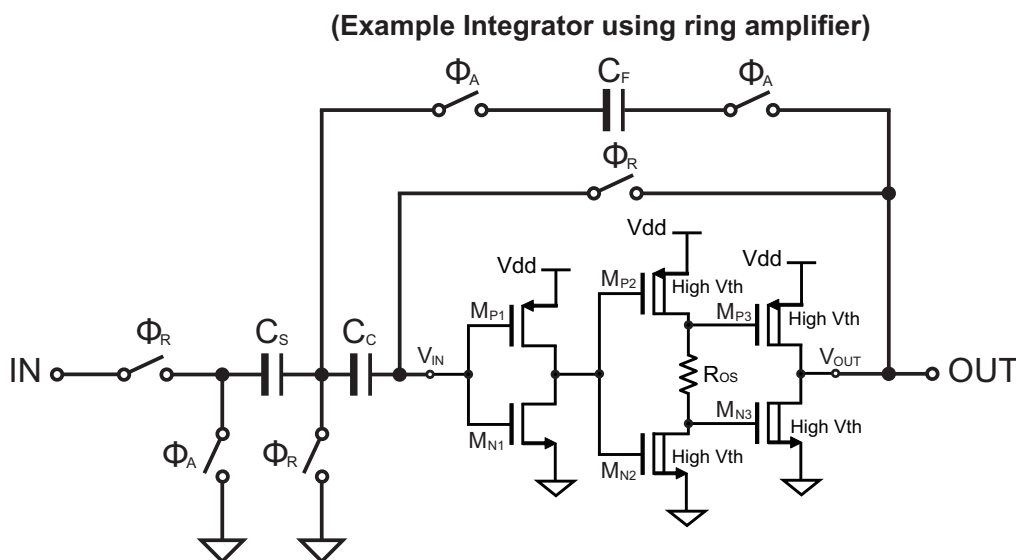
FIGURE 1.6: Implementation of integrator using ring amplifier

In order to achieve the maximum power-efficiency of ADC, the use of the dynamic amplifier (eg. logic inverter or ring amplifier) instead of OTA (Operational Transconductance Amplifier) has been proposed and results in dynamic-analog-components-based Nyquist ADC [11], [12]. Ring amplification is a concept, it can be realized by the variety of architectures and design choices. One such implementation is shown in Fig. 1.6 which embodies the key features of ring amplification. However, there are a lot of implementation approaches available, each with their own pros and cons in terms of operation speed, accuracy, and energy efficiency. Fundamentally, the

ring amplifier is a ring oscillator which is split into two separate signal paths by a resistor or capacitor. A different offset is embedded into each signal path in order to create a range of input values for which neither output transistor nor of Fig. 1.6 (M_{P3} and M_{N3}) will fully conduct. If this non-conduction "dead-zone" is sufficiently large, the ring amplifier will operate by slewing-to, stabilizing, and then locking into the dead-zone region. When placed in the feedback structure which is a example switched capacitor integrator of Fig. 1.6, this charging and settling behavior results in the stabilized waveforms.

the basic characteristics of ring amplifier will be discussed as following, the capacitor C_C shown in Fig. 1.6 is used to cancel the difference between the integrator virtual-node sampling reference and the trip-point of the first stage inverter. It ensures that the ideal settled value is independent of the actual inverter threshold. Namely, the generation of operating point depend on the capacitor, rather than the bias current as the traditional amplifier. The input-referred value of offset voltage is negligibly small. The dead-zone of the ring amplifier in Fig. 1.6 is embedded prior to the second stage inverters by storing a voltage offset across resistor. Any value for within the dead-zone region is a viable steady-state solution for the ring amplifier, and the input-referred value of the dead-zone will determine the overall accuracy of the amplifier for most practical cases. In other words, the error voltage V_{error} at when the amplifier has stabilized and locked will be

$$V_{error} \leq V_{DZ} / A_{amp}, \tag{1.4}$$

where, V_{DZ} is the dead-zone region, A_{amp} is the final settled small-signal gain of the first stage inverter, and finite gain effects of the latter stages are ignored. It is worth briefly noting that there are many additional options for both where and how to embed the dead-zone offset into the ring amplifier, and for different target accuracies and design applications it may be useful to consider additional possibilities and their respective advantages and disadvantages. The ring amplifier has several characteristic which is different from the traditional amplifier. The embedding resistor allows to accurately and linearly set the dead-zone offset value. Its stability is gained by embedding the offset prior to the second stage inverters, rather than

the first or third stage. Due to the accuracy limitations imposed by equation 1.4, the input-referred dead-zone value of a few millivolts or less is supposed to achieve the high performance amplification. For medium accuracy ring amplifiers, embedding the dead-zone offsets immediately after the first gain stage will create input-referred dead-zone sizes small enough to achieve desired accuracies while still keeping the embedded offset large enough to easily tune with a simple voltage reference.

Although, the ring amplifier has above superiority, the behaviour of ring amplifier is different from that of the traditional amplifier, the ring amplifier requires to generate the operating point by performing the reset operation before the amplification. Since the output of ring amplifier is disabled in the process of the reset, the load capacitance must be unconnected to the output of the ring amplifier in the reset operation. Furthermore, since SAR quantizer is used as an internal quantizer in the delta sigma modulator, unlike flash ADC, SAR quantizer requires an extra phase for the signal sampling. Because of the above two factors, the clock timing design of delta sigma modulator using SAR quantizer and ring amplifier is more difficult than that of the delta sigma modulator using traditional amplifier and flash ADC. In this paper, several design technique is proposed for improving the performance of delta sigma modulator using dynamic analog components. The ring amplifier is used for realizing the integrator in the proposed delta sigma modulator. The foible of ring amplifier can be avoided by using the proposed design technique. Benefit from the ring amplifier has the favourable linearity, the in-band noise of the delta sigma modulator can be adequately suppressed. The bias circuit not requited in the ring amplifier, not only the power consumption can be reduced, the energy efficiency of delta sigma modulator can also be improved. Moreover, in the proposed design technique of delta sigma modulator, the SAR quantizer with dynamic comparator is used to realized the internal multi-bit quantizer, which not only can relax the slew-rate requirement on the amplifier but also can improve the energy efficiency of the delta sigma modulator.

**Title: Study on Design Technique of High Resolution ADC
Using Dynamic Analog Components**

Chapter 1: Introlduction (Background, Objectives, Construction)

Chapter 2: Theory of Delta Sigma Modulator

**The functional verification of delta sigma modulator
using dynamic compinents (ring amplifer)**

**Chapter 3: Proposed 2nd-Order Delta Sigma Modulator Using
Ring amplifier and Passive Adder Embedded SAR Quantizer**

**The operating speed of delta sigma modulator using ring amplifer
is enhanced by improving the circuit architecture**

**Chapter 4: Proposed 2nd-Order Delta Sigma Modulator Using
Ring Amplifier and SAR Quantizer with Simplified Operation Mode**

**The performance of delta sigma modulator using ring amplifer
is enhanced by using proposed noise coupling technique**

**Chapter 5: Proposed 3rd-Order Noise Coupled Delta Sigma Modulator
Using Passive Adder Embedded Noise Shaping SAR Quantizer**

**The applications of delta sigma modulator using ring amplifer
are expanded by using proposed complex integrator**

**Chapter 6: Proposed 6th-Order Quadrature Bandpass Delta Sigma Modulator
Using Dynamic Amplifier and Noise Coupling SAR Quantizer**

Chapter 7: Conclusion

FIGURE 1.7: Construction of this dissertation

1.3   Construction

The construction of this dissertation is shown in Fig. 1.7. It is structured as the following: In the chapter 2, The discussion in this section is an introduction to the theory of the delta sigma modulator. The oversampling technique, noise shaping technique and the basic architectures of delta sigma modulators are discussed. Moreover, the theoretical performance represented by signal to quantization-noise ratio (SQNR) of the high order delta sigma modulator with multi-bit internal quantizer are summarized.

In the chapter 3, a 2nd-order delta sigma modulator using dynamic analog component is proposed to improve the energy efficiency. The proposed delta sigma modulator is realized by the integrator using the ring amplifier and the passive-adder

embedded multi-bit SAR quantizer. Because the operating point of ring amplifier is generated by the reset operation dynamically, the current bias circuit is not required. The passive-adder embedded multi-bit SAR quantizer using dynamic comparator not only realizes the multi-bit quantization, but also realizes an adder for the summation of analog signal without active analog component, since the high energy efficiency can be maintained. Moreover, for conforming the noise characteristic of the dynamic analog components, the noise models of dynamic amplifier (ring amplifier) and dynamic comparator are created, and these noise analysis are carried out. For demonstrating the proposed techniques, the proof-of-concept prototype of proposed delta sigma modulator using dynamic analog components is designed and fabricated in TSMC 90nm 1P9M CMOS technology. Measurement results show the feasibility of the proposed delta sigma modulator.

In the chapter 4, the drawback of the proposed delta sigma modulator using dynamic analog components in the chapter 3 is discussed. In order to ensure the ring amplifier's reset time and that the output operation of the ring amplifier and the sampling operation of asynchronous SAR quantizer are performed at the same time, the 4 operation phases are required for once AD conversion, which limited the operation speed of proposed delta sigma modulator using dynamic analog components. 4 factors need to be guaranteed when designing the delta sigma modulator using ring amplifier and SAR quantizer are summarized for For improving the performance of proposed 2nd-order delta sigma modulator using dynamic analog components. Moreover, the 2nd-order delta sigma modulator using dynamic analog components with simplified operation phase is proposed. The improved delta sigma modulator has been designed and fabricated in 90 nm CMOS technology. Benefit from the reduction of the number of the delta sigma modulator operation phase, the speed of delta sigma modulator is improved. Measurement results show the feasibility of the improved delta sigma modulator using dynamic analog components.

In the chapter 5, a 3rd-order delta sigma modulator using ring amplifier and noise shaping SAR quantizer is proposed for enhancing the performance of the delta sigma modulator using dynamic analog components. A novel noise shaping SAR quantizer without active components realized in analog domain is proposed to extend

the order of the delta sigma modulator (the signal band width can be extend at the same sampling rate). The proposed passive adder embedded noise shaping SAR quantizer not only can realize the summation of analog signals without the active amplifier, Because a passive adder is embedded to the proposed noise shaping SAR quantizer, the summation of analog signals in front of input port of the internal quantizer can be realized without power hungry amplifier. And, it can also feed the shaped quantizer noise to the loop filter of the delta sigma modulator, which achieve an addition 1st-order noise shaping without the extra integrator. Moreover, the pseudo differential ring amplifier with modified common feedback circuit (CMFB) is proposed to improve the common-mode rejection ratio (CMRR). The proposed the modified CMFB circuit does not include capacitors in series, hence, it can directly feed the common mode signal from the output port of the ring amplifier's core to the input port of the ring amplifier's core for obtaining the maximum CMRR. As a result, the 3rd-order noise coupled delta sigma modulator is realized by two integrators with ring amplifier and the proposed noise shaping SAR quantizer, it achieved the greater bandwidth and the better performance (eg. better FOMW and FOMS) than that of proposed 2nd-order delta sigma modulator using dynamic analog component in previous work. The SPICE simulation results demonstrate the feasibility of the proposed delta sigma modulator in 90 nm CMOS technology.

In the chapter 6, a 6th-order complex quadrature delta sigma modulator (QBPDSM) with 2nd-order image rejection using dynamic amplifier and noise coupling (NC) SAR quantizer embedded by passive adder is proposed for the application of wireless communication system. A novel implementation of complex integrator circuit is proposed for improving the energy efficiency and reducing the circuit area of QBPDSM. The dynamic amplifier instead of the operational transconductance amplifier (OTA) is used to achieve the maximum power-efficiency of the operating amplifier in the complex integrator circuit. The proposed complex integrator circuit requires fewer operation phases than the conventional complex integrator for once

complex integration operation, hence the energy efficiency can be improved. Furthermore, the proposed complex integrator circuit use less capacitance than the conventional complex integrator, which can reduce the circuit area of QBPDSM. Moreover, the digitized NC SAR quantizer is used for realizing high order noise shaping and image rejection for maintaining the high energy efficiency. In the proposed 6th-order QBPDSM, two complex integrators consist of ring amplifiers are used to realize the 2nd-order noise shaping, the passive adder embedded NC SAR quantizer is used to realize the summation of analog signal, quantization, noise shaping and image rejection. SPICE simulation results including the thermal noise and the flicker noise have been done to verify the effectiveness of the proposed architecture and to confirm the performance of the modulator.

In the chapter 7, the conclusion of this dissertation is described.

References

[1] M. Shrivastava et al. "Toward system on chip (SOC) development using FinFet technology: Challenges, solutions, process co-development and optimization guidelines". In: *IEEE Trans. Electron Devices* vol.58 (June 2011), pp. 1597–1607 (cit. on pp. 3, 6).

[2] B. Murmann. "ADC Performance Survey 1997-2018". In: *[Online]. Available: http://web.stanford.edu/ murmann/adcsurvey.html.* (2018) (cit. on p. 3).

[3] B. Jonsson. "On CMOS scaling and A/D-converter performance". In: *NORCHIP 2010* (Nov. 2010), pp. 1–4 (cit. on p. 3).

[4] R. H. Walden. "Analog-to-digital converter survey and analysis". In: *IEEE J. Select. Areas Commun.* vol.17 (Apr. 1999), pp. 539–550 (cit. on p. 4).

[5] R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004 (cit. on pp. 4, 7).

[6] A.M.A. Ali et al. "A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration". In: *IEEE J. Solid-State Circuits* vol.45 (Dec. 2010), pp. 2602–2612 (cit. on p. 4).

[7]   Y.-S Shu, L.-T Kuo, and T.-Y. Lo. "An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS". In: *IEEE J. Solid-State Circuits* vol.51 (Dec. 2016), pp. 2928–2940 (cit. on p. 4).

[8]   W. Tseng, W. Lee abd C. Huang, and P. Chiu. "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for digitally-assisted wireless transmitters". In: *IEEE J. Solid-State Circuits* vol.51 (Oct. 2016), pp. 2222–2231 (cit. on p. 4).

[9]   J. Silva et al. "Wideband lowdistortion delta-sigma ADC topology". In: *Electronics Letters* vol.37 (June 2001), pp. 737–738 (cit. on p. 6).

[10] K. Lee, M.R. Miller, and G.C. Temes. "An 8.1 mW, 82 dB DeltaSigma ADC With 1.9 MHz BW and -98 dB THD". In: *IEEE J. Solid State Circuits* vol.44 (Aug. 2009), pp. 2202–2211 (cit. on p. 7).

[11] Y. Chae and G. Han. "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator". In: *IEEE J. Solid State Circuits* vol.44 (Feb. 2009), pp. 458–472 (cit. on p. 7).

[12] B. Hershberg et al. "Ring amplifiers for switched capacitor circuits". In: *IEEE J. Solid State Circuits* vol.47 (Dec. 2012), pp. 2928–2942 (cit. on p. 7).

Chapter 2

Theory of Delta Sigma Modulator

2.1 Preface

The discussion in this section is an introduction to the theory of the delta sigma modulator. The oversampling and noise shaping techniques well be discussed. The basic architectures of delta sigma modulators will be presented.

2.1.1 Oversampling
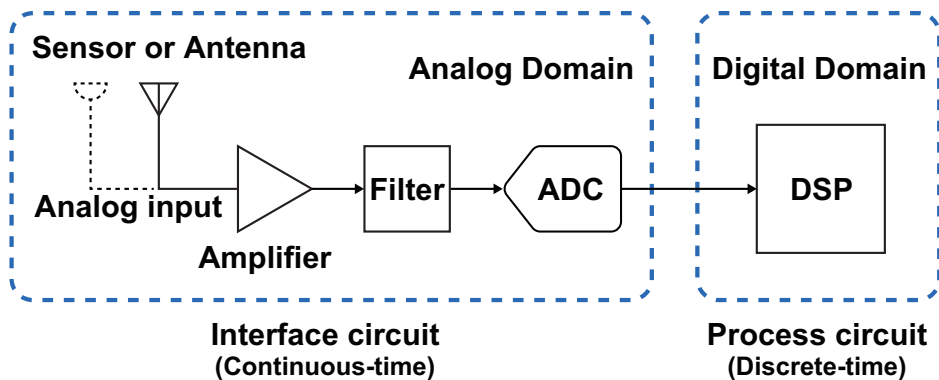
FIGURE 2.1: A typical DSP system with interface circuit.

Figure 2.1 shows a typical DSP system that consist of interface circuit and digital signal process circuit. The interface circuit includes the sensor circuit or antenna, amplifier, analog filter and ADC. As shown, the analog input signal is magnified and filtered firstly, then, it is input to ADC and transformed to a digital data stream. The digital data stream is processed by the DSP circuit. Usually, the ADC can be classified into two main categories, the Nyquist-rate ADC and oversampled ADC. The

Nyquist-rate ADC has some specific property that are a one-to-one correspondence between the input and output samples. The each sampled input signal is separately transformed to the corresponding digital code, regardless of the other sampled input signal (Nothing to do with earlier and later input signal); thus, the Nyquist-rate ADC has no memory property. If to apply the digital input word containing bits $b_1, b_2, b_3, ..., b_{N-1}, b_N$ of ADC to a ideal DAC, the analog output of ideal DAC can be represented as:

$$V_{out} = V_{ref} \times (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-4} + ... + b_{N-1} 2^{-(N-1)} + b_N 2^{-N}) + \epsilon, \quad (2.1)$$

where V_{ref} is the reference voltage, ϵ is the DC offset associated with the implementation of ADC (eg. SAR-ADC is a mid-tread quantizer, Flash-ADC is a mid-rise quantizer, they have a different DC offset value). The conversion resolution of ADC can be evaluated by comparing the actual value of V_{out} with the ideal value represented by (2.1).

The sampling rate of Nyquist-rate converter must satisfy the sampling rate required in the Nyquist's criterion (twice the bandwidth of the input signal). The actual rate is usually somewhat higher than this minimum value required in the Nyquist's criterion. The resolution and linearity of a Nyquist-rate ADC constructed from current sources or switched-capacitor circuit is determined by the matching accuracy of the analog components (eg. resistors, capacitors and transistor) used in the implementation. Thus, the analog components must have a relative matching error less than 2^N to guarantee an integral-non-linearity (INT) less than 0.5 least-significant-bit (LSB), it is very difficult to realize the high resolution Nyquist-rate ADC.

However, in some applications such as medical imaging device and digital audio device, higher resolution and linearity is required [1] [2]. The resolution as much as 18 or even 20 bits for ADC is requisite, generally. If the ADC is realized at the Nyquist-rate, then only integrating-ADC or counting-ADC can be used for realizing the capacity such as accuracy above 20 bits. However, the integrating-ADC or counting-ADC require at least 2^N clock periods to convert a sampled signal, since,

they are too slow for most signal-processing applications. The ADC using over-sampling technique are able to achieve over 20 bit resolution at reasonably high conversion speeds by relying on a trade-off. The sampling rate of converter using oversampling technique much higher than the Nyquist-rate, it is typically higher by a factor between 4 and 256, or even higher. The factor is represented as OSR in almost all literatures. Moreover, the converter using oversampling technique generate each output utilizing all preceding input values. Thus, the converter incorporates memory elements (eg. integrator) in its structure. This property destroys the one-to-one relation between input signal and output signal. Fortunately, in the time domain or in the frequency domain, the comparison of the complete input and output waveforms can be used to evaluate the resolution of ADC.

2.1.2 Noise Shaping

The delta sigma modulator using oversampling technique can realize the high resolution AD conversion without the high precision analog component. Since it is a digital rich architecture, and have been used widely in the circuit using nanometer CMOS technology.
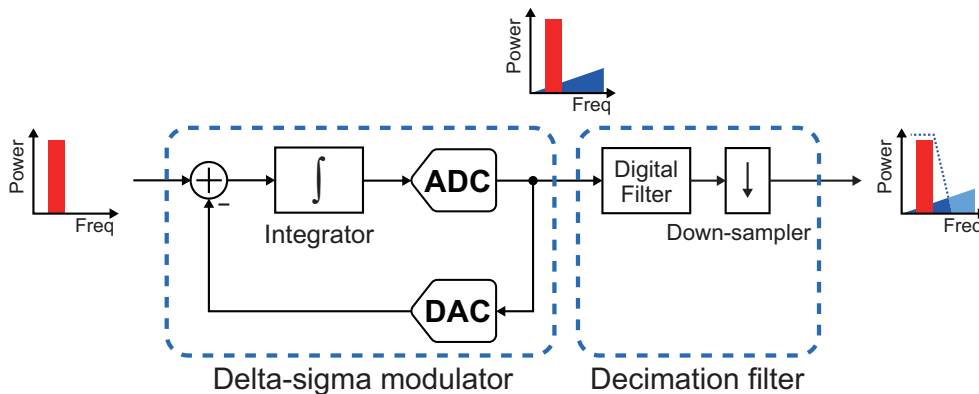
FIGURE 2.2: System model of the delta sigma modulator.

Figure 2.2 shows the system model of a first-order delta sigma modulator. It is a feedback loop, containing an internal low-resolution ADC and digital-to-analog converter (DAC) as well as a loop filter. As shown, the quantization noise is shifted to the high frequency domain by delta sigma modulator, and then the quantization

noise in the high frequency domain is filtered and down-sampled by the decimation filter. Since the quantization noise power in the baseband (i.e. the signal with spectra centred around dc) is reduced, the high SNDR ADC can be realized easily. However, due to the quantizing effect of the internal ADC and the memorability of the integrator, the delta sigma modulator is a non-linear system. The analysis of the delta sigma modulator is a difficult mathematical task.
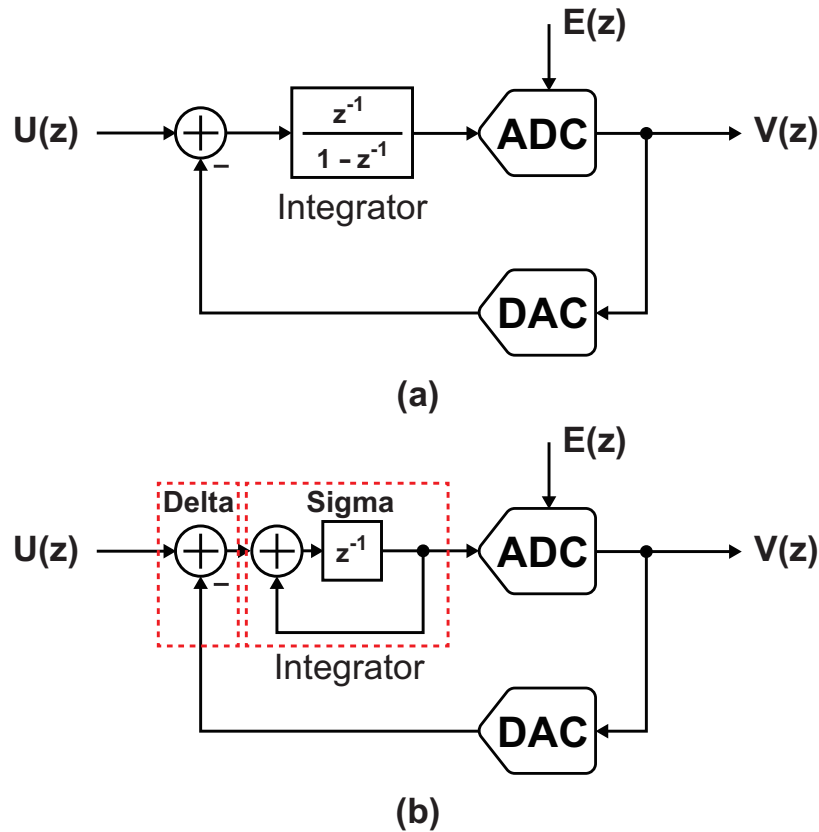
FIGURE 2.3: Block diagram of delta sigma modulator. (a) Using discrete integrator. (b) Using delay circuit.

Figure 2.3 illustrates a block diagram of basic delta sigma modulator. the block diagram of delta sigma modulator using the discrete integrator and the delay circuit are shown in the Figure 2.3(a) and (b), respectively. Where the $U(z)$ is the sampled input signal, the $E(z)$ is the quantization noise of the internal ADC, the $V(z)$ is the output signal of the delta sigma modulator. Figure 2.3 (b) shows the concept of "delta" and "sigma" that represent what is "delta" and what is "sigma". For analysing the mathematical model of the delta sigma modulator, the internal ADC can be represented as a linearized model which consists of a unity-gain amplifier and a quantization noise

$E(z)$. The DAC is seen as a ideal DAC with the reference voltage of $V_{ref} = 1V$. By analyzing the model of the delta sigma modulator, its output signal can be represented as:

$$v(n) = u(n) + e(n) - e(n-1),\qquad(2.2)$$

in the time-domain, and,

$$V(z) = U(z) + (1 - z^{-1})E(z),\qquad(2.3)$$

in the z-domain. The digital output signal includes the analog input signal $U(z)$ and a difference of the quantization between $E(z)$ and its delay $z^{-1}E(z)$. The equation (2.3) means that the analog input signal $U(z)$ is not changed by the delta sigma modulation process, so that, the analog input signal can be recovered by the decimation filter without using the integrator in the demodulation operation. Moreover, there are not the amplification of in-band noise and distortion at the delta sigma modulator, the differentiation of the error $E(z)$ suppresses the in-band noise and the distortion. Therefore, the delta sigma modulator has a unity-gain to the input signal $U(z)$ in the signal band, while, the quantization noise is strongly attenuated, this signal process is called as noise shaping in almost all literatures.

The quantization noise and non-linearity of ADC in the delta sigma modulator are shaped, suppressed in the bandwidth. However, due to the non-linearity of DAC in the delta sigma modulator is not any shaped, the output signal and performance of the delta sigma modulator is affected by the DAC. Thus, the non-linearity of DAC is a major limitation that affect the attainable performance of the delta sigma modulator. For multi-bit quantization, digital correction or dynamic matching techniques can be used for weakening the influence of the DAC's non-linearity. Furthermore, there are more simple ways, for example, the single-bit quantization has the characteristic of the DAC consists of only two points on its input and output. Since, the single-bit DAC's operation is inherently linear.

2.2   Mathematical Model of Delta Sigma Modulator

2.2.1   Noise Transfer Function
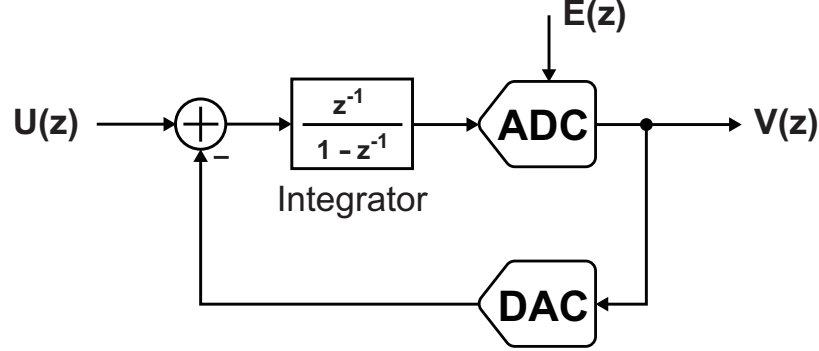
FIGURE 2.4: Block diagram of first-order delta sigma modulator.

Figure 2.4 illustrates a block diagram of the first-order delta sigma modulator. For simplicity, next, the mathematical model of the delta sigma modulator will be discussed by using the model of the first-order delta sigma modulator. The output noise of the first-order delta sigma modulator due to the quantization error of the internal ADC can be represented as:

$$Q(z) = (1 - z^{-1})E(z), \tag{2.4}$$

in the z-domain, as shown by (2.3). The the transfer function of the quantization noise (NTF) can be represented as:

$$NTF(z) = (1 - z^{-1}), \tag{2.5}$$

the z in the equation (2.3) can be replaced by $e^{j\omega}$, this becomes

$$NTF(e^{j\omega}) = (1 - e^{-j\omega}), \tag{2.6}$$

where, $\omega = 2\pi f T$, assuming f_s as the sampling rate, then, $T = 1/f_s$ is the sampling period. Assuming $S_e(f)$ as the power-spectral-density (PSD) of the quantization error of the internal ADC of the delta sigma modulator. The PSD of the output noise

of the delta sigma modulator can be deduced as:

$$S_q(f) = NTF(e^{j2\pi fT})^2 S_e(f) \tag{2.7}$$

$$= (1 - e^{-j2\pi fT})^2 S_e(f) \tag{2.8}$$

$$= ((1 - cos(2\pi fT))^2 + sin(2\pi fT)^2) S_e(f) \tag{2.9}$$

$$= (1 - 2cos(2\pi fT) + cos(2\pi fT)^2 + sin(2\pi fT)^2) S_e(f) \tag{2.10}$$

$$= 2(1 - cos(2\pi fT)) S_e(f) \tag{2.11}$$

$$= (2sin(\pi fT))^2 S_e(f). \tag{2.12}$$

The equation (2.12) means that the PSD of the output noise of the delta sigma modulator can be computed by the product of the NTF's PSD $(2sin(\pi fT))^2$ and the PSD of the internal ADC's quantization error $S_e(f)$.

2.2.2 Quantization Error Model

Next, considering that how to calculate the PSD of the quantization error of the internal ADC. Figure 2.5 illustrates the transfer function diagram of mid-rise and mid-tread quantizer and their quantization error function diagram. The the output of quantizer generates a rise or step when the input of zero is input to the quantizer, as shown in the figure 2.5(a), since it has the characteristic of mid-rise such as SAR ADC. In the figure 2.5(c), the the output of quantizer is a middle of a flat portion i.e. a tread when the input of zero is input to the quantizer, since it has the characteristic of mid-tread such as Flash-ADC. The step size Δ is set as 2 in figure 2.5(a) and (c) that make the quantization levels of the both types quantizer to be integer values that lead to the difference between input thresholds i.e. the size of LSB equal the Δ (LSB=2). Therefore, in mid-rise quantizer, the quantization levels are odd integers, opposite, the quantization levels are even integers in mid-tread quantizer.

Figures 2.5(b) and (d) illustrate the quantization error function of the mid-rise and mid-tread quantization, respectively. It can be knew from the figures 2.5(b) and (d) that the input and output of the mid-rise quantizer are between -8 and +8, the input and output of mid-tread quantizer are between -9 and +9. The above means,
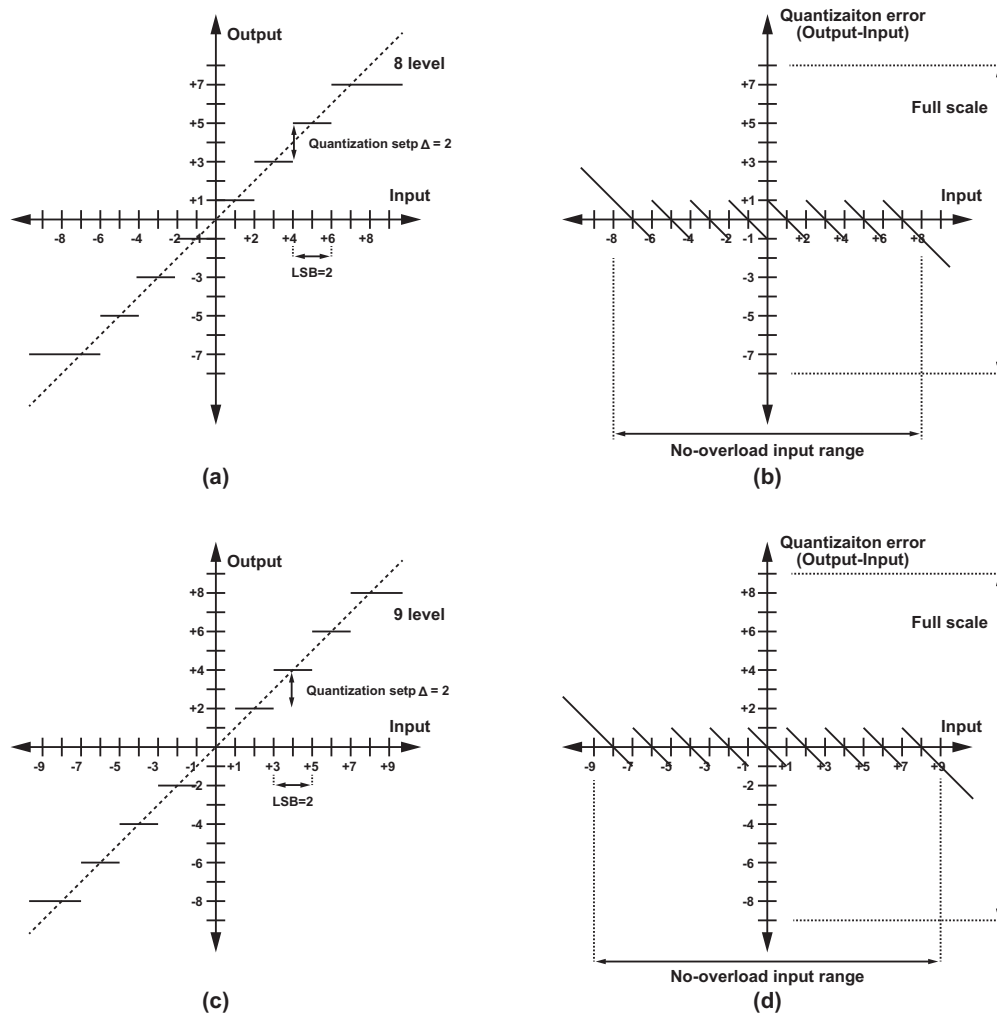
FIGURE 2.5: Transfer function of mid-rise and mid-tread quantizer.
(a) Transfer function of the mid-rise quantizer (8 level). (b) Quantiza-
tion error function of the mid-rise quantizer. (c) Transfer function of
the mid-tread quantizer (9 level). (d) Quantization error function of
the mid-tread quantizer.

in the case that the same reference voltage is used, the mid-tread quantizer has a

larger full-scale (FS) than the mid-rise quantizer (i.e. the difference between the

lowest and highest levels of the mid-tread quantizer is a larger LSB under the same

reference voltage). However, the mid-rise and mid-tread quantizer have the same

quantization error which between -1 and 1.

Considering the ideal quantizer, the output and quantization error of the ideal quan-

tizer are fully determined by the input of the ideal quantizer. However, if the input

signal of the ideal quantizer stays within the input range of the ideal quantizer, and

the changes of input signal are sufficiently large amounts from sample to sample,

so that, the position of the input signal within a quantization interval is essentially random, then it is permissible to assume that the quantization error is a white noise process with samples uniformly distributed between $-\Delta/2$ and $+\Delta/2$. Therefore, the probability density function of the quantization error can be draw as shown in figure 2.6,
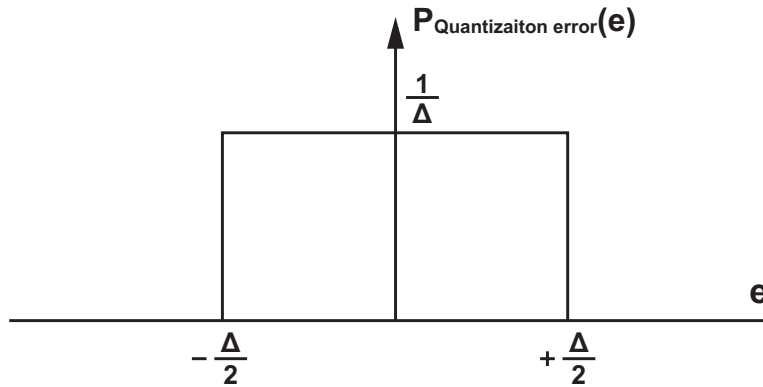
FIGURE 2.6: Probability density function of the quantization error.

the probability density the quantization error is $1/\Delta$ at between $-\Delta/2$ and $+\Delta/2$. For rapidly and randomly varying input signals, that means the quantization error is not correlate with the input signal, and, the quantization error of the two samples is also uncorrelated. So that, the power of the quantization error of the internal ADC σ_e can be computed as:

$$\sigma_e^2 = \int_{-\Delta/2}^{+\Delta/2} e^2 \frac{1}{\Delta} \, de = \frac{\Delta^2}{12}, \tag{2.13}$$

where, the Δ is the quantization step size (i.e. Δ = Full Scale/Number of Quantization Level) of the internal ADC. As an example, in the fully-differential 4-bit quantizer circuit, the number of quantization level = 16, while the reference voltage = $\pm 1V$, namely, the FS = +1 - (-1) = 2, then, Δ = 2/16 = 0.125. Thus, in this case that the quantization error is assumed as the uniform distribution, it is easy to derive that the quantization error has the mean value of $\mu = 0$, and the mean-square value of $\sigma_e^2 = \Delta^2/12$. Therefore, the quantization error can be added to the input of the quantizer to give the output.

Moreover, the single-sided PSD of the quantization error of the internal ADC $S_e(f)$ can be represented as:

$$S_e(f) = \frac{\sigma_e^2}{f_s/2} = \frac{\Delta^2/12}{f_s/2} = \frac{\Delta^2}{6f_s}, \tag{2.14}$$

where the f_s is the sampling rate of the delta sigma modulator (that same as the sampling rate of internal ADC).

2.2.3 Calculation of In-Band Noise Power

For calculating the in-band noise power, the OSR is defined as:

$$OSR = \frac{f_s}{2f_B}, \tag{2.15}$$

where f_B is the maximum signal bandwidth (maximum frequency of input signal). The OSR is defined as that how much faster the sample rate in the delta sigma modulator than in a Nyquist-rate converter.
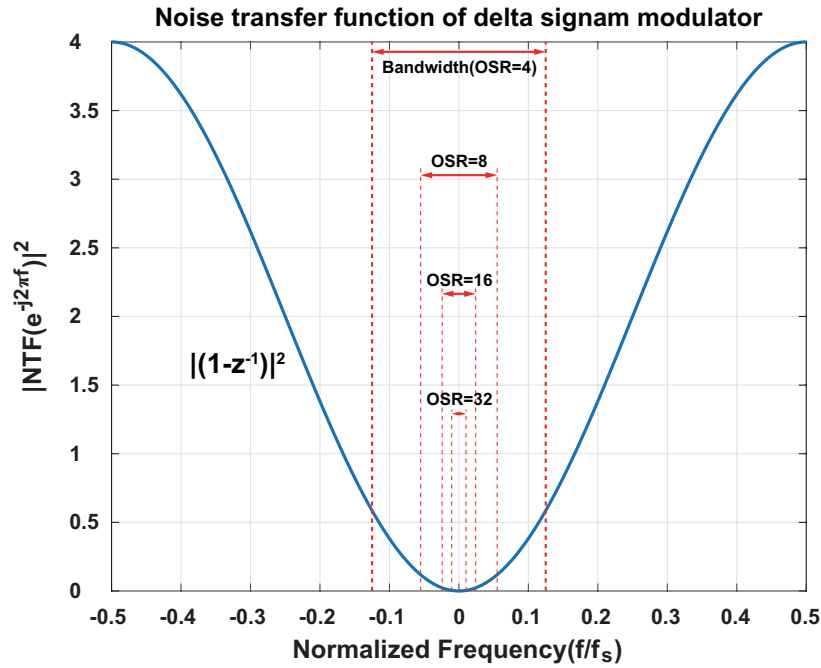
FIGURE 2.7: Noise transfer function of first-order delta sigma modulator.

As an example, the figure 2.7 illustrates the noise transfer function (NTF) of first-order delta sigma modulator and the signal bandwidth at the different OSR (OSR

= 4, 8, 16, 32, respectively). The NTF is a high-pass filter function, it suppresses the quantization noise at the frequencies around direct current (DC), i.e. frequency is equal to zero. Oppositely, the quantization noise at the frequencies around f_S is enhanced by the NTF.

According to the equation (2.12), the in-band noise power can be calculated by integrating $S_q(f)$ between 0 and f_B that can be represented as:

$$Quantization\_noise^2_{In-band} = \int_0^{f_B} S_q(f)\,df \tag{2.16}$$

$$= \int_0^{f_B} (2sin(\pi fT))^2 S_e(f)\,df, \tag{2.17}$$

$$= \frac{\Delta^2}{6f_S} \int_0^{f_B} (2sin(\pi fT))^2\,df \tag{2.18}$$

where, $S_e(f)$ is replaced by using the equation (2.14). Take notice of $sin(\pi fT) = sin(\pi f_B/f_S)$, when $f = f_B$ and $T = 1/f_S$, and the relation of $f_B/f_S \ll 1/2$ can be obtained by assuming $OSR = f_S/2f_B \gg 1$ (i.e. $\pi f_B/f_S \rightarrow 0$ or $\pi fT \rightarrow 0$). Thus, an approximate can be got as:

$$sin(\pi fT) = \pi fT, when\ (OSR \gg 1), \tag{2.19}$$

by using the following formula:

$$\lim_{x \to 0} \frac{sin(x)}{x} = 1 \Rightarrow \lim_{x \to 0} sin(x) = x. \tag{2.20}$$

Therefore, the equation (2.18) can be expressed as:

$$Quantization\_noise^2_{In-band} = \frac{\Delta^2}{6f_S} \int_0^{f_B} (2sin(\pi fT))^2\,df \tag{2.21}$$

$$= \frac{\Delta^2}{6f_S} \int_0^{f_B} (2\pi fT)^2\,df \tag{2.22}$$

$$= \frac{\Delta^2}{6f_S} 4\pi^2 T^2 \int_0^{f_B} f\,df \tag{2.23}$$

$$= \frac{\Delta^2}{6f_S} 4\pi^2 T^2 \frac{f^3}{3}\Big|_0^{f_B} \tag{2.24}$$

$$= \frac{\Delta^2}{6f_S} 4\pi^2 T^2 \frac{f_B^3}{3}, \tag{2.25}$$

substituting $T = 1/f_S$ and $f_B = f_S/2OSR$ into equation (2.25), we get

$$Quantization\_noise^2_{In-band} = \frac{\Delta^2}{6f_S} 4\pi^2 T^2 \frac{f_B^3}{3} \tag{2.26}$$

$$= \frac{\Delta^2}{6f_S} \frac{\pi^2 f_S}{6(OSR)^3} \tag{2.27}$$

$$= \frac{\Delta^2 \pi^2}{36(OSR)^3}. \tag{2.28}$$

The equation (2.28) means that the quantization noise power is relate with the OSR and the quantization step size of the internal quantizer. Moreover, the in-band noise power of the delta sigma modulator decreases with increasing OSR and decreasing the quantization step size.
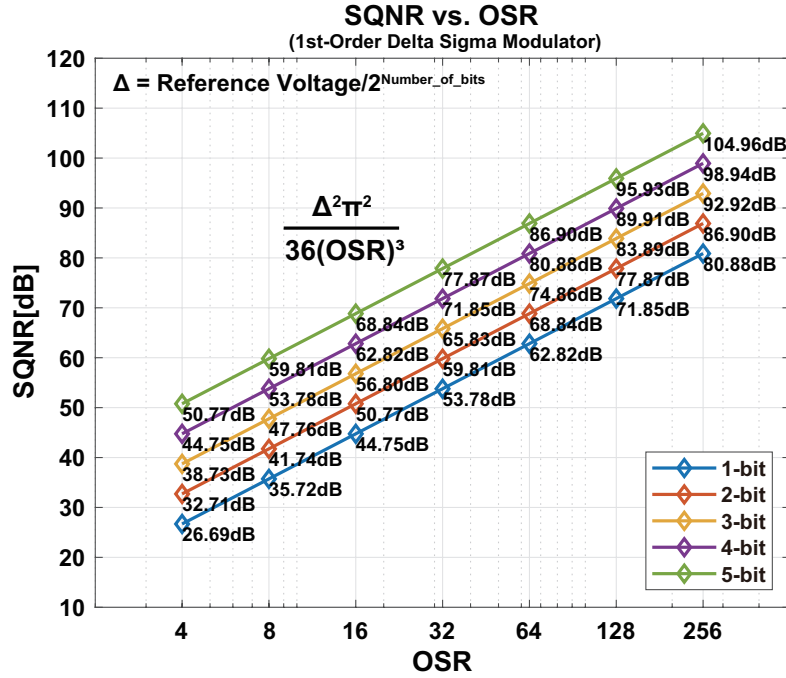
FIGURE 2.8: SQNR versus OSR of first-order delta sigma modulator using the internal quantizer with the different resolution ($1 \sim 5$bit).

The maximum performance of delta sigma modulator on theory can also be estimated by using the equation (2.28). Normally, the signal-to-quantization-noise-ratio (SQNR) and effective-number-of-bits (ENOB) are used to measure the performance of the delta sigma modulator, they have the relationship of $ENOB = (SQNR - 1.76)/6.02$.

The SQNR can be calculated as:

$$SQNR = 10 \times log_{10}(\frac{Power_{Input\_signal}}{Power_{In-band\_quantization\_noise}}) \ [dB], \qquad (2.29)$$

where $Power_{In-band\_quantization\_noise}$ can be calculated by using the equation (2.28), and the $Power_{Input\_signal}$ equal to the $(Amplitude\ of\ sine\ input\ singal)^2/2$.

The SQNR versus OSR of first-order delta sigma modulator using the internal quantizer with the different resolution (1-5 bit) is shown in the figure 2.8. It can be known that for every doubling of OSR, the SQNR is increased by 9 dB and the ENOB is enhanced by 1.5 bits. Furthermore, for every increase the resolution of the internal quantizer by 1 bit, the SQNR can be increased by 6 dB. Although, the equation (2.28) and figure 2.8 only show the characteristics of the first-order delta sigma modulator, it is possible to assess the theoretical performance of the high order delta sigma modulator by extending the equation (2.28) before designing the delta sigma modulator circuit. The next discussion is about the high order delta sigma modulator.

2.3   High Order Delta Sigma Modulator

For increasing the resolution of the delta sigma modulator, the addition another integrator and feed-back path are used to realize the higher order loop filter. Therefore, in the high order delta sigma modulator circuit, the loop filter is a higher-order circuit, it can generate a output signal which is more close to the input signal.

2.3.1   Feed-back Structure

As a typical implementation, the figure 2.9 illustrates a realizable block diagram of second-order feed-back structure delta sigma modulator. The output signal of the second-order feed-back structure delta sigma modulator can be represented as:

$$V(z) = z^{-1}U(z) + (1 - z^{-1})^2E(z), \qquad (2.30)$$
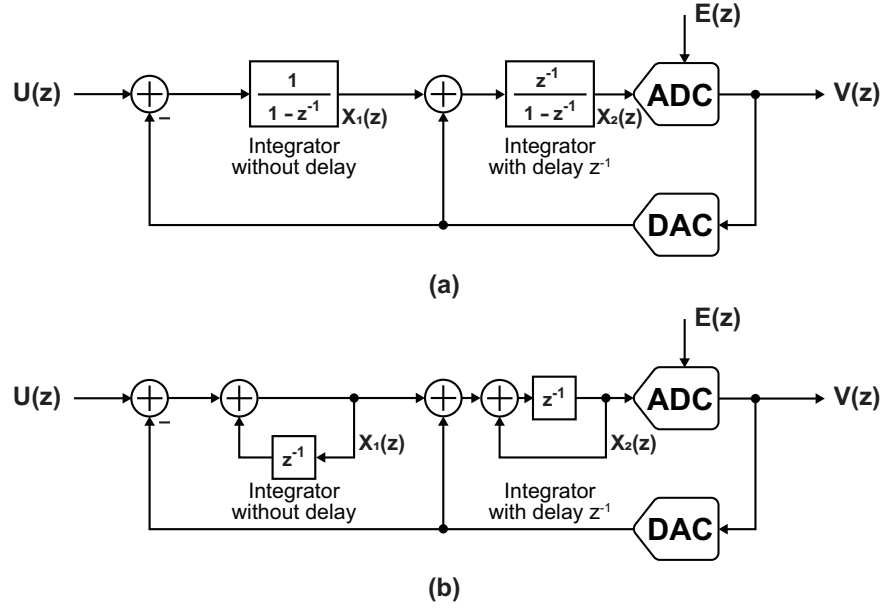
FIGURE 2.9: Block diagram of second-order feed-back structure delta sigma modulator. (a) Using discrete integrator. (b) Using delay circuit.

in the z-domain. Thus, its signal-transfer-function (STF) and noise-transfer-function (NTF) are indicated as:

$$STF_{2nd-order-FB}(z) = z^{-1}U(z),\tag{2.31}$$

and,

$$NTF_{2nd-order}(z) = (1 - z^{-1})^2 E(z),\tag{2.32}$$

respectively. In the same way as the equation (2.12), the NTF of the second-order feed-back structure delta sigma applies a quantization noise shaping function:

$$S_{q(2nd-order)}(f) = NTF_{2nd-order}(e^{j2\pi fT})^2 S_e(f)\tag{2.33}$$

$$= (2sin(\pi fT))^4\tag{2.34}$$

to the PSD of the quantization error, where z is replaced by $e^{j2\pi fT}$. Moreover, the in-band quantization noise power of the second-order feed-back structure delta sigma

modulator can be calculated as:

$$Quantization\_noise^2_{In-band(2nd-order)} = \int_0^{f_B} S_{q(2nd-order)}(f)\,df \qquad (2.35)$$

$$= \frac{\Delta^2 \pi^4}{60(OSR)^5}. \qquad (2.36)$$

by using the same way as the equation (2.18). From the equation (2.36), it can be known that for every doubling of OSR, the SQNR is increased by 15 dB, and the ENOB is enhanced by about 2.5 bits.
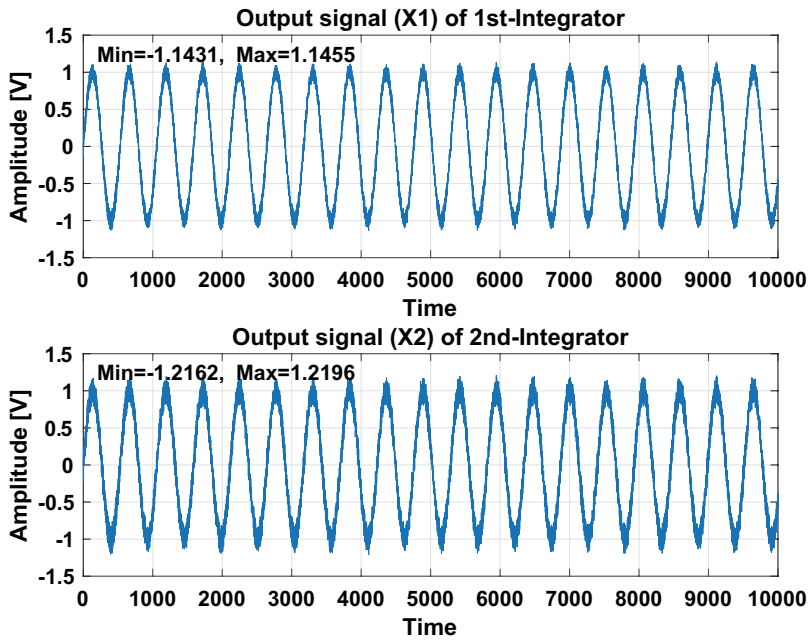
FIGURE 2.10: Output waves of integrators in the second-order feed-back delta sigma modulator using 4-bits internal quantizer while the sine signal with an amplitude of ± 1 V is input ($V_{\text{reference}} = 1.2$V).

Figure 2.10 shows the output signal waves of the integrators of the second-order feed-back delta sigma modulator using 4-bits internal quantizer, when the sine signal with an amplitude of 1V is input. In the figure 2.10, the X_1 and X_2 represent the output waves of 1st-integrator and 2nd-integrator, respectively. Maximum and minimum amplitude of the 1st-integrator output signal are -1.1431 and +1.1455, respectively. Maximum and minimum amplitude of the 2nd-integrator output signal are -1.2162 and +1.2196, respectively. The amplitude of wave output by integrator are larger than the amplitude of input signal wave, since, it is requirement that the operational amplifier in the integrator maintain a good linearity over the full scale

range for realizing a good performance of the delta sigma modulator. So that, the design of the operational amplifier is very difficult. Next, we will see that this problem will be solved in the feed-forward structure delta sigma modulator.

2.3.2   Feed-forward Structure

The figure 2.11 illustrates the block diagram of second-order feed-forward structure delta sigma modulator.
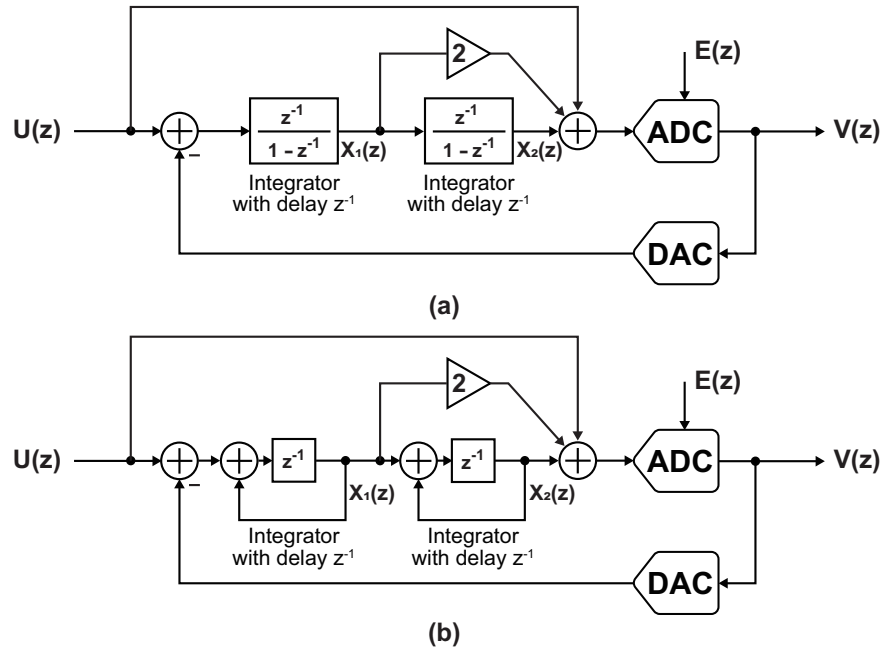
FIGURE 2.11: Block diagram of second-order feed-forward structure delta sigma modulator. (a) Using discrete integrator. (b) Using delay circuit.

The output signal of the second-order feed-forward structure delta sigma modulator can be represented as:

$$V(z) = U(z) + (1 - z^{-1})^2 E(z), \tag{2.37}$$

in the z-domain. Since, the STF (equal to a constant value of 1) does not include the unit delay of z^{-1}, the stability of the second-order feed-forward structure delta sigma modulator is better than the one of the second-order feed-back structure. The NTF of second-order feed-forward structure delta sigma modulator and the NTF of

second-order feed-back structure delta sigma modulator are same. Hence, both have the same noise transfer characteristic.

However, in the second-order feed-forward structure delta sigma modulator, only shaped quantization noise of $(1 - z^{-1})^2 E(z)$ is input to the loop-filter of the delta sigma modulator.
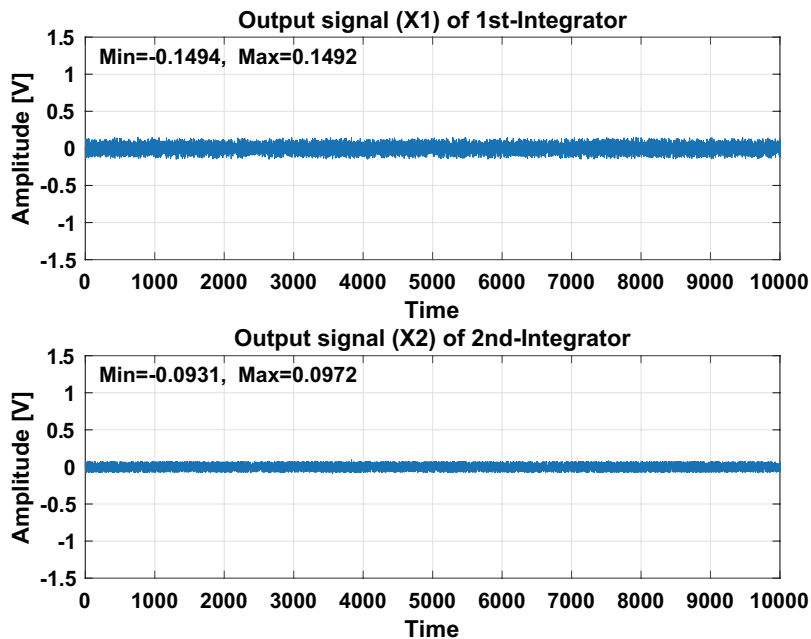
FIGURE 2.12: Output waves of integrators in the second-order feed-forward delta sigma modulator using 4-bits internal quantizer while the sine signal with an amplitude of ± 1 V is input ($V_{\text{reference}} = 1.2$V).

In the figure 2.11, the X_1 and X_2 express the output wave of 1st-integrator and 2nd-integrator, respectively. Figure 2.12 shows the output signal waves of the integrators of the second-order feed-forward delta sigma modulator using 4-bits internal quantizer when the sine signal with am amplitude of +-1V is input. Maximum and minimum amplitude of the 1st-integrator output signal are -0.1494 and +0.1492, respectively. Maximum and minimum amplitude of the 2nd-integrator output signal are -0.0931 and +0.0972, respectively. Comparing with the second-order feed-back structure delta sigma modulator (figure 2.10), the output signals of integrators in the second-order feed-forward structure delta sigma modulator are compressed to a very small voltage as shown in the figure 2.12. Therefore, the feed-forward structure delta sigma modulator can reduce the output swing of the integrator, which can relax the linearity requirements on the amplifier in the integrators, and, the distortion

on the internal amplifier can also be tolerated.

2.3.3 Performance Estimation

A conventional method of implementing high-order delta sigma modulator is that add more integrators and feedback branches to the loop filter for achieving high-order NTFs. Generally, an Rth-order loop filter is requirement for realizing the NTF of $(1 - z^{-1})^R$. By using same calculation method of equations (2.12), (2.18) and (2.28), the in-band quantization noise power of the Rth-order delta sigma modulator can be expressed as:

$$Quantization\_noise^2_{In-band(R^{th}-order)} = \frac{\Delta^2 \pi^{2R}}{(24R + 12)OSR^{2R+1}}, \qquad (2.38)$$

where, Δ is the quantization step size of the internal quantizer, R is order of delta sigma modulator's loop filter, OSR is oversampling rate, and the ENOB added to the resolution of the delta sigma modulator by doubling OSR is calculated by R+0.5.
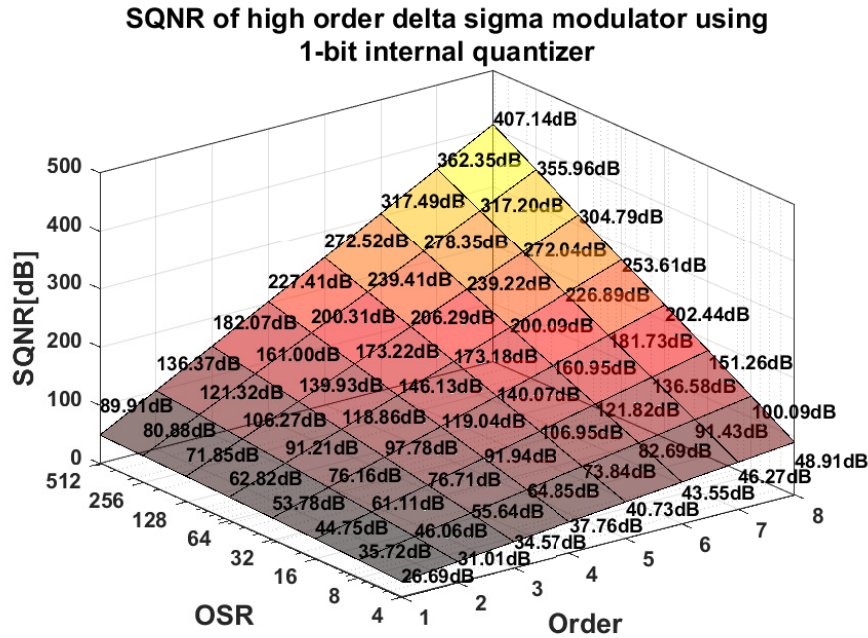
FIGURE 2.13: SQNR of high order delta sigma modulator using 1-bit internal quantizer.

when the resolution of internal quantizer is set, the SQNR of high order delta sigma modulator is a function of Order (R) and OSR based on the equations (2.29) and

(2.38). Assuming the full scale of the delta sigma is 1, the power of input signal can be written as $Power_{input\_signal} = (1/2)^2$, then the SQNR can be represented as:

$$SQNR = 10 \times log10(\frac{2^{2M-1}(24R+12)OSR^{2R+1}}{\pi^{2R}}), \qquad (2.39)$$

where, M means the resolution of the multi-bit internal quantizer. Figure 2.13 illustrates the SQNR varies Order and OSR of high order delta sigma modulator using 1-bit internal quantizer (M = 1). In practice, every increase the resolution of the internal quantizer by 1-bit, the SQNR can be increased by 6 dB, since, the SQNR of high order delta sigma modulator using M-bit internal quantizer can be estimated by the sum of the value shown in the figure 2.13 and $(M-1) \times 6$ dB (eg. when OSR is set as 64, the theoretical SQNR of 3th-order delta sigma modulator using 4-bit internal quantizer can be calculated as 118.86 dB + (4-1)×6 = 136.86 dB, where OSR = 64, R = 3, M = 4). Therefore, when design parameters of OSR, Order of delta sigma modulator, resolution of internal quantizer are confirmed, it is possible that the theoretical maximum SQNR of delta sigma modulator is calculated by using the equation (2.38) and figure 2.13. The SQNRs calculated by the equation 2.39 of high order delta sigma modulator with multi-bit (2 $\sim$ 6bit) internal quantizer are summarized in Appendix A.

2.4 Summary

In this chapter, the basic theory of delta sigma modulator, oversampling and noise shaping techniques are discussed. Moreover, the theoretical performance (SQNR) of the high order delta sigma modulator with multi-bit internal quantizer are summarized. According to design requirements, the parameters of delta sigma modulator can be derived from the equation (2.38) and figure 2.13, which can help circuit designer to define the architecture of delta sigma modulator appropriately.

References

[1]   R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004 (cit. on p. 16).

[2]   S. Pavan, R. Schreier, and G. Temes. *Understanding Delta-Sigma Data Converters (Second Edition)*. Wiley-IEEE Press, 2017 (cit. on p. 16).

Chapter 3

Delta Sigma Modulator Using Ring Amplifier

3.1 Preface

This chapter proposes a prototype of 2nd-order delta sigma modulator with dynamic analog components using multi-bit internal quantizer for low power and high SNDR application. The proposed delta sigma modulator is designed as the feed-forward structure that can tolerate the distortion of the integrator base on amplifier [1]. Moreover, that the multi-bit quantizer is used for the internal quantizer of the delta sigma modulator reduce the amplitude of the signal inside the feed-forward structure delta sigma modulator. Therefore, the slew-rate requirement on the integrator base on amplifier is relaxed for decreasing the difficulty of the amplifier design, and, the the power of the delta sigma modulator can also be reduce [2].

3.1.1 Drawback of Conventional Delta Sigma Modulator

In the conventional feed-forward delta sigma modulator, the integrator is realized by a traditional amplifier (eg. Operational Transconductance Amplifier (OTA)), due to it is necessary that the bias circuit in the traditional amplifier, the power consumption of traditional amplifier is very large. The multi-bit quantizer in the modulator is realized by a flash ADC, the power of the quantizer is still large because the static current though the resistance ladder and dynamic current of numerous comparators,

besides, an active analog adder using an amplifier is necessary at the input node of the quantizer, which increase the power of the modulator.

3.1.2   Concept of Proposed Delta Sigma Modulator

In the proposed delta sigma modulator, the integrators in the modulator are realized by ring amplifier without static current, the multi-bit quantizer and analog adder is realized by a passive-adder embedded SAR quantizer which consists of capacitor array and a dynamic comparator. In the dynamic comparator, the pre-amplifier is not used, since it does not dissipate static power at all.

As a result, an implementation architecture of 2nd-order feed-forward delta sigma modulator without active analog adder using ring amplifier is proposed for reducing the power consumption of the delta sigma modulator [3]. The proof-of-concept prototype of proposed modulator designed and fabricated in TSMC 90nm 1P9M CMOS technology is demonstrated. The integrators in the modulator are realized by modified differential ring amplifier with self bias circuits to reduce the static current as the same as that in [4], [5]. A passive-adder embedded SAR quantizer is realized by split capacitor array and a dynamic comparator. Measurement results also show the feasibility of delta sigma modulator with passive adder embedded SAR quantizer and Ring Amplifier [6].

3.2   Architecture

Figure 3.1 shows the block diagram proposed 2nd-order feed-forward delta sigma modulator with passive-adder embedded SAR quantizer. The feed-forward architecture is adopted to compress the distortion of integrators base on the amplifier.

The integrators consist of the ring amplifier in the loop filter of the proposed delta sigma modulator are introduced to reduce the power consumption of delta sigma modulator. A 4-bit SAR quantizer is chosen to realize the internal quantizer, it not only improve the stability of the modulator, but also relax the requirement on the slew-rate of amplifier. The SAR quantizer used as a multi-bit internal quantizer has
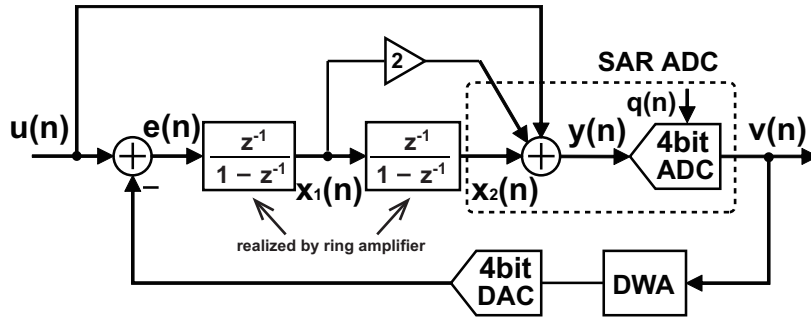
FIGURE 3.1: Block diagram of proposed 2nd-order feed-forward delta sigma modulator with passive-adder embedded SAR quantizer

three input terminals (As the figure 3.2, three input terminals of SAR quantizer are named as V_U, V_{o1} and V_{o2}, respectively.), and, the SAR quantizer converts the summation of three inputs to digital code. Hence, the analog adder at the front of the internal quantizer is realized by capacitor array and without operational amplifier. Due to the mismatches among the unit elements in a multi-bit digital-to-analog convertor (DAC) cause the harmonic distortion in the signal band of the delta sigma modulator, the data-weighted-averaging (DWA) logic circuit is applied to the delta sigma modulator to reduce the influence of DAC non-linearity errors.

3.3 Implementation

Figure 3.2 illustrates the simplified circuit implementation and clock timing chart of proposed 2nd-order feed-forward delta sigma modulator. Although a single-ended configuration is shown for simplicity, the actual circuit implementation is a fully differential structure.

3.3.1 Integrator using Ring Amplifier

Fully-Differential Ring Amplifier

Figure 3.3(a) shows the schematic diagram of proposed fully differential ring amplifier. The core of fully differential ring amplifier is shown in Figure 3.3(b). while C_C are added to the input nodes of amplifier to realize the amplifier input offset cancellation for the integrator. The amplifier is the key components of the modulator to
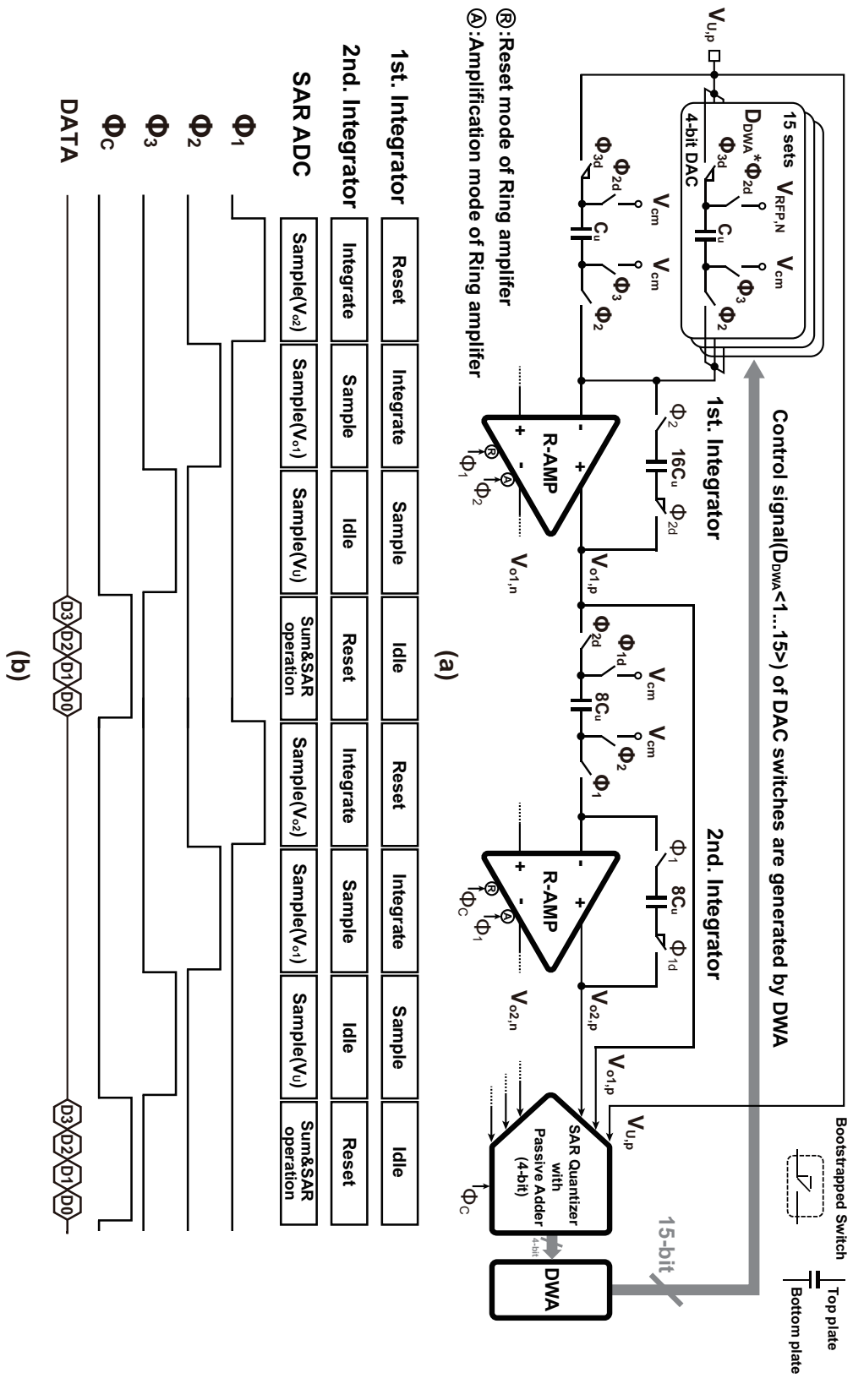
FIGURE 3.2: Circuit implementation of Proposed 2nd-order feed-forward delta sigma modulator using ring amplifier (R-AMP). (a) Schematic diagram. (b) Clock timing chart.
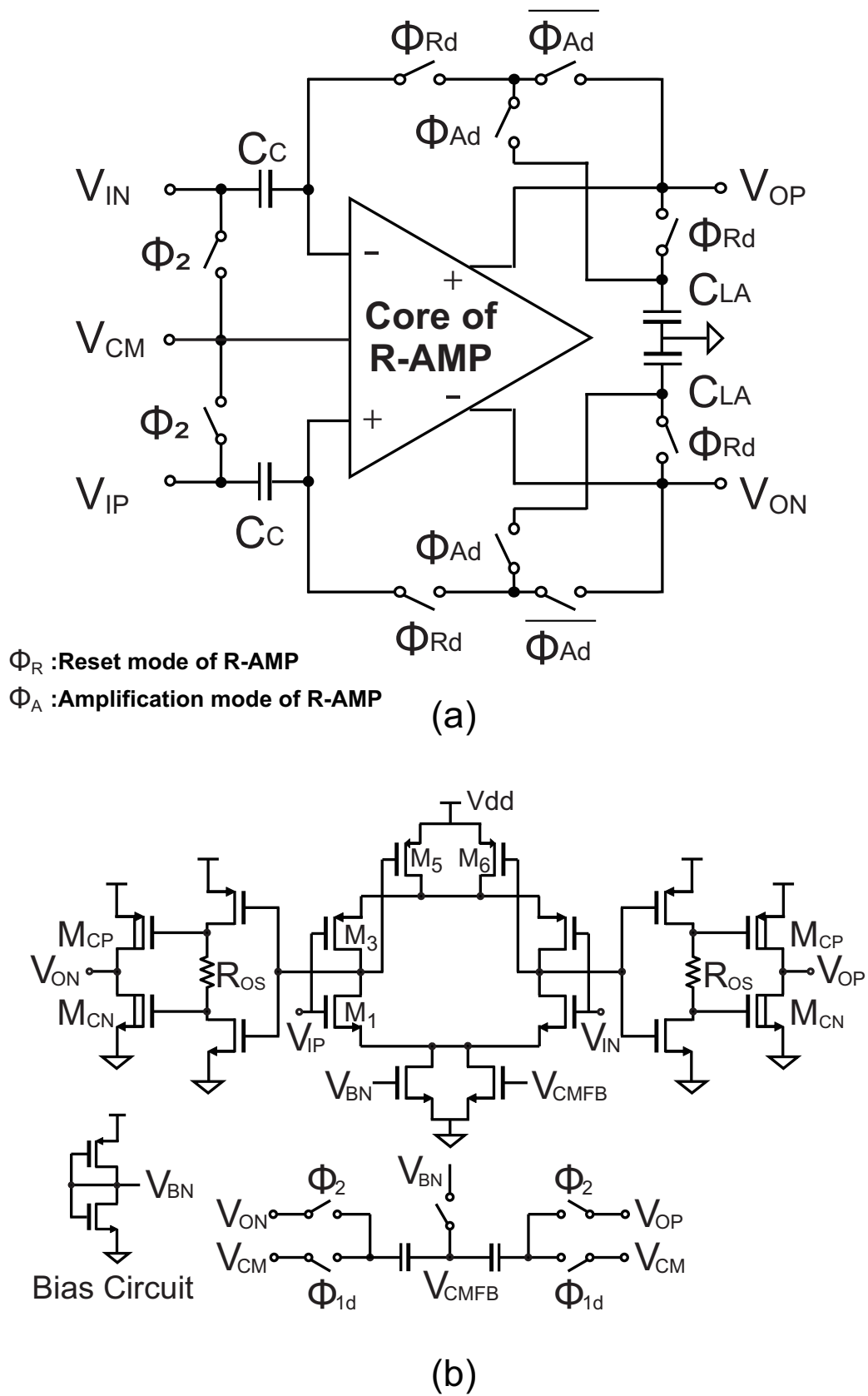
FIGURE 3.3: Schematic of fully differential R-AMP (Ring-Amplifier).
(a) R-AMP (Ring-Amplifier). (b) Core of R-AMP.

realize the integrator, and it is the most power-hungry circuit block in the modulator. Ring amplifier for multiplying digital-to-analog converter (MDAC) circuit has been proposed and demonstrated to reduce the power of the pipeline ADC [5]. In this paper, the integrator using the ring amplifier is proposed to reduce the power consumption.

Figure 3.3(b) shows the core of fully differential ring amplifier with the self bias circuit and the common-mode-feedback (CMFB) circuit. The fully differential ring amplifier is constructed with cascaded three stage inverters, it is similar to a ring oscillator. In order to stabilize the ring amplifier, The resistor R_{OS} is inserted at the output of the 2nd stage inverter as shown in the figure 3.3(b) to generate the different offset voltages to the gate of M_{CP} and M_{CN}. Moreover, the high threshold voltage MOSFET M_{CP} and M_{CN} are used in the 3rd stage to extend the stable offset voltage range for the integrator. As a result, there is no static current though M_{CP} and M_{CN}, the power consumption of integrator can be reduced dramatically. Because, M_{CP} and M_{CN} do not need to be biased in the saturated region like as conventional amplifier, the rail-to-rail output is allowed for the ring amplifier. The main structure of the ring amplifier in the proposed delta sigma modulator is based on the ring amplifier in [7], however, the simplified the bias and CMFB circuits are proposed for low supply voltage in this work. In [7], a cascaded PMOS is inserted between M_5 and M_3 to reduce the thermal noise of the amplifier. Because the thermal noise requirement on the amplifier in the delta sigma modulator can be relaxed much more than that in a Nyquist-rate ADC, the cascaded PMOS is removed to relax the headroom voltage of amplifier under low supply voltage. Furthermore, the bias circuit for ring amplifier can also be more simplified, only one PMOS and one NMOS are used to generate the bias voltage V_{BN} for the ring amplifier.

Action of Ring Amplifier

Because the operation of the integrator using inverter is similar as the operation of the ring amplifier's 3rd-stage, the operation of ring amplifier is discussed by means of the integrator using inverter for understanding the ring amplifier's action.

Figure 3.4 illustrates the schematic diagram of integrator using dynamic amplifier
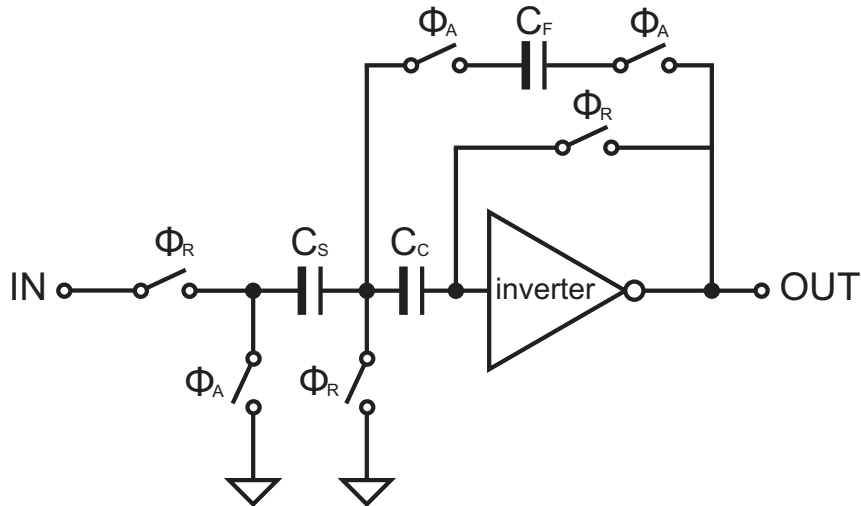
FIGURE 3.4: Integrator using dynamic amplifier consist of inverter.

consist of inverter. The C_S and the C_F are used as the sampling capacitor and the transition capacitor, respectively.

In sampling and reset mode, the input signal is sampled at the capacitor C_S, while the input terminal and output terminal of inverter are shorted as shown in the 3.5(a). Hence, the inverter forms a feed-back loop, that the both of the transistors (PMOS and NMOS of the inverter) are biased at the weak inversion region during the steady state can provide high DC-gain. The offset voltage between ground and inverter's input terminal can be saved on the offset cancel capacitor C_C.

In the transition mode, the input terminal of the inverter V_X is changed to (V_{OFF} − V_I) as shown in the figure 3.5(b). When the input signal V_I is greater than the common mode voltage ($V_I > 0$), the PMOS transistor is biased at the strong inversion region while the NMOS transistor is cut off. Oppositely, when the input signal V_I is less than the common mode voltage (($V_I < 0$)), the NMOS transistor is biased at the strong inversion region while the PMOS transistor is cut off. As a result, the negative feedback is formed, the charge on the sampling capacitor C_S is transferred to the transition capacitor C_F, and, the voltage of node V_X is recovered to the offset voltage V_{OFF}. When the charge transmission is completed, the both of the transistors (PMOS and NMOS) are operated at the weak inversion region again. Since, the transistor is operated at the strong inversion region during the transition mode for providing the high slew rate, the high slew rate can be realized with minimum static current.
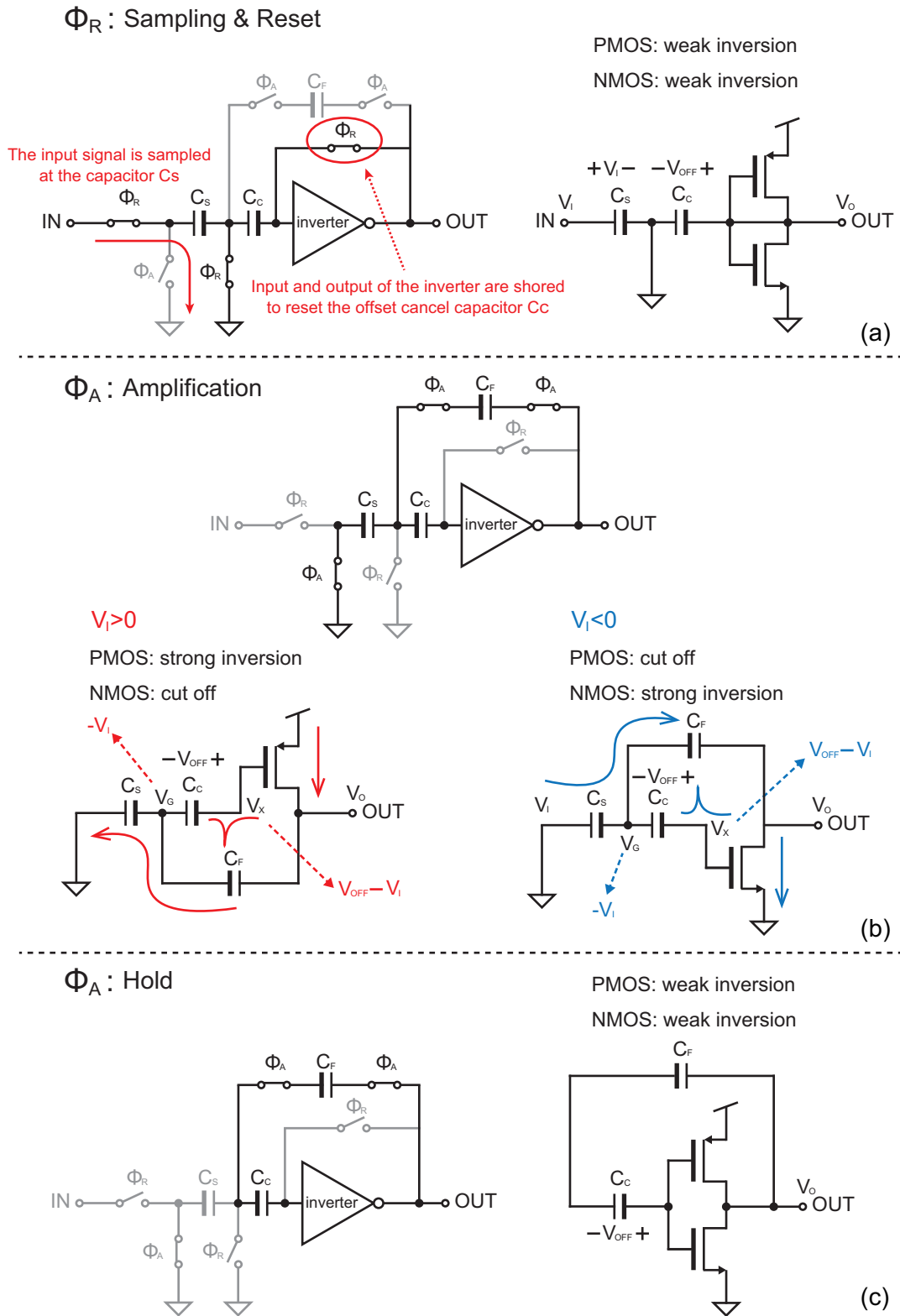
FIGURE 3.5: Operation of integrator using dynamic amplifier consist of inverter. (a) Sampling mode & Reset mode. (b) Amplification mode. (c) Hold mode.

Through Rate of Ring Amplifier

Since the output current of ring amplifier is not limited by the bias current, the setting time is decided by the output resistor of ring amplifier R_{out} and the load capacitance C_L, it can be calculated by

$$\tau_{setting\_time} = nR_{out}C_L, \tag{3.1}$$

where, n is a constant associated with the SNR requirement on the actual circuit.

Performance of Ring Amplifier

According to SPICE simulation results [3], the DC gain of ring amplifier reached to 84 dB with 74° phase margin with a 1.1 V supply voltage while the ring amplifier is biased at $V_{dd}/2$.
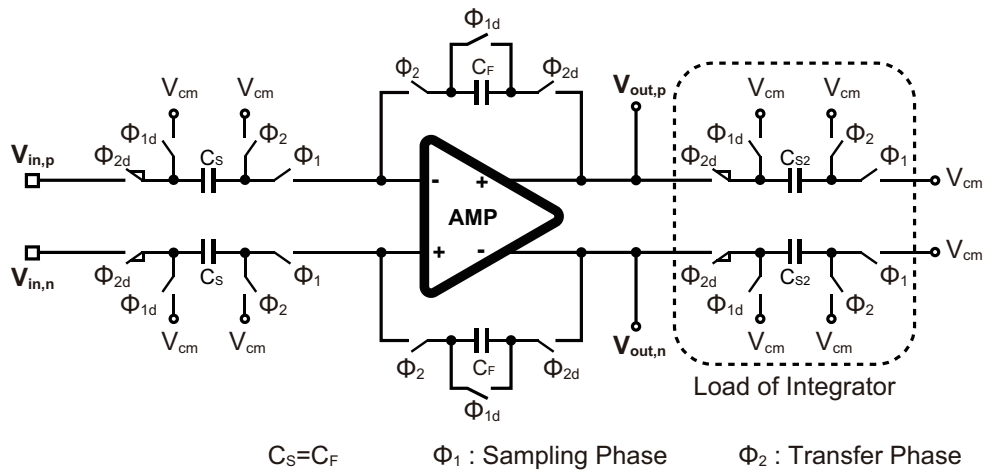
FIGURE 3.6: Track hold circuit using ring amplifier.
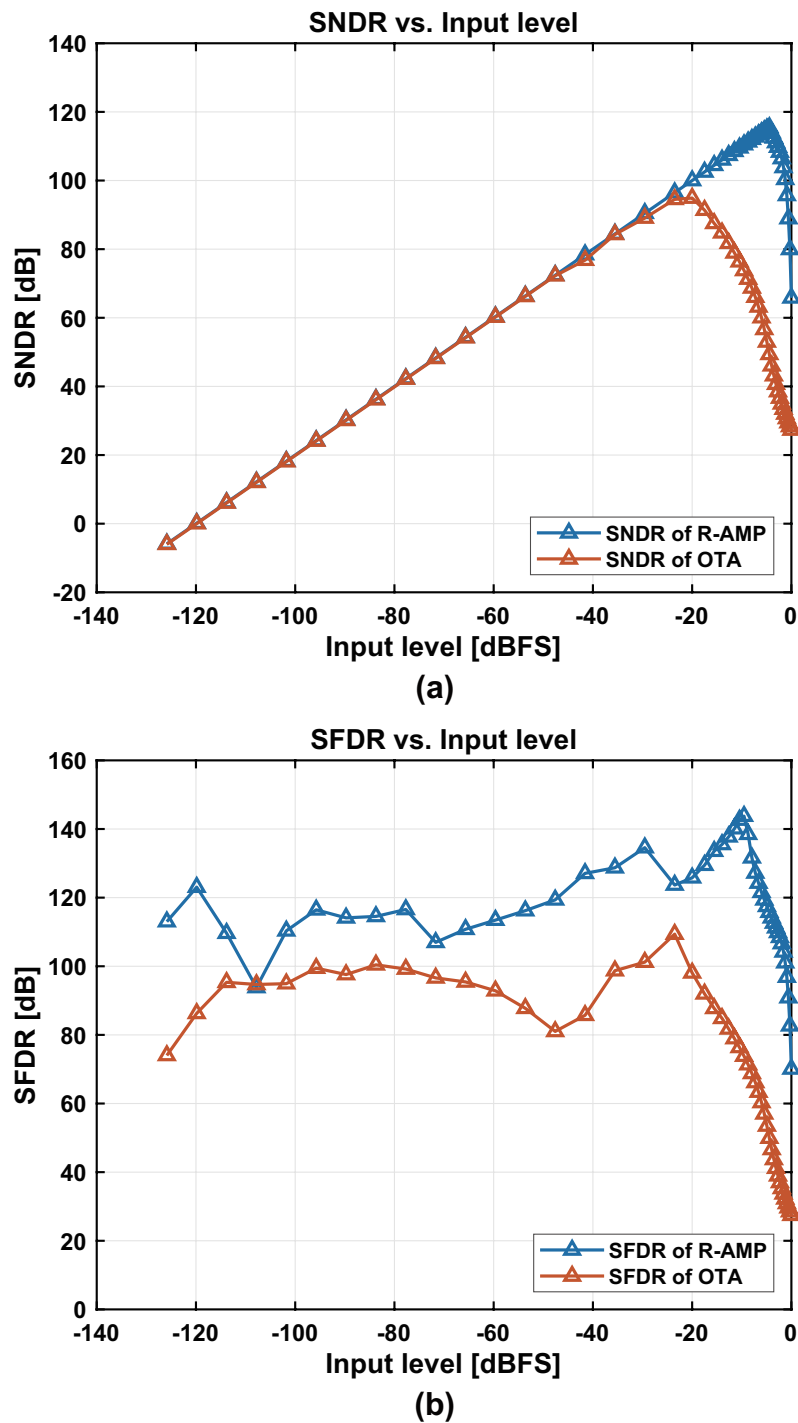
FIGURE 3.7: SNDR & SFDR versus Input level of T/H circuit using ring amplifier and OTA.

The track hold circuit shown in the figure 3.6 is proposed for conforming the performance of ring amplifier and comparing with the cascode OTA. In this T/H circuit, capacitor and switch are ideal analog components, only the ring amplifier and the cascode OTA are transistor level circuits, thus the performance of integrator is decided by amplifier circuits. Performing a transient simulation on the T/H circuit, we can get the PSD of output signal of the integrator. The performances of the ring amplifier and the cascode OTA can be conformed by calculating the SNDR, SFDR and THD of the output signal of the integrator using ring amplifier.
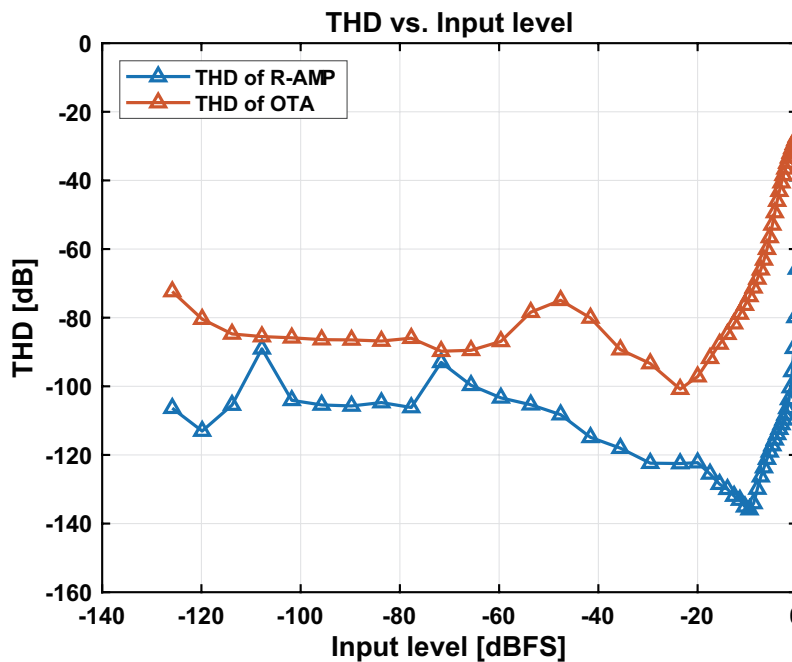
FIGURE 3.8: THD versus Input level of T/H circuit using ring amplifier and OTA.

Figure 3.7 shows the SNDR & SFDR versus input signal level of the T/H circuit using the ring amplifier and the cascode OTA, respectively, the SNDR and SFDR of the T/H using the ring amplifier are higher than that of the T/H using the cascode OTA. Figure 3.8 shows the THD versus input signal level of the T/H circuit using the ring amplifier and the cascode OTA, respectively. That the ring amplifier has lower THD than the cascode OTA means the linearity of the ring amplifier is better than the cascode OTA. As a result, the ring amplifier has the better performance than the cascode OTA at the same input level.

3.3.2 SAR Quantizer with Passive Adder

Capacitor Array & Operation Mode
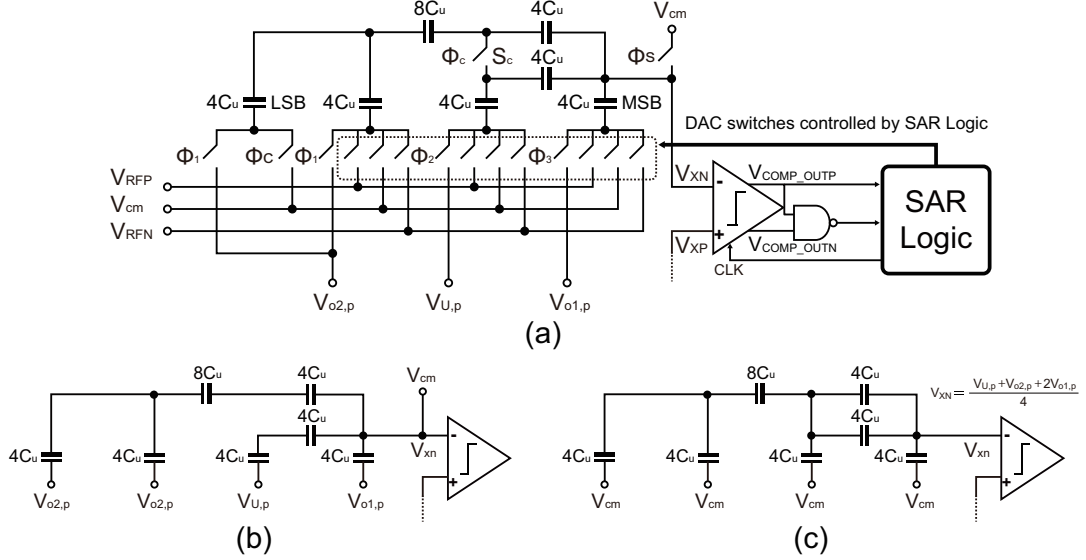
FIGURE 3.9: Implementation of proposed charge redistribution SAR quantizer and it's the equivalent circuit at two kinds of operation mode. (a) Schematic diagram. (b) Sampling mode. (c) Summation & SAR mode.

Figure 3.9(a) shows the schematic diagram of proposed SAR quantizer with embedded adder and figure 3.9(b)(c) shows two operation modes for equivalent circuit of passive-adder. In the sampling mode, the bottom plate of sampling capacitors are connected to input signals of $V_{U,p}$, $V_{o1,p}$ and $V_{o2,p}$ as shown in figure3.9(b) respectively. The capacitor ratio for 3 input signals is 1:1:2, then the total charge stored on the capacitors Q_{SA} can be expressed as:

$$Q_{SA} = 2C_u \times V_{o2,p} + 2C_u \times V_{U,p} + 4C_u \times V_{o1,p} \qquad (3.2)$$

In the summation mode shown in figure 3.9(c), the bottom plates of sampling capacitors are connected to V_{cm}, then the total capacitance between the input node of the comparator and V_{cm} is $8C_u$. The total charge on capacitor $8C_u$ is

$$Q_{SU} = 8C_u \times V_{xn} \qquad (3.3)$$

According to charge conservation law, we have

$$Q_{SA} = Q_{SU}. \tag{3.4}$$

Then, we get that

$$V_{XN} = \frac{Q_{SA}}{8C_u} = \frac{V_{o2,p} + V_{U,p} + 2V_{o1,p}}{4} \tag{3.5}$$

Equation (3.5) means that the summation of 3 input signals can be realized by proposed sampling technique for capacitor array. After the analog input summation is finished, the AD conversion is carried out from MSB to LSB as the same as a conventional SAR quantizer.

Switching Procedure
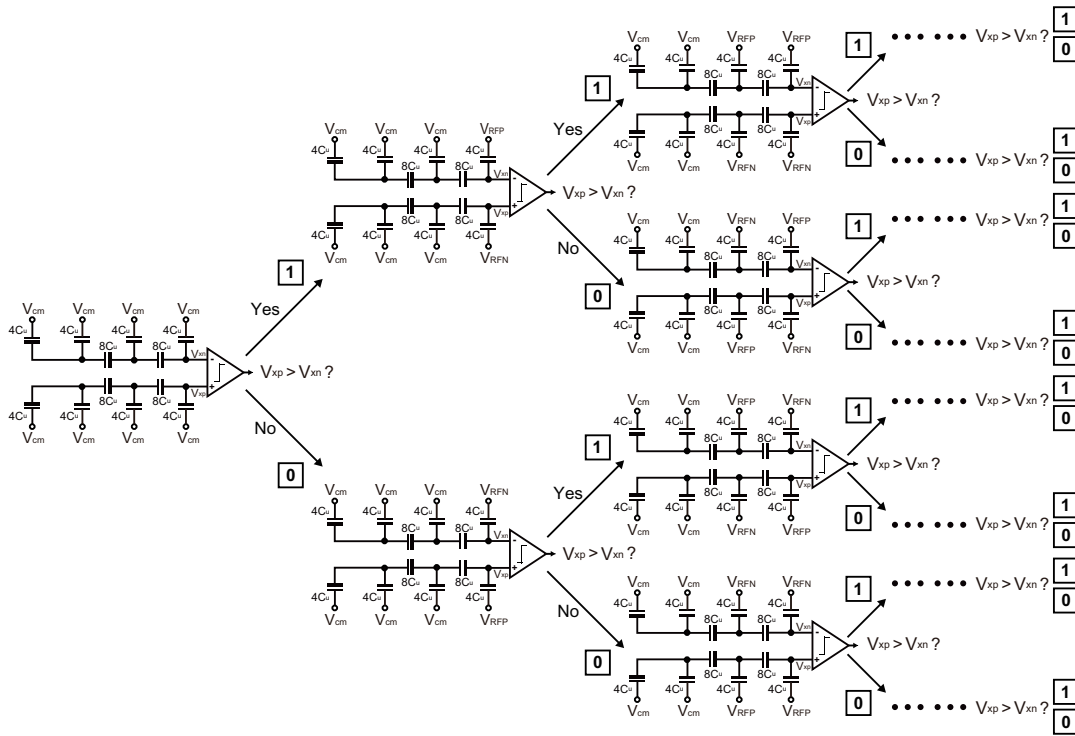
FIGURE 3.10: Switching procedure of proposed 4-bit SAR quantizer.

Figure 3.10 shows the switch procedure of proposed 4-bit SAR quantizer, and detailed the possible switching cases of the first 3 MSB bits. The switching cases of the LSB are omitted for simplicity. After the operations of sampling and summation are finished, the comparator performs the MSB comparison without switching any capacitors. Therefore, the switch procedure is efficient benefit from it do not consume

energy before the MSB comparison. As mentioned above, proposed SAR quantizer realizes not only a 4-bit quantizer but also an analog adder with the split capacitor array and a comparator, so that the power consumption of modulator can be reduce than the conventional feed-forward modulator using the active adder realized by amplifier.

The switch S_C is designed in the DAC capacitor array for realizing the coefficient of equation (3.2). Because the compare error of SAR quantizer can be seen as the quantization noise q(n) as shown in figure 3.1, the compare error is 2nd-order shaped by the delta sigma modulator that can be express the following equation (3.6)

$$V(z) = U(z) + (1 - z^{-1})^2 E_{com},$$ (3.6)

where the E_{com} is the compare error of the SAR quantizer. Therefore, the influence of the comparator error caused by the parasitic capacitor and the leakage current of the switch S_C can be weaken.

Dynamic Comparator Circuit
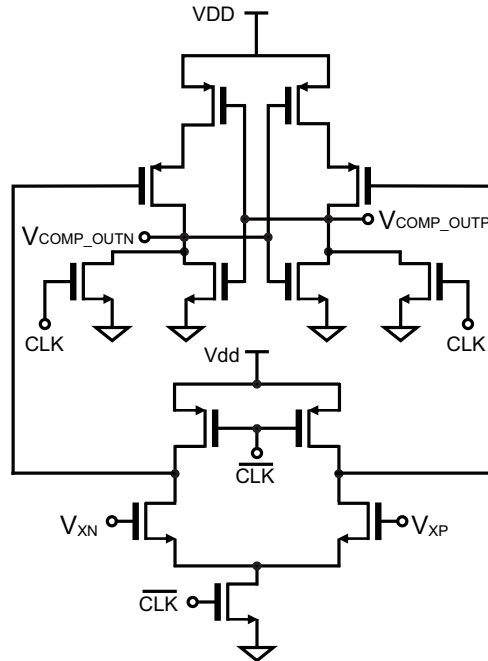
FIGURE 3.11: Schematic diagram of dynamic comparator.

Figure 3.11 shows the schematic of a comparator used in SAR quantizer. The differential output nodes of the dynamic comparator [8] is followed by a NAND gate

as shown figure 3.9(a). The inputs of NAND sense the toggle of differential comparator's output to realize the asynchronous operation of the SAR quantizer. While CLK is High, the comparator is in reset mode, the output nodes of V_{COMP_OUTP} and V_{COMP_OUTN} are reset to VDD. While CLK changes from High to Low, the voltage comparison of two input nodes is done. Then the comparator changes to the latch mode, the comparison result appear at nodes of V_{COMP_OUTP} and V_{COMP_OUTN}. Because these two output nodes are bounded to the inputs of NAND gate, while the voltage comparison is finished, NAND gate outputs a valid signal as a trigger signal of the asynchronous SAR logic circuit [9]. In a synchronous SAR quantizer, the CLK speed is limited by the worst-case cycle time. However, in the asynchronous SAR quantizer, the valid signal is generated by NAND gate, so that the conversion steps are executed consecutively. Therefore the speed of the asynchronous SAR logic is faster than the conventional synchronization SAR logic.

Asynchronous Successive Approximation Logic Circuit

3.3.3 Data Weighed Average Logic Circuit
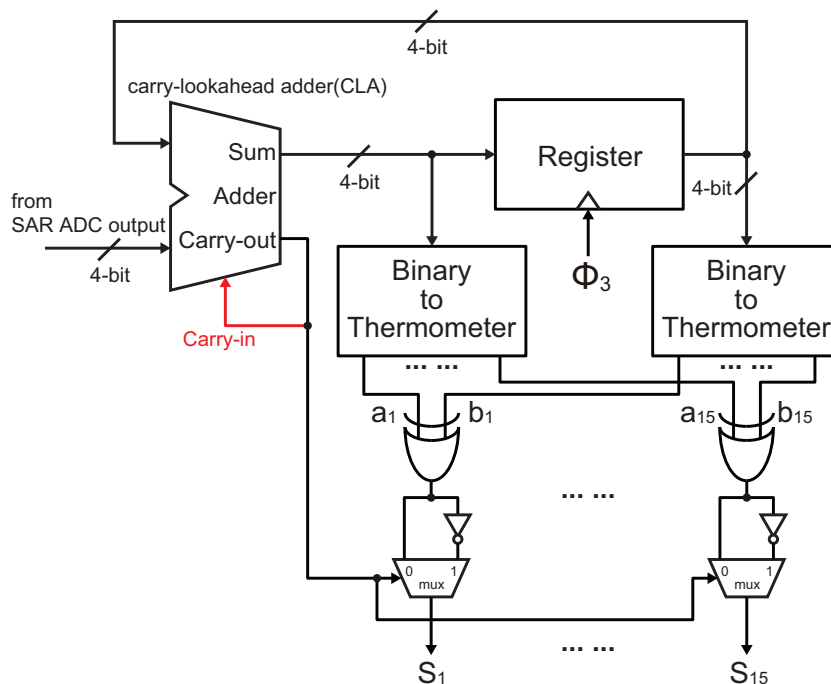
FIGURE 3.12: Schematic diagram of data-weighted-averaging.
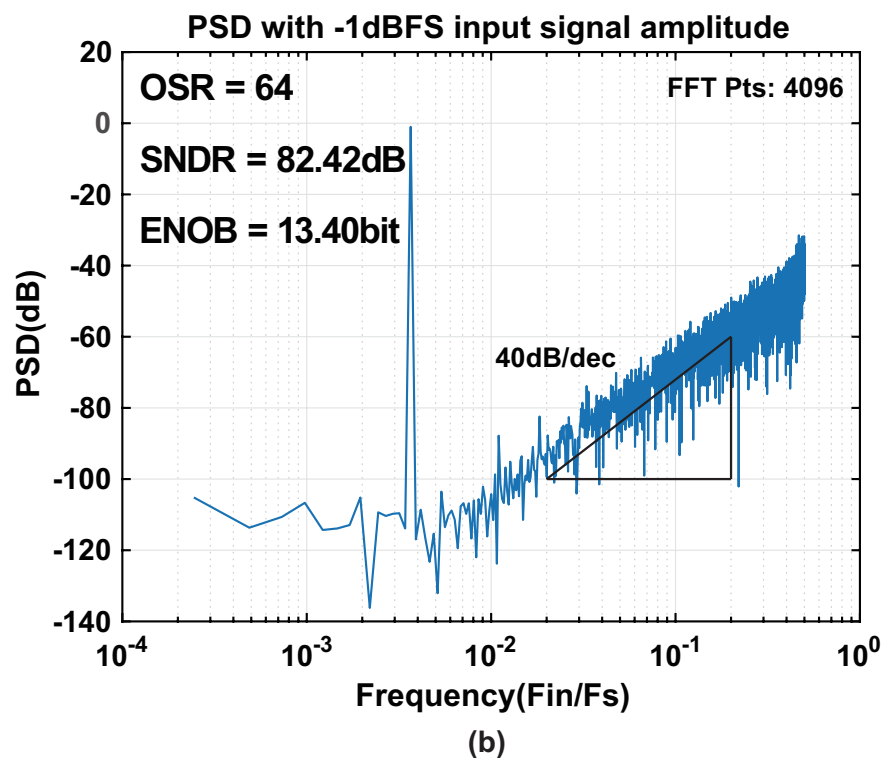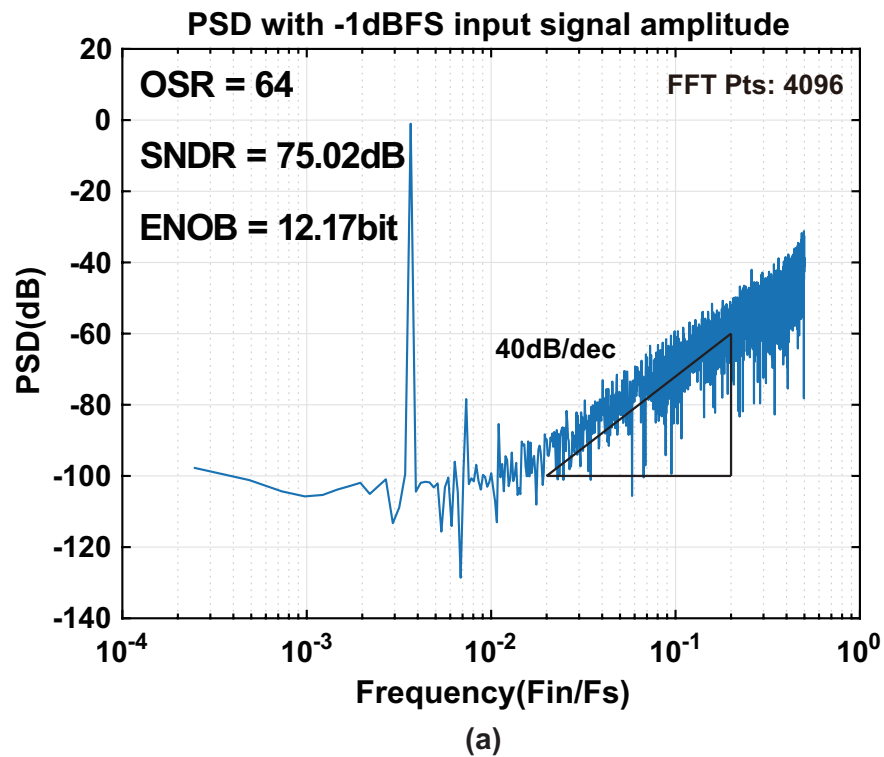
FIGURE 3.13: SPICE simulated results comparison of delta sigma modulator power spectrum at the ON/OFF mode of DWA. (a) DAC with 1% unit capacitance mismatches while DWA OFF Mode. (b) DAC with 1% unit capacitance mismatches while DWA ON Mode.

A 4-bit capacitor DAC is used for the 1st integrator, the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the DWA logic circuit [2] is applied to the delta sigma modulator to reduce the influence of DAC non-linearity errors. The implementation of DWA circuit is proposed in the previous work [10]. However, the DWA circuit converts the 4-bit quantizer output to the 16-bit control signals, it only can be used when a mid-tread quantizer which like the 4-bit flash ADC is used as the internal quantizer of the delta sigma modulator. In this work, because the 4-bit mid-rise SAR quantizer is used as an internal quantizer of the delta sigma modulator, the DWA circuit with 15-bit output control signals is requited. In this paper, an implementation of the DWA circuit is proposed for the 4-bit SAR quantizer as shown in figure 3.12. The proposed DWA circuit is adapted from the previous work [10], the carry-out of adder is feedback to the carry-in of adder in the DWA circuit. Therefore, one bits control signal of the DWA circuit is canceled. The proposed DWA circuit can convert the 4-bit SAR quantizer output to the 15-bit control signals, $S_i, i = 1, 2, ..., 15$, for the element selection of the 1st integrator's DAC as shown in figure 3.2. To illustrate the effect of the DWA logic circuit, SPICE simulation comparison with the proposed modulator is performed in 2 cases: (1) 4-bit DAC with 1% unit-capacitance mismatches while DWA at OFF mode; (2) 4-bit DAC with 1% unit-capacitance mismatches while DWA at ON mode. The output spectrum for above 3 cases are shown in figure 3.13(a) and (b), respectively. While the DAC with capacitance mismatches is used, the non-linearities of DAC raise the in-band noise floor, and cause the harmonic distortion as shown in figure 3.13(a). On the other hand, while DWA technique is applied, not only the in-band noise but also the harmonic distortion in the signal band are noise-shaped as shown in figure 3.13(b).

3.4   Noise Analysis

3.4.1   Noise Analysis of Ring Amplifier

Because the input-referred thermal noise voltage of ring amplifier is decided by the circuit of 1st-stage of ring amplifier, then, the noise voltage of ring amplifier is inspected as shown in the figure 3.14.
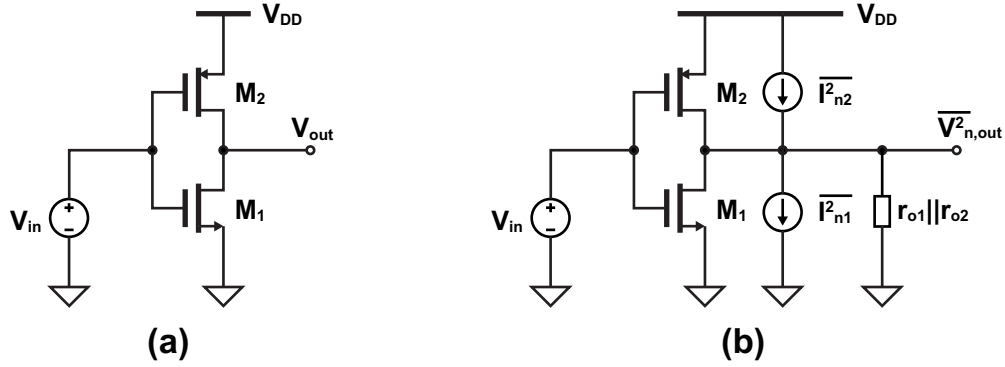
FIGURE 3.14: Schematic diagram of 1st-stage of ring amplifier for calculating the input-referred thermal noise voltage.

Assuming both transistors PMOS and NMOS as shown in the figure 3.14(a) are in saturation. Thus, the noise current sources of both transistors PMOS and NMOS can be drew as shown in the figure 3.14(b). The total output noise thermal noise can be determined when the ring amplifier drives a load capacitance C_L. The output signal-to-noise ratio can also be calculated when a low-frequency sinusoid of peak amplitude V_{peak} is applied to the input terminal of ring amplifier.

Because the noise current sources of both transistors PMOS and NMOS are uncorrelated, the noise by M_1 and M_2 at output terminal can be represented as:

$$S_{n,out}(f) = 4kT\gamma(g_{m1} + g_{m2})(r_{o1}||r_{o2})^2, \tag{3.7}$$

where, the γ is constant associated with CMOS technology, in reality, γ may not be the same for NMOS and PMOS devices, Since the voltage gain is equal to $(g_{m1} +$

$g_{m2})(r_{o1}||r_{o2})$, the total input-referred noise voltage to the gates of M$_1$ and M$_2$ is

$$S_{n,in}(f) = \frac{\overline{V_{n,out}^2}}{((g_{m1}+g_{m2})(r_{o1}||r_{o2}))^2} \tag{3.8}$$

$$= \frac{4kT\gamma}{g_{m1}+g_{m2}}. \tag{3.9}$$

The total output noise is calculated by integrating the equation (3.7) across the band:

$$\overline{V_{n,out,tot}^2} = \int_0^\infty 4kT\gamma(g_{m1}+g_{m2})(r_{o1}||r_{o2})^2 \frac{df}{1+(r_{o1}||r_{o2})^2C_L^2(2\pi f)^2} \tag{3.10}$$

$$= \gamma(g_{m1}+g_{m2})(r_{o1}||r_{o2})\frac{kT}{C_L}. \tag{3.11}$$

Therefore, a low-frequency input sinusoid signal of amplitude V$_{peak}$ yields an output signal of amplitude $(g_{m1}+g_{m2})(r_{o1}||r_{o2})V_{peak}$. The SNR of output signal is equal to the ratio of the signal power and noise power:

$$SNR_{out} = [\frac{((g_{m1}+g_{m2})(r_{o1}||r_{o2})V_{peak})^2}{2}] \times \frac{1}{\gamma(g_{m1}+g_{m2})(r_{o1}||r_{o2})(kT/C_L)}. \tag{3.12}$$

In order to conform the output noise of ring amplifier, the transient simulation with random noise calculated by the thermal noise model of transistor on the T/H circuit shown in the figure 3.6 has been preformed. Figure 3.15 shows the simulated output power spectrum of T/H circuit using ring amplifier. The values of SNDR, SFDR and THD are shown in the figure 3.15(a) and (b), respectively. Because the OSR of proposed 2nd-order delta sigma modulator using ring amplifier is set to 64, as shown in the figure 3.15(b), the delta sigma modulator using ring amplifier can realize the maximum SNDR of 89.31 dB due to the noise limitation on the ring amplifier.

3.4.2 Noise Analysis of Integrator using Ring Amplifier

The input referred noise of ring amplifier has been discussed at above article. Next to consider the noise analysis the integrator using ring amplifier shown in the figure 3.16. As shown, the input signal is sampled on the capacitor C$_S$ during the phase Φ_R,and The charge C$_s$V$_{IN}$ is stored at the end of the phase. The input and output
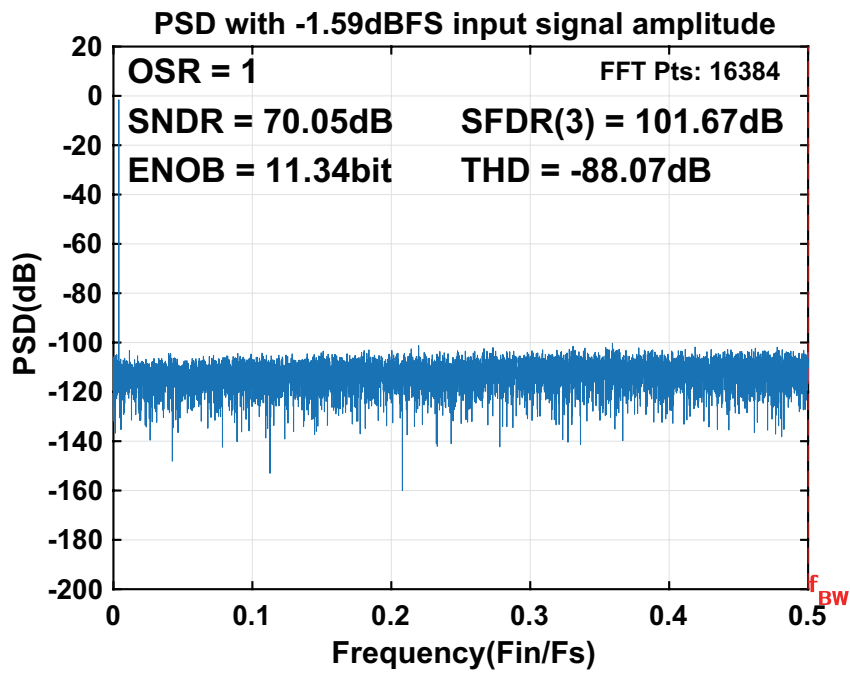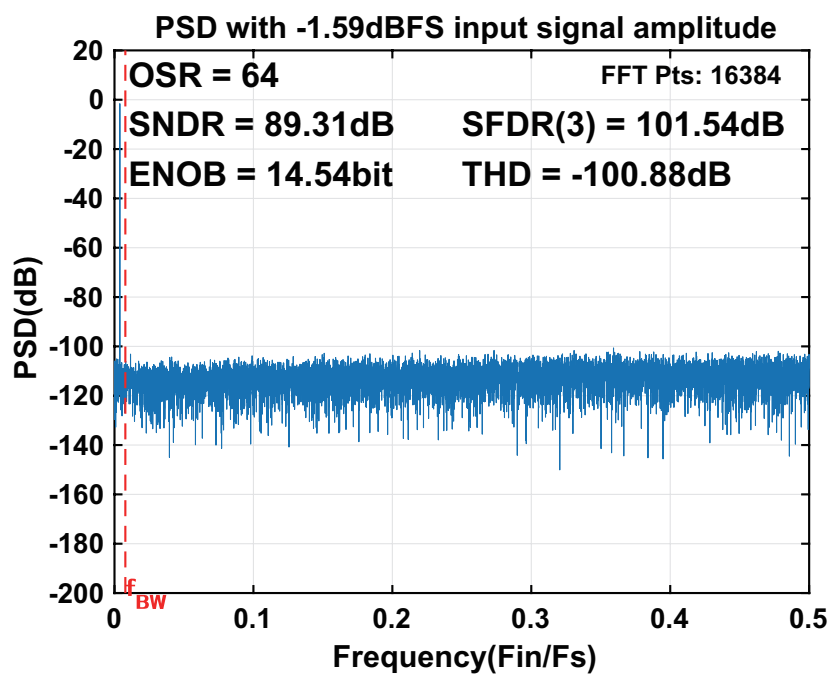
FIGURE 3.15: Simulated output power spectrum of T/H circuit using ring amplifier.
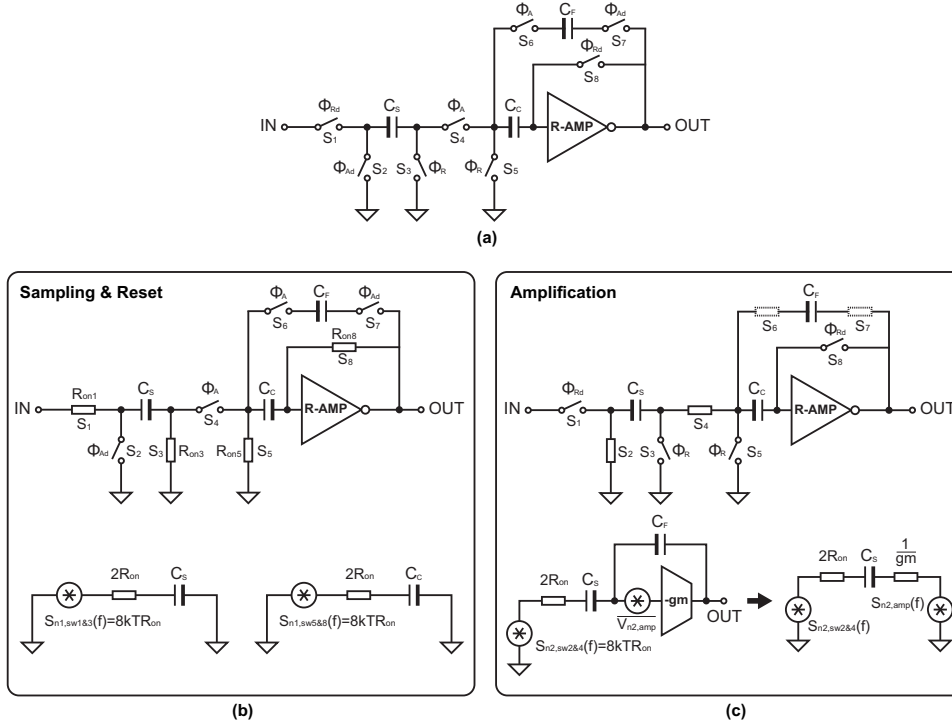
FIGURE 3.16: Noise analysis of integrator using ring amplifier. (a) Circuit implementation of integrator using ring amplifier. (b) The equivalent circuit with noise source at the sampling and reset phase. (c) The equivalent circuit with noise source at the amplification phase.

terminal of ring amplifier are shored, the difference between input terminal of ring amplifier and ground is stored in C_C.

In the phase Φ_R, the significant noise effect introduced by these switches is thermal noise. To find the thermal noise generated in switches S_1, S_3 and S_5, S_8, assume the input signal equal to zero. The conducting switches S_1, S_3 and S_5, S_8 can be replaced by their noise voltages and on-resistances, and the noise voltages and resistors can be pairwise combined as shown in the figure 3.16(b). Assuming that all switches have the same R_{on}, the combined switch resistance is $2R_{on}$ and the PSD of the associated noise voltages is

$$S_{n1,sw1\&3}(f) = S_{n1,sw5\&8}(f) = 4kT(2R_{on}) = 8kTR_{on}. \tag{3.13}$$

The mean square value of noise generated in switches S_1, S_3 can be calculated as

$$\overline{V^2_{n1,sw1\&3}} = \int_0^\infty 8kTR_{on} \frac{1}{1 + (2R_{on})^2 C_S^2 (2\pi f)^2} \, df \tag{3.14}$$

$$= \frac{8kTR_{on}}{4(2R_{on})C_S} \tag{3.15}$$

$$= \frac{kT}{C_S} \tag{3.16}$$

which is independent of R_{on}. In a similar way, the mean square value of noise generated in switches S_5, S_8 can be given by

$$\overline{V^2_{n1,sw5\&8}} = \frac{kT}{C_C}. \tag{3.17}$$

When phase Φ_A rises, switches S_2, S_4 close. C_S discharges $C_S V_{IN}$ into the virtual ground generated by the ring amplifier during the phase Φ_A. This causes the charge stored in C_F at the end of Φ_A. The on-resistances and noise voltages of the two switches have been combined, and, when the amplifier drive a high impedance circuit, the circuit integrator in the phase Φ_A is simplified as shown in figure 3.16(c). The noise power (mean-square value) caused by switches S_2, S_4 in C_S can be given by

$$\overline{V^2_{n2,sw2\&4}} = \int_0^\infty 8kTR_{on} \frac{1}{1 + (2R_{on} + 1/g_m)^2 C_S^2 (2\pi f)^2} \, df \tag{3.18}$$

$$= \frac{8kTR_{on}}{4(2R_{on} + 1/g_m)C_S}. \tag{3.19}$$

The input-referred noise voltage of single-ended ring amplifier has been calculated by the equation (3.9), When assuming the differentially ring amplifier is symmetrical, the input-referred noise voltage of differentially ring amplifier is double of value represented by equation (3.9). Hence, the noise power (mean-square value) in C_S due to amplifier can be calculated as

$$\overline{V^2_{n2,ramp}} = \int_0^\infty \frac{8kT\gamma}{g_{m1} + g_{m2}} \frac{1}{1 + (2R_{on} + 1/g_m)^2 C_S^2 (2\pi f)^2} \, df \tag{3.20}$$

$$= \frac{4kT\gamma}{8(g_{m1} + g_{m2})(2R_{on} + 1/g_m)C_S}. \tag{3.21}$$

where, g_{m1} and g_{m2} are the transconductance of NMOS and PMOS in 1st-stage of ring amplifier, respectively, the g_m is the transconductance of ring amplifier. If PMOS and NMOS of 1st-stage of ring amplifier have same transconductance, i.e. g_{m1} equal to g_{m2}, the equation (3.21) can be simplified as:

$$\overline{V_{n2,ramp}^2} = \frac{kT\gamma}{2R_{on}g_{m1} + g_{m1}/g_m}. \tag{3.22}$$

Moreover, the noise voltages on the output of integrator caused by switches S_6 and S_7 not be amplified by the ring amplifier, since, they are negligible compare to that of switches S_1, S_2, S_3, S_4. Considering the total noise power stored in the sampling capacitor C_S. At the end of clock phase Φ_R, as illustrated in the figure 3.16(b), The sampling capacitor C_S had acquired a noise voltage $\overline{V_{n1,sw1\&3}^2}$ whose noise power was given by the equation (3.16). During phase Φ_A, the noise voltage becomes $\overline{V_{n1,sw5\&8}^2}+$ $\overline{V_{n2,sw2\&4}^2}+ \overline{V_{n2,ramp}^2}$, which have the noise powers given by equations (3.17), (3.19) and (3.21). Since the three noise voltages are uncorrelated, their power are added. if the conditions $R_{on}g_{m1} \gg 1$ and $0 < g_{m1}/g_m < 1$ hold, all of the noise is contributed by the switches. Due to the input-referred noise of the ring amplifier is inversely proportional to g_m, the noise from the ring amplifier is negligible. Hence, the total input-referred noise power of integrator using amplifier is

$$\overline{V_{n,tot,ramp}^2} = \overline{V_{n1,sw1\&3}^2} + \overline{V_{n1,sw5\&8}^2} + \overline{V_{n2,sw2\&4}^2} \tag{3.23}$$

$$= \frac{2kT}{C_S} + \frac{kT}{C_C}. \tag{3.24}$$

Since,the sampling capacitor of integrator affect the chip area, power consumption and the resolution of the delta sigma modulator, the capacitance of sampling capacitor in the 1st integrator is determined according to the sampled thermal noise (kT/C noise) of switched-capacitor circuits. The theory of kT/C noise in integrator using amplifier is calculated at the above discussion. The input capacitors associated with thermal noise is given by

$$C = \frac{2(2n+1)kT \times 10^{\frac{SNDR}{10}}}{nV_{FS}^2} \frac{1}{OSR}. \tag{3.25}$$

where, that the capacitance C_C is n times of C_S (i.e. $C_C = n \times C_S$) is defined, k = 1.38×10^{-23}J/K is the Boltzmann's constant, T is the absolute temperature of the device in degrees Kelvin, V_{FS} is the full scale voltage of the input signal, and OSR is oversampling ratio of the modulator. In our modulator, the full scale voltage of input amplitude is designed as 2 V (the peak-to-peak voltage of differential signals) while the supply voltage is $V_{dd} = 1.2$V. As a result, the sampling capacitor of the first integrator is designed as 400 fF according to equation (3.25) to guarantee the thermal noise is small enough for ENOB = 14 bit (SNDR = 86.04 dB) with -1 dBFS input at OSR = 64. The input noise at the 2nd integrator can be shaped by the 1st integrator, the in-band noise power is much more smaller than the 1st integrator. Therefore, the input capacitance of the 2nd integrator can be scaled down. In this work, we focus the research target on the feasibility verification of the integrator with ring amplifier. The sampling capacitor of the 2nd integrator is designed as 200 fF, which is scaled to one half of that in the 1st integrator to reduce the total power and active area of the modulator.

Due to the noise power cause by the offset cancel capacitor C_C is discharge to the output of integrator using ring amplifier, the total input-referred noise power of integrator using ring amplifier is larger than that of integrator using OTA gived by 2kT/C_S [2]. However, since the ring amplifier has the flat open-loop-gain, its linearity is better than the traditional OTA.

3.4.3   Noise Analysis of Dynamic Comparator

Noise Analysis using PSS+PNOSE Simulation

Due to the dynamic comparator does not include the bias circuit, the DC operation point of the dynamic comparator can not be conformed, the traditional noise analysis simulation method is not suitable for the noise analysis of the dynamic comparator.

The noise analysis simulation methods using the periodic steady-state analysis (PSS) and the periodic noise analysis (PNOISE) have been proposed for calculating the noise of dynamic comparator [11]. Figure 3.17 shows the schematic diagram for the
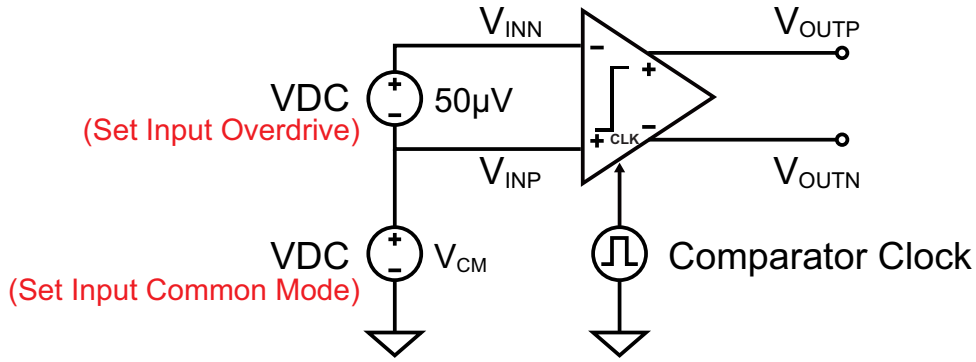
FIGURE 3.17: Schematic diagram for the noise analysis simulation of dynamic comparator using PSS and PNOISE.

noise analysis simulation of dynamic comparator using PSS and PNOISE. The PSS and PNOISE simulation can calculate the noise power of the dynamic comparator by means of the statistics of the jitter noise in the frequency domain. The dynamic comparator shown in the figure 3.11 has the input equivalent noise of 0.185 μW that can be calculated by using the PSS and PNOISE simulation methods. Thus, when the sine signal with the maximum amplitude of 1.2 V is input to the dynamic comparator, the SNR can be expressed as:

$$SNR = 20 \times log10(\frac{Amplitude_{Input\_sine\_signal}^2/2}{Power_{Input\_equivalent\_noise}}) \, [dB], \quad (3.26)$$

where, the SAR quantizer using the dynamic comparator can realize the maximum SNR of 75.90 dB (i.e. the maximum ENOB of 12.32 bit). Since, the SAR quantizer with the resolution of 6-bit is required for ensuring the 4-bit quantization and the summation of 3 input analog signals in the proposed delta sigma modulator, according to the simulation result of PSS and PNOISE, the proposed dynamic comparator can be used to realize the 4-bit SAR quantizer with passive adder.

Noise Analysis using Time-Transient Simulation with Random Noise

In order to obtain noise power of the dynamic comparator closer to the actual situation, in this paper, the noise analysis method using the time transient simulation with random noise is proposed for the noise analysis of the dynamic comparator. The proposed noise analysis method can estimate the the noise power of dynamic
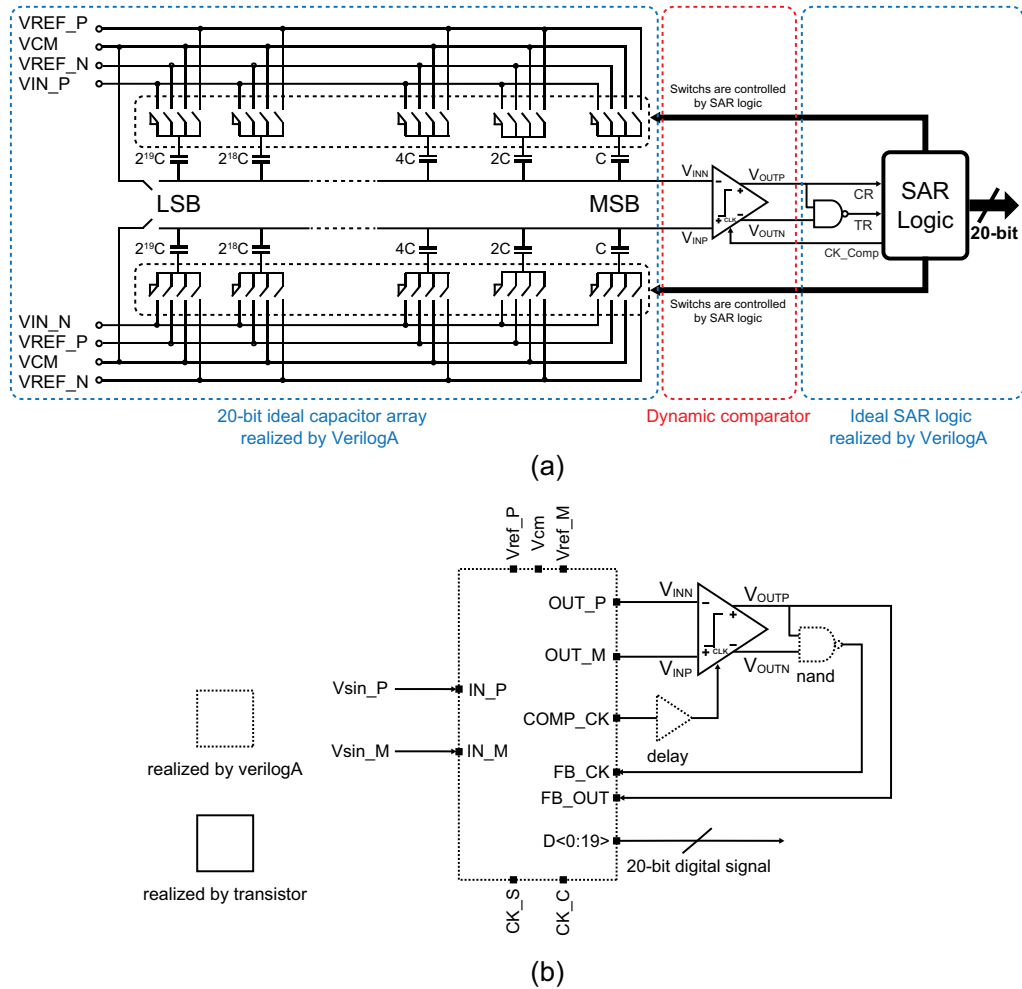
FIGURE 3.18: Circuit implementation for noise analysis of dynamic comparator. (a) Architecture of ideal 20-bit SAR quantizer. (b) Schematic diagram of ideal 20-bit SAR quantizer.

comparator by performing the time transient simulation with random noise of 20-bit ideal SAR quantizer. Figure 3.18(a) shows the architecture of the ideal 20-bit SAR quantizer. Except for the dynamic comparator circuit realized by transistors, the capacitor array, switch array and the successive approximation logic circuit (SAR Logic) of the ideal 20-bit SAR quantizer are realized by verilog-A code. Therefore, the noise power of the dynamic comparator can be obtain by measuring the performance of the ideal 20-bit SAR quantizer, when the noise power of the dynamic comparator is larger than the noise power of the 20-bit SAR quantizer. Figure 3.18(b) shows the schematic diagram of the ideal 20-bit SAR quantizer used for measuring the noise power of the dynamic comparator. Because, the ideal 20-bit capacitor DAC, ideal SAR logic, "delay" circuit, and "nand" logic gate are realized by verilog-A code, they can be seen as the ideal analog components (not include any noise). The verilog-A codes associated with the ideal 20-bit SAR quantizer are appended in the Appendix B.

Time transient simulation with random noise has been performed for measuring the performance of the ideal 20-bit SAR quantizer. The dynamic comparator shown in the figure 3.11 is used in the ideal 20-bit SAR quantizer circuit. The power spectrum of the ideal 20-bit SAR quantizer is shown in the figure 3.19. Figure 3.19(a) illustrates the power spectrum of ideal 20-bit quantizer without noise, since, it does not include any noise, the SNDR of 122.18 dB and the ENOB of 20.00 bit are achieved. Figure 3.19(b) illustrates the power spectrum of ideal 20-bit quantizer with random noise. The SNDR of 79.46 dB and the ENOB of 12.94 bit are achieved, that means the maximum 12.94 bit ADC can be realized when the dynamic comparator is used. Although the result of transient simulation with random noise is similar as the one of the PSS and PNOISE simulation, since, the transient simulation of the ideal 20-bit SAR quantizer with random noise closer to the real situation, it can provide the more accurate noise estimate.
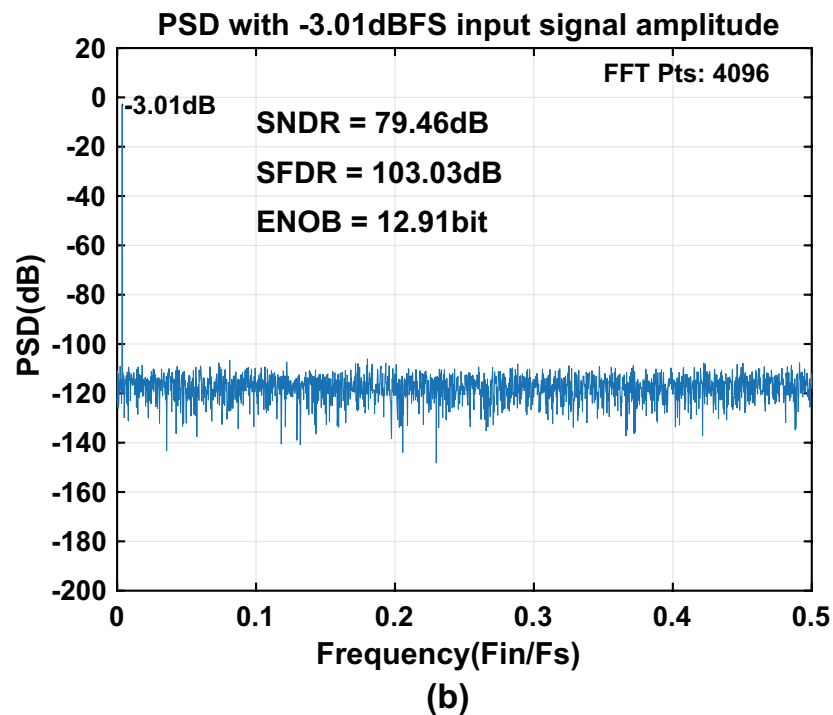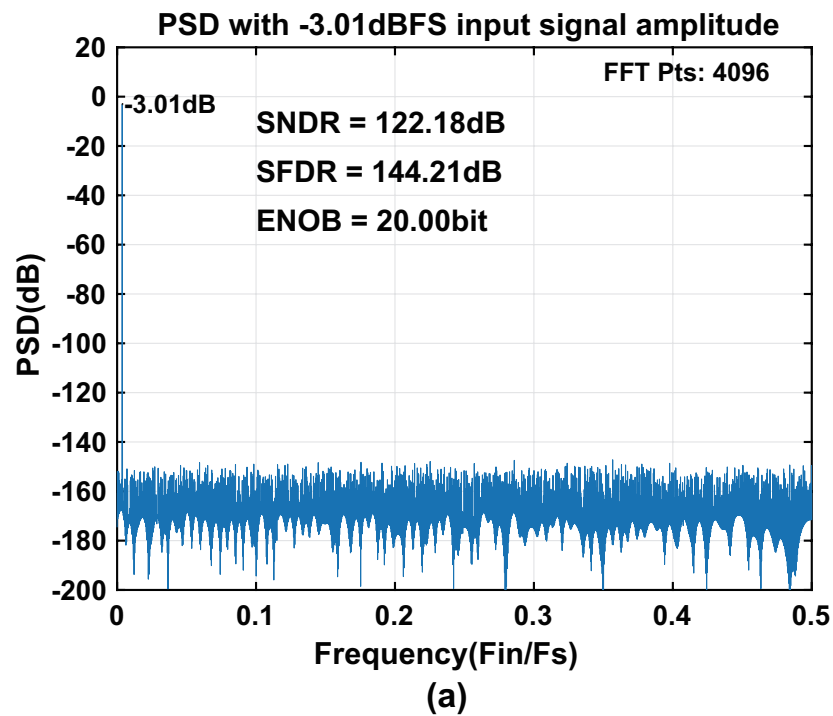
FIGURE 3.19: Power spectrum of ideal 20-bit SAR quantizer. (a) Power spectrum of ideal 20-bit SAR quantizer without noise. (b) Power spectrum of ideal 20-bit SAR quantizer with noise.

TABLE 3.1: Simulation parameters of delta sigma modulator

Technology	TSMC 90nm CMOS
Supply voltage	1.2V
Input frequency	146.5kHz
Input amplitude	2Vpp
Sampling rate	40MS/s
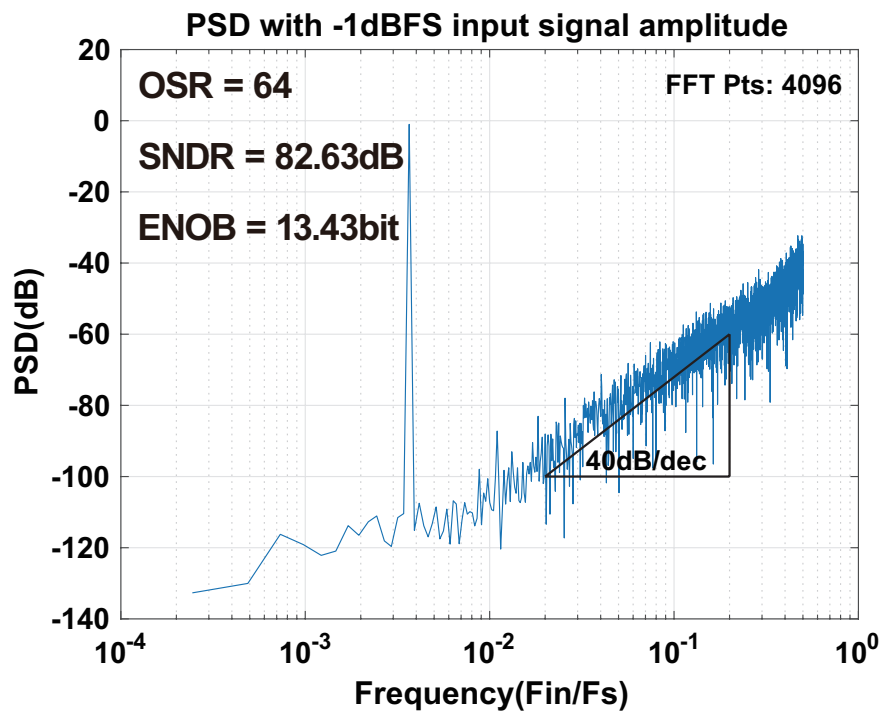
FIGURE 3.20: Simulated output power spectrum of proposed 2nd-order feed-forward delta sigma modulator (@Supply voltage = 1.2 V).

3.5 Simulation

The propose delta sigma modulator shown in figure 3.2 is designed in TSMC 90 nm CMOS technology. The switched-capacitor integrators are realized by ring amplifier. The quantizer is a 4-bit SAR quantizer with the embedded passive adder. 4-bit DAC on the feedback path is constructed by capacitor array. The DWA logic circuit is designed to reduce the influence of the non-linearities which occurred by the capacitors mismatch of the multi-bit DAC[2]. SPICE simulations have been done to confirm the functionality of the modulator and to verify the effectiveness of the proposed architecture. The simulation parameters are shown in Tab. 3.1. Figure 3.20 shows the simulated spectrum result of the proposed delta sigma modulator without DAC unit-capacitance mismatches. Figure 3.13(b) shows the simulated spectrum result of the proposed modulator with 1% DAC unit-capacitance mismatches. The peak SNDR of 82.42 dB is reached while OSR = 64 for a sinusoid input at 146.5 kHz with -1 dBFS input amplitude (The thermal noise of the modulator is not included in the SPICE simulation).

3.6 Measurement

3.6.1 Layout and Microphotograph

The proposed delta sigma modulator was fabricated in TSMC 90 nm 1P9M CMOS technology. Figure 3.21 shows the chip microphotograph and layout of the delta sigma modulator. The active area of the delta sigma modulator is 0.155 mm^2. Bootstrapped switch is used at the inputs of the 1st integration and the input of the SAR quantizer to reduce the nonlinear effect of ON-resistance [12]. All capacitors were laid out using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized by using the MIM capacitors for high density capacitance in a small chip area. Careful layout design has been done to keep the analog part of the delta sigma modulator is symmetrically arranged. The attention also paid to keeping the sensitive analog signals away from the noisy digital signal paths.
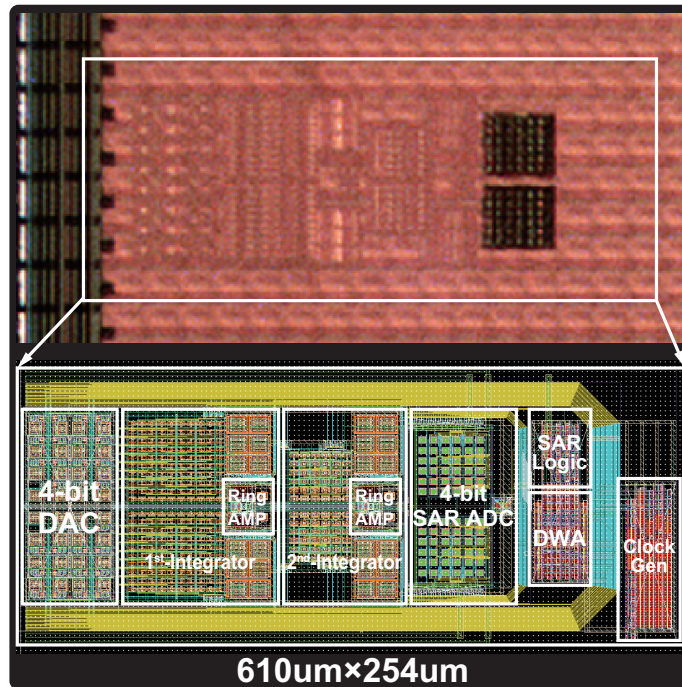
FIGURE 3.21: Chip microphotograph and layout of the prototype modulator.

3.6.2 Measurement Results

The proposed 2nd-order delta sigma modulator is designed and fabricated in the TSMC 90nm 1P9M CMOS technology without any option for precision capacitors and low threshold voltages. Figure 3.21 shows a microphotograph of the experimental prototype and the layout of the delta sigma modulator. The active area of the delta sigma modulator is $610\bar{}$m $\times$ $254\bar{}$m. Bootstrapped switch is used at the inputs of the delta sigma modulator to reduce the nonlinear effect of ON-resistance [12]. All capacitors were laid out using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized by using the MIM capacitors for high density capacitance in a small chip area. Careful layout design has been done to keep the analog part of the delta sigma modulator is symmetrically arranged. The attention is also paid to keep the sensitive analog signals away from the noisy digital signal path.

Figure 3.22 shows the measured output power spectrum of the prototype modulator for a 5.493 kHz sinusoid differential -1 dBFS input sampled at 12 MS/s. The peak
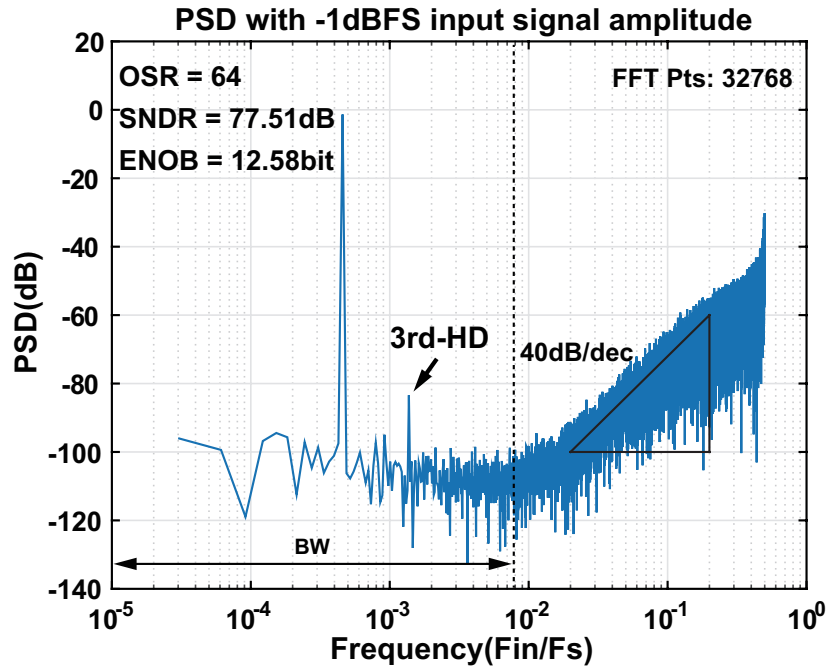
FIGURE 3.22: Measured output power spectrum of proposed 2nd-order feed-forward delta sigma modulator (@Supply voltage = 1.1 V).
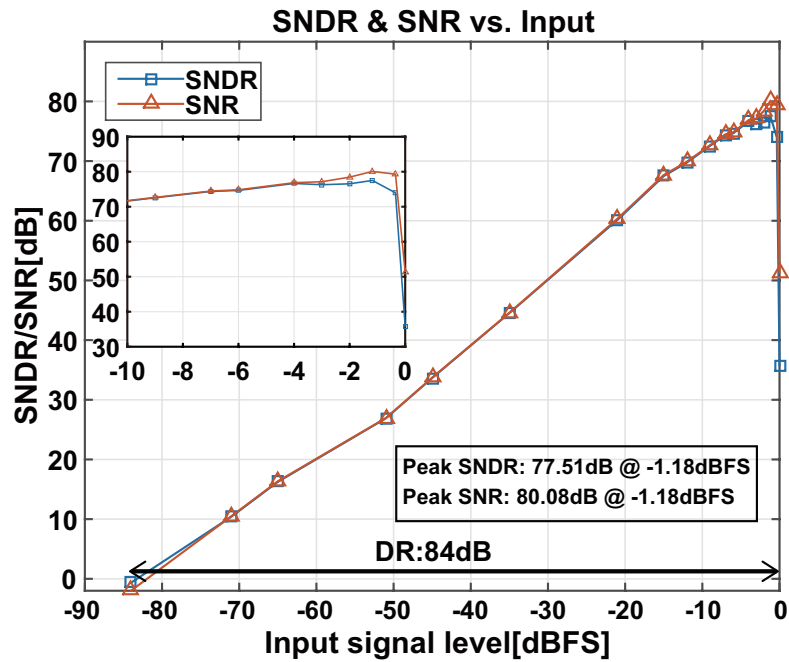
FIGURE 3.23: Measured SNDR and SNR vs. input signal level.
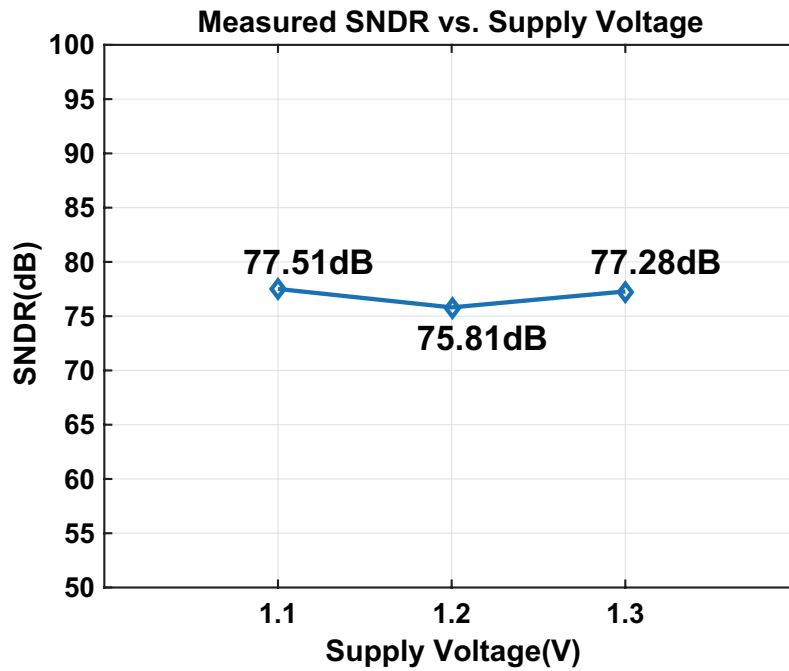
FIGURE 3.24: Measured SNDR vs. supply voltage.

SNDR = 77.51 dB is achieved for 94 kHz bandwidth (OSR = 64). Comparison to simulated spectrum shown in figure 3.13(b), flicker noise is observed in low frequency band, in-band noise floor becomes higher, and the 3rd-order harmonic distortion also appeared. However, the measured results is reasonable with the consideration including the influence of non-ideal factors of amplifier non-linearities and evaluation systems. Figure 3.23 shows the measured SNR and SNDR vs. input signal level. Peak SNDR of 77.51 dB and SNR of 80.08 dB at -1 dBFS are achieved, respectively. The measurement results of the modulator show that linear SNDR response up to the full scale, and the dynamic range of 84dB is achieved. The total power consumption of this work is 0.37 mW. Both the analog and digital circuits supply voltage is 1.1 V. The Schreier and Walden FOMs are 161.5 dB and 0.32 pJ/conversion-step, respectively. Figure 3.24 shows the measured SNDR for the prototype modulator versus supply voltage. Measured SNDR is not degraded significantly even the supply voltage is variate. The performance of the proposed delta sigma modulator is summarized in Table 3.2 in comparison with the previous works. This proposed delta sigma modulator achieves the best Schreier FOM, SNR, and SNDR with the lowest sampling frequency. Measurement results show the reliability of delta sigma modulator with dynamic analog components.

TABLE 3.2: Performance summary and comparison with previous works

Specification	Bilhan[13]	Rajaee[14]	This work
Technology(nm)	90	180	90
Supply voltage(V)	1.2	1.2	1.1
Sampling rate (MS/s)	60	25	12
OSR	15	8	64
Signal BW (kHz)	2×10^3	1.56×10^3	94
SNR (dB)	56	N/A	80.08
SNDR (dB)	N/A	75	77.51
Power (mW)	1.56	2.6(A)	0.37
		3.75(D)	
FOMW (pJ/conv.-step)	0.75	0.44	0.32
FOMS (dB)	147.1	158.9	161.5
Active area (mm2)	N/A	3.79	0.155

3.7   Summary

A novel feed-forward multi-bit delta sigma modulator using dynamic amplifier have been designed and fabricated in 90nm CMOS technology. The passive-adder embedded SAR quantizer is proposed instead of active adder and quantizer. Full differential integrator with ring amplifier is proposed to extend the dynamic range of modulator for higher SNDR. The delta sigma modulator circuit is realized by dynamic amplifier and a dynamic comparator. For conforming the noise characteristic of the dynamic analog components, the noise models of dynamic amplifier (ring amplifier) and dynamic comparator are created, and these noise analysis are carried out. Measurement results show the reliability of proposed modulator.

References

[1]   J. Silva et al. "Wideband lowdistortion delta-sigma ADC topology". In: *Electronics Letters* vol.37 (June 2001), pp. 737–738 (cit. on p. 35).

[2]   R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004 (cit. on pp. 35, 51, 58, 64).

[3]   C. Pan and H. San. "A ΔΣAD Modulator with SAR Quantizer and Ring Amplifier". In: *IEICE Trans. on Fundamentals (Japansese Edition)* vol.J99-A (Aug. 2016), pp. 262–269 (cit. on pp. 36, 43).

[4]   B. Hershberg et al. "Ring amplifiers for switched capacitor circuits". In: *IEEE J. Solid State Circuits* vol.47 (Dec. 2012), pp. 2928–2942 (cit. on p. 36).

[5]   Y. Lim and M. Flynn. "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers". In: *IEEE ISSCC 2014 Dig of Tech* (Feb. 2014), pp. 202–203 (cit. on pp. 36, 40).

[6]   C. Pan and H. San. "Experimental Implementation of ΔΣAD Modulator with Dynamic Analog Components". In: *Analog Integrated Circuits and Signal Processing, Springer* Vol.97, Issue 2 (June 2018), pp. 215–223 (cit. on p. 36).

[7]   Y. Lim and M. Flynn. "A 1mW 71.5dB SNDR 50MS/s 13bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC". In: *IEEE J. Solid State Circuits* vol.50 (Dec. 2015), pp. 2901–2911 (cit. on p. 40).

[8]   M. Elzakker et al. "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge Redistribution ADC". In: *IEEE ISSCC 2008 Dig of Tech* (Feb. 2008), pp. 244–245 (cit. on p. 48).

[9]   I. Chao et al. "A Single Opamp Third-Order Low-Distortion Delta-Sigma Modulator with SAR Quantizer Embedded Passive Adder". In: *IEICE Trans. on Electronics* vol.E97-C, no.6 (June 2014), pp. 526–537 (cit. on p. 49).

[10]   T. Kuo, K. Chen, and H. Yeng. "A wideband CMOS sigma-delta modulator with incremental data weighted averaging". In: *IEEE J. Solid-State Circuits* vol.37 (Jan. 2002), pp. 11–17 (cit. on p. 51).

[11]   Inc Cadence. "A New Methodology for Cynamic Comparator Noise Analysis". In: *EE Journal Chalk Talk Series* (Dec. 2016) (cit. on p. 58).

[12]   A.M. Abo and P.R. Gray. "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter". In: *IEEE J. Solid-State Circuits* vol.34 (May 1999), pp. 599–606 (cit. on pp. 64, 65).

[13]   E. Bilhan and F. Maloberti. "A wideband sigma-delta modulator with cross-coupled two-paths". In: *IEEE Trans. Circuits Syst. I* vol.56 (May 2009), pp. 886–893 (cit. on p. 68).

[14]   O. Rajaee et al. "Low-OSR over-ranging hybrid ADC incorporating noise-shaped two-step quantizer". In: *IEEE J. Solid-State Circuits* vol.46 (Nov. 2011), pp. 2458–2468 (cit. on p. 68).

Chapter 4

Improved Delta Sigma Modulator Using Ring Amplifier

4.1 Preface

In this chapter, an improved 2nd-order feed-forward delta sigma modulator using ring amplifier with passive adder embedded SAR quantizer will be discussed. The improved delta sigma modulator architecture can simplify the operation phase with guaranteed the reset time for ring amplifier and sampling time for asynchronous SAR quantizer. Therefore, the phase requirement on delta sigma modulator is relaxed, the operation speed of the improved delta sigma modulator is enhanced.

4.1.1 Drawback of Proposed DSM using Ring Amplifier

In chapter 3, the implementation of 2nd-order feed-forward delta sigma modulator using ring amplifier with passive adder embedded SAR quantizer is proposed [1]. The measurement results show the feasibility of delta sigma modulator using ring amplifier and SAR quantizer. However, due to the reset operation of the dynamic analog component (eg. ring amplifier) and the sampling operation of asynchronous SAR quantizer are required in the proposed delta sigma modulator. In order to ensure the ring amplifier's reset time and asynchronous SAR quantizer's operating time, the delta sigma modulator require 4 operation phases for performing the AD

conversion of 1 sample. As a result, the delta sigma modulator is complicated and the operation speed of the delta sigma modulator is limited.

Figure 4.1 shows the block diagram of 2nd-order delta sigma modulator using SAR quantizer and ring amplifier in chapter 3 [1]. The switched-capacitor integrator of the delta sigma modulator is realized by the ring amplifier. Due to the input and output of ring amplifier are shorted to recover the bias voltage on the offset capacitor of the ring amplifier at the reset mode, the load capacitance of the integrator must be disconnected from the output of ring amplifier at the reset mode. Oppositely, the load capacitance of the integrator is connected to the output of the ring amplifier at the amplification mode. Therefore, the operation of ring amplifier is different from the conventional amplifier, it needs to operate alternately between the reset mode and the amplification mode for realizing the amplification function. Furthermore, because SAR quantizer is used as an internal quantizer in the delta sigma modulator, unlike the flash ADC, SAR quantizer need to use an extra phase for the sampling operation.
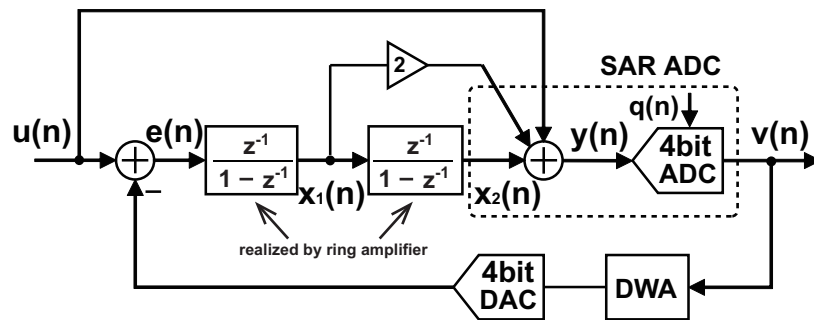
FIGURE 4.1: Block diagram of proposed delta sigma modulator.

4.1.2 Design Considerations of DSM using Ring Amplifier

Due to the constraint of the above two factors, the clock timing design of the delta sigma modulator using ring amplifier and SAR quantizer is much more difficult than the delta sigma modulator using the traditional amplifier and flash ADC. Hence, the following four factors need to be guaranteed when designing the delta sigma modulator using ring amplifier and SAR quantizer, 1) the sampling capacitor of the 2nd integrator and one of the sampling capacitors of the SAR quantizer are connected to

the output of the 1st integrator at the same time; 2) the sampling capacitor of the 1st integrator and one of the sampling capacitors of the SAR quantizer are connected to input signal at the same time; 3) the successive approximation operation of asynchronous SAR quantizer also need to use an extra phase; 4) the DAC embedded in the 1st integrator is driven by the output of the SAR quantizer, therefore, the amplification operation of the 1st integrator need to wait for the feedback signal from the SAR quantizer output.
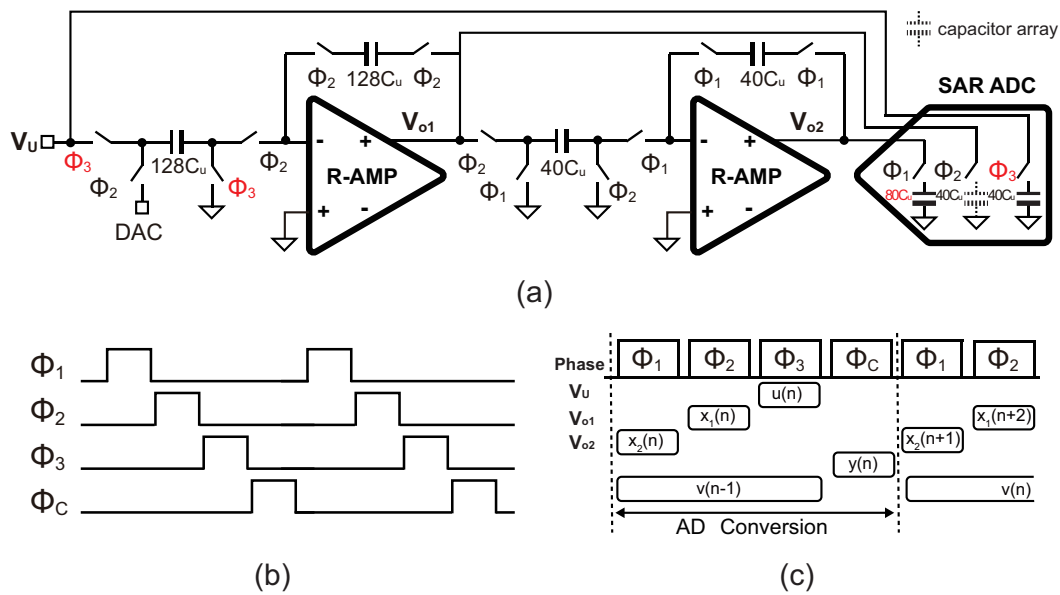
FIGURE 4.2: Simplified circuit implementation of proposed delta sigma modulator. (a) Simplified circuit schematic diagram. (b) Timing clock chart. (c) Operation mode diagram

Considering the above factors, in order to correctly implement the transfer function $V(z) = U(z) + (1 - z^{-1})^2 E(z)$ of the 2nd-order delta sigma modulator, the delta sigma modulator needs to be operated in 4-phases. Figure 4.2(a) shows the simplified circuit schematic diagram of the delta sigma modulator using SAR quantizer and ring amplifier(R-AMP) in the previous work (Chapter 3), its timing clock chart and the operation mode diagram are shown in figure 4.2(b) and figure 4.2(c). The delta sigma modulator is complicated and the speed of operation is limited.

4.2 Architecture

In order to simplify the operation phase of the delta sigma modulator to improve the speed of the delta sigma modulator, the improved delta sigma modulator architecture shown in figure 4.3 is proposed, it allows the delta sigma modulator to work in 3-phases.

4.2.1 Structure of Improved Delta Sigma Modulator
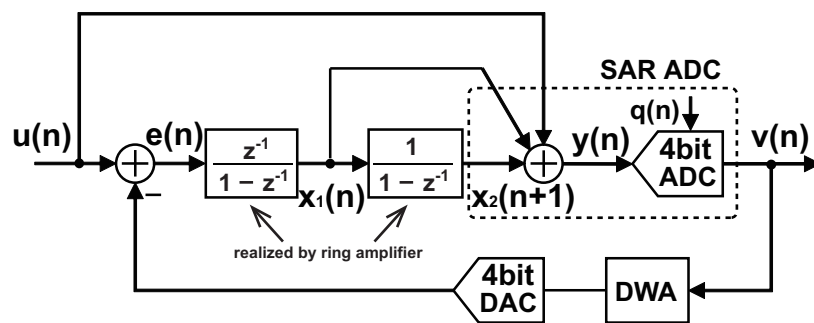
FIGURE 4.3: Block diagram of improved delta sigma modulator.

Figure 4.4(a) shows the simplified circuit schematic diagram of proposed delta sigma modulator using SAR quantizer and ring amplifier (R-AMP) with the improved operation phase, its timing clock chart and the operation mode diagram are shown in figure 4.4(b) and figure 4.4(c). The improved delta sigma modulator only use 3-phases for preforming one AD conversion operation, so that the speed of modulator can be enhanced than that in the previous work.

Although, the operation timing of two kinds of delta sigma modulator (figure 4.1 and figure 4.3) are different, that the architecture of the improved delta sigma modulator (figure 4.3) still realize the 2nd-order noise shaping transfer characteristic can be proved as the following.
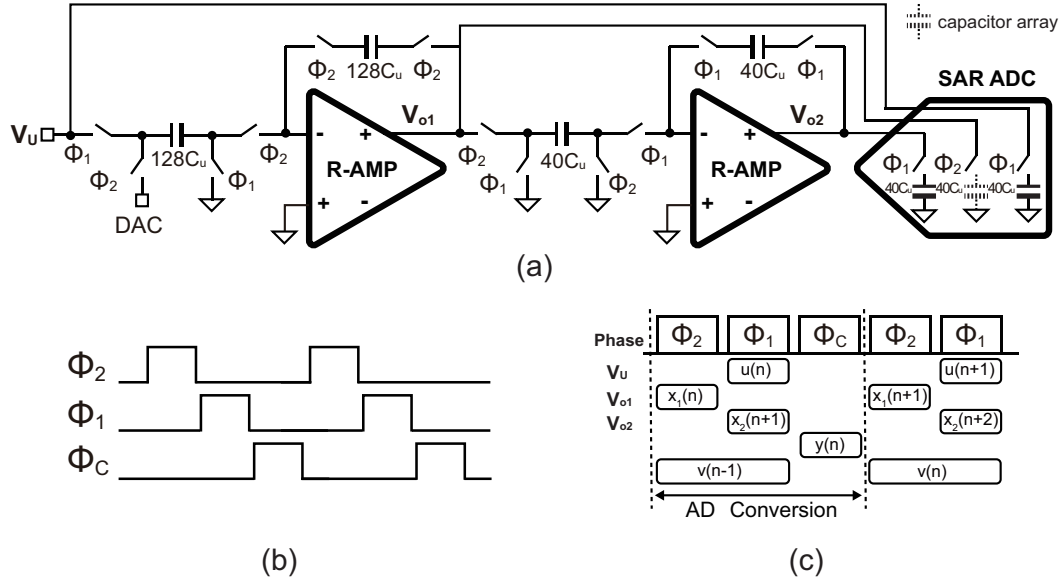
FIGURE 4.4: Simplified circuit implementation of improved delta sigma modulator. (a) Simplified circuit schematic diagram. (b) Timing clock chart. (c) Operation mode diagram.

4.2.2 Transmission Function of Improved Delta Sigma Modulator

In figure 4.1, u(n) is the input, v(n) is the output of the delta sigma modulator. The input signal of the internal quantizer y(n) is given as

$$y(n) = u(n) + 2x_1(n) + x_2(n) \tag{4.1}$$

where $x_1(n)$ is the output signal of the 1st integrator , $x_2(n)$ is the output signal of the 2nd integrator.

Since the output signal of the 2nd integrator obeys the following relationship

$$x_2(n+1) = x_1(n) + x_2(n) \tag{4.2}$$

by combining it with equations (4.1) and (4.2) will lead to

$$y(n) = u(n) + x_1(n) + x_2(n+1) \tag{4.3}$$

Consequently, the architecture of the delta sigma modulator can be changed as shown in figure 4.3(a). The output signal of the delta sigma modulator is obtained as

$$v(n) = u(n) + q(n) + x_1(n) + x_2(n+1) \tag{4.4}$$

The z-domain expression of equation (4.4) can be expressed as

$$V(z) = U(z) + Q(z) + X_1(z) + X_2(z)z \tag{4.5}$$

In figure 4.3, the z-domain expression of the 1st and the 2nd integrator's outputs are given as

$$X_1(z) = [U(z) - V(z)]\frac{z^{-1}}{1 - z^{-1}} \tag{4.6}$$

$$X_2(z)z = \frac{X_1(z)}{1 - z^{-1}} \tag{4.7}$$

Substituting equations (4.6) and (4.7) into equation (4.5), we get

$$V(z) = U(z) + (1 - z^{-1})^2 Q(z) \tag{4.8}$$

The transfer function of the improved delta sigma modulator equation (4.8) indicates the 2nd-order noise sharp characteristic which is the same as that in figure 4.1. As a result, the equivalence of the two kinds of delta sigma modulator architecture (figure 4.1 and figure 4.3) are confirmed. However, only 3 operation phases are required for one AD conversion in the improved delta sigma modulator, Therefore, the operation speed of delta sigma modulator can be enhanced.

4.3   Implementation

Figure 4.5(a) illustrates the schematic diagram of the proposed delta sigma modulator using SAR quantizer and ring amplifier(R-AMP) with the simplified operation phase in this work, its timing diagram is shown in figure 4.5(b). In the feed-forward delta sigma modulator, the input signal to the loop filter contains only the shaped quantization noise, so that the modulator can reduce the influence of amplifier's
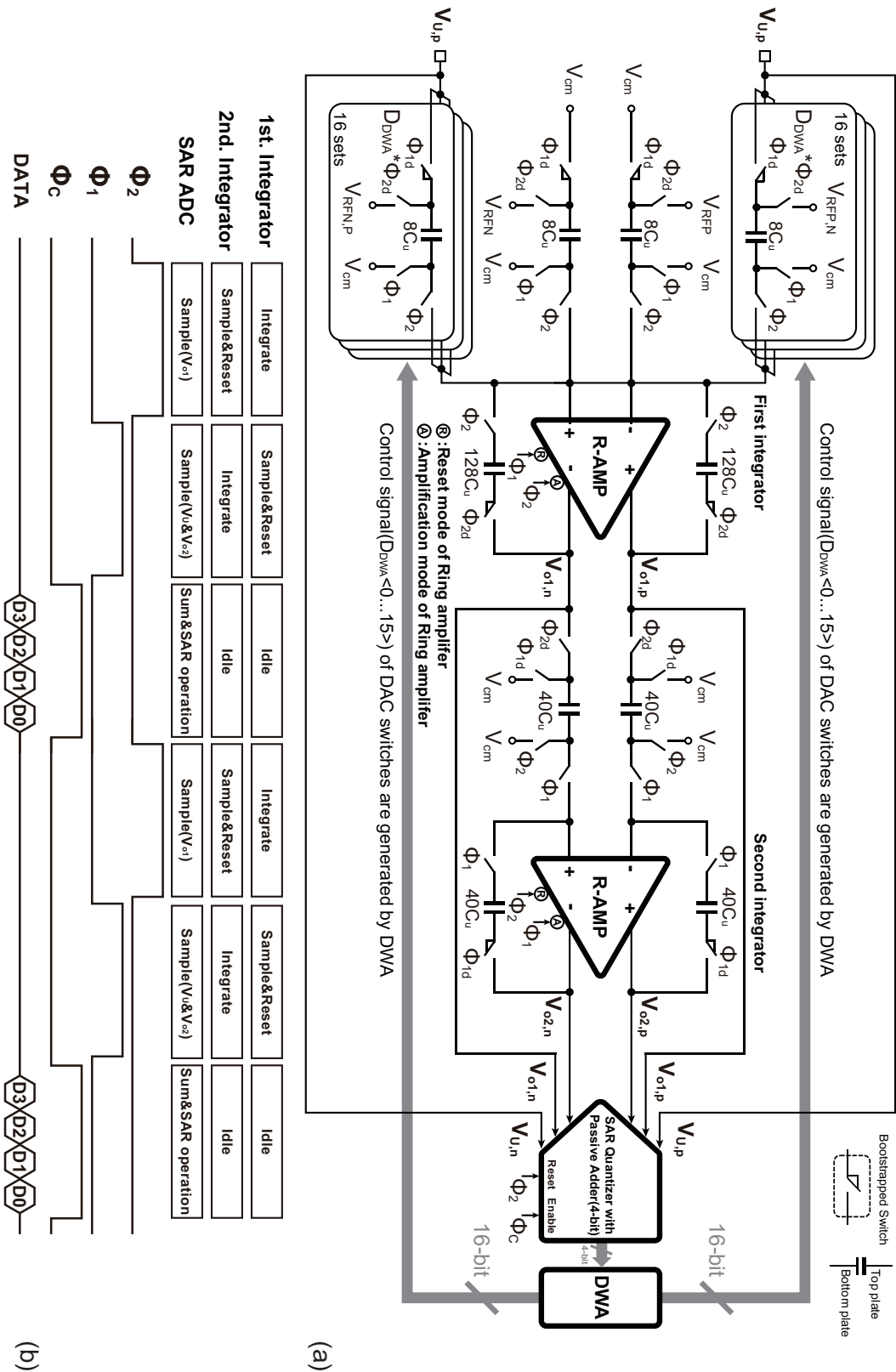
FIGURE 4.5: Circuit implementation of proposed 2nd-order feed-forward delta sigma modulator using ring amplifier (R-AMP) with simplified operation phase. (a) Schematic diagram. (b) Timing chart & operation mode.

non-linearity for higher SNDR [2]. Moreover, the ring amplifier can realize higher gain than traditional amplifier at low supply voltage, and the static current of the ring amplifier is very small, so that the power consumption of the modulator can be maintained low. An asynchronous SAR quantizer is used as a 4-bit quantizer. It not only improve the stability of the modulator, but also relax the requirement on the slew-rate of amplifier. The 4-bit SAR quantizer have 3 inputs terminal (V_U, V_{o1} and V_{o2}), since the SAR quantizer converts the summation of them to digital code, the analog adder is realized by capacitor array without amplifier. Although the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the DWA logic circuit is applied to the delta sigma modulator to reduce the influence of DAC nonlinearity errors [3].

4.3.1 Pseudo Differential Ring Amplifier

Figure 4.6(a) shows the pseudo differential ring amplifier with switched-capacitor common-mode-feedback (CMFB) structure. C_Cs are added to the input nodes of amplifier to realize the amplifier input offset cancellation for the integrator [4]. Figure 4.6(b) shows the schematic of the ring amplifier's core in the proposed delta sigma modulator with self bias circuit. It is constructed with cascaded 3-stage inverters, so that it is similar to a ring oscillator in the amplifier. The input of the MOSFET M_{P1} and M_{N1} is biased at V_{cm} when the ring amplifier forms a feedback loop. Therefore, the M_{P1} and M_{N1} operate in the wake inversion region current during the steady state of the amplifier with a very low static. The inverter which consist of M_{P1} and M_{N1} behaves as a class-AB amplifier providing high DC-gain and good linearity. Resistor R_{OS} is inserted to the output of the 2nd stage inverter. The R_{OS} not only compress the drain-source voltage of the M_{P2} and M_{N2} to the boundary between the weak and strong inversion regions for obtaining both high DC-gain and wide gain-bandwidth product[5], but also to generate the different offset voltages to the gate of the M_{P3} and M_{N3}. During the steady state, the gate-source voltage of the both M_{P3} and M_{N3} are set at less than their threshold voltage, thus the M_{P3} and M_{N3} are cut off, there is not static current flow though the amplifier. During transition state, one of the two transistors M_{P3}, M_{N3} is operating in the strong inversion region, while

Φ_R :Reset mode of R-AMP
Φ_A :Amplification mode of R-AMP
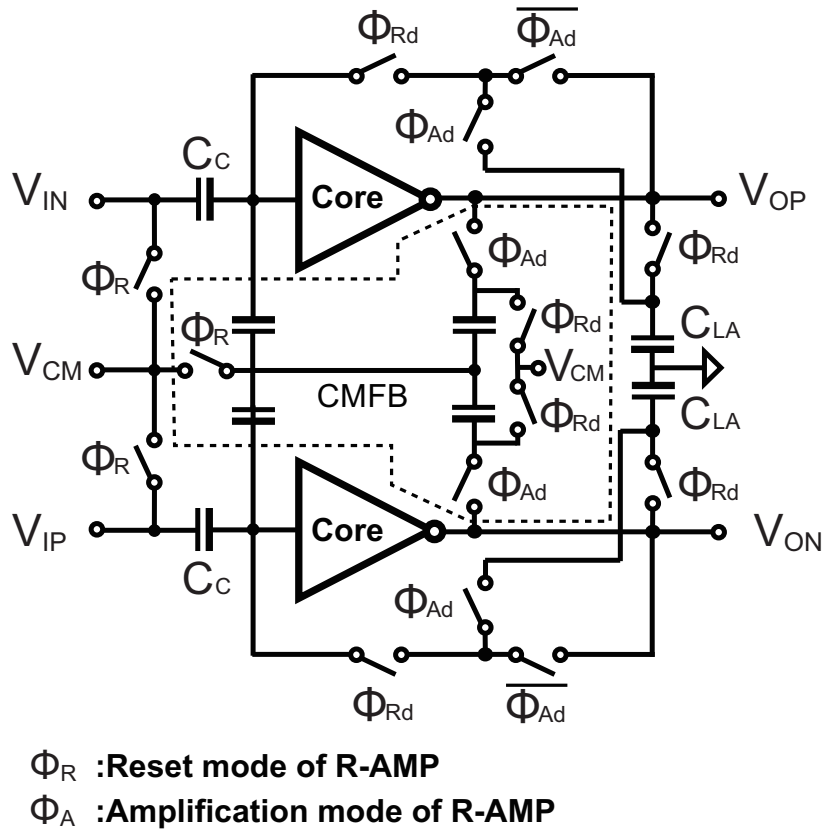
(a)
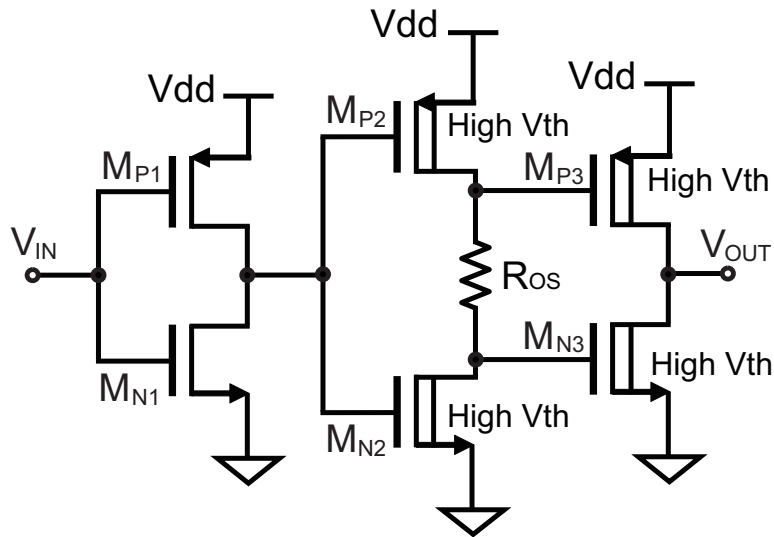
(b)

FIGURE 4.6: Schematic of pseudo differential ring amplifier (R-AMP).
(a) Ring amplifier (R-AMP). (b) Core of R-AMP.

the other one is set to off state completely, so that higher slew rate can be realized. The push-pull inverter which consist of M_{P3} and M_{N3} behaves as a class-C amplifier and the rail-to-rail output is allowed for the ring amplifier. The setting time and power consumption of the ring amplifier can be reduced dramatically. Moreover, high threshold voltage $M_{P2,3}$ and $M_{N2,3}$ are used in the 2nd and 3rd-stage to extend the stable offset voltage range for the amplifier.
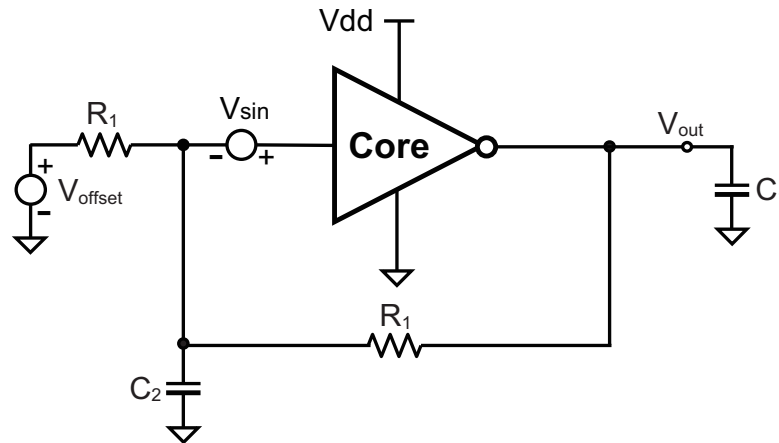
(a)
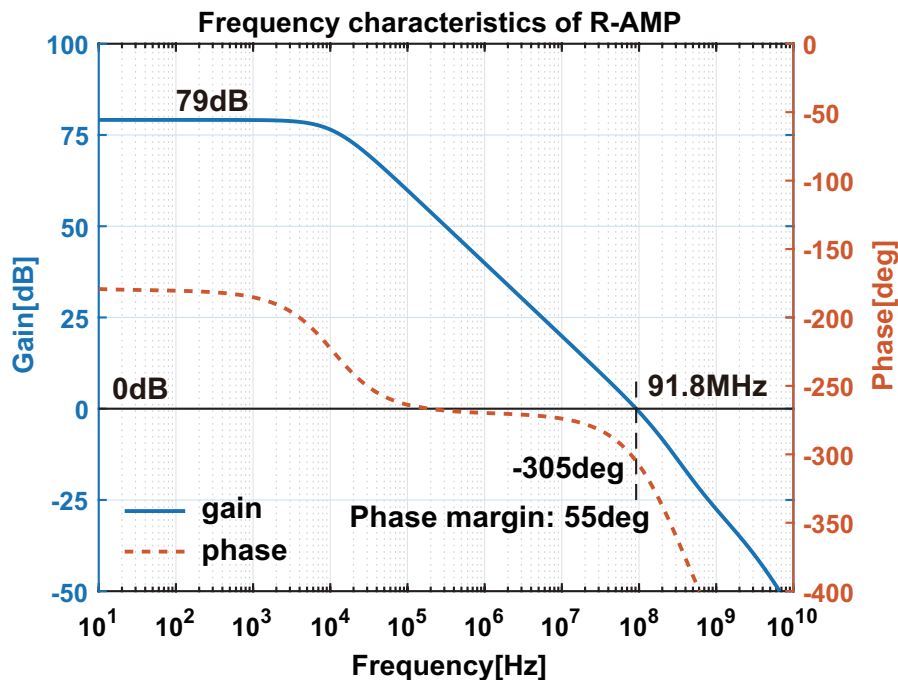
(b)

FIGURE 4.7: AC analysis circuit of ring amplifier. (a) Simulation circuit. (b) Frequency characteristics of ring amplifier.

In order to confirm the performance of ring amplifier, SPICE simulation of AC analysis is introduced using the circuit shown in figure 4.7(a). The SPICE simulation result is shown in figure 4.7(b). The DC gain of ring amplifier reached to 79 dB with 55° phase margin and 91.8 MHz unity-gain bandwidth. Simulation parameters of the ring amplifier are shown in table 4.1.

TABLE 4.1: AC analysis simulation parameters of R-AMP

Technology	TSMC 90nm CMOS
Supply voltage	1.2V
V_{offset}	0.6V
R_1	10GΩ
C_1	640fF
C_2	1uF
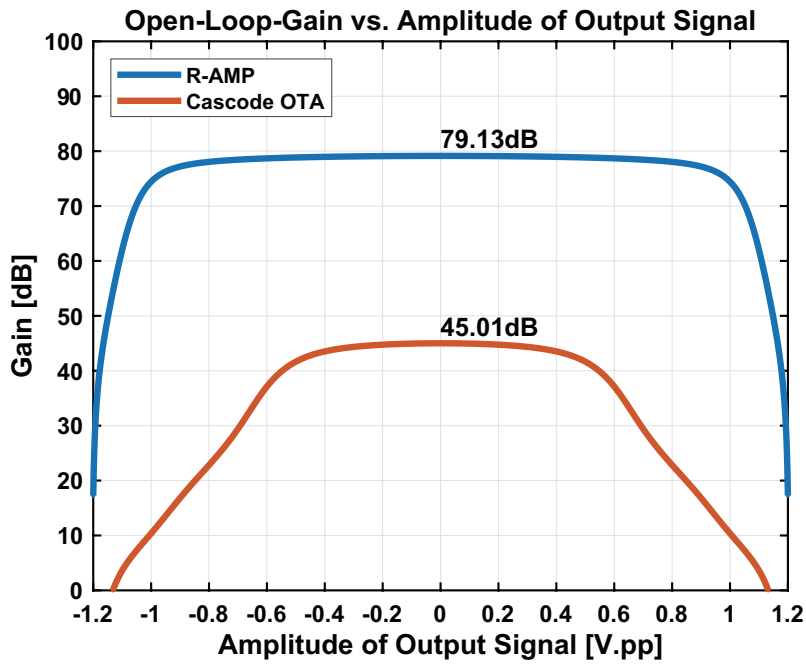
FIGURE 4.8: Open-Loop-Gain of Ring Amplifier versus Amplitude of Output Signal.

An ideally flat Open-Loop-Gain vs. output swing characteristic will result in a simple first-order gain error when the amplifier is placed in feedback, enabling high linearity to be achieved even with a low-gain amplifier. The ring amplifier not only has the flat Open-Loop-Gain, but also the gain is larger than that of OTA as shown

in the figure 4.8.

4.3.2   Improved SAR quantizer with Passive Adder

Figure 4.9 shows the schematic diagram of the proposed charge redistribution asynchronous SAR quantizer with passive adder. It consist of capacitor array, a dynamic comparator and asynchronous SAR logic circuits. Capacitors connected to V_U, V_{o2}, V_{o1} are used for a passive-adder, and the capacitors surround by the dash line are also used as the capacitor DAC for SAR DAC.

Figure 4.10 shows two operation modes for equivalent circuit of passive-adder. In the sampling mode, the bottom plate of sampling capacitors are connected to input signals of V_U, V_{o1} and V_{o2}, the top plate of sampling capacitors are connected to V_{cm} as shown in figure 4.10(a), respectively. The capacitor ratio for 3 input signals is 1:1:1, then the total charge stored on the capacitors Q_S can be expressed as:

$$Q_S = 40C_u \times V_U + 40C_u \times V_{o2} + 40C_u \times V_{o1} \tag{4.9}$$

In the summation mode shown in figure 4.10(b), the bottom plate of sampling capacitors are connected to V_{cm}. The total capacitance between the input node of the comparator and V_{cm} is $120C_u$. The total charge Q_C of this summation mode on capacitors is

$$Q_C = 120C_u \times V_{IN(P,N)} \tag{4.10}$$

According to charge conservation law, we have

$$Q_C = Q_S. \tag{4.11}$$

Then, we get that

$$V_{IN(P,N)} = \frac{Q_S}{120C_u} = \frac{V_U + V_{o2} + V_{o1}}{3} \tag{4.12}$$

Equation (4.12) means that the summation of 3 input signals can be realized by the proposed sampling technique for capacitor array. After the analog input summation
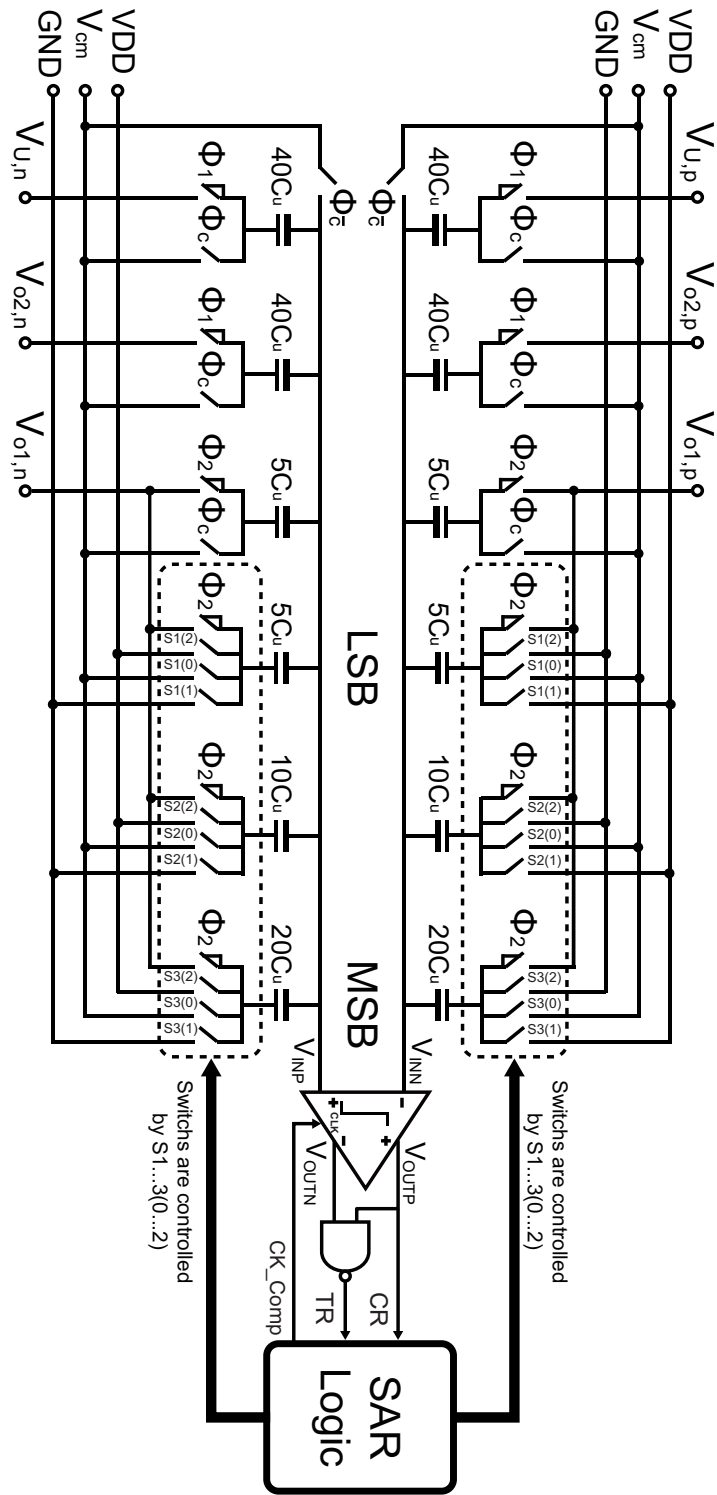
FIGURE 4.9: Circuit implementation of the improved charge redistribution asynchronous SAR quantizer with passive adder.

is finished, the AD conversion is carried out from MSB to LSB in the successive approximation manner.
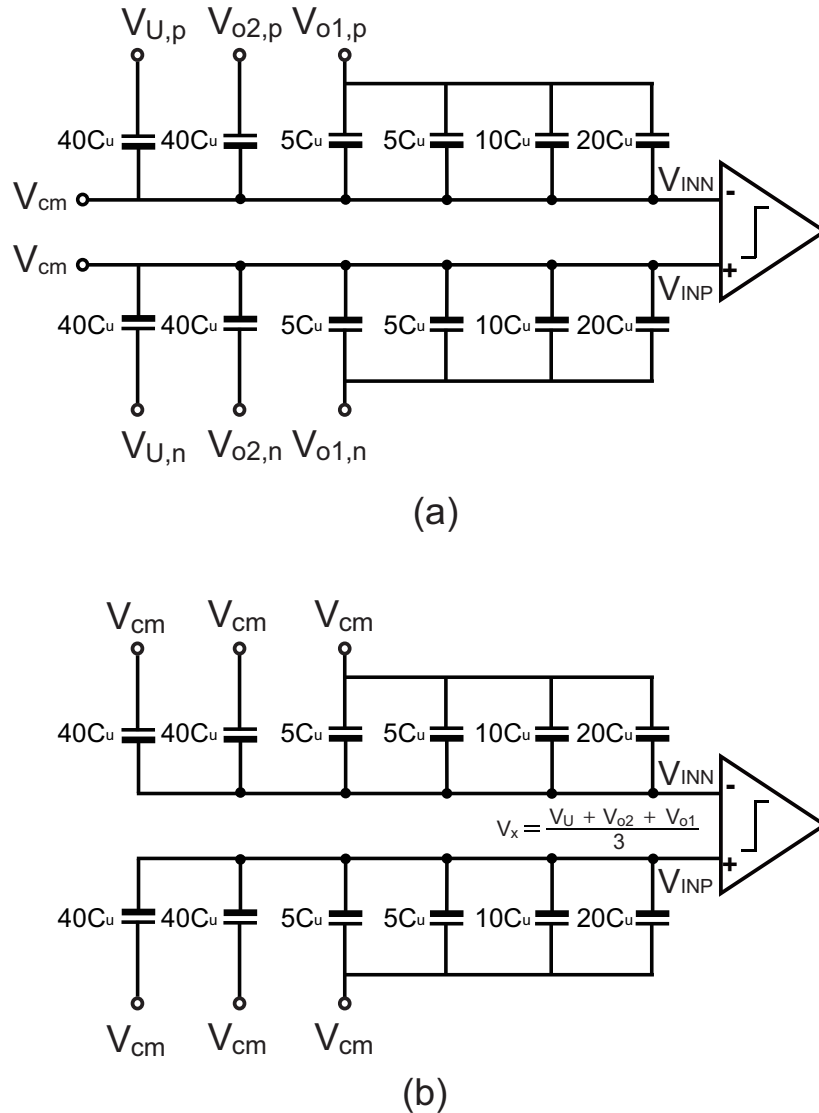
FIGURE 4.10: Equivalent circuit of the improved charge redistribution SAR quantizer in the different operation. (a) Sampling mode. (b) Summation and successive approximation mode.

Asynchronous SAR logic circuit is shown in figure 4.11(a), it generates the control signal to drive the capacitor switches of DAC in the SAR quantizer. Φ_C is enable signal and Φ_2 is reset signal for the asynchronous SAR logic circuit. S1(1) and S1(2), S2(1) and S2(2), S3(1) and S3(2) are control signals for the DAC capacitor switches, which are connected to reference voltages, VDD and GND. S1(0), S2(0) and S3(0) are control signals for the DAC capacitor switches, which are connected to common voltage, V_{cm}.
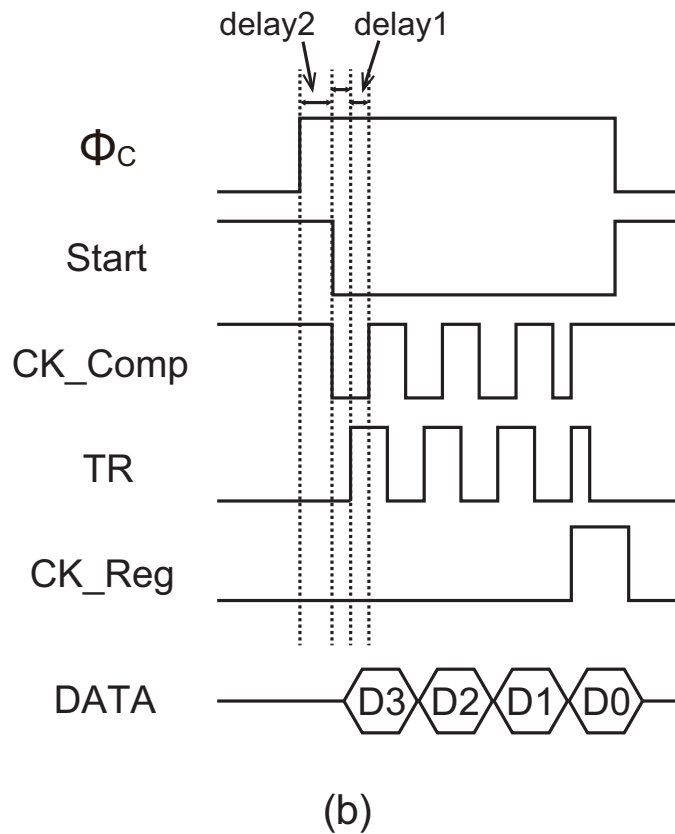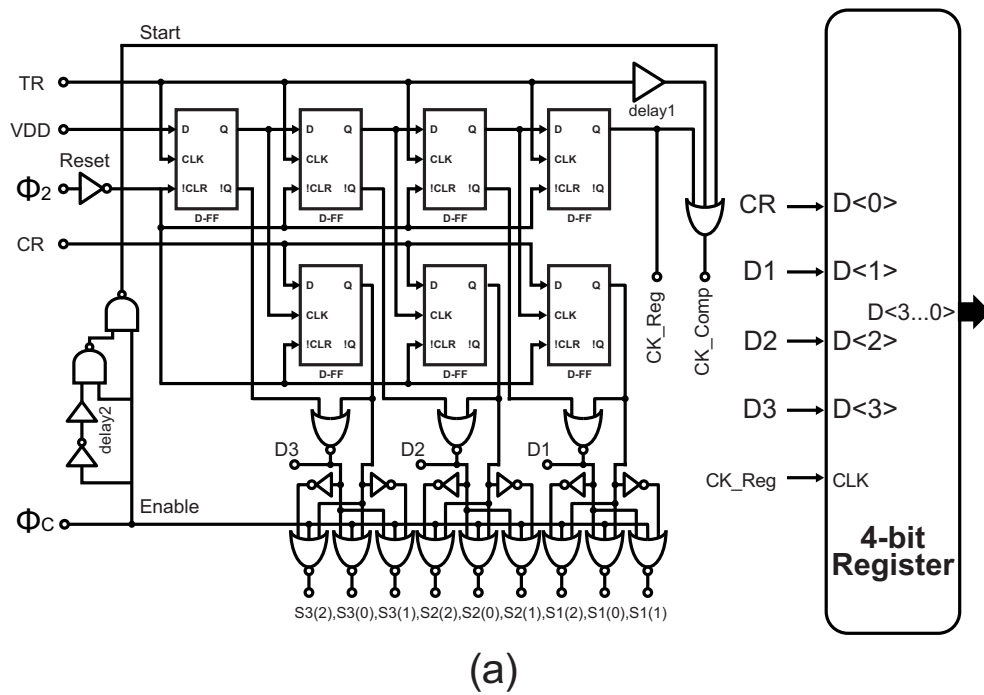
FIGURE 4.11: Schematic diagram of asynchronous SAR logic. (a) Circuit implementation of asynchronous SAR logic. (b) Timing diagram of SAR logic circuit.
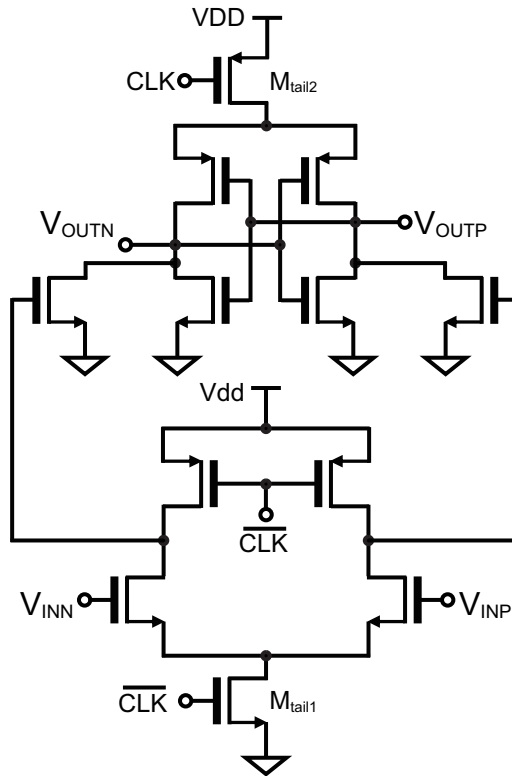
FIGURE 4.12: Schematic diagram of the double-tail dynamic comparator used in SAR quantizer.

Figure 4.12 shows the schematic diagram of the double-tail dynamic comparator used in SAR quantizer [6]. This topology has less stacking current and therefore it can operate at lower supply voltages. The differential output nodes of the dynamic comparator are followed by a NAND gate as shown in figure 4.9. The inputs of NAND sense the toggle of differential comparator's output to realize the asynchronous operation of the SAR quantizer. While the clock signal "CLK" of the comparator is High (M_{tail1} and M_{tail2} are off), the output nodes of comparator V_{OUTP} and V_{OUTN} are reset to VDD. While the clock signal "CLK" of the comparator changes from High to Low (M_{tail1} and M_{tail2} are turned on), the voltage comparison of two input nodes of V_{INP} and V_{INN} is done, the comparison result appears at nodes of V_{OUTP} and V_{OUTN}. The comparison result (signal "CR") is saved in the D flip-flop (DFF) of the asynchronous SAR logic circuit provisionally, then the comparator changes to the latch mode. Because these two output nodes are bounded to the inputs of NAND gate, while the voltage comparison is finished, NAND gate outputs a trigger signal "TR" to drive the operation of the asynchronous SAR logic circuit. The

buffer "delay1" inserted between the clock signal "TR" and one of the inputs of the 3-input OR gate that can prolong the usable DAC setting time, when the SAR quantizer operates at the successive approximation mode. When the comparator makes the decision of the last bit (D0), the signal "CK_Reg" goes high to trigger the 4-bit register, the comparison results D3, D2, D1 (saved in the DFF previously) and the LSB result D0 (the last signal "CR") are transferred to 4-bit register as shown in figure 4.11(a). The buffer "delay2" is used for delaying the signal "Start" (enable signal of asynchronous SAR logic) that can prolong the setting time of passive adder, to guarantee the the addition result is complete settled (the charge redistribution on capacitor array to be finished) before AD conversion. Figure 4.11(b) shows the timing diagram of asynchronous SAR logic circuit. In a conventional synchronous SAR quantizer, the speed of the comparator clock signal is limited by the worst-case cycle time. However, in the asynchronous SAR quantizer, the signal "TR" is generated by NAND gate, so that the conversion steps are executed consecutively. Therefore, the speed of the asynchronous SAR logic is faster than that of the conventional synchronization SAR logic.

As mentioned above, the proposed SAR quantizer realizes not only a 4-bit quantizer but also an analog adder with the capacitor array using a comparator, so that the power consumption of modulator can be reduce from the conventional feed-forward modulator using the active adder realized by amplifier. Furthermore, since SAR quantizer is implemented by dynamic comparators and asynchronous successive approximation logic circuits [7], it can work at high speed.

4.3.3 Multi-bit DAC and DWA Logic Circuit

A 4-bit capacitor DAC is used for the 1st integrator as shown in figure 4.5, the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the DWA logic circuit [8] is applied to the delta sigma modulator to reduce the influence of DAC non-linearity errors. To illustrate the effect of the DWA logic circuit, SPICE simulation comparison with the proposed modulator is performed in 2 cases: (1) 4-bit DAC with 1% unit-capacitance mismatches while DWA at OFF mode; (2) 4-bit DAC with 1% unit-capacitance mismatches while DWA
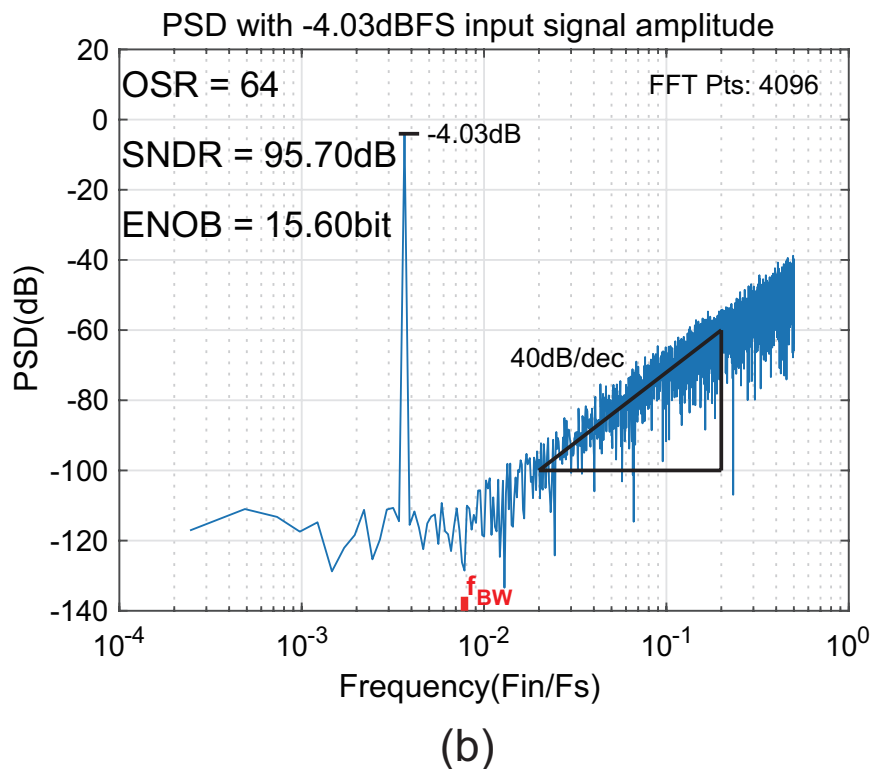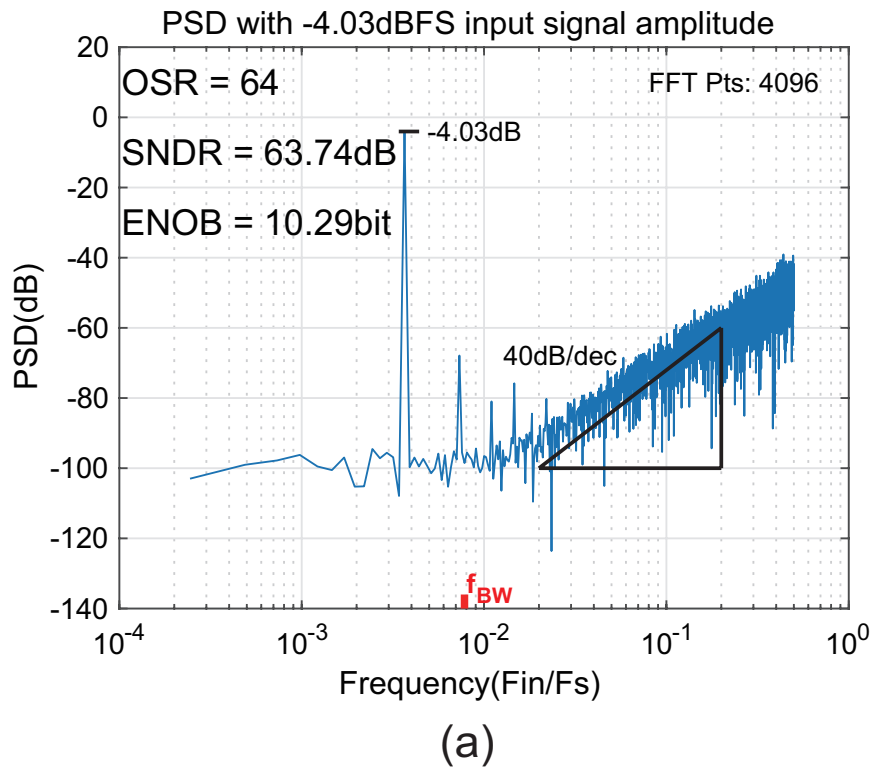
FIGURE 4.13: SPICE simulated results comparison of delta sigma modulator power spectrum at the ON/OFF mode of DWA. (a) DAC with 1% unit capacitance mismatches while DWA OFF Mode. (b) DAC with 1% unit capacitance mismatches while DWA ON Mode.

at ON mode. The output spectrum for the above 2 cases are shown in figure 4.13(a) and (b), respectively. When the unit-capacitance of DAC is variated without DWA, the non-linearities of DAC raise the in-band noise floor, and cause the harmonic distortion as shown in figure 4.13(a). On the other hand, while DWA technique is applied, not only the in-band noise but also the harmonic distortion in the signal band are noise-shaped as shown in figure 4.13(b).

4.4 Simulation

TABLE 4.2: Simulation parameters of delta sigma modulator

Technology	TSMC 90nm CMOS
Supply voltage	1.2V
Input frequency	219.7kHz
Input amplitude	2Vpp
Sampling rate	60MS/s
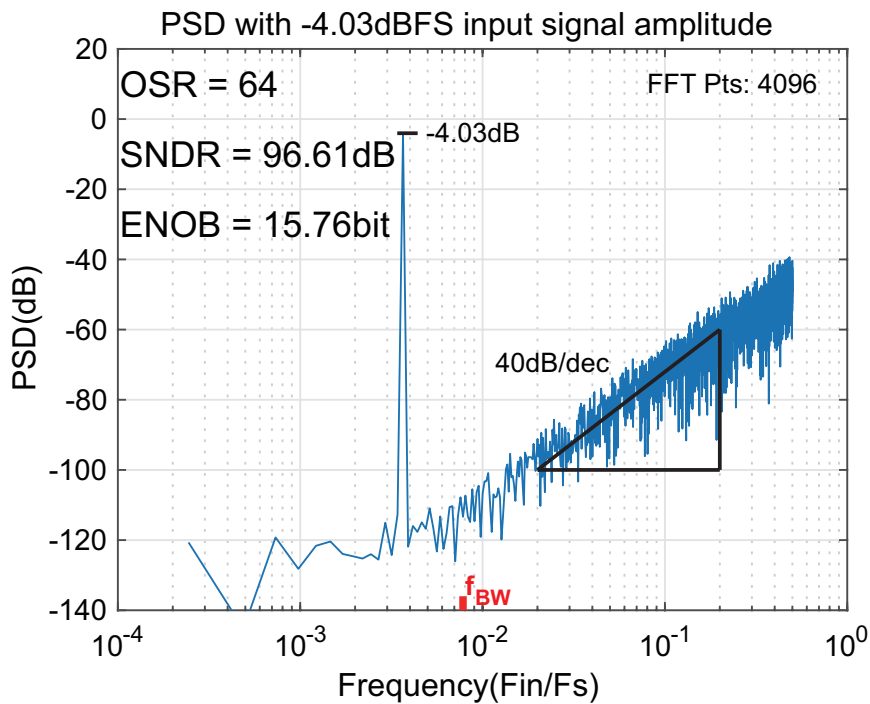
FIGURE 4.14: Simulated output power spectrum of improved 2nd-order feed-forward delta sigma modulator using dynamic analog component.

The propose delta sigma modulator shown in figure 4.5 is designed in TSMC 90 nm CMOS technology. The switched-capacitor integrators are realized by ring amplifier. The quantizer is a 4-bit SAR quantizer with the embedded passive adder. 4-bit DAC on the feedback path is constructed by capacitor array. The DWA logic circuit is designed to reduce the influence of the non-linearities which occurred by the capacitors mismatch of the multi-bit DAC[3]. SPICE simulations have been done to confirm the functionality of the modulator and to verify the effectiveness of the proposed architecture. The simulation parameters are shown in Tab. 4.2. Figure 4.14 shows the simulated spectrum result of the proposed delta sigma modulator without DAC unit-capacitance mismatches. Figure 4.13(b) shows the simulated spectrum result of the proposed modulator with 1% DAC unit-capacitance mismatches. The peak SNDR of 95.70 dB is reached while OSR = 64 for a sinusoid input at 219.7 kHz with -4.03 dBFS input amplitude (The thermal noise of the modulator is not included in the SPICE simulation). The power consumption of analog part in the proposed modulator is 1.67 mW at 1.2 V supply.

4.5   Measurement

4.5.1   Layout and Microphotogragh

The proposed delta sigma modulator was fabricated in TSMC 90 nm 1P9M CMOS technology. Figure 4.15 shows the chip microphotograph and layout of the delta sigma modulator. The active area of the delta sigma modulator is 0.14 mm^2. Bootstrapped switch is used at the inputs of the 1st integration and the input of the SAR quantizer to reduce the nonlinear effect of ON-resistance [9]. All capacitors were laid out using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized by using the MIM capacitors for high density capacitance in a small chip area. Careful layout design has been done to keep the analog part of the delta sigma modulator is symmetrically arranged. The attention also paid to keeping the sensitive analog signals away from the noisy digital signal paths.

Layout

Chip micrograph

530µm

268µm

TSMC 90nm CMOS Technology

Active area : 0.14 mm²
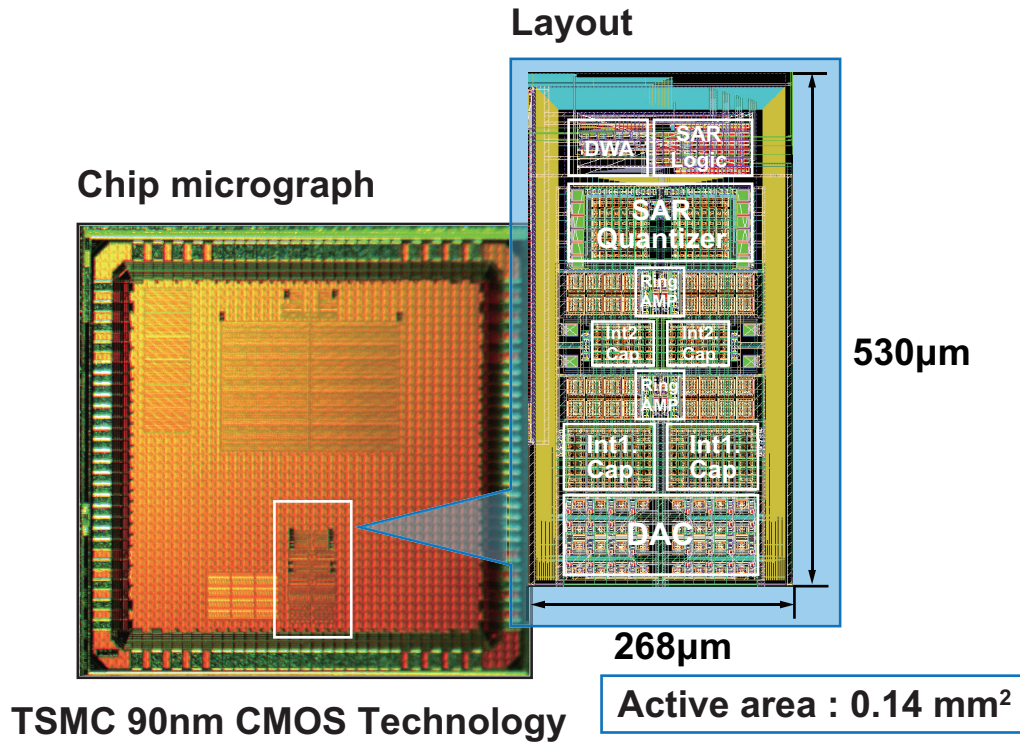
FIGURE 4.15: Chip microphotograph and layout of the prototype modulator.

4.5.2 Measurement Results

Figure 4.16 shows the measured output power spectrum of the prototype modulator for a 26.92 kHz sinusoid differential -4 dBFS input being sampled at 14 MS/s. The peak SNDR = 77.93 dB is achieved for 109 kHz bandwidth (OSR = 64). The measured SFDR is 80.60 dB. Due to the influence of the bootstrapped switch's non-linearity, when a full dynamic range signal is input, the 3rd-order harmonics distortion imposes some performance issue that is verified by the SPICE simulation. Figure 4.17 shows the measured SNR and SNDR vs. input signal level. Peak SNDR of 77.93 dB and SNR of 84.16 dB at -1.24 dBFS and -4.37 dBFS are achieved, respectively. The measurement results of the modulator show that linear SNDR responses up to the full scale, and the dynamic range of 85 dB is achieved. The total power consumption of this work is 720 μW. Both analog and digital circuits supply voltage are 1.2 V. The Schreier FOM$_{SNDR}$ is 159.7 dB. The performance of the proposed delta sigma modulator is summarized in Table 4.3 in comparison with the previous works.
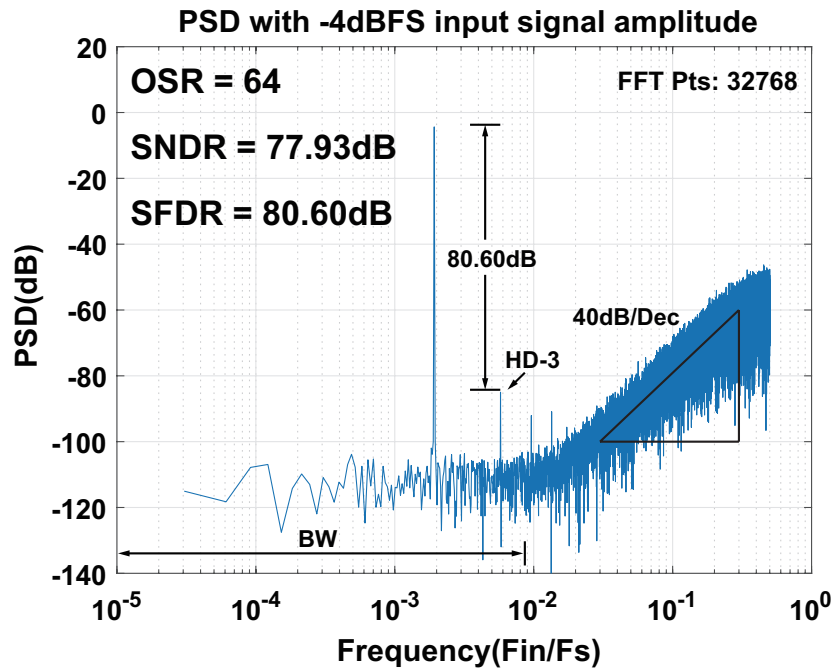
FIGURE 4.16: Measured output spectrum for f_{in} ≈26.92kHz and -4dBFS input signal amplitude.
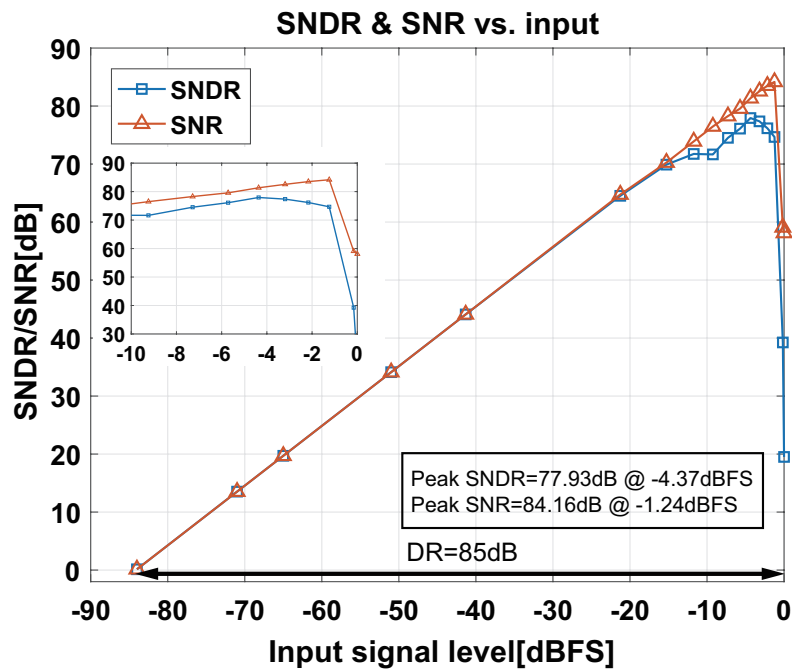
FIGURE 4.17: Measured SNDR and SNR vs. input signal level.

TABLE 4.3: Performance summary and comparison with previous works

Specification	[10]	[11]	[12]	[13]	This work	
Technology (nm)	180	180	180	90	90	
Supply voltage (V)	5	1.8	0.7	1.1	1.1	1.2
Sampling rate (MS/s)	2.56	6.1	5	12	14	
OSR	64	152.5	100	64	64	
Signal BW (kHz)	20	20	25	94	109	
SNDR (dB)	99.3	97.7	95	77.51	77.82	77.93
SNR (dB)	99.5	98.6	100	80.08	84.05	84.16
DR (dB)	101.3	100.5	100	84	85	
Power (mW)	1.1	0.3	0.87	0.37	0.42	0.72
FOMW(pJ/conv.-step)	0.36	0.12	0.38	0.32	0.30	0.51
FOMS$_{SNDR}$ (dB)	171.9	175.9	169.5	161.5	162.0	159.7
FOMS$_{DR}$ (dB)	173.9	178.7	174.6	168.0	169.2	166.8
Active area (mm2)	0.38	0.31	2.16	0.16	0.14	

$\text{FOMW} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$
$\text{FOMS}_{\text{SNDR}} = \text{SNDR} + 10 \times \log_{10}(\text{BW}/\text{Power})$
$\text{FOMS}_{\text{DR}} = \text{DR} + 10 \times \log_{10}(\text{BW}/\text{Power})$

4.6 Summary

A 2nd-order delta sigma modulator with simplified operation mode using ring amplifier and asynchronous SAR quantizer has been designed and fabricated in 90 nm CMOS technology. Benefit from the reduction of the number of the delta sigma modulator operation mode, the speed of delta sigma modulator can be improved. Moreover, the pseudo-differential amplifier based ring amplifier is used for extending the dynamic range of the modulator for higher SNDR, and the SAR quantizer with the passive-adder is used to instead of quantizer and active adder. The delta sigma modulator circuit is realized by dynamic analog component, therefore the power consumption can be kept at low level. Measurement results show the feasibility of the proposed delta sigma modulator.

References

[1] C. Pan and H. San. "Experimental Implementation of ΔΣAD Modulator with Dynamic Analog Components". In: *Analog Integrated Circuits and Signal Processing, Springer* Vol.97, Issue 2 (June 2018), pp. 215–223 (cit. on pp. 71, 72).

[2]   J. Silva et al. "Wideband lowdistortion delta-sigma ADC topology". In: *Electronics Letters* vol.37 (June 2001), pp. 737–738 (cit. on p. 78).

[3]   R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004 (cit. on pp. 78, 90).

[4]   B. Hershberg et al. "Ring amplifiers for switched capacitor circuits". In: *IEEE J. Solid State Circuits* vol.47 (Dec. 2012), pp. 2928–2942 (cit. on p. 78).

[5]   Y. Chae and G. Han. "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator". In: *IEEE J. Solid State Circuits* vol.44 (Feb. 2009), pp. 458–472 (cit. on p. 78).

[6]   D. Shinkel et al. "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time". In: *IEEE ISSCC 2007 Dig of Tech* (Feb. 2007), pp. 314–315 (cit. on p. 86).

[7]   I. Chao et al. "A Single Opamp Third-Order Low-Distortion Delta-Sigma Modulator with SAR Quantizer Embedded Passive Adder". In: *IEICE Trans. on Electronics* vol.E97-C, no.6 (June 2014), pp. 526–537 (cit. on p. 87).

[8]   T. Kuo, K. Chen, and H. Yeng. "A wideband CMOS sigma-delta modulator with incremental data weighted averaging". In: *IEEE J. Solid-State Circuits* vol.37 (Jan. 2002), pp. 11–17 (cit. on p. 87).

[9]   A.M. Abo and P.R. Gray. "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter". In: *IEEE J. Solid-State Circuits* vol.34 (May 1999), pp. 599–606 (cit. on p. 90).

[10] T. Wang et al. "A 101 dB DR 1.1 mW audio delta-sigma modulator with direct-charge-transfer adder and noise shaping enhancement". In: *IEEE ASSCC* (Nov. 2012), pp. 249–252 (cit. on p. 93).

[11] K. Lee, M.R. Miller, and G.C. Temes. "An 8.1 mW, 82 dB DeltaSigma ADC With 1.9 MHz BW and -98 dB THD". In: *IEEE J. Solid State Circuits* vol.44 (Aug. 2009), pp. 2202–2211 (cit. on p. 93).

[12] Y. Park et al. "A 1.1 V 82.3dB audio $\Delta\Sigma$ ADC using asynchronous SAR type quantizer". In: *IEEE ICECS 2012* (Dec. 2012), pp. 637–640 (cit. on p. 93).

[13] C. Pan, H. San, and T. Shibata. "A 2nd-order Delta Sigma AD Modulator using Dynamic Amplifier and Dynamic SAR Quantizer". In: *IEEE ISPACS 2016* (Oct. 2016), pp. 528–532 (cit. on p. 93).

Chapter 5

3rd-Order Noise Coupled Delta Sigma Modulator

5.1 Preface

This chapter discusses a 3rd-order delta sigma modulator using ring amplifier and noise shaping SAR quantizer. The proposed noise shaping SAR quantizer can realize an addition 1st-order noise shaping to enhance the performance of delta sigma modulator.

5.1.1 Error Feedback Technique

Error feedback technique (noise coupling) also has been proposed to aggressive the noise shaping characteristic of the delta sigma modulator [1]. Because SAR ADC have the worthy features that can hold the quantization noise when the successive approximation is finished, the noise coupling technique realized by SAR quantizer is proposed in recently published papers [2, 3]. The previously reported works [1] and [2] require the residue sampling and the active buffer circuit, that accompany the high power consumption. Although the digital domain noise coupling techniques can eliminate the drawbacks of analog domain noise coupling techniques, for realizing the re-quantization of quantization noise, a redundant 8-bit SAR ADC is used as the 4-bit internal quantizer [3]. It dissipates quantization ability of the internal quantizer of the delta sigma modulator (eg. the SQNR of 2nd-order delta sigma

modulator with 8-bit internal quantizer is similar to the SQNR of 4th delta sigma modulator with 4-bit internal quantizer).

5.1.2   Comparison of Noise Coupling Implement Method

In this work, an approach is proposed for realizing the quantization noise coupling, without the residue sampling circuit, the active buffer circuit and the redundant SAR quantizer. The proposed noise coupling technique is realized in the analog domain, but it avoids the drawbacks of previous analog domain noise coupling techniques. The proposed 3rd-order noise coupling structure delta sigma modulator with ring amplifier using the proposed passive adder embedded quantization noise shaping (QNS) SAR quantizer is discussed in this chapter. The proposed passive adder embedded quantization noise shaping QNS SAR quantizer can feedback shaped quantization noise and realize an additional 1st-order noise shaping by noise coupling technique. Moreover, in order to achieve the maximum power-efficiency of the amplifier in ADC, the use of the dynamic amplifier (eg. logic inverter or ring amplifier) instead of the operational transconductance amplifier (OTA) has been proposed and thus results in dynamic-analog-components-based ADC [4, 5].

As a result, the 3rd-order noise coupled delta sigma modulator is realized by two integrators with ring amplifier and the proposed QNS SAR quantizer. The SPICE simulation results demonstrate the feasibility of the proposed delta sigma modulator in 90 nm CMOS technology. Simulated SNDR of 81.05 dB is achieved while a sinusoid -4.32 dBFS input is sampled at 100 MS/s and the bandwidth is BW = 3.125 MHz. The total power consumption in the modulator is 4.58 mW while the supply voltage is 1.2 V.

5.2   Architecture

Figure 5.1 shows the block diagram of the proposed 3rd-order delta sigma modulator. It consists of two integrators, a 5-bit QNS SAR quantizer with passive adder, two DACs and data-weighted-averaging (DWA) logic. Two integrators are used to
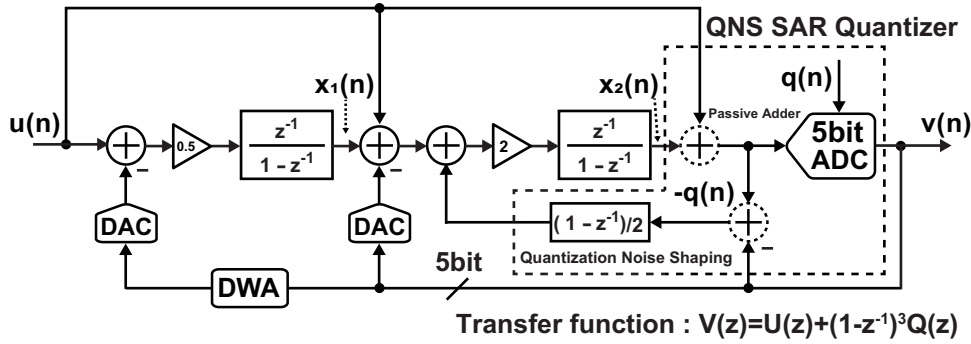
FIGURE 5.1: Block diagram of proposed 3rd-order delta sigma modulator using QNS SAR Quantizer.

realize the 2nd-order noise shaping. The 5-bit passive adder embedded QNS SAR quantizer is used to realize analog signal summation, quantization and quantization noise shaping. The proposed QNS SAR quantizer is used not only as an internal quantizer, but also as a noise coupling circuit. The QNS circuit realizes the transfer function of $(1 - z^{-1})/2$ for quantization noise -q(n) as shown in figure 5.1. The signal $-(1 - z^{-1})q(n)/2$ is transferred to the input node of the 2nd integrator, so that the quantization noise is re-injected to modulator for realizing an addition 1st-order noise shaping. Therefore, the noise coupled delta sigma modulator realizes 3rd-order noise shaping function by using two integrators. Moreover, the analog signal summation in front of SAR quantizer is realized by the passive circuit instead of the active adder with a power hungry amplifier. Above techniques are conducted to reduce the active area and power dissipation of the proposed delta sigma modulator. The DWA technique is also provided to the modulator for suppressing the influence of DAC mismatch.

5.3 Implementation

Figure 5.2 illustrates the schematic diagram of the proposed 3rd-order delta sigma modulator with two ring-amplifier-based integrators and a 5-bit QNS SAR quantizer with passive adder. Its clock timing chart and operation mode diagram are shown in figure 5.3(a) and figure 5.3(b), respectively. The proposed delta sigma modulator is the feed-forward architecture, and the input signal to the loop filter contains
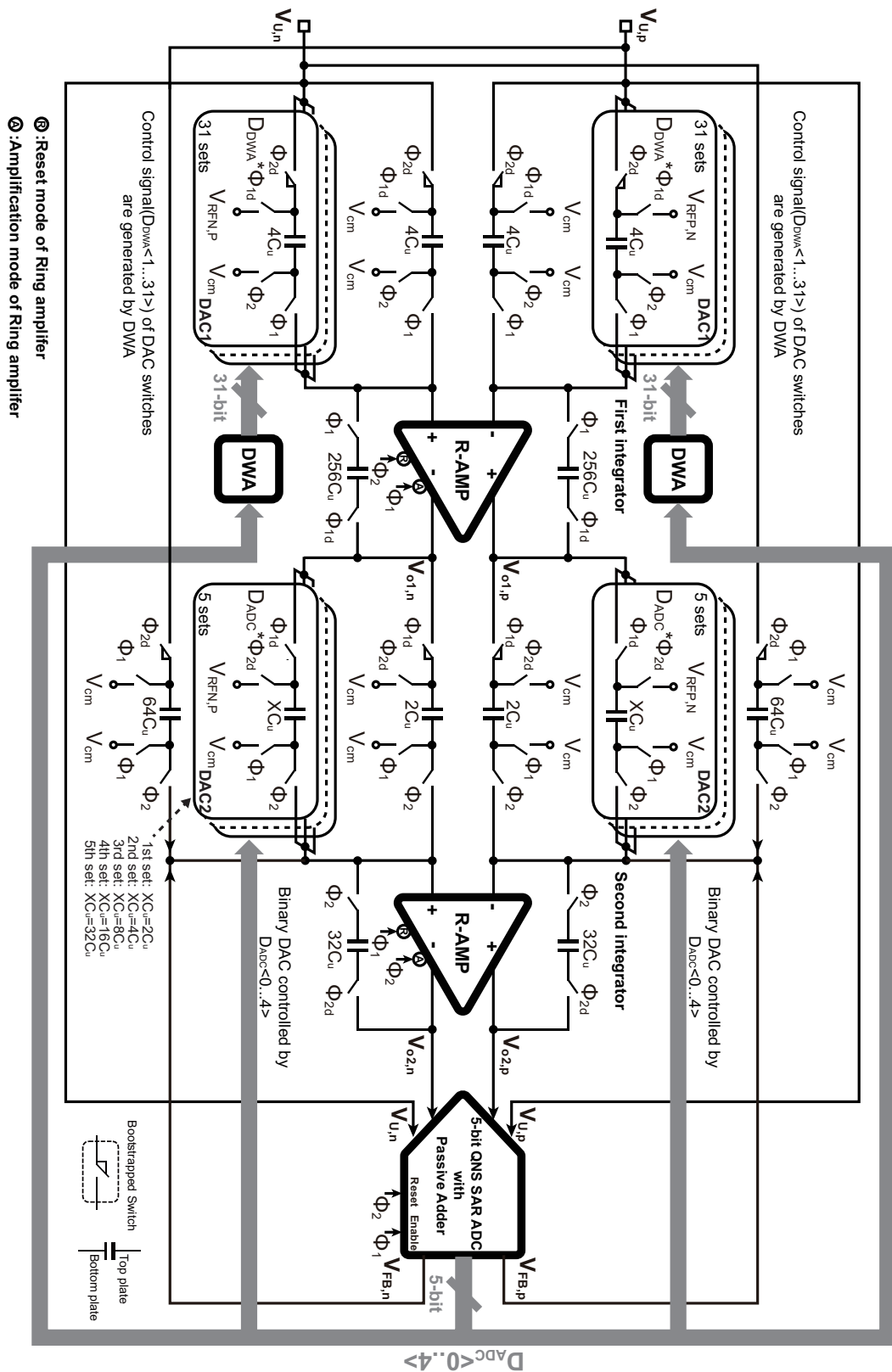
FIGURE 5.2: Schematic diagram of proposed 3rd-order feed-forward
delta sigma modulator using ring amplifier (R-AMP) with QNS SAR
quantizer.
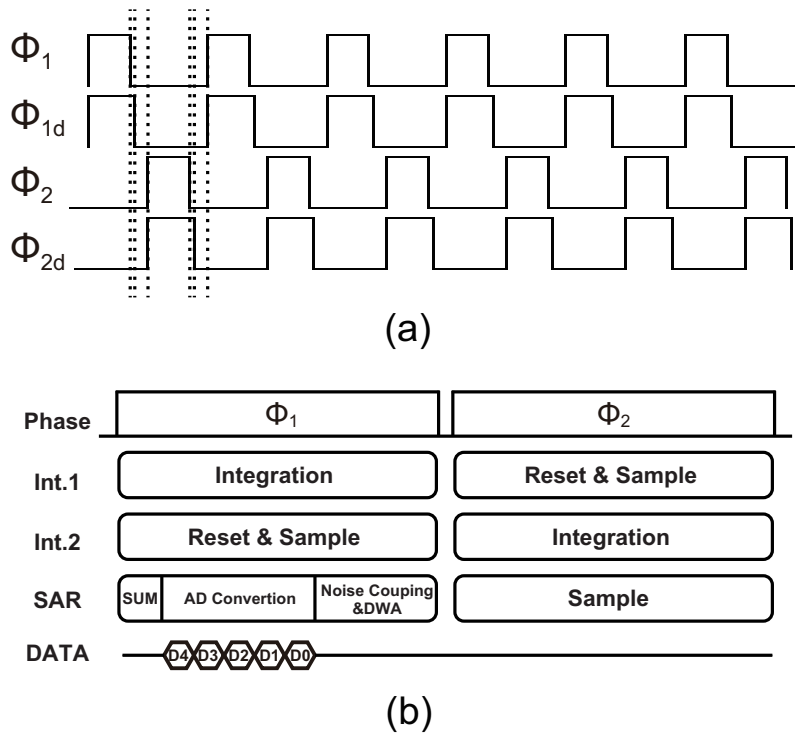
FIGURE 5.3: Timing chart of proposed 3rd-order feed-forward delta sigma modulator using ring amplifier (R-AMP) with QNS SAR quantizer.

only the shaped quantization noise, so that the modulator can reduce the influence of amplifier's non-linearity for higher SNDR [6]. The ring amplifier for the integrators can realize higher gain than the traditional amplifier at low supply voltage, and the static current of the ring amplifier is very small, so that the power consumes of the modulator can be maintained low. The 5-bit QNS SAR ADC is used as a multibit quantizer in the modulator, not only the stability of the 3rd-order modulator is improved, but also the requirement on the slew-rate of amplifier is relaxed. In addition, the quantizer can also feedback the signal containing the quantization noise of $-(1 - z^{-1})q(n)/2$ for realizing noise coupling. The 5-bit QNS SAR ADC has 2 inputs terminal (V_U and V_{o2}), since the quantizer converts the summation of them to digital code by passive capacitor, the analog adder with amplifier is not necessary. A 5-bit capacitive DAC (DAC1) with unit-segment-element in figure 5.2 is used for the 1st integrator. While the capacitor mismatches among the unit elements in a multibit DAC cause the harmonic distortion in the signal band, the DWA logic circuit [7] is applied to reduce the influence of DAC nonlinearity errors. Although the noise

caused by the capacitor mismatch of DAC2 is injected into the delta sigma modula-
tor from the input of the 2nd integrator, the non-linear noise is 1st-order shaped by
the 1st integrator. Therefore, the 5-bit capacitive DAC (DAC2) in figure 5.2 for the
2nd integrator is designed as a binary-weighted-element without DWA for simplic-
ity.

5.3.1   Pseudo Differential Ring Amplifier with improved CMFB

In this work, we use the pseudo differential ring amplifier proposed in the previous
work [5, 8] to realize the integrator for achieving the maximum power-efficiency
of the amplifier in the delta sigma modulator. figure 5.4(a) shows the pseudo dif-
ferential ring amplifier. Capacitors (C_C) are added to the input nodes of amplifier
to realize the amplifier input offset cancellation for the integrator. In the previous
works [5] and [8], the voltage division from the C_C and the capacitors of the com-
mon mode feedback (CMFB) circuit cause the reduction of common mode rejection
ratio (CMRR). This paper proposes the modifying CMFB circuit as shown in figure
5.4(a). Because the CMFB circuit not include capacitors in series, it can directly feed-
back the common mode signal from the output terminal of the ring amplifier's core
to the input terminal of the ring amplifier's core for obtaining the maximum CMRR.
The core of ring amplifier is shown in figure 5.4(b). It is constructed with three stage
cascaded inverters. The input of the MOSFET M_{P1} and M_{N1} are biased at V_{cm} when
the ring amplifier forms a feedback loop, therefore, the M_{P1} and M_{N1} operate in the
weak inversion region during the steady state of the amplifier with a very low static
current. The inverter which consists of M_{P1} and M_{N1} behaves as a class-AB amplifier
providing high DC-gain and good linearity. The R_{OS} can compress the drain-source
voltage of the M_{P2} and M_{N2} to the boundary between the weak and strong inver-
sion regions for obtaining both high DC-gain and wide GB [4]. In addition, it also
generates the different offset voltages to the gate of M_{P3} and M_{N3} for setting their
gate-source voltage at lower than threshold. Therefore, the push-pull inverter con-
sisting of M_{P3} and M_{N3} behaves as a class-C amplifier for reducing the setting time
of the ring amplifier dramatically.
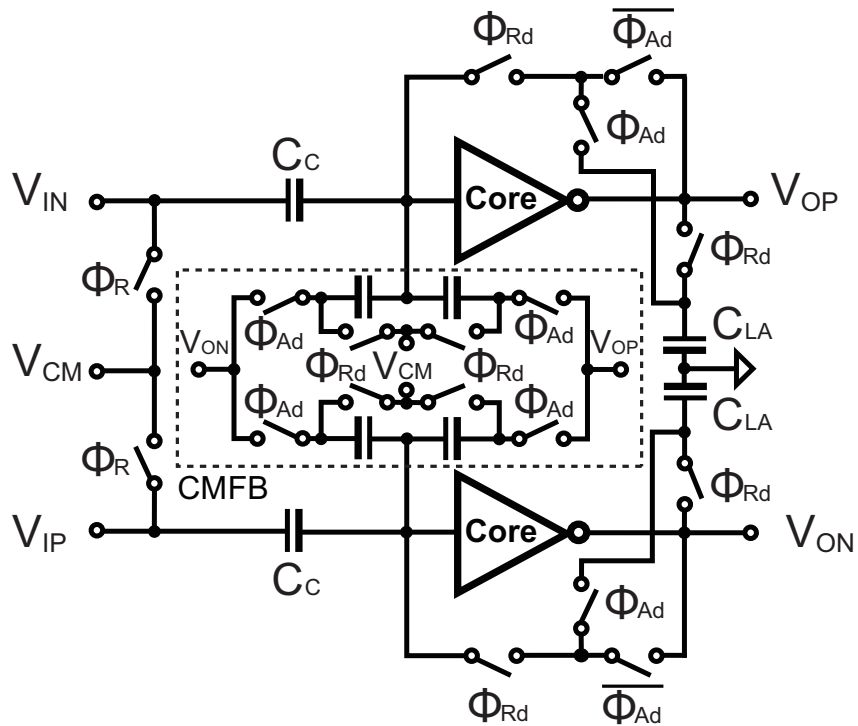
Φ_R : Reset mode of R-AMP
Φ_A : Amplification mode of R-AMP
(Φ_R=Φ_2,Φ_A=Φ_1,in the 1st integrator)
(Φ_R=Φ_1,Φ_A=Φ_2,in the 2nd integrator)

(a)
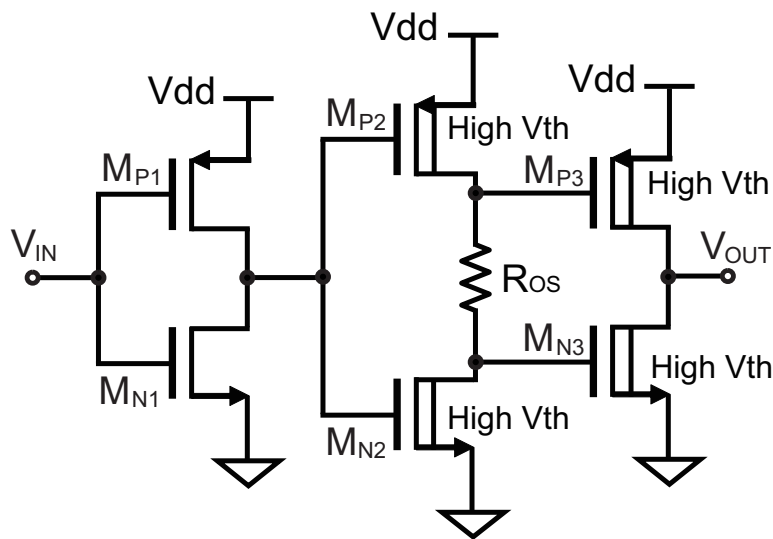
(b)

FIGURE 5.4:   Schematic of pseudo differential R-AMP (Ring-Amplifier). (a) R-AMP (Ring-Amplifier). (b) Core of R-AMP.

Resistor R_{OS} is inserted to the output of the 2nd stage inverter. M_{P3} and M_{N3} are cut off during the steady state of the amplifier without static current, therefore, the power consumption of the integrator based on ring amplifier can be reduced. For two transistors M_{P3} and M_{N3}, one of them is operating in the strong inversion region while the other is completely off during transition providing high slew rate, so that the setting time of the ring amplifier can be reduced dramatically. and the rail-to-rail output is allowed for the ring amplifier. Because the input referred noise of SC integrator using the ring amplifier depends on the class-AB amplifier which consist of M_{P1} and M_{N1} mainly, , the power of the input referred noise is obtained as

$$\frac{GB}{f_s} \times \frac{4}{3}\frac{kT}{g_m} \approx \frac{20}{3}\frac{kT}{g_m} \tag{5.1}$$

where the ratio of the unit-gain-bandwidth(GB) and sampling frequency(f_s) is set as 5 in the delta sigma modulator. the noise level of a ring-amplifier-based SC integrator is better than the thermal noise of a conventional SC integrator using an OTA [4]. Moreover, high threshold voltage $M_{P2,3}$ and $M_{N2,3}$ are used in the 2nd, 3rd-stage to extend the stable offset voltage range for the amplifier.

5.3.2 Passive Adder embedded QNS SAR Quantizer

Figure 5.5 shows the schematic diagram of the proposed passive adder embedded QNS SAR quantizer. It consists of QNS circuit, capacitive DAC, a dynamic comparator(figure 5.6) and asynchronous SAR logic circuits. Figure 5.7(a) and figure 5.7(b) show the equivalent circuit of capacitor array as the passive adder at two kinds of operation mode. Note that the QNS circuit consists of five parts of capacitors which have the same capacitance ($32C_u$). In the sampling mode (Φ_2), the bottom plates of two capacitors among the QNS circuit's capacitors ($64C_u$) are connected to the output of the 2nd integrator(V_{o2}). Meanwhile, the top plates of SAR DAC's capacitors ($64C_u$) are connected to the input of the $\Delta\Sigma$AD modulator (V_U) as shown in figure 5.7(a). The capacitor ratio for 2 input signals is 1:1, then the total charge stored on the capacitor Q_s can be expressed as

$$Q_S = 64C_u \times V_U + 64C_u \times V_{o2}. \tag{5.2}$$
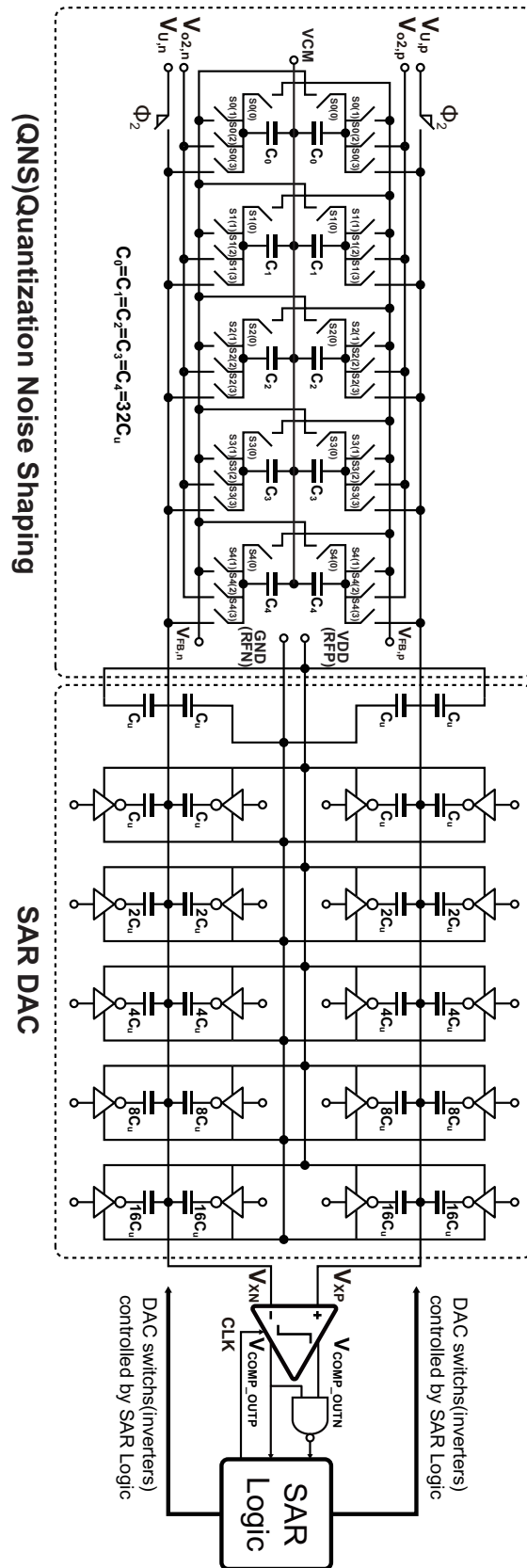
FIGURE 5.5: Circuit implementation of proposed passive adder embedded QNS SAR Quantizer.

In the summation mode (Φ_1), the bottom plates of two sampled capacitors are connected to the input node of comparator (V_X) as shown in figure 5.7(b). Because the total capacitance at the node V_X is $128C_u$, the total charge Q_C of this summation mode on capacitors is

$$Q_C = 128C_u \times V_X. \tag{5.3}$$

According to the charge-conservation law, we have

$$Q_C = Q_S. \tag{5.4}$$

Then, we get equation

$$V_X = \frac{Q_S}{128C_u} = \frac{V_U + V_{o2}}{2}, \tag{5.5}$$

that means the summation of 2 input signals can be realized by capacitor array. After the analog input summation is finished, the AD conversion is carried out from MSB to LSB in the successive approximation manner.
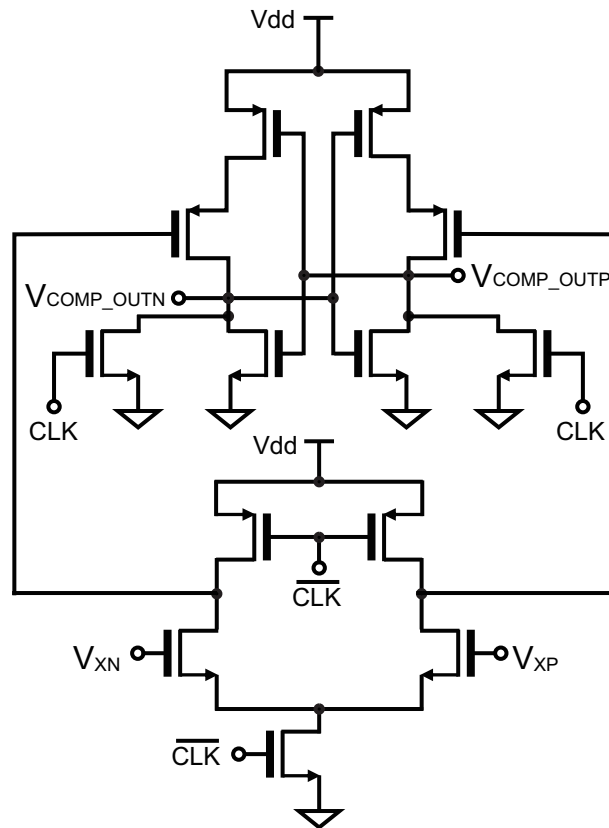
FIGURE 5.6: Schematic diagram of the dynamic comparator used in SAR quantizer.

(b)

$$V_{XP}-V_{XN}=\frac{(V_{U,p}-V_{U,n})+(V_{o2,p}-V_{o2,n})}{2}$$

(c)
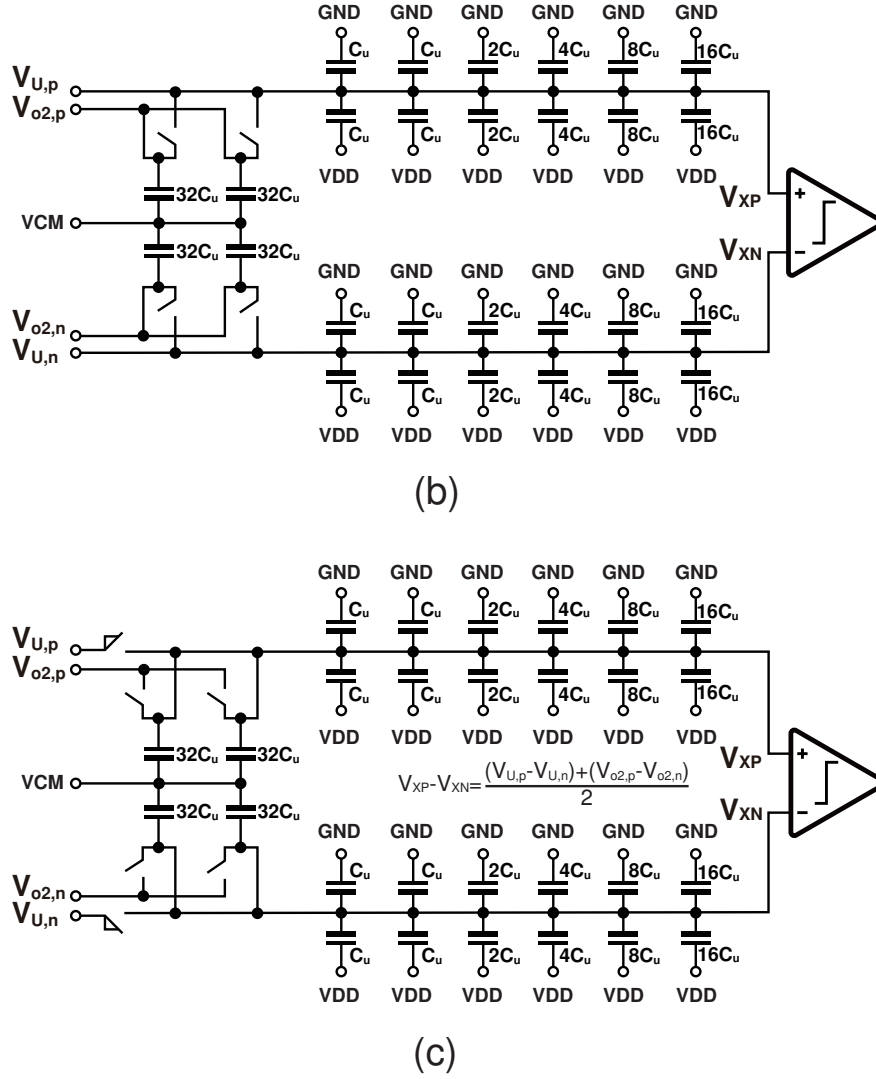
FIGURE 5.7: Equivalent circuit of the proposed QNS SAR quantizer in the different operation. (a) Sampling mode. (b) Summation and successive approximation mode.

When the successive approximation is finished, the voltage of comparator's input node V_X equals to the half of negative quantization noise $-q(n)/2$, and the residual voltage is stored on the two capacitors used for sampling among the 5 capacitors in QNS circuit. Moreover, the QNS circuit not only save the residual voltage of quantization noise, but also realize the transfer function $(1-z^{-1})/2$ by controlling the switches of the QNS circuit. Figure 5.8(a) illustrates the schematic diagram of the clock generator for the QNS circuit. S0(0) to S4(3) shown in figure 5.8(b) are control signals for the switches of QNS circuit as shown in figure 5.8(a), it realizes the five kinds of QNS circuit's operation states. Figure 5.9 illustrates the equivalent circuits of the QNS circuit in five kinds of the operation states. In the state 0, C_0 and C_4 are

used for sampling during Φ_2 and passive addition during Φ_1. When the successive approximation of the quantizer is finished, $-q(n)/2$ is stored on C_0 and C_4. In the next operation period, the QNS circuit become to state 1 by rotating the capacitors around the midpoint, C_3 and C_2 are used for the sampling during Φ_2 and passive addition during Φ_1. C_0 is connected to V_{FB} that can realize $-q(n)/2$. Meanwhile, C_1 with the quantization noise of the previous period is connected to V_{FB} which can realize $-z^{-1}(-q(n)/2)$. As the result, the QNS circuit is rotated among five kinds of state continuously, and the noise signal $(1 - z^{-1})(-q(n))/2$ is outputted from the terminal of the QNS circuit V_{FB}. The signal V_{FB} is connected to the input node of the 2nd integrator that realize an extra 1st-order noise shaping by our proposed noise coupling technique. Therefore, the 3rd-order noise shaping characteristics is realized only with two dynamic amplifiers (ring amplifier), thus the power consumption can be kept at a low level in the proposed delta sigma modulator. Moreover, since the capacitors of the QNS circuit are used for sampling and feedback in the rotated manner at each period, as the same as the DWA manner, the capacitors mismatch of $(C_0...C_4)$ in the QNS circuit can also be shaped.

Asynchronous SAR logic circuits [9] are used to control the capacitor DAC of 5-bit SAR quantizer. The operation speed of the asynchronous SAR logic circuit may be reduced at the PVT worst case. Since the required operation time of asynchronous SAR logic circuit in our modulator can be drastically relaxed than a high speed ADC, the speed reduction of SAR logic circuit can considered have no significant influence on the proposed QNS SAR quantizer. Moreover, the proposed quantization noise coupling technique is not requite using the active analog component, the lower power consumption can be maintained.

5.3.3 Multi-bit DAC and DWA Logic Circuit

A 5-bit capacitor DAC is used for the 1st integrator as shown in figure 5.2, the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the data-weighted-averaging (DWA) logic circuit [7] is applied to the delta sigma modulator to reduce the influence of DAC non-linearity errors. To illustrate the effect of the DWA logic circuit, the Monte Carlo analysis comparison
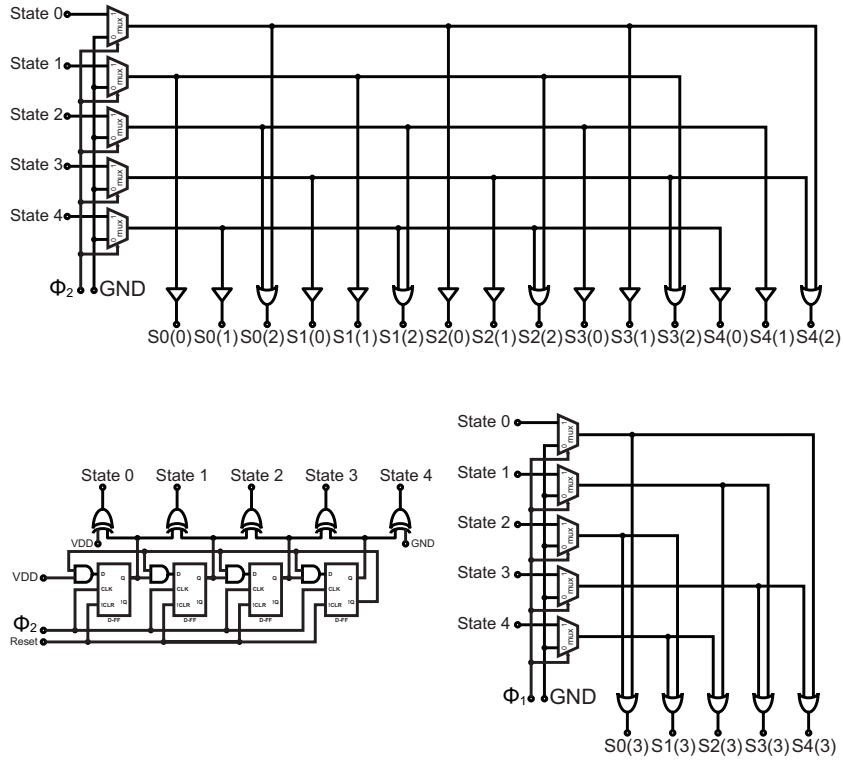
(a)
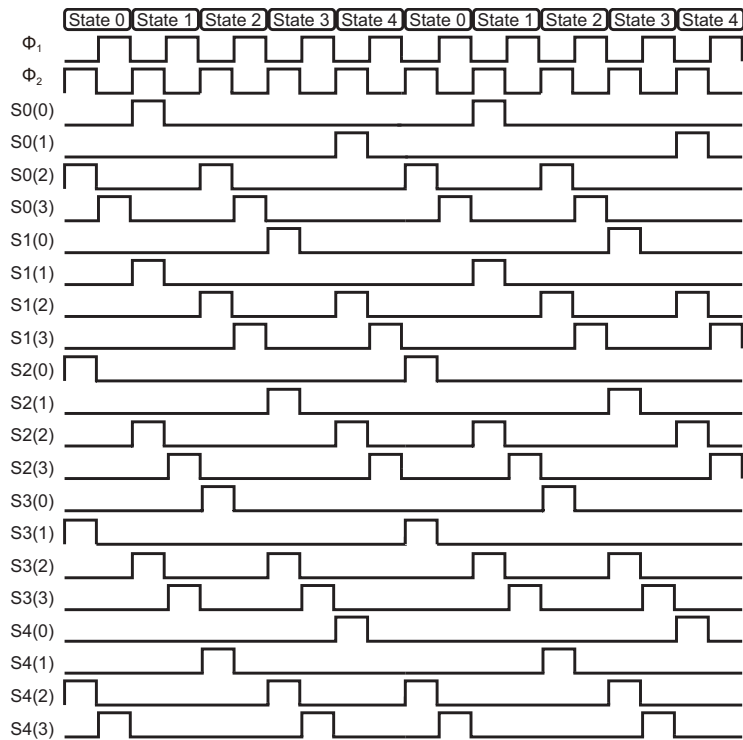
(b)

FIGURE 5.8: Circuit implementation of proposed the QNS circuit. (a) Clock generator of the QNS circuit. (b) Clock timing chart of the QNS circuit.
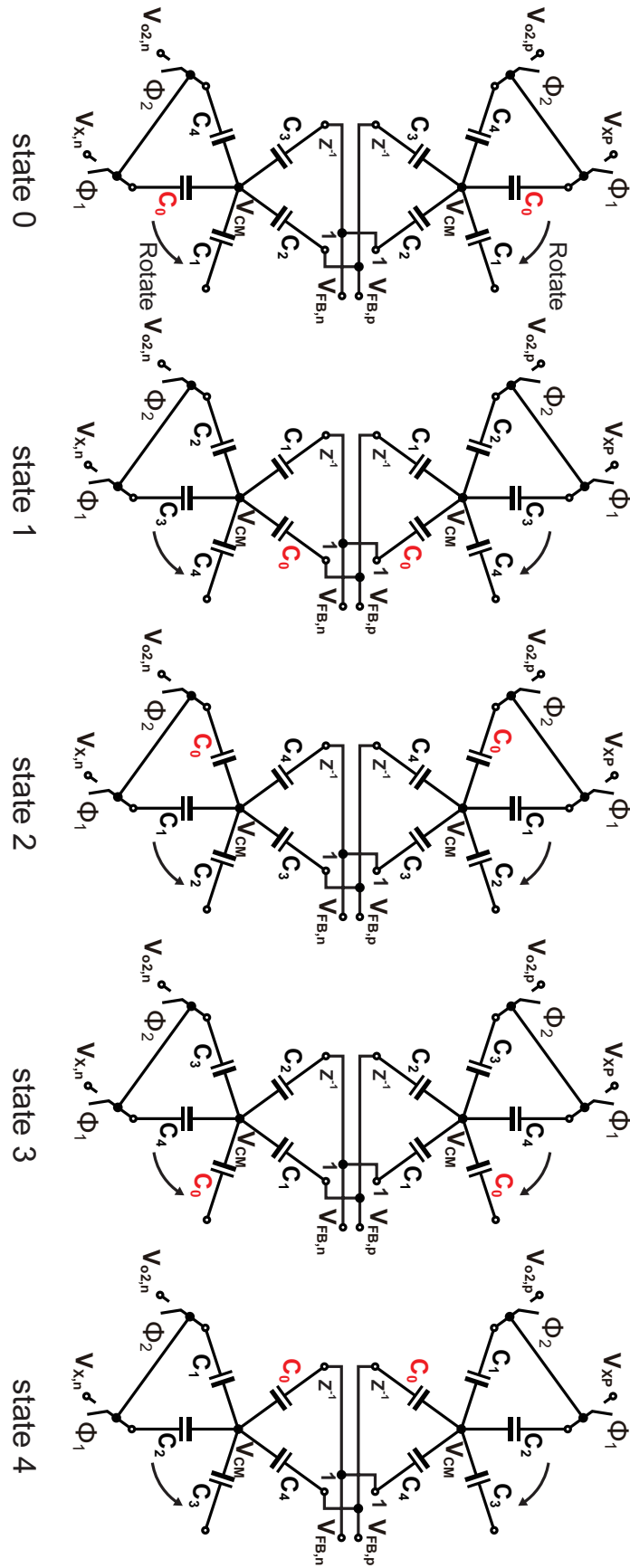
FIGURE 5.9: Equivalent circuits of the five kinds of the QNS circuit's state
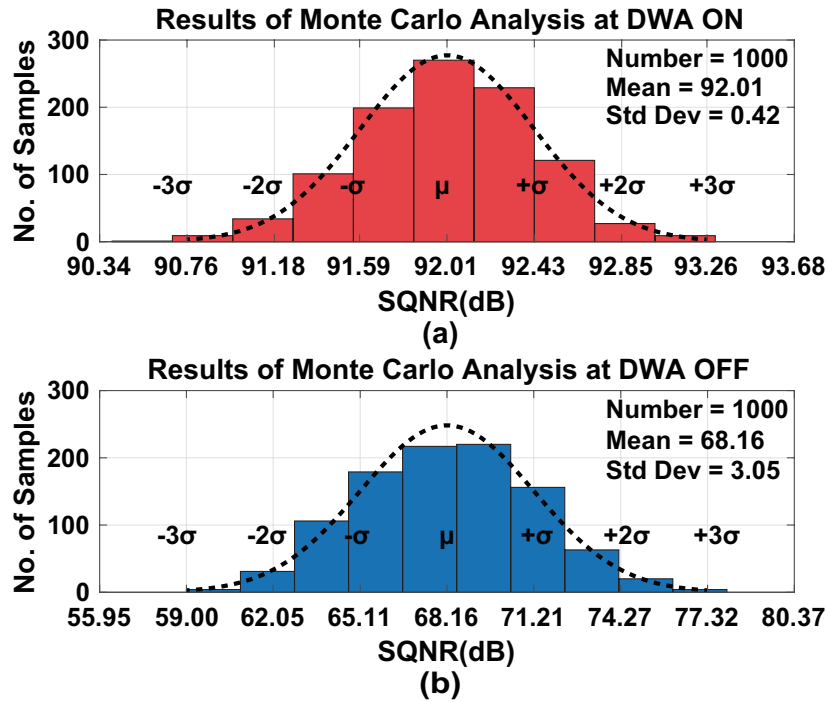
FIGURE 5.10: Monte carlo analysis results comparison of delta sigma modulator performed by matlab with ≤1% unit-capacitance random mismatches of DAC. (a) DWA ON. (b) DWA OFF.

with the proposed modulator is performed by MATLAB in 2 cases: (a) 4-bit DAC with ≤1% unit-capacitance random mismatches while DWA at ON mode; (b) 4-bit DAC with ≤1% unit-capacitance random mismatches while DWA at OFF mode. Analyzed results of the above 2 cases are shown in figure 5.10(a) and (b), respectively. While the unit-capacitance of DAC is variated without DWA, the non-linearities of DAC raise the in-band noise floor, and cause the harmonic distortion, the average SQNR of 68.16 dB is shown in figure 5.10(b). On the other hand, while DWA technique is applied, the in-band noise and the harmonic distortion in the signal band are noise-shaped, the average SQNR reaches 92.01 dB as shown in figure 5.10(a).

5.4 Simulation

5.4.1 Noise Analysis of Integrator with Different DAC

Figure 5.11 shows two different implementation (A and B) of the first integrator with DAC in the proposed delta sigma modulator. The input branches are different, the
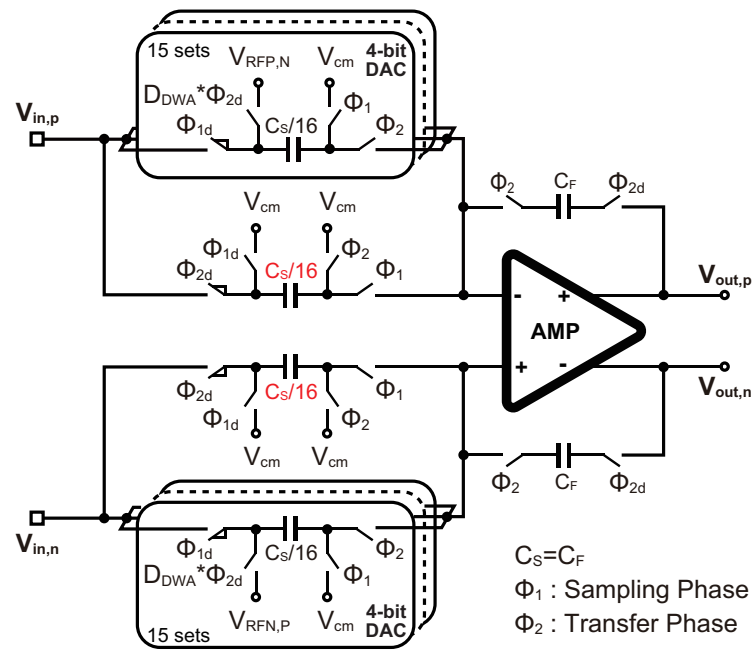
Implementation A
(The load on the reference supply depend on the size of the input signal)

(a)
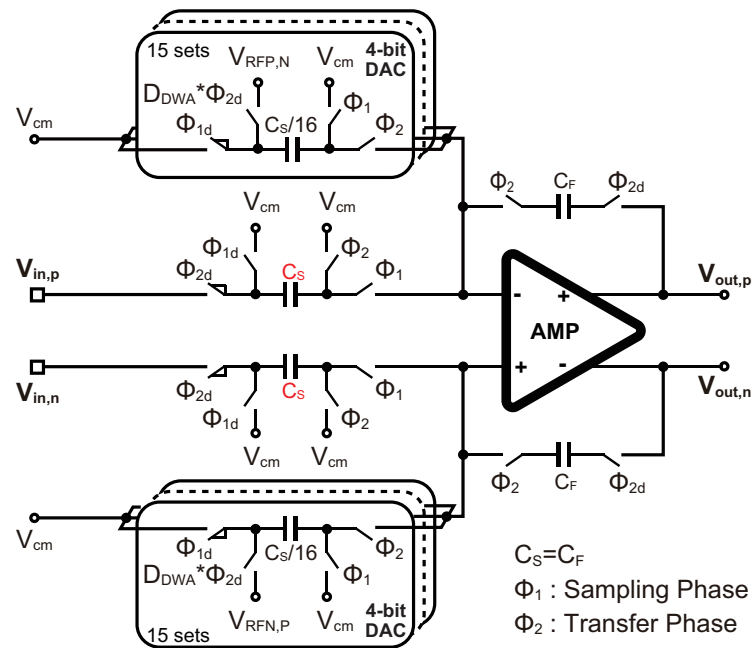
Implementation B
(The load on the reference supply is independent on the size of the input signal)

(b)

FIGURE 5.11: Circuit implementation of the first integrator with DAC. (a) The load on the reference supply depend on the size of input signal. (b) The load on the reference supply is independent on the size of input signal.

sampling capacitors of implementation A shown in the figure 5.11(a) are shared, oppositely, the sampling capacitors of implementation B shown in the figure 5.11(b) the sampling capacitor are separated from DAC capacitors. Theoretically, the implementation A has half of kT/C noise than the implementation B, since the less input capacitance at the input branch of the first integrator with DAC.

5.4.2 Simulation with Thermal Noise

The proposed 3rd-order delta sigma modulator is designed in TSMC 90nm CMOS technology. The proposed delta sigma modulator operates at a clock rate of 100 MHz for a 3.125 MHz BW with an OSR of 16, and power consumption 4.58 mW under supply voltage of 1.2 V for both analog circuit part and digital circuit part. Transistor-level SPICE simulations have been conducted to confirm the performance of the modulator and to verify the effectiveness of the proposed architecture. The simulated spectrum results with a -4.32 dBFS 366.21 kHz sine signal and the SNDR of the proposed modulator are shown in figure 5.12. Figure 5.12(a) shows the simulated spectrum result without the thermal noise and the flicker noise. When the DWA is not applied, the only peak SNDR of 70.59 dB and SFDR of 71.74 dB are achieved. When the DWA is applied, the SNDR and SFDR are improved to 91.64 dB and of 101.03 dB, respectively. In order to show close to the measured performance of the delta sigma modulator as much as possible, the simulation including both thermal noise and flicker noise calculated by the SPICE simulator according to the CMOS process library model is performed. The maximum noise frequency parameter of the simulator is set as the clock rate of 100 MHz, it controls the amount of energy each noise source can emit. The minimum noise frequency parameter of the simulator is set as 10 KHz, it establishes the lower frequency bound on flicker noise modeling [10]. Figure 5.12(b) shows the simulated spectrum result including thermal noise and flicker noise. When the DWA is not applied, the peak SNDR of 70.20dB and SFDR of 71.42dB are achieved. When the DWA is applied, the SNDR and SFDR are improved to 81.05dB and 91.00dB, respectively. Moreover, the simulated spectrum results shown in both of figure 5.12(a) and (b) also considered the affect of $\leq 1\%$ unit-capacitance random mismatches of DAC. Figure 5.13 illustrates the percentage
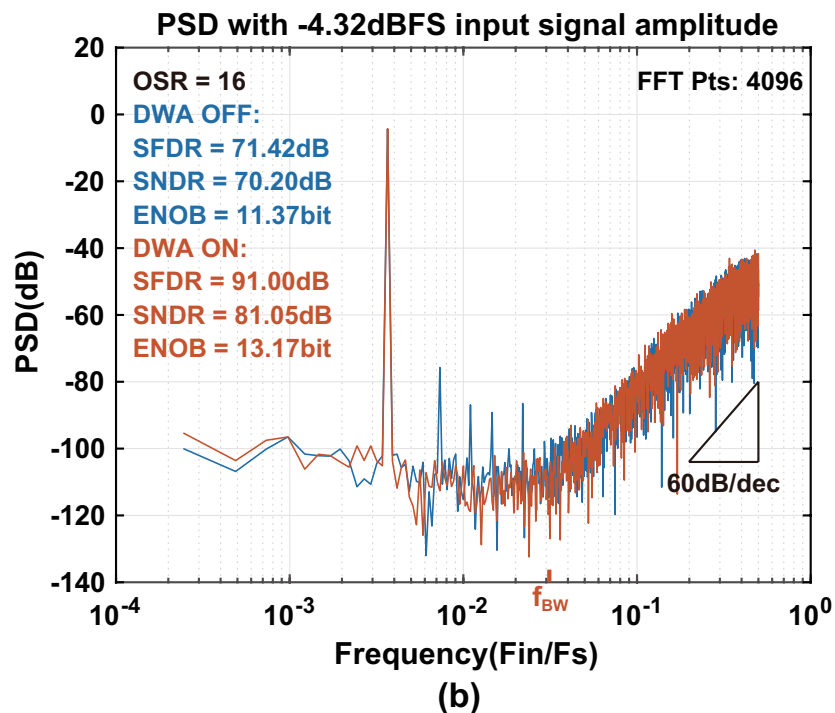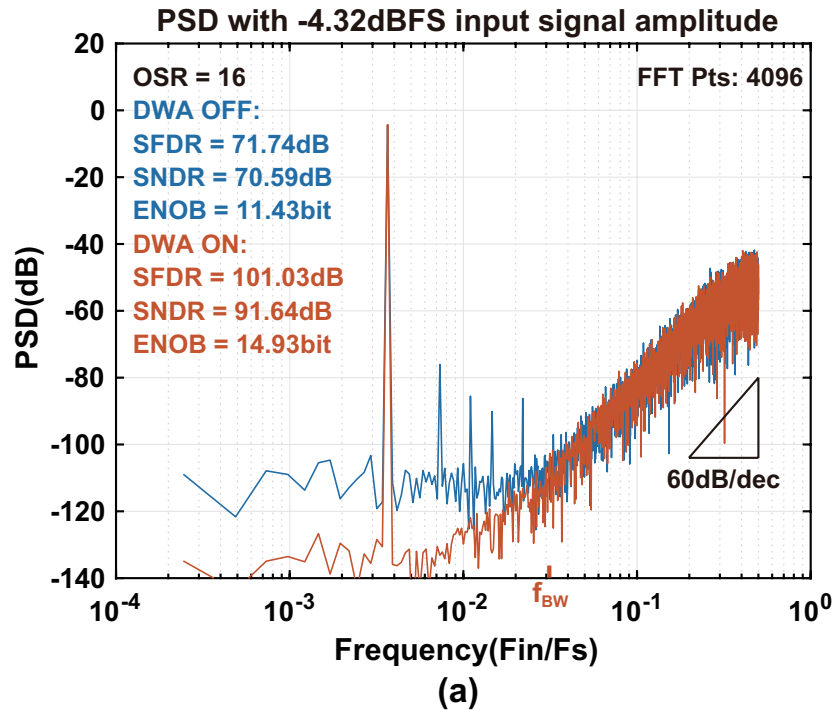
FIGURE 5.12: Simulated output spectrum with ≤1% unit-capacitance mismatches of DAC for f_{in} ≈366.21 kHz and -4.32 dBFS input signal amplitude. (a) without thermal noise and flicker noise. (b) with thermal noise and flicker noise.

of power consumption for each module: the integrators about 60.3% of the total power; the SAR quantizer about 15.9%; the QNS control circuit about 3.5%; the DWA circuit about 3.2%; and the other digital circuit, including the SAR logic circuit, DAC control circuit and the clock buffer about 17.1%.
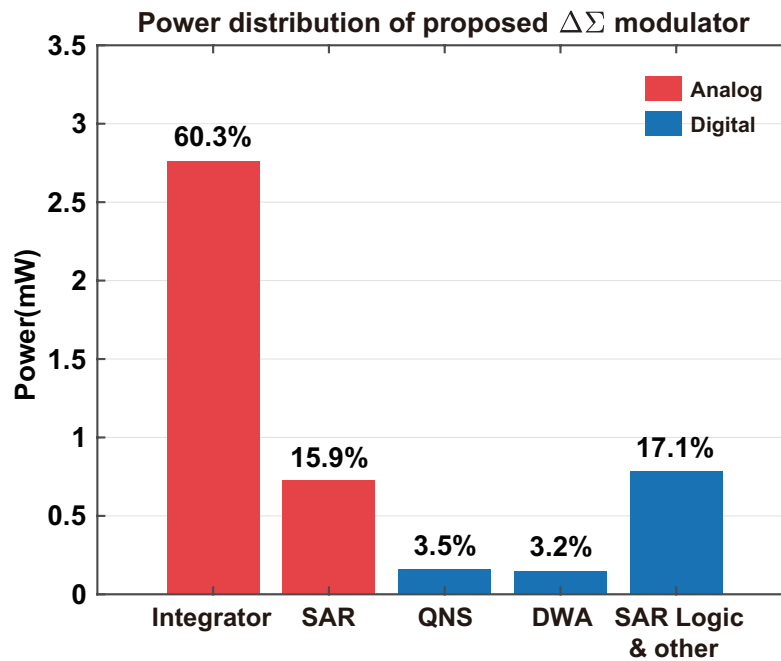
FIGURE 5.13: Power distribution of proposed delta sigma modulator.

The performance of the proposed delta sigma modulator is summarized in Table 5.1 in comparison with the previous works. The operation speed and the signal band width are comparable to other works. The calculated FOMW and FOMS are 79.4 fJ/conversion-step and 169.4 dB respectively. Compared with other similar BW work, the simulations show an better FOM. Although the influence of thermal noise, flicker noise and cap-mismatch are considered in the simulation results of proposed delta sigma modulator, it is not a chip's measurement, the SNDR and FOM of the prototype modulator should be degraded from the SPICE simulation results. However, the operation speed and the signal band width often meet the comparable value to the SPICE simulation results.

TABLE 5.1: Performance summary and comparison with previous
works

Specification	[3][***]	[2][***]	[11][***]	[12][***]	[13][*]	[14][*]	[15][**]	This work	
Technology(nm)	28	65	55	180	90	90	90	90	
Architecture	CT-4th	CT-6th	CT-4th	DT-3rd	DT-2nd	DT-3rd	DT-3rd	DT-3rd	
Supply voltage(V)	1.1/1.2	1.8	1.2/1.8	1.2	1.2	1.2	1.2	1.2	
Sampling rate (MS/s)	320	900	140	25	60	80	60	100	
OSR	16	10	32	8	15	16	16	16	
Signal BW (MHz)	10	45	2.2	1.56	2	2.5	1.875	3.125	
SNDR (dB)	74.4	75.3	90.4	75	56	81.97	78.8	91.64(N)	81.05(T)
Power (mW)	4.2	24.7	4.5	2.6(A)	1.56	2.53(A)	1.59(A)	3.49(A)	
				3.75(D)		1.64(D)	1.26(D)	1.09(D)	
FOMW (fJ/conv.-step)	49.3	57.7	37.8	442.1	756.5	81.5	95.2	23.4(N)	79.4(T)
FOMS (dB)	168.1	167.9	177.3	158.9	147.1	169.7	168.0	179.9(N)	169.4(T)

[***] : Experimental results with thermal noise
[**] : Post-layout simulation results without thermal noise
[*] : Transistor-level simulation results without thermal noise
A : Analog, D : Digital, N : Without thermal noise and flicker noise, T : With thermal noise and flicker noise
$\text{FOMW} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$
$\text{FOMS} = \text{SNDR} + 10 \times \log_{10}(\text{BW}/\text{Power})$

5.5 Summary

A 3rd-order delta sigma modulator with noise coupling technique using passive adder embedded quantization noise shaping (QNS) SAR quantizer has been designed in 90 nm CMOS technology. Benefit from the quantization noise feedback function of the proposed QNS SAR quantizer, an additional 1st-order noise shaping can be realized by the noise coupling technique. The proposed noise coupling technique is not requite using the active analog component, the lower consumption can be maintained. Furthermore, only two non-overlapped clocks are required for the proposed delta sigma modulator, which is realized by a sample clock generator. The delta sigma modulator circuit is realized by dynamic analog component, therefore the power consumption can be kept at a low level. The simulation results including both thermal noise and flicker noise show the feasibility of the proposed delta sigma modulator.

References

[1] K. Lee, M.R. Miller, and G.C. Temes. "An 8.1 mW, 82 dB DeltaSigma ADC With 1.9 MHz BW and -98 dB THD". In: *IEEE J. Solid State Circuits* vol.44 (Aug. 2009), pp. 2202–2211 (cit. on p. 95).

[2] B. Wu et al. "A 24.7mW 45MHz-BW 75.3dB-SNDR SAR Assisted CT ΔΣModulator with 2nd-Order Noise Coupling in 65nm CMOS". In: *IEEE ISSCC 2016 Dig of Tech* (Feb. 2016), pp. 270–271 (cit. on pp. 95, 114).

[3] Jang et al. I. "A 4.2mW 10MHz BW 74.4dB SNDR Fourth-order CT DSM with Second-order Digital Noise Coupling Utilizing an 8b SAR ADC". In: *IEEE Symp. VLSI Circuits Dig. Tech.* (2017) (cit. on pp. 95, 114).

[4] Y. Chae and G. Han. "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator". In: *IEEE J. Solid State Circuits* vol.44 (Feb. 2009), pp. 458–472 (cit. on pp. 96, 100, 102).

[5] B. Hershberg et al. "Ring amplifiers for switched capacitor circuits". In: *IEEE J. Solid State Circuits* vol.47 (Dec. 2012), pp. 2928–2942 (cit. on pp. 96, 100).

[6] J. Silva et al. "Wideband lowdistortion delta-sigma ADC topology". In: *Electronics Letters* vol.37 (June 2001), pp. 737–738 (cit. on p. 99).

[7] T. Kuo, K. Chen, and H. Yeng. "A wideband CMOS sigma-delta modulator with incremental data weighted averaging". In: *IEEE J. Solid-State Circuits* vol.37 (Jan. 2002), pp. 11–17 (cit. on pp. 99, 106).

[8] Y. Lim and M. Flynn. "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers". In: *IEEE ISSCC 2014 Dig of Tech* (Feb. 2014), pp. 202–203 (cit. on p. 100).

[9] Y. Zhu et al. "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS". In: *IEEE J. Solid-State Circuits* vol.45 (June 2010), pp. 1111–1121 (cit. on p. 106).

[10] Inc Synopsys. *HPISCE User Guide : Advanced Analog Simulation and Analysis*. Version M-2017.03-SP1, June 2017 (cit. on p. 111).

[11] C.-Y. Ho et al. "A 4.5 mW CT self-coupled ΔΣ modulator with 2.2 MHz BW and 90.4 dB SNDR using residual ELD compensation". In: *IEEE J. Solid-State Circuits* vol.50 (Dec. 2015), pp. 2870–2879 (cit. on p. 114).

[12]   O. Rajaee et al. "Low-OSR over-ranging hybrid ADC incorporating noise-shaped two-step quantizer". In: *IEEE J. Solid-State Circuits* vol.46 (Nov. 2011), pp. 2458–2468 (cit. on p. 114).

[13]   E. Bilhan and F. Maloberti. "A wideband sigma-delta modulator with cross-coupled two-paths". In: *IEEE Trans. Circuits Syst. I* vol.56 (May 2009), pp. 886–893 (cit. on p. 114).

[14]   I.J. Chao et al. "A third-order low-distortion delta-sigma modulator with opamp sharing and relaxed feedback path timing". In: *IEICE Trans. on Electronics* vol.E95-C, no.11 (Nov. 2012), pp. 1799–1809 (cit. on p. 114).

[15]   I. Chao et al. "A Single Opamp Third-Order Low-Distortion Delta-Sigma Modulator with SAR Quantizer Embedded Passive Adder". In: *IEICE Trans. on Electronics* vol.E97-C, no.6 (June 2014), pp. 526–537 (cit. on p. 114).

Chapter 6

6th-Order Quadrature Bandpass Delta Sigma Modulator

6.1 Preface

In wireless communication systems, the digital signal processing with complex signals is widely used in the receiver circuit. High speed, high resolution, low power consumption Analog-to-Digital Converter (ADC) is necessary in both I-channel and Q-channel complex signal paths, respectively as shown in figure 6.1(a). Due to the performance of the baseband receiver (low-frequency receiver) circuit using Nyquist-rate ADC is easily affected by the DC-offset and the flicker noise ($1/f$ noise), the quadrature bandpass delta sigma AD modulator (QBPDSM) shown in figure 6.1(b) is proposed [1] for reducing the influence of the DC-offset and the flicker noise. QBPDSM can be used in the mixed-signal system-on-chip (SoC) in the fields of both the digital radio and the gyro sensor. Several techniques have been proposed to improve the performance and the energy efficiency of QBPDSM.

6.1.1 Image Rejection Technique

Image rejection technique is proposed [1] to reduce the influence of the mismatch of I and Q paths. Multi-bit internal quantizer can relax the slew-rate requirement on the amplifier to reduce the power consumption of the modulator [2]. Feed-forward structure is used to reduce the output swing of the integrator, which can relax the
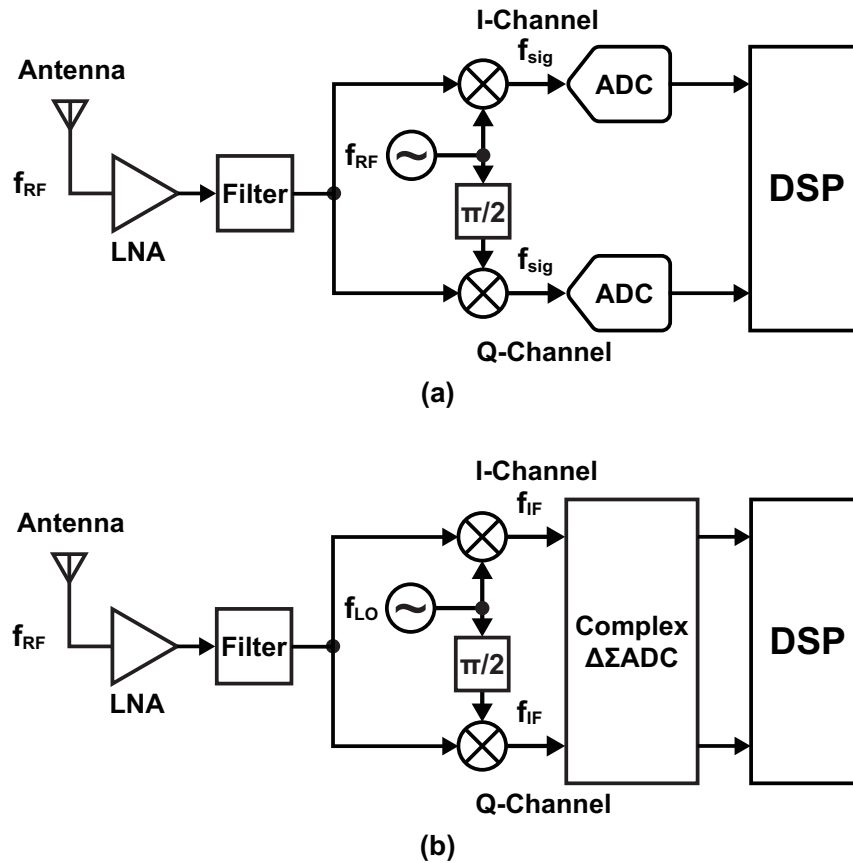
FIGURE 6.1: Radio receiver for wireless communication systems. (a)
Baseband receiver. (b) Intermediate frequency (IF) receiver.

linearity requirements on the amplifier in the integrator, and can reduce the power
consumption of the delta sigma AD modulator [3].

6.1.2   Comparison of Complex Integrator Implement Method

For realizing the integration of the complex signal, the traditional complex integra-
tor circuit is proposed in the previous work [1]. The amplifiers used to achieve the
traditional complex integrator circuit perform twice charge transfer actions (two op-
eration phases are required) for once integration operation of complex signal, which
accompany the high power consumption and the low energy efficiency. In this work,
a novel implementation of complex integrator circuit is proposed for improving the

energy efficiency and reducing the circuit area of QBPDSM. The dynamic amplifier instead of the operational transconductance amplifier (OTA) is used to implement the complex integrator circuit for maximizing the power efficiency of the amplifier. The proposed complex integrator only requires once charge transfer action for once complex integration operation, which can reduce the power consumption of QBPDSM. Furthermore, the load capacitance of proposed complex integrator circuit is half compare with the conventional complex integrator, which can reduce the circuit area of QBPDSM.

6.1.3 Concept of Proposed Quadrature Bandpass DSM

This chapter proposed a 6th-order QBPDSM with 2nd-order image rejection using the dynamic-analog-components (ring-amplifier) based complex integrators and the digital domain noise coupling (DDNC) SAR quantizer. In order to improve the performance of QBPDSM, the noise coupling (NC) SAR quantizer is used for realizing high order noise shaping and image rejection. The SAR-assisted digital domain noise coupling technique can easily realize the high order noise shaping with maintaining the high energy efficiency, which is verified in pervious works [4]. In this work, the digital domain noise coupling technique is applied to the implementation of the NC SAR quantizer, moreover, a passive adder is embedded in the NC SAR quantizer to further improve the energy efficiency of the QBPDSM. Two complex integrators consist of ring-amplifiers are used to realize the 2nd-order noise shaping. The passive adder embedded DDNC SAR quantizer is used to realize the analog adder in front of SAR quantizer, the quantization of input analog signal and the quantization noise coupling. Besides, the quantization noise is re-quantized, 4th-order digital shaped and re-injected to the delta sigma modulator, therefore, an additional 2nd-order noise shaping and 2nd-order image rejection is realized. SPICE simulations including the thermal noise and the flicker noise have been done to verify the effectiveness of the proposed architecture, and to confirm the performance of the QBPDSM. The peak SNDR of 76.30dB is achieved while OSR=8 for sinusoid input at 8.33MHz with -3.25dBFS input amplitude.

SAR Quantizer with Noise Coupling in Digital Domain

Passive Adder

u(n)

$\dfrac{z^{-1}}{1-jz^{-1}}$ $\dfrac{j}{1-jz^{-1}}$

DAC

$x_1(n)$ $x_2(n+1)$

6-bit DAC $-2z^{-2}-z^{-4}$ 4-bit ADC

q(n)

5-bit ADC   v(n)

5-bit DAC

q(n)

Q-DWA

5bit
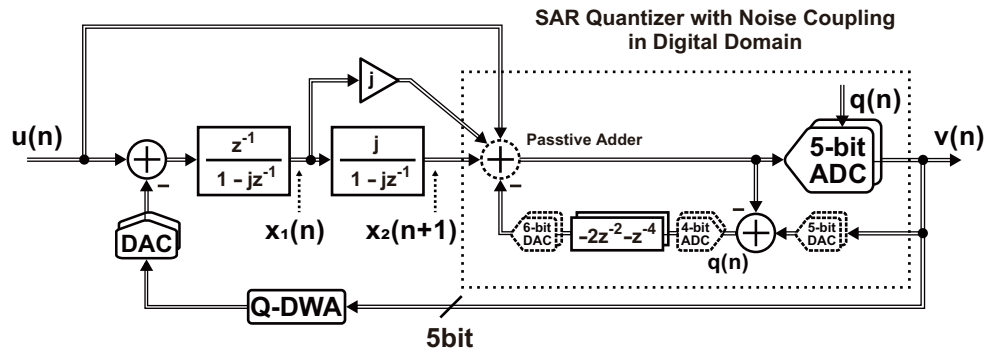
Transfer function : $V(z)=U(z)+(1-jz^{-1})^4(1+jz^{-1})^2Q(z)$

(a)

Im

4th-Order Zero points   +j $f_{IR}=Fs/4$

$\omega=\pi/2$

-1   +1 **Re**

2nd-Order Zero points   -j $f_{IM}=3Fs/4$
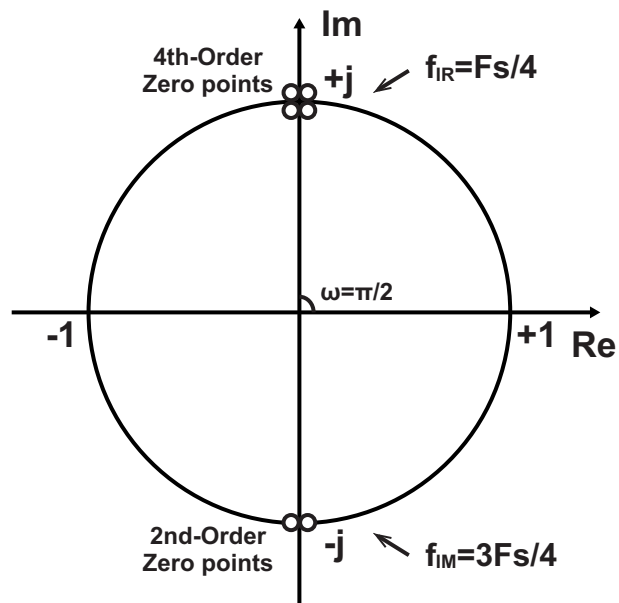
(b)

FIGURE 6.2: Block diagram of proposed 6th-order complex bandpass delta sigma modulator. (a) Signal flow diagram. (b) Zero points of noise transfer function.

6.2 Architecture

Figure 6.2(a) shows the block diagram of the proposed QBPDSM which can realize the transfer function of

$$V(z) = U(z) + (1 - jz^{-1})^4(1 + jz^{-1})^2 Q(z) \qquad (6.1)$$

where, V(z) is output signal, U(z) is input signal, Q(z) is quantization noise. The signal transfer function (STF) and noise transfer function (NTF) can be represented as

$$STF = 1 \qquad (6.2)$$

and

$$NTF = (1 - jz^{-1})^4(1 + jz^{-1})^2, \qquad (6.3)$$

respectively. It is consists of two complex integrators, two 5-bit DDNC SAR quantizers with passive adder, two DACs and a quadrature data-weighted-averaging (Q-DWA) logic. The proposed complex integrators using ring-amplifier are used to realize the 2nd-order noise shaping for reducing the circuit area and improving the energy efficiency of QBPDSM. The 5-bit passive adder embedded DDNC SAR quantizer is used to realize the summation of three analog input signals, quantization and noise shaping. The DDNC SAR quantizer is used not only as an internal quantizer, but also as a noise coupling circuit. As shown in figure 6.2(a), the quantization noise q(n) is converted to digital code by the internal 4-bit ADC, firstly. The digitized quantization noise q(n) is then processed by the digital filter with the transfer function of $-2z^{-2} - z^{-4}$. The output signal of the digital filter is finally coupled with the input signal of the DDNC SAR quantizer by the internal 6-bit DAC in the next period, so that, the FIR filtered quantization noise $(-2z^{-2} - z^{-4})q(n)$ is re-injected to the QBPDSM, which realize an addition 2nd-order noise shaping and 2nd-order image rejection. As a results, the proposed QBPDSM realizes 4th-order noise shaping and 2nd-order image rejection by using two complex integrators and the DDNC SAR quantizer as the figure 6.2(b). The zero points of proposed QBPDSM's noise transfer function ($z_1 = z_2 = z_3 = z_4 = +j$ and $z_5 = z_6 = -j$) are designed at the

signal center frequency f_{IR} = Fs/4 and the image frequency f_{IM} = 3Fs/4, respectively. The noise caused by the mismatch of I, Q-paths in image frequency band is attenuated, so that, the noise reflected from image frequency band to desired signal band is suppressed, which can maintain the high SNDR for the proposed QBPDSM. Moreover, the passive capacitor array instead of the active adder with a power hungry amplifier realizes the summation of analog signals in the front of DDNC SAR quantizer. Above techniques are conducted to improve the energy efficiency and to reduce the area of the proposed QBPDSM. The Quadrature-DWA circuit is also provided to the QBPDSM for suppressing the influence of DAC mismatch.

6.3   Implementation

Figure 6.3 illustrates the schematic diagram of the proposed 6th-order QBPDSM with two ring-amplifier based complex integrators and two passive adder embedded 5-bit DDNC SAR quantizers. Its clock timing chart and operation mode diagram are shown in figure 6.4(a) and figure 6.4(b), respectively. The proposed QBPDSM operates at 3 phases. During the phase Φ_1, the 1st-integrator performs the integration operation, the 2nd-integrator performs the sampling operation while the inside ring-amplifier is reset, and the output signals of 1st-integrator are sampled on the capacitors of the DDNC SAR quantizer. In addition, in the phase Φ_1, the digitized quantization noise of the previous period is also digital processed by the 4th-order FIR filter included in the DDNC SAR quantizer. During the phase Φ_2, the input signal of QBPDSM is sampled on the sampling capacitors of 1st-integrator and the DDNC SAR quantizer meanwhile, because the active part of 1st-integrator is idle, its power is cut off for maintaining the high energy efficiency. The 2nd-integrator performs the integration operation in the phase Φ_2, and the digital processed quantization noise is coupled to the QBPDSM at the same time for achieving the additional 2nd-order noise shaping and 2nd-order image rejection. During the phase Φ_3, the 1st-integrator is reset for the integration of the next period, the active part of 2nd-integrator is idle, so that its power is cut off, when the summation of 3 input analog signals is finished by the passive capacitor array, the DDNC SAR quantizer carry out
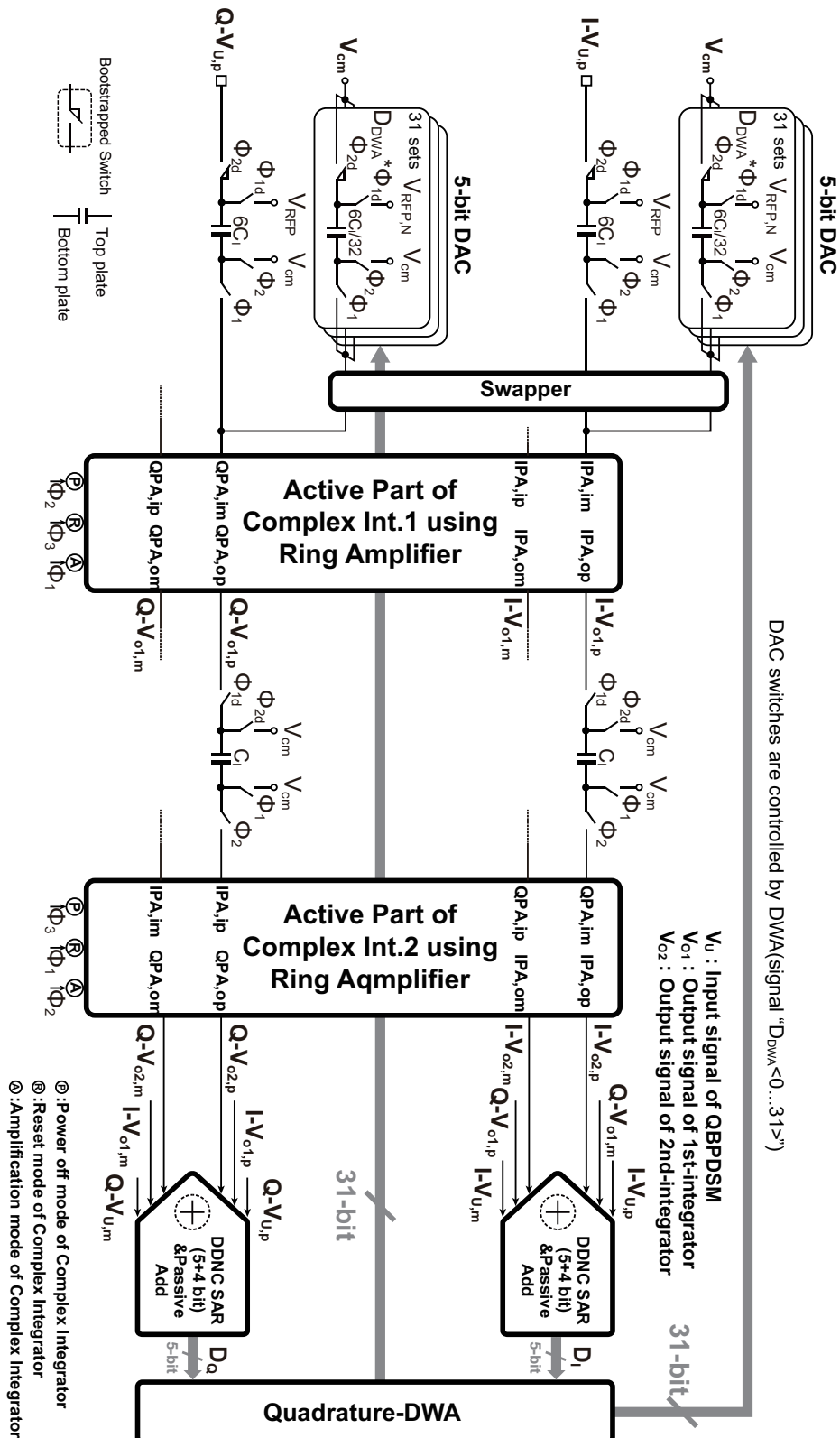
FIGURE 6.3: Schematic diagram of the proposed 6th-Order Complex Bandpass Delta Sigma AD Modulator with Image Rejection Using Dynamic Amplifier and SAR Quantizer.

(a)

Phase	Φ_1	Φ_2	Φ_3
Int.1	Integration	Sample & AMP OFF	Reset
Int.2	Reset & Sample	Integration	AMP OFF
SAR	Sample(V_{o1})&DP	Sample(V_U&V_{o2})&NC	SUM / 9-bit AD Convertion / DWA
DATA			D8 D7 … … D1 D0

(b)
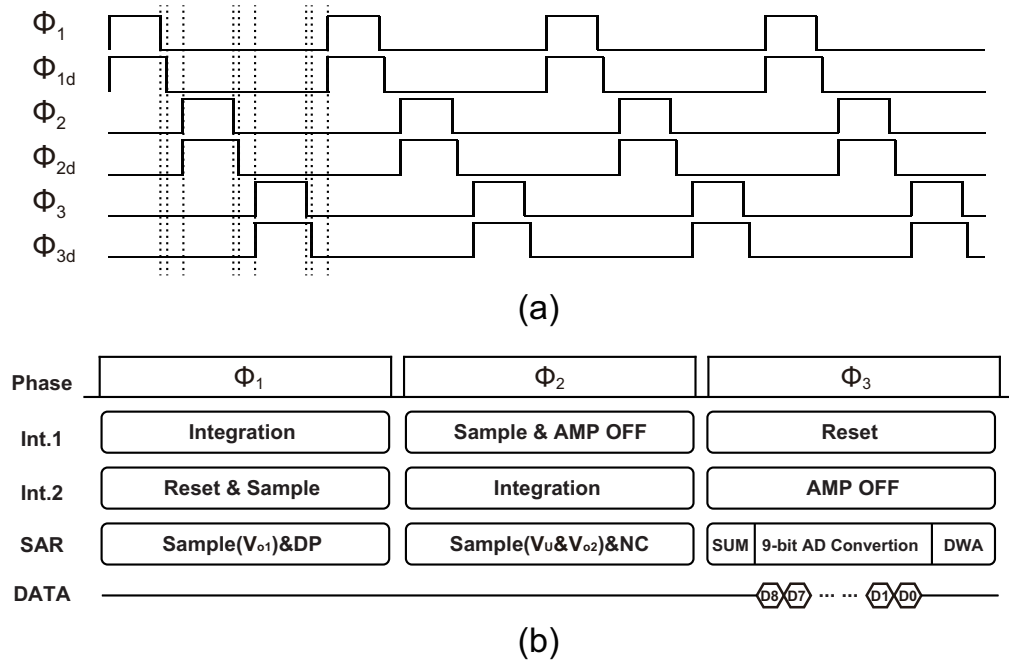
FIGURE 6.4: Clock timing chart of the proposed 6th-Order Complex Bandpass Delta Sigma AD Modulator with Image Rejection Using Dynamic Amplifier and SAR Quantizer. (a) Clock timing chart. (b) Operation mode diagram.

$X_R(z)+jX_I(z)$ → $\dfrac{z^{-1}}{1-(d+jc)z^{-1}}$ → $Y_R(z)+jY_I(z)$

(a)

(b)
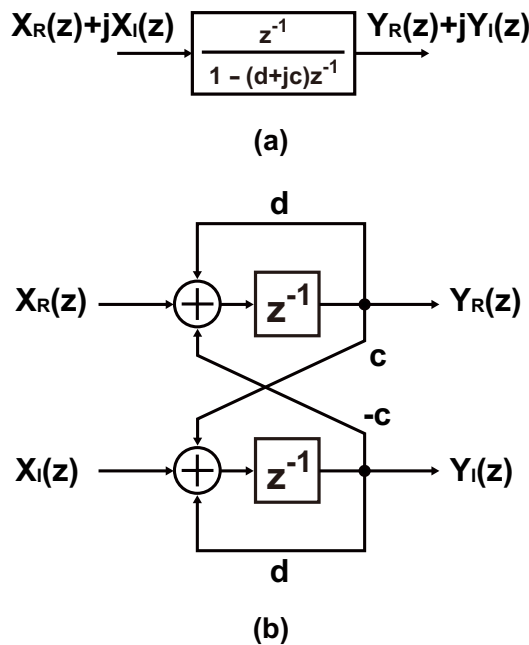
FIGURE 6.5: Block diagram of complex integrator. (a) Block diagram represented by transmission function. (b) Block diagram represented by delay.
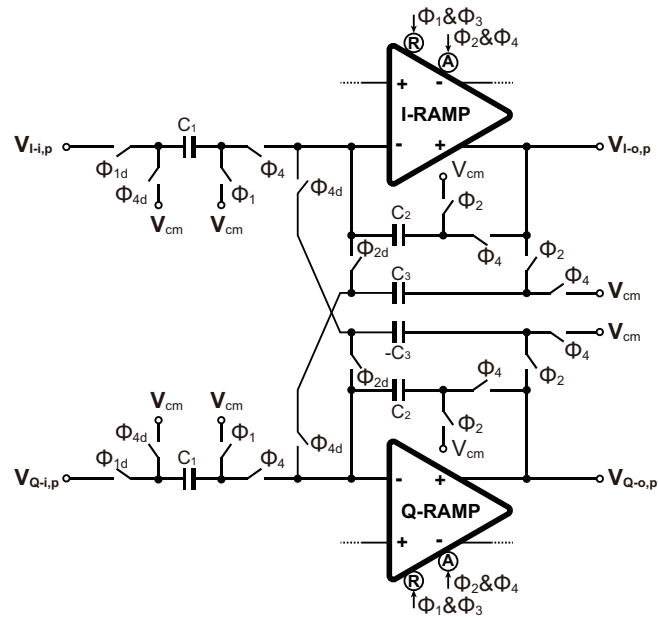
FIGURE 6.6: Schematic diagram of traditional complex integrator.

the 9-bit AD conversion which include the 5-bit digital output signal and the 4-bit quantization noise.

In the proposed QBPDSM, the input signal of the QBPDSM and the output signal of 1st-integrator are fed to the DDNC SAR quantizer, which form the delta sigma modulator with the feed-forward architecture, hence, the signal input to the loop filter contains only the shaped quantization noise, the requirement of the slew-rate on the ring-amplifier can be relaxed, and the effect of amplifier's non-linearity can be reduced for the higher SNDR [3]. The proposed complex integrator using ring-amplifier shown in figure 6.7 can realize the complex integration by one phase, and it does not require the extra capacitors (C_3s shown in figure 6.6) for realizing the multiplication operation of the complex constant *j*, which is different from the conventional complex integrator. Therefore, not only the operation speed can be improved, but the circuit area can also be reduced. Moreover, the ring-amplifier can realize higher gain than the traditional amplifier at the low supply voltage, and the static current of the ring-amplifier is very small, so that it is suitable to achieve the QBPDSM with high energy efficiency. The 5-bit internal quantizer is realized by the SAR quantizer with digital domain noise coupling. It not only can improve the stability of the 6th-order QBPDSM, but also relax the requirement on the slew-rate of amplifier in the complex integrator. Furthermore, the DDNC SAR quantizer can also couple the quantization noise of

$$(-2z^{-2} - z^{-4})q(n) \tag{6.4}$$

shaped by digital signal process circuit for realizing an addition 2nd-order noise shaping and 2nd-order image rejection. The summation of 3 input signals (V_U, V_{o1} and V_{o2}) is realized by reconstituting the capacitor array of the DDNC SAR quantizer, thus, the analog adder with amplifier is not required. Two 5-bit capacitive DACs with the unit element shown in figure 6.3(a) are used for the feedback of the complex digital output signal of the QBPDSM. It is well known that the non-linearity caused by the capacitor mismatches of multi-bit DAC appears as the harmonic distortion which affect the SNDR of the QBPDSM. The Quadrature-DWA logic circuit [5] is used for reducing the influence of the DAC's non-linearity.

6.3.1 Proposed Complex Integrator Circuit

Figure 6.5(a) illustrates the block diagram of the complex integrator, it can also be represented by the delay circuit as shown in figure 6.5(b). The schematic diagram and the operation phase diagram of traditional complex integrator using OTA are shown in figure 6.6(a). The input signal is sampled on the capacitor C_1 during the phase Φ_1, and the charge stored on C_2 is transferred to C_3 at the same time. During the phase Φ_2, the summation of the charge on C_1 and C_3 is transferred to C_2 that achieve once complex integration operation. However, the amplifiers in the traditional complex integration circuit require to perform twice amplification actions for realizing once complex integration. Hence, two phases are required for performing once complex integration operation, which accompany the low power efficiency and the limited operation speed. In the traditional complex integrator using ring-amplifier circuit, the above defects will become worse. Due to the ring-amplifier requires the extra phase for the reset operation, four phases are required for performing once complex integration operation as shown in figure 6.6(b).

For solving the above problems, in this work, a novel implementation of the complex integrator using ring-amplifier is proposed as shown in figure 6.7(a). It is consists of the sampling circuit and the active part with ring-amplifier. The proposed complex integrator ($C_1 + C_2 + C_3 + C_4 = 4C$ in figure 6.7(a)) use the fewer capacitors compare with the traditional complex integrator ($(C_2 \times 2 + C_3 \times 2) \times 2(\text{differential circuit}) = 8C$ in figure6.6) to achieve the integration operation of the complex signal, and only one amplification action is required for once complex integration. Thereby, the energy efficiency can be improved and the area of circuit can be reduced. Figure 6.7(c) shows the control signals of the active part, they are generated by the switching controller circuit shown in figure 6.7(b). By controlling the switches of the active part, the four kinds of states for the proposed complex integrator can be realized.

Figure 6.8 illustrates the equivalent circuits of complex integrator circuit in four kinds of the operation states. In the state-1, C_1, C_2 and C_3, C_4 are connected to the I-Path AMP and Q-Path AMP during Φ_A. When the integration operation is finished, the signals input to I-Path and Q-Path are stored on C_1, C_2 and C_3, C_4, respectively,
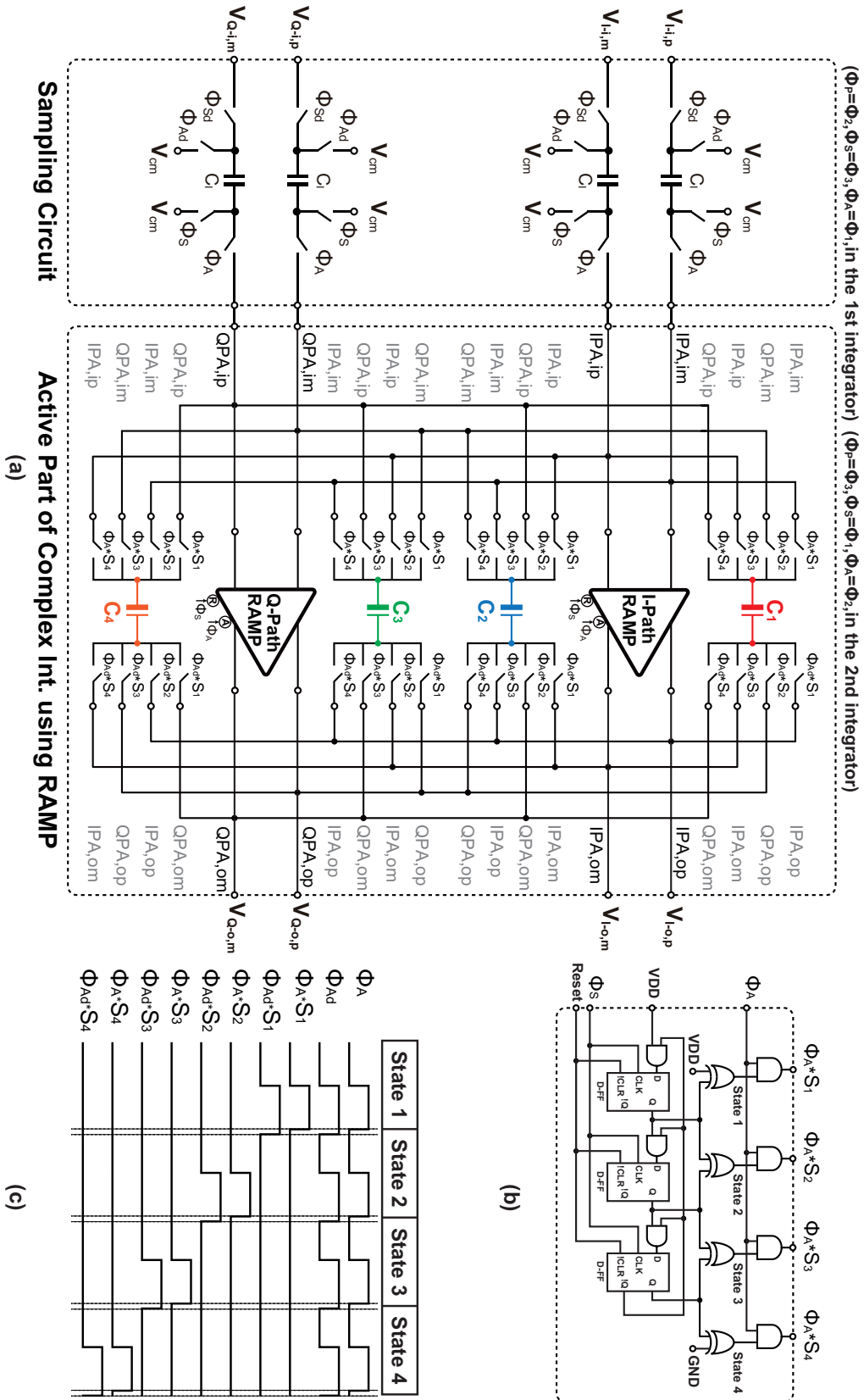
FIGURE 6.7: Circuit implementation of the proposed complex integrator. (a) Circuit schematic diagram. (b) Switching controller circuit. (c) Control signals of switches.
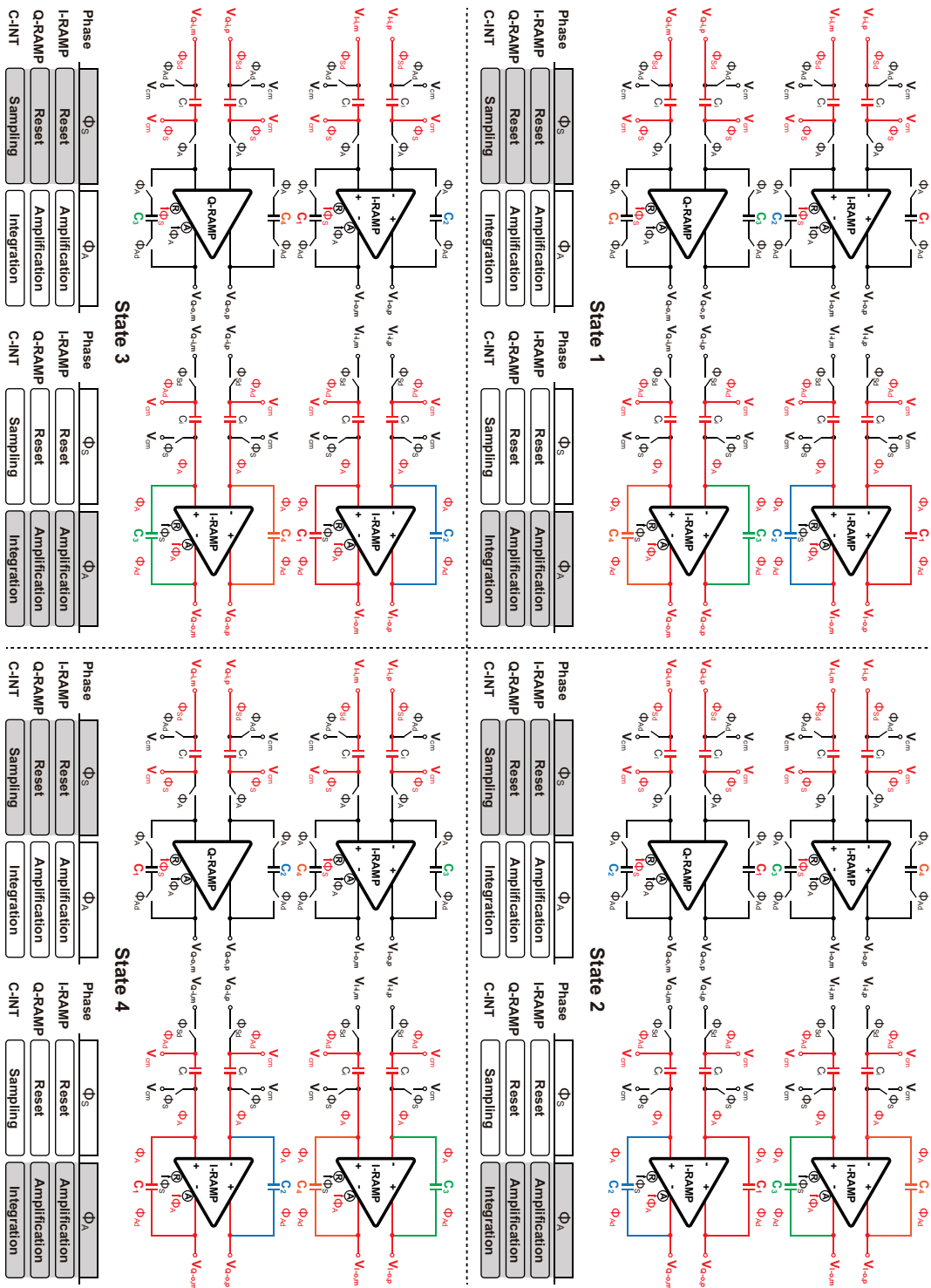
FIGURE 6.8: Equivalent circuits of the proposed complex integrator in the four kinds of state.

as the state-1 shown in figure 6.8. In the next operation period, the complex integrator circuit become to state-2 by controlling the switches of active part. In the Q-Path channel, C_1 and C_2 are connected to the Q-Path AMP (they are connected to the I-Path AMP in the previous period), hence the signal input to I-Path in previous period (they are stored on C_1 and C_2 now) is added with the signal input to Q-Path in the current period. The result of summation is stored on the C_1 and C_2, which realize the additive operation from I-Path to Q-Path in figure 6.5(b). In the I-Path channel, the swapped C_3 and C_4 are connected to the I-Path AMP, so that the negative signal input to Q-Path in the previous period is added with the signal input to I-Path in the current period, the result of summation is stored on the C_3 and C_4 as the state-2 shown in figure 6.8, which realize the subtraction operation from Q-Path to I-Path in figure 6.5(b). As a results, the proposed complex integration circuit can realize the integration operation of complex signal by switching among four kinds of states continuously. It's different from a traditional complex integrator that only one amplification phase is required for achieving the complex integration operation, and the proposed complex integrator use the fewer capacitors than the traditional complex integrator shown in figure 6.6. Therefore, not only the high energy efficiency can be maintained, but the speed limit of QBPDSM can also be relaxed. Moreover, the use of the dynamic amplifier (ring-amplifier) instead of the OTA is used to achieve the maximum power-efficiency of the amplifier in the proposed complex integrator circuit.

6.3.2   Pseudo Differential Ring Amplifier with Energy Saving

In this work, for maximizing the energy-efficiency of the proposed QBPDSM, we use the pseudo differential ring-amplifier to realize the complex integrator. The pseudo differential ring-amplifier is shown in figure 6.9. Its core circuit is consist of three inverters in series as shown in figure 6.10. Capacitors (C_C) are added to the input nodes of amplifier for saving the operation point of ring-amplifier. In the previous works [6] and [7], the common feedback circuit (CMFB) of pseudo differential ring-amplifier is consist of the capacitors C_{cm1}s and C_{cm2}s as shown in figure 6.9(a). C_{cm1}s are used for the detection of the output common voltage, C_{cm2}s are used for the

Φ_R :**Reset mode of R-AMP**
Φ_A :**Amplification mode of R-AMP**

(a)

Φ_P : **Power off mode of R-AMP**
Φ_R : **Reset mode of R-AMP**
Φ_A : **Amplification mode of R-AMP**
($\Phi_P=\Phi_2,\Phi_R=\Phi_3,\Phi_A=\Phi_1$,in the 1st integrator)
($\Phi_P=\Phi_3,\Phi_R=\Phi_1,\Phi_A=\Phi_2$,in the 2nd integrator)
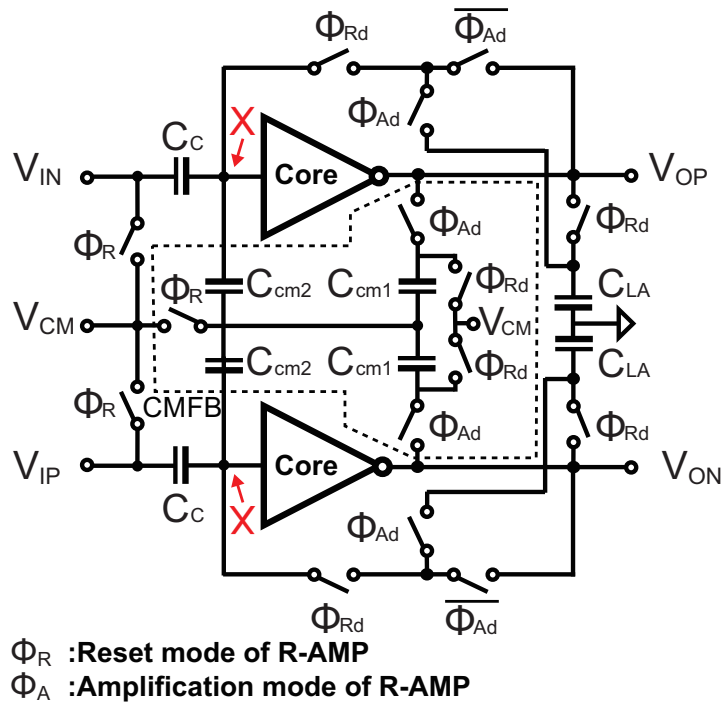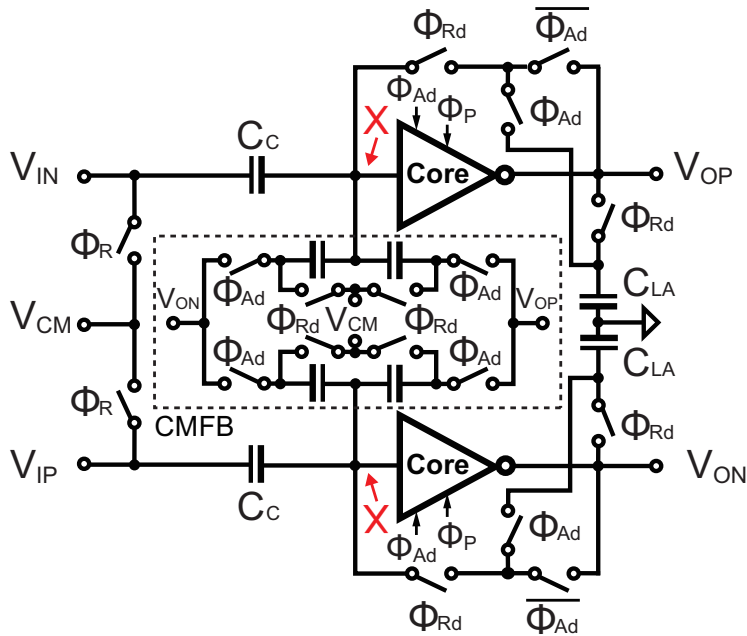
(b)

FIGURE 6.9: Schematic of pseudo differential RAMP (Ring-Amplifier). (a) RAMP proposed in previous work. (b) RAMP proposed in this work.

FIGURE 6.10: Schematic of RAMP's core circuit.

feedback of the common voltage. Due to the C_C and C_{cm2} in series, the common voltage fed to the node "X" in fount of core circuit can be represent as

$$V_{X\_common} = \frac{C_{cm2}}{C_{cm2} + C_C} \times V_{detected\_common},$$ (6.5)

where $V_{detected\_common}$ is the common voltage detected at the output of ring-amplifier. Equation 6.5 means that the voltage division from the C_C and C_{cm2} causes the reduction of common mode rejection ratio (CMRR). This paper proposed the modified CMFB circuit as shown in figure 6.9(b). Because the modified CMFB circuit does not include the capacitors in series, it can feed directly the common mode signal detected at the output port of the ring-amplifier to the input port of the core circuit for obtaining the maximum CMRR. In the modified CMFB circuit, The detected common voltage is fed to node "X" (the input port of the core circuit), rather than is fed to input port of the ring-amplifier (V_{IN} and V_{IP}) as shown in figure 6.9(b), which can avoid that the virtual ground (input port of ring-amplifier) is affect by the common feedback circuit as same as the previous work [8]. When the feedback loop is formed in the input and output of ring-amplifier (eg. in amplification phase or reset phase), the voltage at the gate of the MOSFET M_{P1} and M_{N1} turns to V_{cm} during the steady state of the ring-amplifier. Thus, M_{P1} and M_{N1} operate in the weak inversion region at this time, which can achieve the high DC-gain with a very low static current as
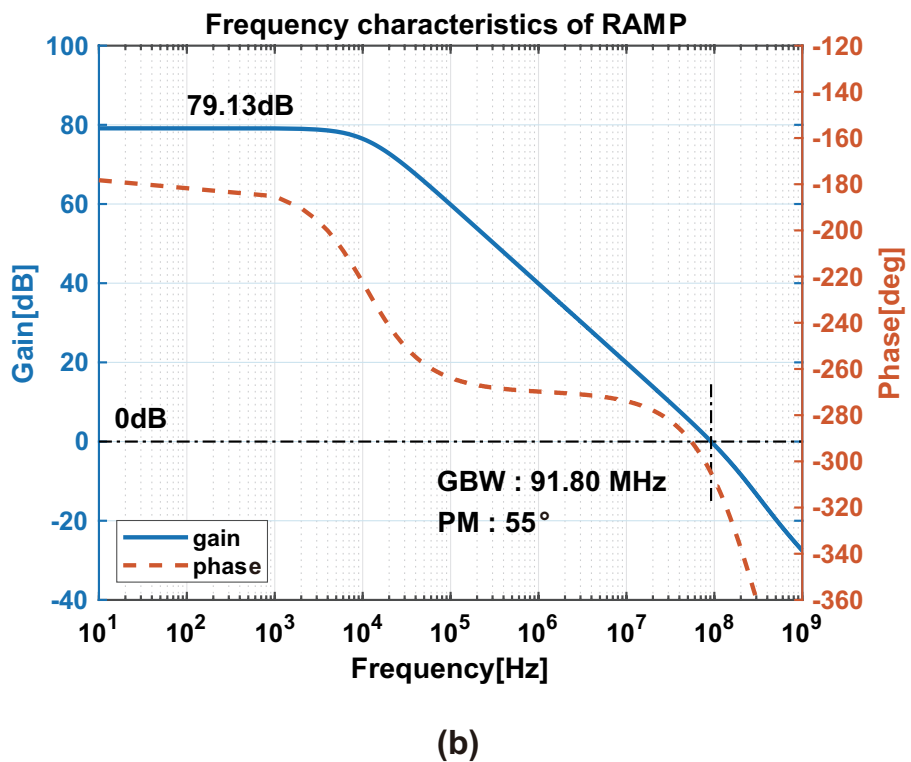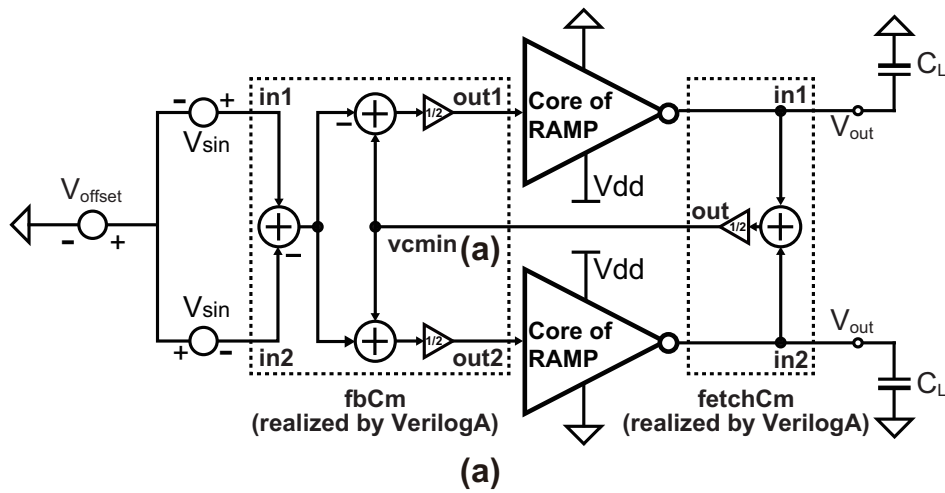
FIGURE 6.11: AC analysis of RAMP (a) Simulation circuit. (b) Frequency characteristics RAMP.

same as the class-AB amplifier. The transmission gate which used as a resistor is inserted at the output port of the 2nd-stage inverter, it can compress the drain-source voltages of M_{P2} and M_{N2} to the boundary between the weak and strong inversion regions for obtaining both wide GB bandwidth and high gain [9]. Moreover, it also establishes the different bias voltages at the gates of M_{P3} and M_{N3} to make the gate-source voltage lower than threshold voltage during the steady state. Therefore, the M_{P3} and M_{N3} behaves as push-pull structure which similar to a class-C amplifier for enhancing the slew-rate. In addition, by controlling the gate voltage of the transmission gate, the current of ring-amplifier's core can be broken in the idle time to maximize the energy efficiency of QBPDSM.

In order to confirm the performance of ring-amplifier, the SPICE simulation of AC analysis using the circuit shown in figure 6.11(a) is introduced. In the simulation circuit, the common feedback circuits "fbCm" and "fetchCm" are realized by Verilog-A program for obtaining the pure gain of ring-amplifier's core B. The simulation results shown in figure 6.11(b) show that the ring-amplifier has DC-gain of 79 dB with $55°$ phase margin and Unity-gain bandwidth of 91.8 MHz.

6.3.3   Noise Coupling SAR Quantizer

The block diagram and schematic diagram of the passive adder embedded noise coupling SAR quantizer are shown in figure 6.12(a) and figure 6.12(b), respectively. It consists of digital process circuit, capacitive DAC, a strong-ARM structure comparator (figure 6.13) and asynchronous SAR logic circuits. The clock timing chart is represented in figure 6.12(c). Figure 6.14(a)$\sim$(d) show the equivalent circuit of the DDNC SAR quantizer at four kinds of operation mode. In the sampling & digital process mode (Φ_1), the bottom plate of one capacitor among the DDNC SAR quantizer (512C) is connected to the output of the 1st integrator (V_{o1}). Meanwhile, the 4-bit digitized quantization noise is digital processed ($-2z^{-2} - z^{-4}$) as shown in figure 6.14(a). In the sampling & noise coupling mode (Φ_2), the bottom plate of another one capacitor among the DDNC SAR quantizer (512C) is connected to the input of the QBPDSM (V_U). The bottom plates of DDNC SAR quantizer's capacitors (512C) are connected to the output of the 2nd integrator (V_{o2}), the top plates
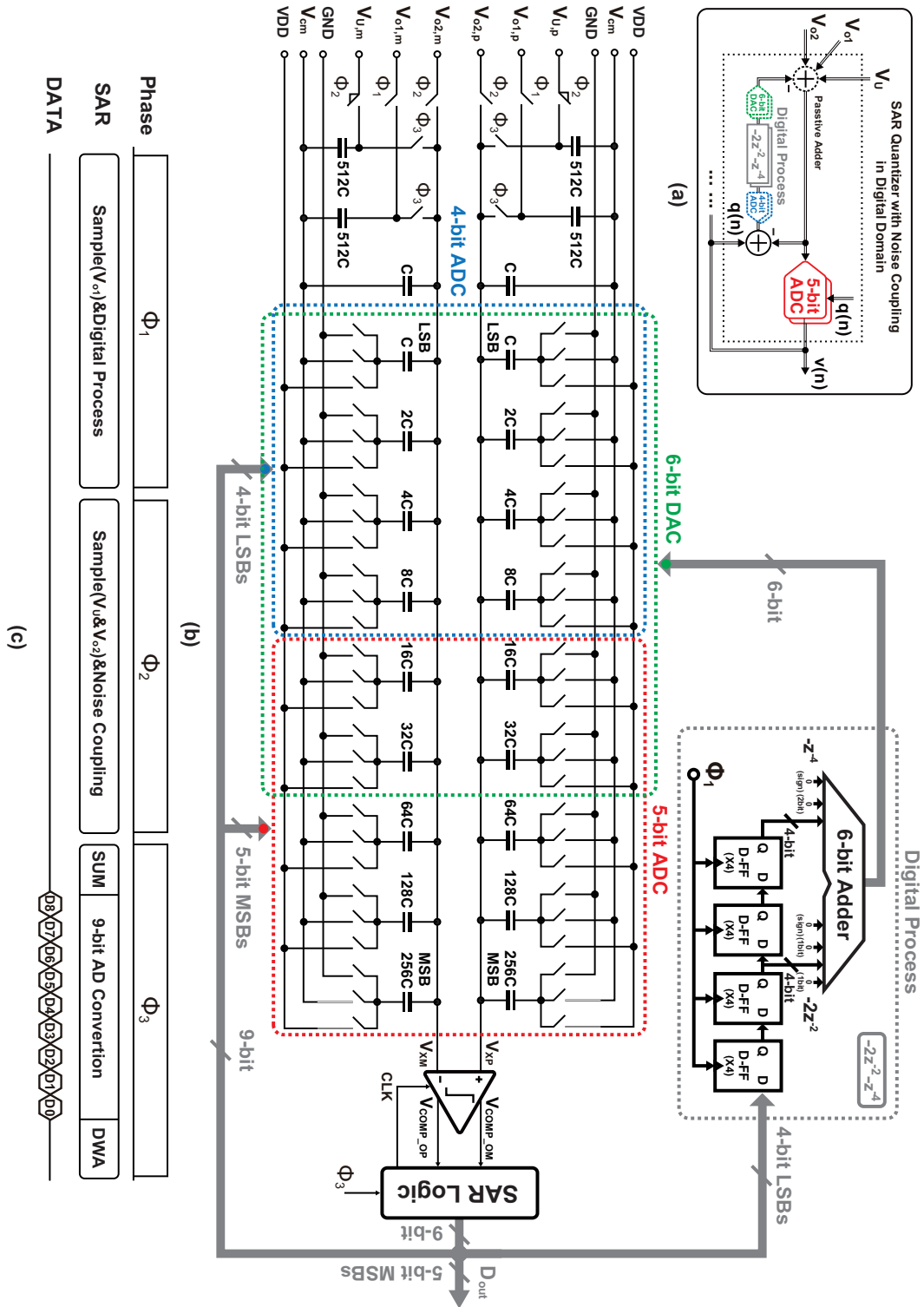
FIGURE 6.12: Circuit implementation of proposed adder embedded SAR Quantizer with noise coupling in digital domain. (a) Block diagram. (b) Schematic diagram. (c) Clock timing chart.
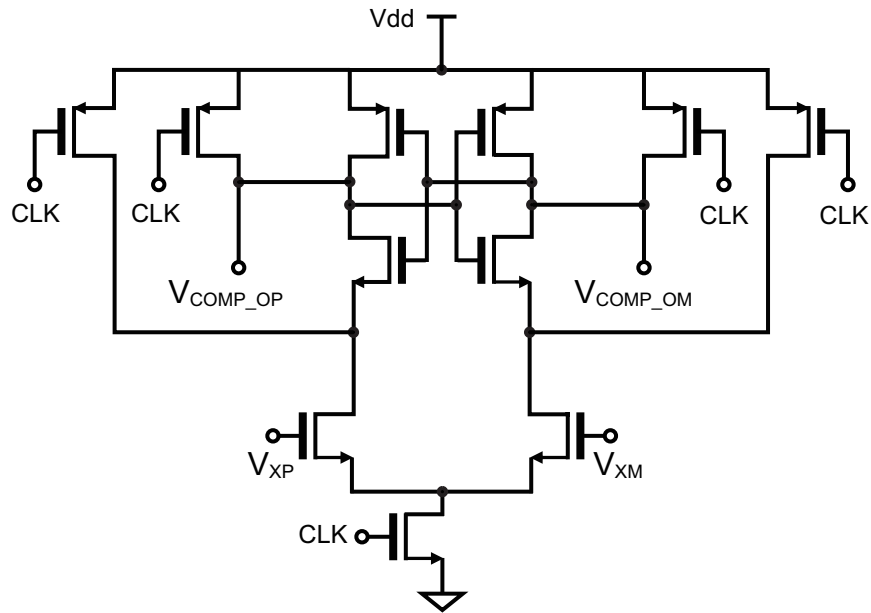
FIGURE 6.13: Schematic diagram of dynamic comparator used in
SAR quantizer.

of the 6-bit LSB capacitors for 6-bit DAC are connected to the reference voltage
according to the output of the digital process circuit at the same time as shown
in figure 6.14(b). Therefore, the shaped noise quantization $(-2z^{-2} - z^{-4})q(n)$ is
coupled to the QBPDSM that can realize an addition 2nd-order noise shaping and
2nd-order image rejection. Moreover, because the capacitor ratio for three input
signals is 1:1:1, the total charge stored on the capacitor Q_S can be expressed as
$Q_S = 512C \times V_U + 512C \times V_{o1} + 512C \times V_{o2}$. In the summation mode Φ_3, the top
plates of three sampled capacitors are connected to the input node of comparator
(V_X) as shown in figure 6.14(c). Because the total capacitance at the node V_X is 1536C,
the total charge Q_C of this summation mode on capacitors is $Q_C = 1536C \times V_X$. Ac-
cording to the charge-conservation law, we have $Q_C = Q_S$. Then, we get equation
$V_X = Q_S/(1536C) = (V_U + V_{o1} + V_{o2})/3$, that means the summation of three in-
put signals can be realized by capacitor array. After the analog input summation
is finished, the AD conversion is carried out from MSB to LSB in the successive ap-
proximation manner as shown in figure 6.14(d). Asynchronous SAR logic circuits are
used to control the capacitor DAC of DDNC SAR quantizer. As the result, the DDNC
SAR quantizer not only realize 5-bit quantization but also realize an addition 2nd-
order noise shaping and 2nd-order image rejection. Moreover, it is not requite using
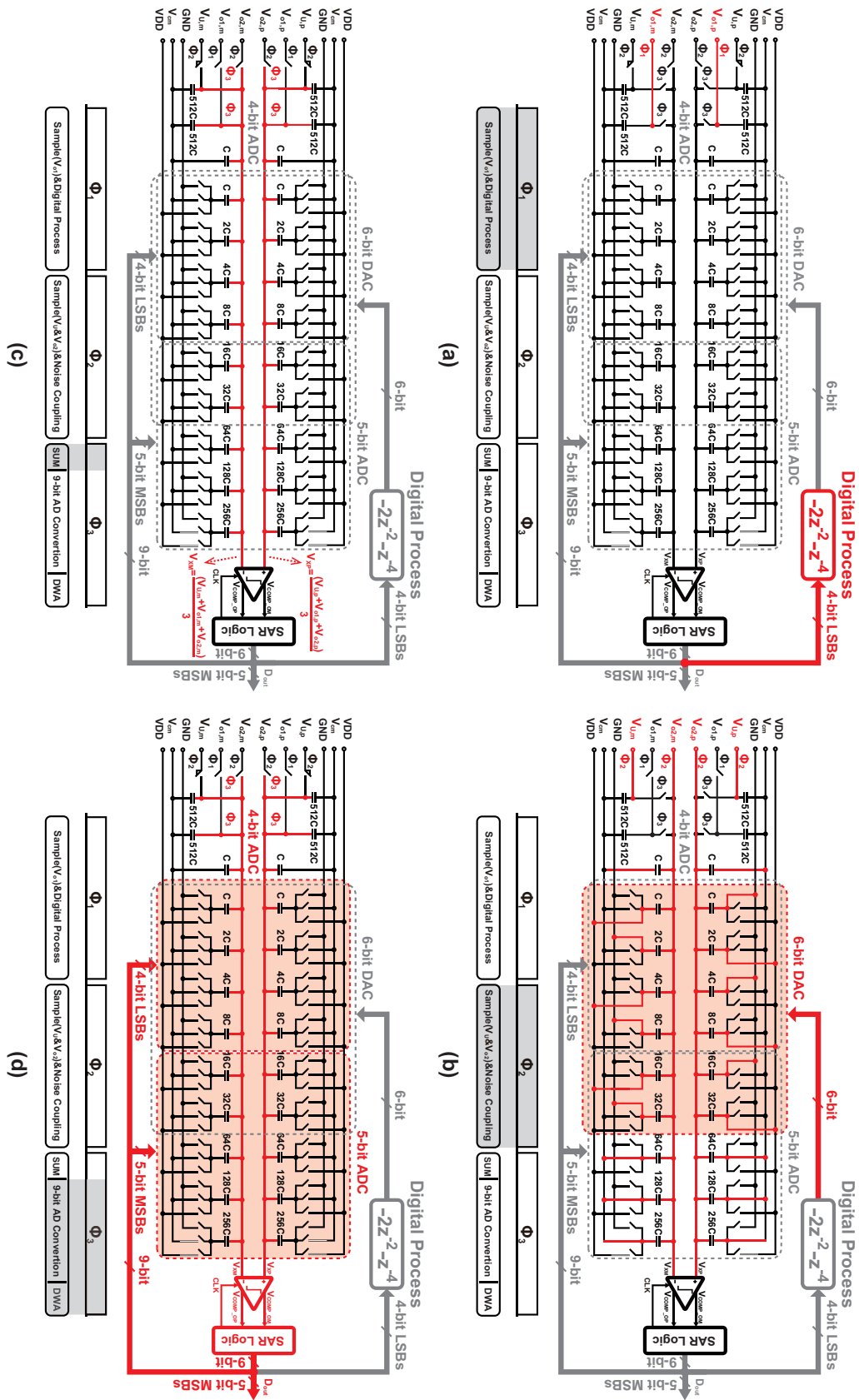
FIGURE 6.14: Equivalent circuits of proposed adder embedded SAR Quantizer with noise coupling in digital domain. (a) Sampling & digital process mode. (b) Sampling & noise coupling mode. (c) Summation mode. (d) Successive approximation mode.

the active analog component, the lower power consumption can be maintained.

6.3.4 Multi-bit DAC and Quadrature-DWA Logic
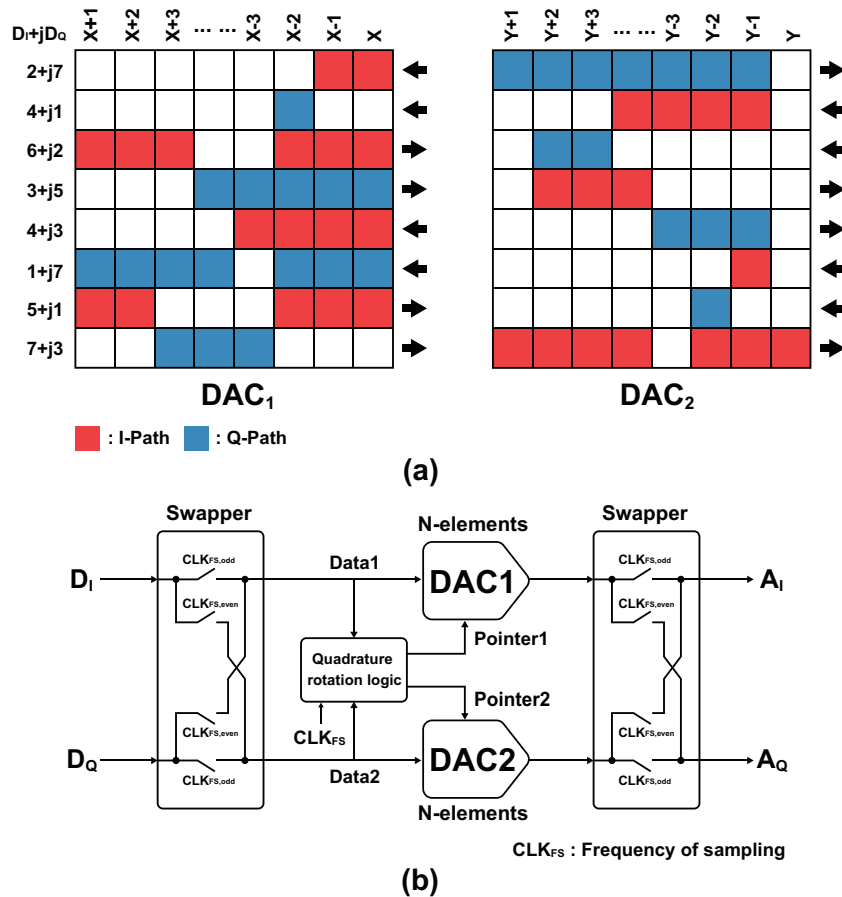
FIGURE 6.15: Quadrature DWA logic. (a) Quadrature element rotation algorithm. (b) An implementation of the Q-DWA logic.

Two 5-bit capacitor DACs are used for the 1st complex integrator as shown in figure 6.3(a), the mismatches among the unit elements in a multi-bit DAC cause the harmonic distortion in the signal band, the quadrature DWA logic circuit [5] is applied to the QBPDSM to reduce the influence of DAC non-linearity errors. The quadrature element rotation algorithm and an implementation of the Q-DWA logic are shown in the figure 6.15(a) and (b), respectively.
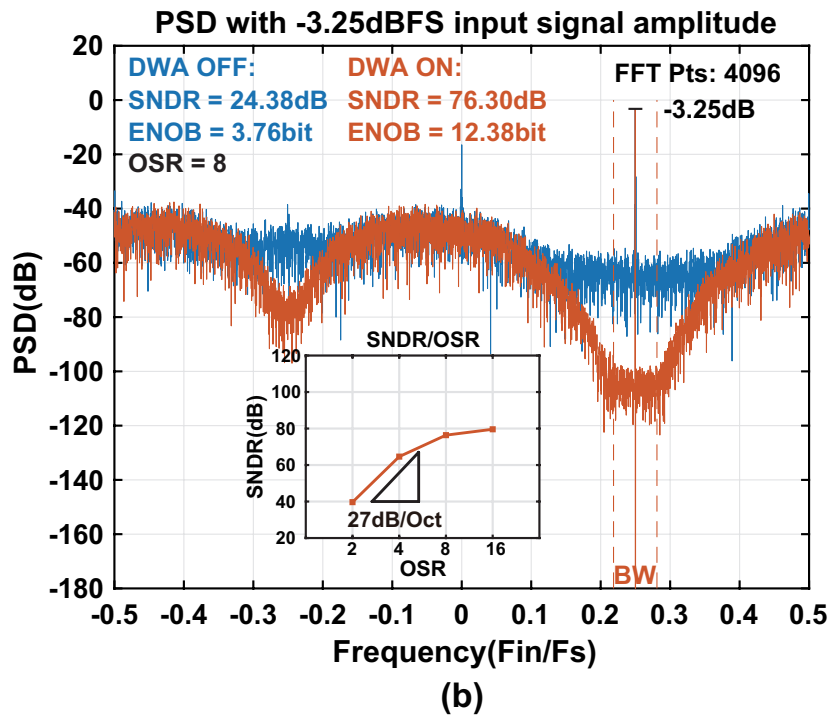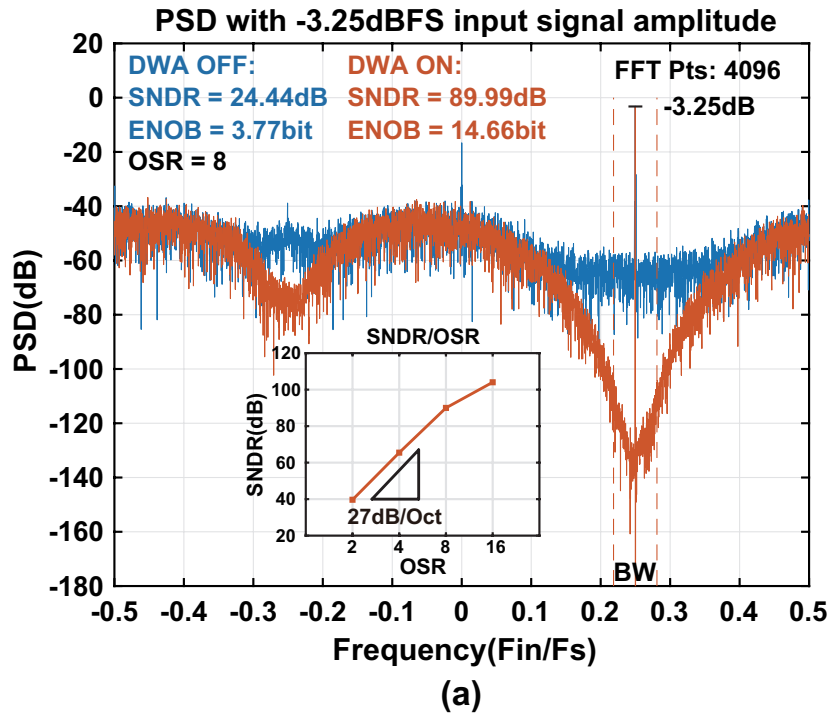
FIGURE 6.16: Simulated output spectrum with ≤1% unit-capacitance mismatches of DAC for single tone (f_{in} ≈8.33 MHz with the input signal amplitude of -3.25 dBFS). (a) without thermal noise and flicker noise. (b) with thermal noise and flicker noise.
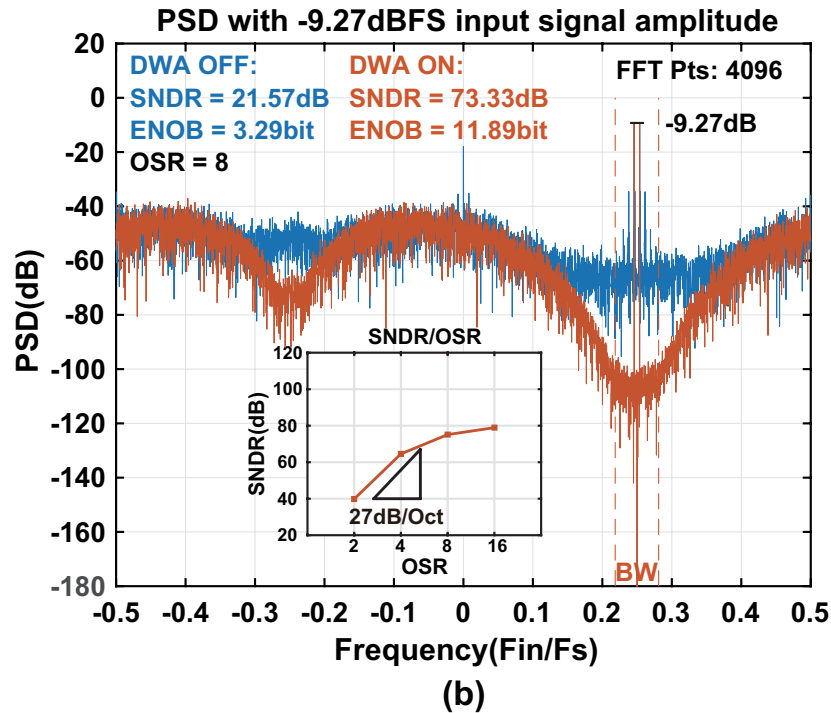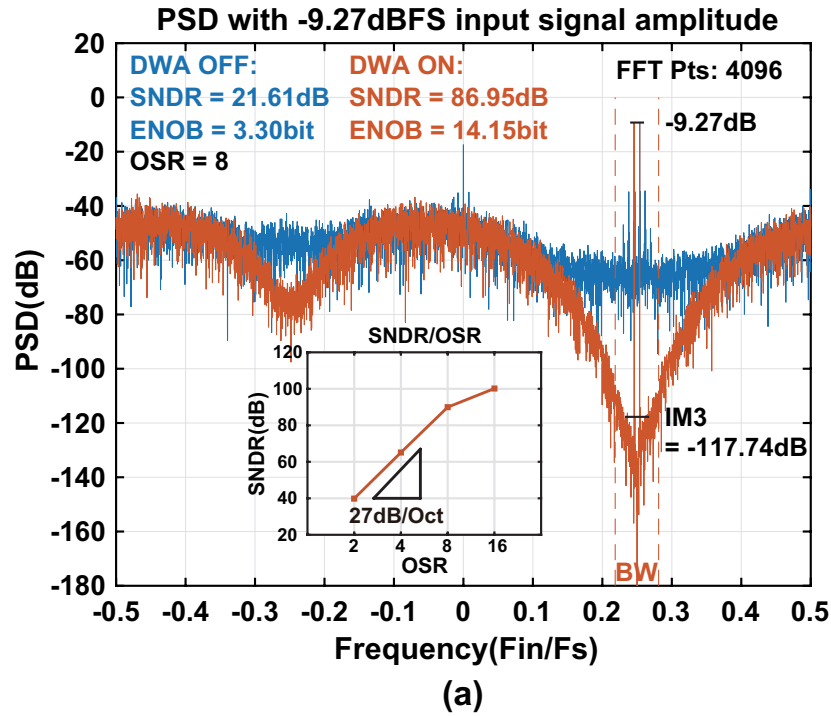
FIGURE 6.17: Simulated output spectrum with $\leq 1\%$ unit-capacitance mismatches of DAC for double tone ($f_{in1} \approx 8.19$ MHz and $f_{in2} \approx 8.45$ MHz with the input signal amplitude of -9.27 dBFS). (a) without thermal noise and flicker noise. (b) with thermal noise and flicker noise.

6.4 Simulation

The proposed 6th-order QBPDSM is designed in TSMC 90nm CMOS technology. It operates at a clock rate of 33.3 MHz for a 2.083 MHz BW with an OSR of 8, and power consumption 6.74 mW under the supply voltage of 1.2 V for both analog circuit part and digital circuit part. Transistor-level SPICE simulations have been conducted to confirm the performance of the QBPDSM and to verify the effectiveness of the proposed architecture. The simulated spectrum results including single tone input signal (8.33 MHz with the amplitude of -3.25 dBFS), double tone input signals (8.19 MHz and 8.45 MHz with the amplitude of -9.27 dBFS) and the SNDR of the proposed QBPDSM are shown in figure 6.16 and figure 6.17. Figure 6.16(a) shows the simulated spectrum results without the thermal noise and the flicker noise. When the DWA circuit is disable, only SNDR of 24.44 dB and ENOB of 3.77 bit are achieved. When the DWA is applied, the SNDR and ENOB are improved to 89.99 dB and of 14.66 bit, respectively. In order to show the performance which close to the realistic circuit as much as possible, the simulated output signal spectrum shown in figure 6.16(b) includes the thermal noise, the flicker noise, the effect of ≤1% unit-capacitance mismatches of DAC, and the effect of non-ideal characteristic of circuit (eg. amplifier and comparator). The noise power and the non-ideal characteristic of transistor are calculated by simulator according to the transistor model of CMOS technology. In the simulation parameters, the maximum noise frequency is set as 100 MHz, it controls the bandwidth of energy which is emitted by the each noise source in the QBPDSM circuit. The minimum noise frequency is set as 10 KHz, it is used to establish the lower frequency bound on flicker noise modeling [10]. As shown in figure 6.16(b), When the DWA is disable, the peak SNDR of 24.38 dB and ENOB of 3.76 bit are achieved. When the DWA is applied, the SNDR and ENOB are improved to 76.30 dB and 12.38 bit, respectively. The simulated spectrum results shown in both of figure 6.16(a) and (b) also considered the affect of ≤1% unit-capacitance random mismatches of DAC. Moreover, figure 6.17(a) and (b) shown the simulated spectrum results with double tone input signal, the IM3 of -117.74 dB is achieved when the thermal noise and the flicker noise is considered, which indicate that the distortion

TABLE 6.1: Performance summary and comparison with previous works

Specification	[11]	[12]	[13]	[14]	[15]	This work	
Technology(nm)	65	65	180	180	180	90	
Architecture	CT-4th	CT-2nd	CT-2nd	CT-4th	DT-2nd	DT-6th	
Supply voltage(V)	1.25	1.2	1.8	3.3	1.8	1.2	
Sampling rate (MS/s)	800	160	120	264	60	33.3	
OSR	16.7	16	12	15.5	30	8	
Signal BW (MHz)	24	5	5	8.5	1	2.083	
SNDR (dB)	58	65.9	61.2	77	65.1	89.99(N)	76.30(T)
Power (mW)	12	4.2	8.9	375	16	6.74	
FOMW (pJ/conv.-step)	0.385	0.261	0.949	3.805	5.441	0.06(N)	0.303(T)
FOMS (dB)	151	157	149	151	143	174.9(N)	161.2(T)

CT : Continuous time, DT : Discrete time
N : Without thermal noise and flicker noise
T : With thermal noise and flicker noise
$\text{FOMW} = \text{Power}/(2 \times \text{BW} \times 2^{(\text{SNDR}-1.76)/6.02})$
$\text{FOMS} = \text{SNDR} + 10 \times \log_{10}(\text{BW}/\text{Power})$

of proposed QBPDSM is acceptable. The performance of the QBPDSM is summarized in Table 6.1 in comparison with the previous works. The calculated FOMW and FOMS are 0.303 pJ/conversion-step and 161.2 dB respectively. Compared with the other works which have the similar signal bandwidth, the simulation results show that the proposed QBPDSM has an better energy efficiency (FOM). Although the noise and the non-ideal characteristic of circuit are considered in the simulation results, it is not the measurement the actual chip, the SNDR and FOM of the prototype modulator should be degraded from the SPICE simulation results. However, the operation speed and the signal bandwidth often meet the comparable value to the SPICE simulation results.

6.5   Summary

A 6th-order quadrature bandpass delta sigma AD modulator using dynamic amplifier and digital domain noise coupling SAR quantizer has been designed in 90 nm CMOS technology. A novel complex integrator circuit using ring-amplifier is proposed to improve the energy efficiency and to reduce the area of circuit. The

proposed complex integrator only requires one amplification operation for the complex integration, so that the QBPDSM can operate at the high speed. Benefit from an additional 2nd-order noise shaping and the 2nd-order image rejection are realized by the digital domain noise coupling SAR quantizer, not only the bandwidth of the QBPDSM is extended, but also the influence of I,Q-path mismatch is reduced. Moreover, the digital signal process technique is used for the process of the quantization noise in the noise coupling SAR quantizer, the use of active analog component is not requited, thus the high energy efficiency is maintained. The simulation results show the feasibility of the proposed QBPDSM.

References

[1]   A. Jantzi, K.W. Martin, and A.S. Sedra. "Quadrature bandpass $\Delta\Sigma$ modulator for digital radio". In: *IEEE J. Solid-State Circuits* vol.32 (Dec. 1997), pp. 1935–1949 (cit. on pp. 117, 118).

[2]   R. Schreier and G. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004 (cit. on p. 117).

[3]   J. Silva et al. "Wideband lowdistortion delta-sigma ADC topology". In: *Electronics Letters* vol.37 (June 2001), pp. 737–738 (cit. on pp. 118, 126).

[4]   Jang et al. I. "A 4.2mW 10MHz BW 74.4dB SNDR Fourth-order CT DSM with Second-order Digital Noise Coupling Utilizing an 8b SAR ADC". In: *IEEE Symp. VLSI Circuits Dig. Tech.* (2017) (cit. on p. 119).

[5]   S. Kundu et al. "DAC mismatch shaping for quadrature sigma-delta data converters". In: *IEEE Int. Midwest Symp. Circuits Syst.* (2015), pp. 1–4 (cit. on pp. 126, 138).

[6]   B. Hershberg et al. "Ring amplifiers for switched capacitor circuits". In: *IEEE J. Solid State Circuits* vol.47 (Dec. 2012), pp. 2928–2942 (cit. on p. 130).

[7]   Y. Lim and M. Flynn. "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers". In: *IEEE ISSCC 2014 Dig of Tech* (Feb. 2014), pp. 202–203 (cit. on p. 130).

[8]   T. Christen. "A 15-bit 140-μW scalable-bandwidth inverter-based $\Delta\Sigma$ modulator for a MEMS microphone with digital output". In: *IEEE J. Solid-State Circuits* vol.48 (July 2013), pp. 1605–1614 (cit. on p. 132).

[9]   Y. Chae and G. Han. "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator". In: *IEEE J. Solid State Circuits* vol.44 (Feb. 2009), pp. 458–472 (cit. on p. 134).

[10]   Inc Synopsys. *HPISCE User Guide : Advanced Analog Simulation and Analysis*. Version M-2017.03-SP1, June 2017 (cit. on p. 141).

[11]   H. Chae et al. "A 12 mW low power continuous-time bandpass $\Delta\Sigma$ modulator with 58 dB SNDR and 24 MHz bandwidth at 200 MHz IF". In: *IEEE J. Solid-State Circuits* vol.49 (Feb. 2013), pp. 405–415 (cit. on p. 142).

[12]   Z. Zhang et al. "A 5/20 MHz-BW 4.2/8.1 mW CT QBP $\Delta\Sigma$ modulator with digital I/Q calibration for GNSS receivers". In: *IEEE ASSCC* (Nov. 2013), pp. 393–396 (cit. on p. 142).

[13]   C.-Y. Ho et al. "A quadrature bandpass continuous-time delta-sigma modulator for a tri-mode GSM-EDGE/UMTS/DVB-T receiver". In: *IEEE J. Solid-State Circuits* vol.46 (Nov. 2011), pp. 2571–2582 (cit. on p. 142).

[14]   R. Schreier et al. "A 375-mW quadrature bandpass $\Delta\Sigma$ ADC with 8.5-MHz BW and 90-dB DR at 44 MHz". In: *IEEE J. Solid-State Circuits* vol.41 (Dec. 2006), pp. 2632–2640 (cit. on p. 142).

[15]   I. Galdia et al. "0 MHz IF 1 MHz bandwidth two-path bandpass modulator with 72 dB DR consuming 16 mW". In: *IEEE J. Solid-State Circuits* vol.43 (July 2008), pp. 1648–1656 (cit. on p. 142).

Chapter 7

Conclusion

7.1 Conclusion

This dissertation proposes several circuit design techniques of delta sigma modulator using dynamic analog components to improve the performance of the delta sigma modulator. The effectiveness of the proposed design techniques is demonstrate, and the details of analyses and circuit implementation are also presented. The main contributions of this dissertation are summarized as follows:

Chapter 2 is an introduction to the theory of the delta sigma modulator. The oversampling technique, noise shaping technique and the basic architectures of delta sigma modulators are discussed in this chapter. Moreover, the theoretical performance represented by SQNR of the high order delta sigma modulator with multi-bit internal quantizer are summarized. According to design requirements, the parameters of delta sigma modulator can be derived from the calculated relational expression with respect to OSR, order and the resolution of internal quantizer, which can help circuit designer to define the architecture of delta sigma modulator appropriately.

Chapter 3 proposed a 2nd-order delta sigma modulator using dynamic analog components for verifying the functionality of the delta signal modulator with the dynamic comparator and the dynamic amplifier. The proposed 2nd-order delta sigma modulator is realized by the integrator using the ring amplifier and the passive-adder embedded 4-bit SAR quantizer. Because the ring amplifier does not include
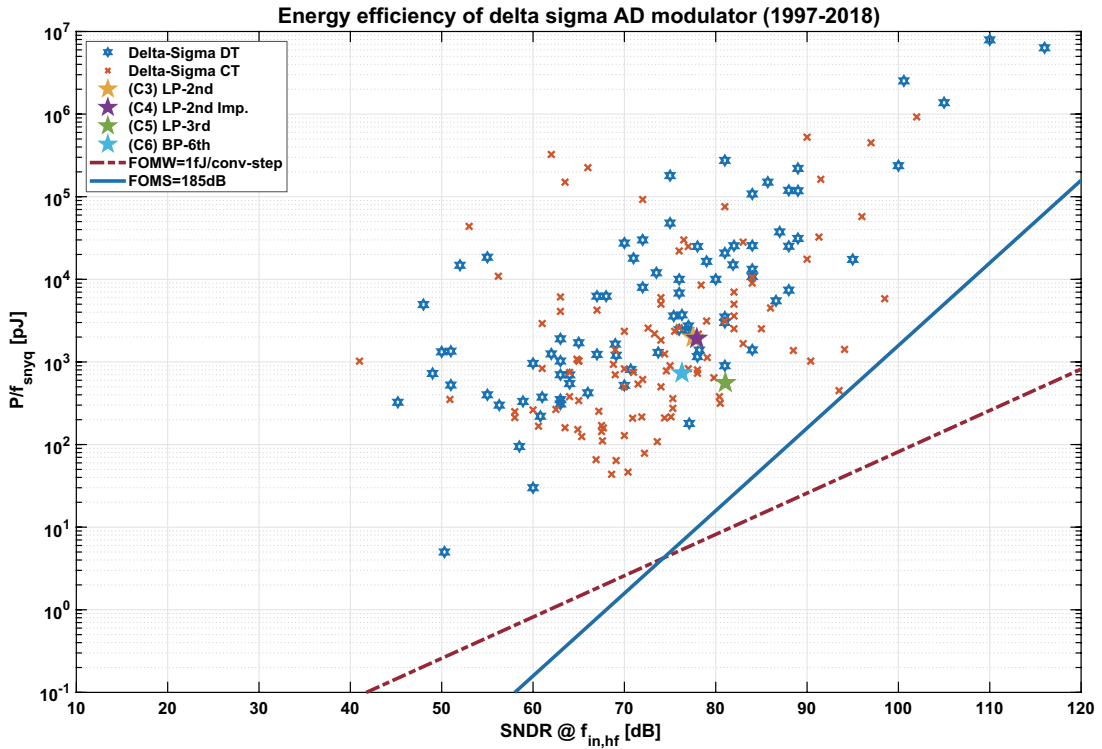
FIGURE 7.1: Energy efficiency of ADC

the static bias current and the passive-adder embedded 4-bit SAR quantizer is used as the analog signal adder which does not use the active amplifier and an 4-bit internal quantizer, the energy efficiency of the proposed 2nd-order delta sigma modulator can be improved. In order to demonstrate the design techniques of the proposed delta sigma modulator, the proof-of-concept prototype of proposed 2nd-order delta sigma modulator using dynamic is designed and fabricated in TSMC 90nm 1P9M CMOS technology without any option for precision capacitors and low threshold voltage transistor. The active area of the proposed delta sigma modulator is $610\mu \times 254\mu$. Bootstrapped switch is used at the input ports of the delta sigma modulator to reduce the non-linear effect of ON-resistance. All capacitors were laid out using multiple unit-capacitor cells for accurate ratio matching of coefficients. Unit-capacitor cells were realized by using the MIM capacitors for high density capacitance in a small chip area. Careful layout design has been done to keep the analog part of the delta sigma modulator is symmetrically arranged. The attention is also paid to keep the sensitive analog signals away from the noisy digital signal path.

The peak 77.51 dB of SNDR is achieved for 94 kHz bandwidth (OSR = 64). The measurement results of the modulator show that linear SNDR response up to the full scale, and the dynamic range of 84dB is achieved. The total power consumption of this work is 0.37 mW under the analog and digital circuits supply voltage is 1.1 V. Schreier FOM and Walden FOM are 161.5 dB and 0.32 pJ/conversion-step, respectively. Measurement results show the feasibility of the proposed circuit technique of the delta sigma modulator and the measured SNDR is not degraded significantly even the supply voltage is variate. For conforming the noise characteristic of the dynamic analog components, the noise models of dynamic amplifier (ring amplifier) and dynamic comparator are created, and these noise analysis are carried out.

In the chapter 4, the drawback of the 2nd-order delta sigma modulator using dynamic analog component proposed in the chapter 3 is discussed. The cause which the operating speed is limited is analyzed. 4 factors need to be guaranteed when designing the delta sigma modulator using ring amplifier and SAR quantizer are summarized. In order to improving the performance of the delta sigma modulator using dynamic analog components, an improved 2nd-order delta sigma modulator using dynamic analog components is proposed to simplify the operation phase. The improved delta sigma modulator has been designed and fabricated in 90 nm CMOS technology. Benefit from the reduction of the number of the delta sigma modulator operation phase, comparing with the previous work proposed in the chapter 3, the speed and bandwidth of the delta sigma modulator with simplified operation phase are improved by 16.7% for the same performance level. Moreover, the pseudo-differential ring amplifier without the static current is used for realizing the integrator. Therefore, the energy efficiency of the proposed delta sigma modulator can be kept at high level. The measured results show that the peak SNDR of 77.93 dB and SNR of 84.16 dB at -1.24 dBFS and -4.37 dBFS are achieved, respectively, and the feasibility of the proposed 2nd-order delta sigma modulator using dynamic analog components.

Chapter 5 proposed a 3rd-order delta sigma modulator using ring amplifier and noise shaping SAR quantizer. in order to enhance the performance of the delta sigma
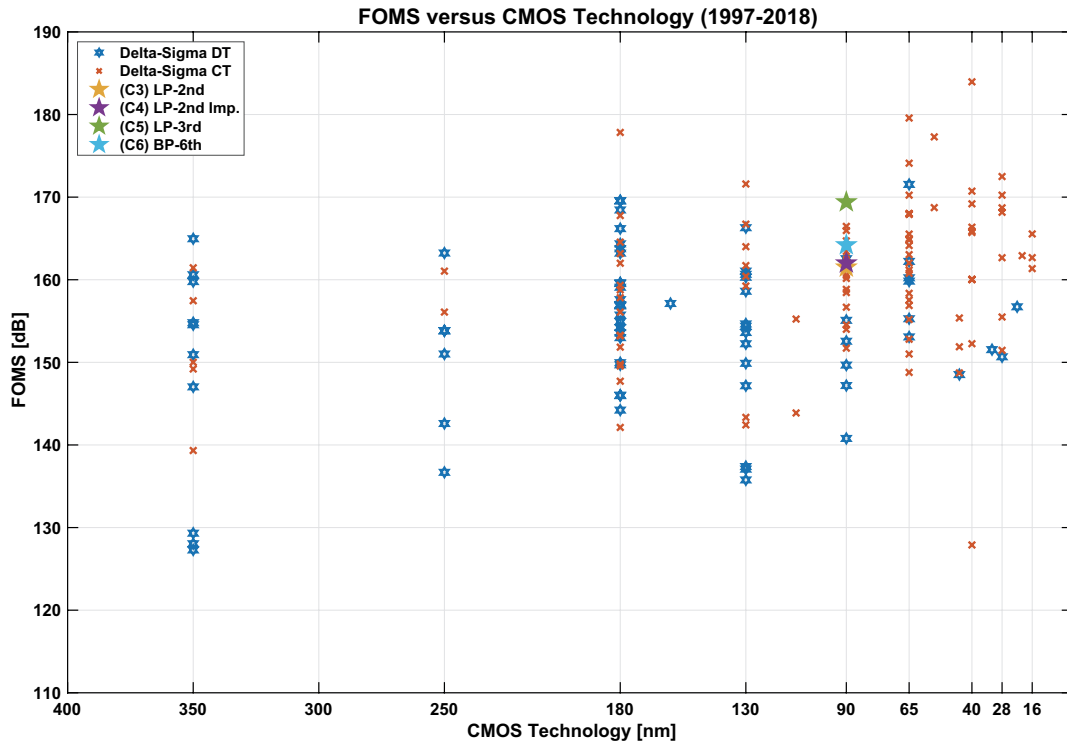
FIGURE 7.2: FOMS versus CMOS Technology

modulator using dynamic analog component, the quantization noise coupling realized by SAR quantizer is used for increasing the order of the delta sigma modulator. The proposed 3rd-order delta sigma modulator using noise coupling technique realized by the passive adder embedded SAR quantizer has been designed in 90 nm CMOS technology. It has 3rd-order noise shaping characteristic, although it is only a 2nd-order feed-forward architecture using two integrators. The realization of the additional 1st-order noise shaping benefit by the quantization noise feedback function of the proposed SAR quantizer with quantization noise coupling. Therefore, the performance of delta sigma modulator is enhanced, nonetheless the extra active analog component is not necessary, which can maintain the high energy efficiency for the delta sigma modulator. Moreover, only two non-overlapped clocks are required in the proposed delta sigma modulator, since the clock generator can be implemented by the simple circuit. The proposed a 3rd-order delta sigma modulator circuit is realized by dynamic analog components, thus the power consumption can be kept at a low level. The simulation results including both thermal noise and flicker noise show that the SNDR of 81.05 dB and SFDR of 91.00 dB are achieved, respectively,

and the feasibility of the proposed 3rd-order delta sigma modulator using dynamic analog components.
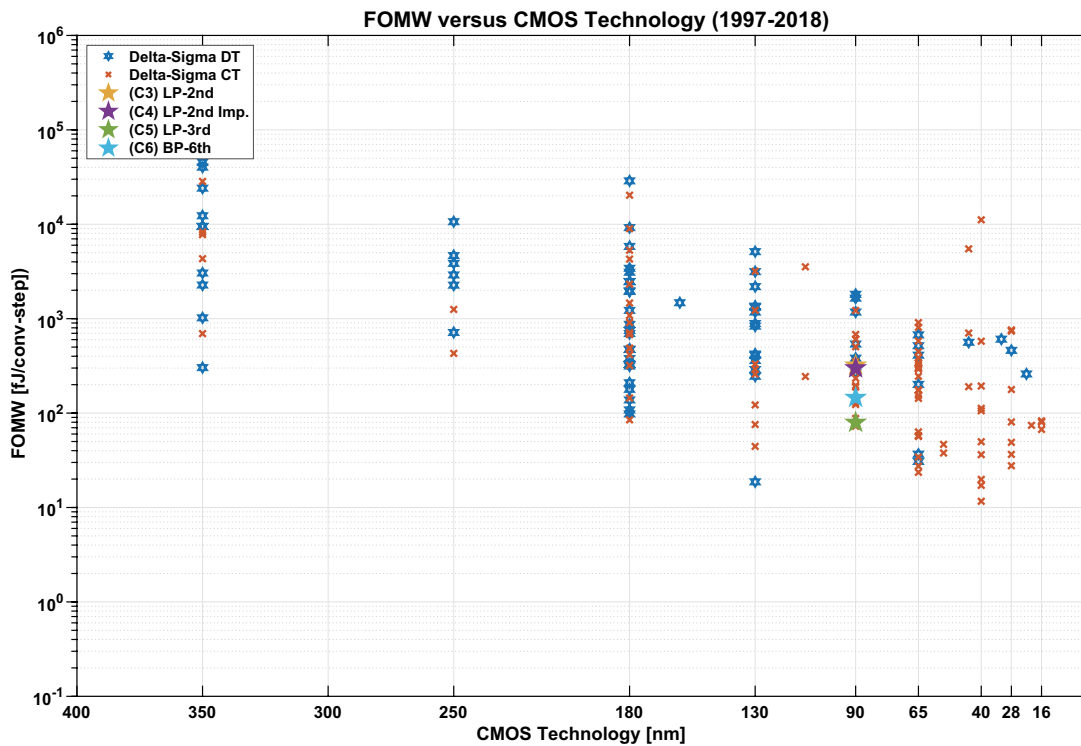
FIGURE 7.3: FOMW versus CMOS Technology

Chapter 6 proposed a 6th-order quadrature bandpass delta sigma modulator with 2nd-order image rejection using dynamic amplifier and noise coupling (NC) SAR quantizer embedded by passive adder for the applications of wireless communication systems. The 6th-order quadrature bandpass delta sigma AD modulator has been designed in 90 nm CMOS technology. A novel complex integrator circuit using ring amplifier is proposed to improve the energy efficiency and to reduce the area of circuit. The proposed complex integrator only requires one amplification operation for the complex integration, so that the QBPDSM can operate at the high speed. Benefit from an additional 2nd-order noise shaping and the 2nd-order image rejection are realized by the digital domain noise coupling SAR quantizer, not only the bandwidth of the QBPDSM is extended, but also the influence of I,Q-path mismatch is reduced. Moreover, the digital signal process technique is used for the process of the quantization noise in the noise coupling SAR quantizer, the use of active analog

component is not requited, thus the high energy efficiency is maintained. The simulation results show the feasibility of the proposed a 6th-order quadrature bandpass delta sigma modulator using dynamic analog components and the peak SNDR of 76.30 dB is achieved.

Chapter 7 described the conclusion of this dissertation. Figure 7.2 views the difference of energy efficiency between proposed delta sigma modulator using dynamic analog components and other works proposed in 1997-2018. Figure 7.3 and figure 7.1 show the difference of figure of merit (FOM) between proposed delta sigma modulator using dynamic analog components and other works proposed in 1997-2018. The proposed 2nd-order delta sigma modulator using dynamic analog components and its improved version have the better FOM in 90 nanometer CMOS process, despite they do not use other advanced techniques. The proposed 3rd-order delta sigma modulator using dynamic analog components has the best FOM in 90 nanometer CMOS technology. In design of the 6th-order quadrature bandpass delta sigma modulator using dynamic analog components, in order to realize the high order noise shaping and the image rejection, a mass of digital circuit using the non-advanced 90 nanometer CMOS technology is used for implementing the digital signal process circuits, hence its energy efficiency has declined. However, the better performance can be expected, if it is designed by the more advanced CMOS technology.

7.2   Future Work

Several design techniques for the delta sigma modulator using dynamic analog component have been proposed in this dissertation. There are some research topics, extended from the proposed design techniques, can be further investigated in the future. The related topics are listed as follows:

1. The dynamic amplifier (ring amplifier) has the limited application range. Due to the common-mode feedback circuit is only capable to keep the output common-mode voltage from drifting due to mismatch, charge injection, etc., but it cannot actively correct a common-mode voltage witch comes from the input port of AD convertor. Hence it cannot be used for the architecture which requires to process

the residual error signal repeatedly (eg. cyclic ADC, pipeline ADC and hybrid ADC). To extend the application range of ring amplifier, developing a simple and effective common-mode feedback circuit is necessary.

2. The ring amplifier is achieved base on the ring oscillator, hence it includes the suited fundamentally to scaling in the underlying circuits. The transistor scaling characteristics can be delivered favourably. The high performance operating amplifier in nanoscale technology can be realized by the dynamic analog circuits. The dynamic analog circuits should be able to achieve the ability to scale at the same pace as digital performance improvements, and it is also a truly scalable amplifier which include the characteristics of scaled CMOS. The abilities of a transistor included by dynamic analog circuits should be exploit fully. Therefore, in order to more fully verify scalable analog techniques, adjusting device sizes of proposed delta sigma modulator with dynamic analog components for each technology node is worthwhile.

Appendix A

SQNR of High Order Delta Sigma Modulator With Multi-bit Quantizer

FIGURE A.1: SQNR of high order delta sigma modulator using 2-bit internal quantizer

**SQNR of high order delta sigma modulator using
3-bit internal quantizer**
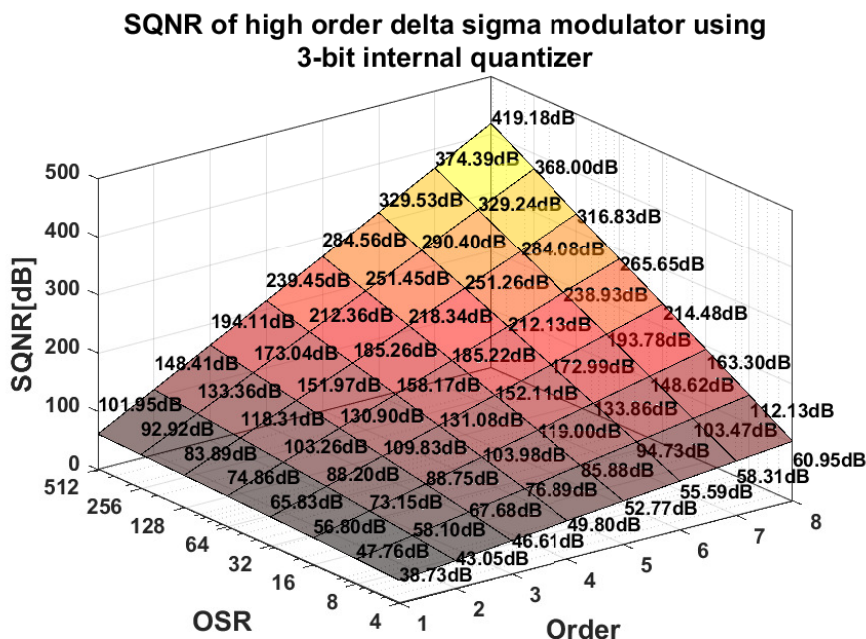
FIGURE A.2: SQNR of high order delta sigma modulator using 3-bit
internal quantizer

**SQNR of high order delta sigma modulator using
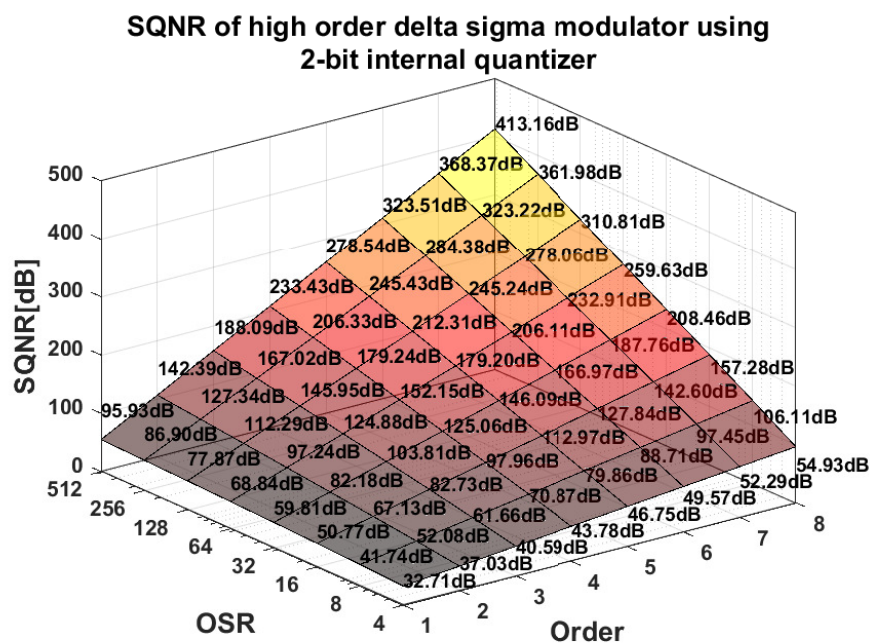4-bit internal quantizer**
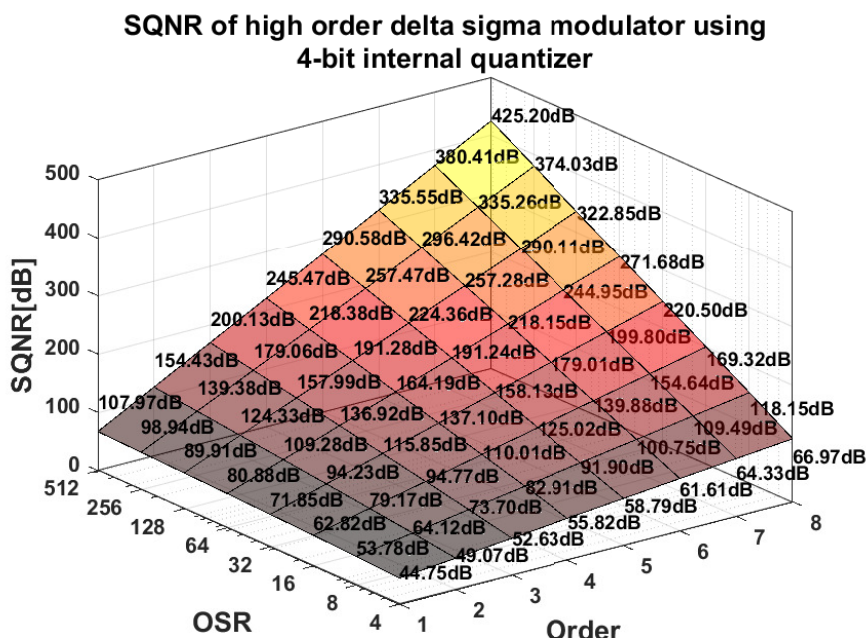
FIGURE A.3: SQNR of high order delta sigma modulator using 4-bit
internal quantizer
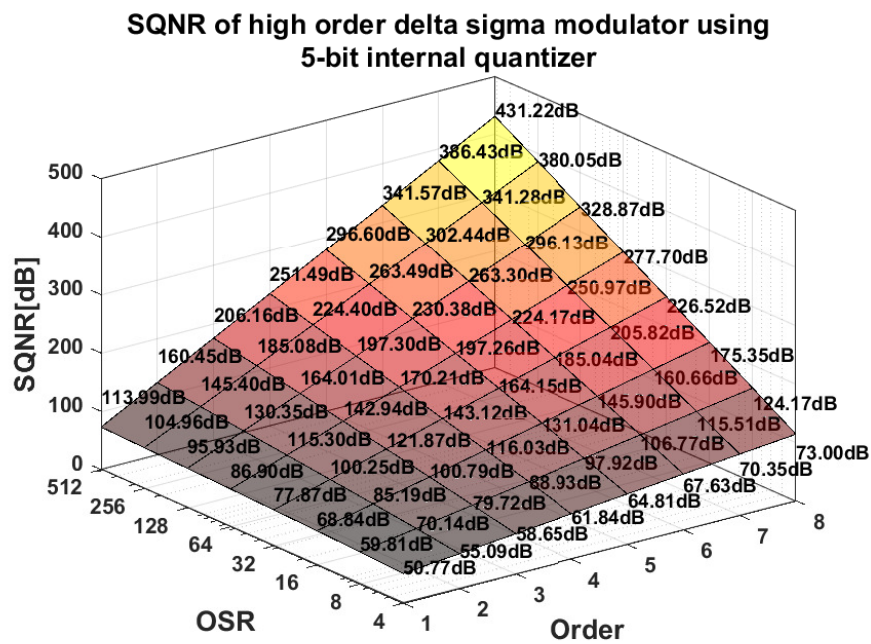
FIGURE A.4: SQNR of high order delta sigma modulator using 5-bit internal quantizer
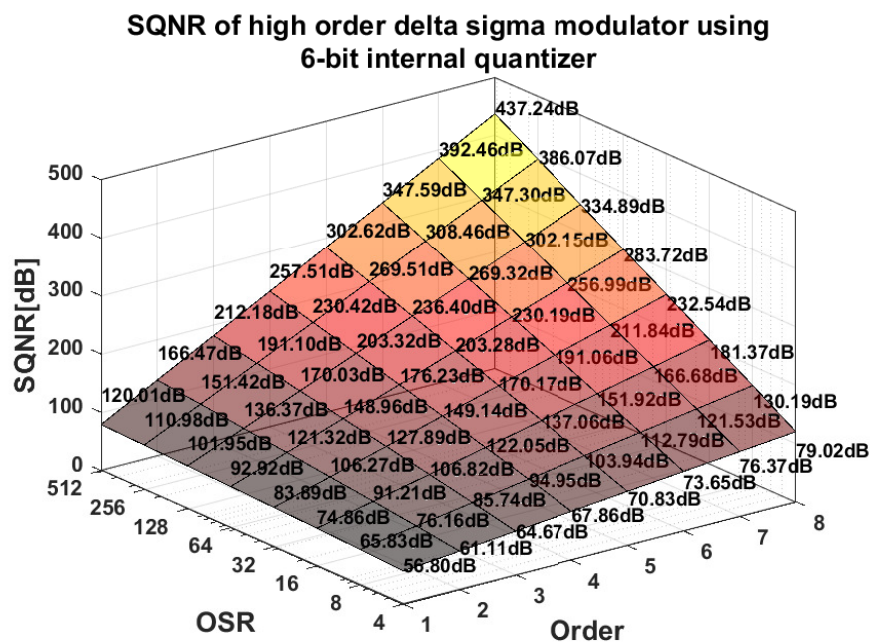
FIGURE A.5: SQNR of high order delta sigma modulator using 6-bit internal quantizer

Appendix B

VerilogA Code

Verilog-A implementation of ideal 20-bit SAR quantizer for noise analysis of dynamic comparator as following :

```
1  // VerilogA for syunki_veriloga , syunki_SAR20bit_for_comp_test , veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module syunki_SAR20bit_for_comp_test(
7  CK_S,CK_C,
8  IN_P,IN_M,OUT_P,OUT_M,D,
9  COMP_CK,
10 Vcm,Vref_P ,Vref_M ,
11 FB_CK,FB_OUT
12 );
13
14 input CK_S,CK_C,IN_P,IN_M,Vcm,Vref_P ,Vref_M ,FB_CK,FB_OUT;
15 electrical CK_S,CK_C,IN_P,IN_M,Vcm,Vref_P ,Vref_M ,FB_CK,FB_OUT;
16
17 output OUT_P,OUT_M,COMP_CK;
18 electrical OUT_P,OUT_M,COMP_CK;
19 output [0:19] D;
20 electrical [0:19] D;
21
22 parameter real vth = 0.6 from [0:inf);
23 parameter real high_level = 1.2 from [0:inf);
24 parameter real low_level = 0 from [0:inf);
25 parameter real trise = 20p from [0:inf);
```

```verilog
26  parameter real tfall = 20p from [0:inf];
27  parameter real tdel = 0 from [0:inf];
28  parameter integer bit_n = 20 from [0:inf];
29
30    genvar gi;
31    integer i;
32    real temp_Vref;
33    real temp_u;
34    real temp_D [0:19];
35    real temp_OUT_D [0:19];
36    real temp_COMP_CK;
37
38    analog begin
39
40      @(initial_step)begin
41        for(i=0;i<bit_n;i=i+1)begin
42          temp_OUT_D[i]=low_level;
43        end
44        temp_COMP_CK=high_level;
45      end
46
47      //sampling
48      @(cross(V(CK_S)-vth,-1,1.0,CK_S.potential.abstol))begin
49        temp_u=V(IN_P,IN_M);
50      end
51
52      @(cross(V(CK_C)-vth,1,1.0,CK_C.potential.abstol))begin
53        i=0;
54        temp_COMP_CK=low_level;
55      end
56
57      //start SAR convert
58      @(cross(V(FB_CK)-vth,1,1.0,FB_CK.potential.abstol))begin
59
60        if(V(CK_C)>vth)begin
61          temp_Vref=V(Vref_P,Vref_M);
62          if(V(FB_OUT)>vth)begin
63            temp_u=temp_u-temp_Vref*pow(2,-(i+1));
64            temp_D[bit_n-1-i]=high_level;
```

```verilog
65          end else begin
66            temp_u=temp_u+temp_Vref*pow(2,-(i+1));
67            temp_D[bit_n-1-i]=low_level;
68          end

69

70          i=i+1;
71          temp_COMP_CK=high_level;

72

73          if(i==bit_n)begin
74            for(i=0;i<bit_n;i=i+1)
75            temp_OUT_D[i]=temp_D[i];
76          end

77

78        end else begin
79          temp_COMP_CK=high_level;
80        end

81

82      end

83

84      //stop SAR convert when the 20bit conversion is finished
85      //the COMP_CK is kept at high_level
86      @(cross(V(FB_CK)-vth,-1,1.0,FB_CK.potential.abstol))begin
87        if(V(CK_C)>vth)begin
88          if(i<bit_n)
89            temp_COMP_CK=low_level;
90        end else begin
91          temp_COMP_CK=high_level;
92        end
93      end

94

95      V(OUT_P)<+V(Vcm)+temp_u/2;
96      V(OUT_M)<+V(Vcm)-temp_u/2;

97

98      V(COMP_CK) <+ transition(temp_COMP_CK, tdel, trise, tfall);
99      for(gi=0;gi<bit_n;gi=gi+1)
100         V(D[gi]) <+ transition(temp_OUT_D[gi], tdel, trise, tfall);

101

102   end

103
```

```
104  endmodule
```

Verilog-A implementation of ideal delay as following :

```verilog
1   // VerilogA for syunki_16, syunki_delay_for_test_veriloga, veriloga
2
3   `include "constants.vams"
4   `include "disciplines.vams"
5
6   module syunki_delay_for_test_veriloga(in, out);
7   input in;
8   output out;
9   electrical in, out;
10
11  parameter real initial_state = 1.2;
12  parameter real vth = 0.6;
13  parameter real vdd = 1.2;
14  parameter real gnd = 0;
15  parameter real trise = 20p from [0:inf);
16  parameter real tfall = 20p from [0:inf);
17  parameter real tdel = 0 from [0:inf);
18
19    real state;
20
21    analog begin
22
23      @(initial_step)begin
24        state=initial_state;
25      end
26
27      @ (cross(V(in) − vth, 1, 1.0, in.potential.abstol) )
28        state=vdd;
29
30      @ (cross(V(in) − vth, −1, 1.0, in.potential.abstol) )
31        state=gnd;
32
33      V(out) <+ transition(state, tdel, trise, tfall );
34    end
35
36  endmodule
```

Verilog-A implementation of ideal nand2 as following :

```
1   // VerilogA for syunki, syunki_nand2_veriloga, veriloga
2
3   `include "constants.vams"
4   `include "disciplines.vams"
5
6   module syunki_nand2_veriloga(A,B,Y);
7   input A,B;
8   output Y;
9   electrical A,B,Y;
10  parameter real vth = 0.6 from [0:inf);
11  parameter real high_level = 1.2 from [0:inf);
12  parameter real low_level = 0 from [0:inf);
13  parameter real trise = 20p from [0:inf);
14  parameter real tfall = 20p from [0:inf);
15  parameter real tdel = 0 from [0:inf);
16
17    real temp_out;
18
19    analog begin
20
21      if(V(A)>vth && V(B)>vth)begin
22        temp_out=low_level;
23      end else begin
24        temp_out=high_level;
25      end
26
27      V(Y) <+ transition(temp_out, tdel, trise, tfall );
28
29    end
30
31  endmodule
```

Verilog-A implementation of fbCm as following :

```verilog
1   // VerilogA for syunki_veriloga , syunki_fbCm_veriloga , veriloga
2
3   `include "constants.vams"
4   `include "disciplines.vams"
5
6   module syunki_fbCm_veriloga(in1 ,in2 ,vcmin ,out1 ,out2 );
7
8   input in1 ,in2 ,vcmin ;
9   electrical in1 ,in2 ,vcmin ;
10  output out1 ,out2 ;
11  electrical out1 ,out2 ;
12
13    analog begin
14
15      V(out1)<+V(vcmin)+V(in1 ,in2 )/2;
16      V(out2)<+V(vcmin)−V(in1 ,in2 )/2;
17
18    end
19
20  endmodule
```

Verilog-A implementation of fetchCm as following :

```verilog
1  // VerilogA for syunki_veriloga , syunki_fetchCm_veriloga , veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module syunki_fetchCm_veriloga(in1,in2,out);
7
8  input in1,in2;
9  electrical in1,in2;
10 output out;
11 electrical out;
12
13   analog begin
14
15     V(out)<+(V(in1)+V(in2))/2;
16
17   end
18
19 endmodule
```

Verilog-A implementation of Quadrature-DWA as following :

```verilog
1
2   // VerilogA for syunki_veriloga , syunki_dwa_for_bp , veriloga
3
4   `include "constants.vams"
5   `include "disciplines.vams"
6
7   module syunki_dwa_for_bp(I_D,Q_D,CLK,EN,S1,S2,EN_CROSS);
8
9   input [0:4] I_D;
10  electrical [0:4] I_D;
11  input [0:4] Q_D;
12  electrical [0:4] Q_D;
13  input CLK,EN;
14  electrical CLK,EN;
15
16  output [1:31] S1;
17  electrical [1:31] S1;
18  output [1:31] S2;
19  electrical [1:31] S2;
20
21  output EN_CROSS;
22  electrical EN_CROSS;
23
24  parameter real vth = 0.6 from [0:inf);
25  parameter real high_level = 1.2 from [0:inf);
26  parameter real low_level = 0 from [0:inf);
27  parameter real trise = 20p from [0:inf);
28  parameter real tfall = 20p from [0:inf);
29  parameter real tdel = 0 from [0:inf);
30  parameter integer bit_n = 5;
31
32  genvar gi;
33  integer i;
34  integer dummy;
35  integer ptr1,ptr2;
36  integer state;
37  integer temp_S [1:31];
38  real temp_in_I [0:4];
```

```verilog
39  real temp_in_Q [0:4];
40  real temp_I;
41  real temp_Q;
42  real temp_out_S1 [1:31];
43  real temp_out_S2 [1:31];
44  real temp_en_cross;
45
46  ////////////////////////////////////////////////////
47  //  ptr_process(si,ei,bit_n,ptr,wa)
48  ////////////////////////////////////////////////////
49  analog function integer ptr_process;
50
51    input si,ei,bit_n;
52    integer si,ei,bit_n;
53
54    output ptr,wa;
55    integer ptr;
56    integer wa [1:31];
57
58    integer mark_pn,i,start_index,end_index;
59
60    begin
61
62      start_index=si;
63      end_index=ei;
64
65      for(i=1;i<pow(2,bit_n);i=i+1)
66        wa[i]=0;
67
68      mark_pn=start_index<=end_index?1:0;
69
70      //processing of start_index
71      case (1)
72        start_index<1 : start_index=pow(2,bit_n)-1+start_index;
73        start_index>pow(2,bit_n)-1 : start_index=start_index-(pow(2,bit_n)
                -1);
74      endcase
75
76      //processing of end_index
```

```
77        case (1)
78          end_index<1 : end_index=pow(2,bit_n)-1+end_index;
79          end_index>pow(2,bit_n)-1 : end_index=end_index-(pow(2,bit_n)-1);
80        endcase
81
82        //generating of weight_array(wa)
83        if(mark_pn==1)begin
84          if(start_index<=end_index)begin
85            for(i=start_index;i<=end_index;i=i+1)
86              wa[i]=1;
87          end else begin
88            for(i=start_index;i<=(pow(2,bit_n)-1);i=i+1)
89              wa[i]=1;
90            for(i=1;i<=end_index;i=i+1)
91              wa[i]=1;
92          end
93        end else begin // mark_pn=0
94          if(end_index<=start_index)begin
95            for(i=end_index;i<=start_index;i=i+1)
96              wa[i]=1;
97          end else begin
98            for(i=end_index;i<=(pow(2,bit_n)-1);i=i+1)
99              wa[i]=1;
100           for(i=1;i<=start_index;i=i+1)
101             wa[i]=1;
102         end
103       end
104
105       ptr=end_index;
106
107     end
108
109 endfunction
110 //////////////////////////////////////////////////////
111
112
113 //////////////////////////////////////////////////////
114 // opdt_process(in,out)
115 //////////////////////////////////////////////////////
```

```veriloga
116   analog function integer opdt_process;
117
118      input in;
119      integer in [1:31];
120      output out;
121      real out [1:31];
122      integer i;
123
124      begin
125         for(i=1;i<pow(2,bit_n);i=i+1)begin
126            out[i]=in[i]==1?high_level:low_level;
127         end
128      end
129
130   endfunction
131   //////////////////////////////////////////////////////
132
133   //////////////////////////////////////////////////////
134   // zero_process(out)
135   //////////////////////////////////////////////////////
136   analog function integer zero_process;
137
138      output out;
139      integer out [1:31];
140      integer i;
141
142      begin
143         for(i=1;i<pow(2,bit_n);i=i+1)begin
144            out[i]=0;
145         end
146      end
147
148   endfunction
149   //////////////////////////////////////////////////////
150
151      analog begin
152
153         @(initial_step)begin
154            state=0;
```

```
155        ptr1=pow(2,bit_n)−1;
156        ptr2=0;
157      end
158
159    @(cross(V(CLK)−vth,1,1.0,CLK.potential.abstol))begin
160
161        temp_in_I[0]=V(I_D[0])>vth?high_level:low_level;
162        temp_in_I[1]=V(I_D[1])>vth?high_level:low_level;
163        temp_in_I[2]=V(I_D[2])>vth?high_level:low_level;
164        temp_in_I[3]=V(I_D[3])>vth?high_level:low_level;
165        temp_in_I[4]=V(I_D[4])>vth?high_level:low_level;
166
167        temp_I=0;
168        for(i=0;i<bit_n;i=i+1)
169          if(temp_in_I[i]>vth)
170            temp_I=temp_I+pow(2,i);
171
172        temp_in_Q[0]=V(Q_D[0])>vth?high_level:low_level;
173        temp_in_Q[1]=V(Q_D[1])>vth?high_level:low_level;
174        temp_in_Q[2]=V(Q_D[2])>vth?high_level:low_level;
175        temp_in_Q[3]=V(Q_D[3])>vth?high_level:low_level;
176        temp_in_Q[4]=V(Q_D[4])>vth?high_level:low_level;
177
178        temp_Q=0;
179        for(i=0;i<bit_n;i=i+1)
180          if(temp_in_Q[i]>vth)
181            temp_Q=temp_Q+pow(2,i);
182
183        if(V(EN)>vth)begin
184
185        case (1)
186          state==0:begin
187            //DAC1
188            if(temp_I==0)
189              dummy=zero_process(temp_S);
190            else
191              dummy=ptr_process(ptr1,ptr1−temp_I+1,bit_n,ptr1,temp_S);
192            dummy=opdt_process(temp_S,temp_out_S1);
193            //DAC2
```

```
194        if (temp_Q==0)
195          dummy=zero_process(temp_S);
196        else
197          dummy=ptr_process(ptr2+1,ptr2+temp_Q,bit_n,ptr2,temp_S);
198        dummy=opdt_process(temp_S,temp_out_S2);
199
200        temp_en_cross=low_level;
201      end
202      state==1:begin
203        //DAC1
204        if (temp_Q==0)
205          dummy=zero_process(temp_S);
206        else
207          dummy=ptr_process(ptr1-1,ptr1-1-temp_Q+1,bit_n,ptr1,temp_S);
208        dummy=opdt_process(temp_S,temp_out_S1);
209        //DAC2
210        if (temp_I==0)
211          dummy=zero_process(temp_S);
212        else
213          dummy=ptr_process(ptr2,ptr2-temp_I+1,bit_n,ptr2,temp_S);
214        dummy=opdt_process(temp_S,temp_out_S2);
215
216        temp_en_cross=high_level;
217      end
218      state==2:begin
219        //DAC1
220        if (temp_I==0)
221          dummy=zero_process(temp_S);
222        else
223          dummy=ptr_process(ptr1,ptr1-1+temp_I,bit_n,ptr1,temp_S);
224        dummy=opdt_process(temp_S,temp_out_S1);
225        //DAC2
226        if (temp_Q==0)
227          dummy=zero_process(temp_S);
228        else
229          dummy=ptr_process(ptr2-1,ptr2-1-temp_Q+1,bit_n,ptr2,temp_S);
230        dummy=opdt_process(temp_S,temp_out_S2);
231
232        temp_en_cross=low_level;
```

```
233              end
234            state==3:begin
235                //DAC1
236              if(temp_Q==0)
237                dummy=zero_process(temp_S);
238              else
239                dummy=ptr_process(ptr1+1,ptr1+temp_Q,bit_n,ptr1,temp_S);
240            dummy=opdt_process(temp_S,temp_out_S1);
241              //DAC2
242              if(temp_I==0)
243                dummy=zero_process(temp_S);
244              else
245                dummy=ptr_process(ptr2,ptr2-1+temp_I,bit_n,ptr2,temp_S);
246            dummy=opdt_process(temp_S,temp_out_S2);
247
248              temp_en_cross=high_level;
249            end
250          endcase
251
252        state=state+1;
253        if(state>3)
254          state=0;
255
256      end else begin
257
258        dummy=zero_process(temp_S);
259        for(i=1;i<=temp_I;i=i+1)
260          temp_S[i]=1;
261        dummy=opdt_process(temp_S,temp_out_S1);
262
263        dummy=zero_process(temp_S);
264        for(i=1;i<=temp_Q;i=i+1)
265          temp_S[i]=1;
266        dummy=opdt_process(temp_S,temp_out_S2);
267
268        temp_en_cross=low_level;
269
270      end
271
```

```
272        end

273

274     V(EN_CROSS) <+ transition(temp_en_cross, tdel, trise, tfall);

275

276     for(gi=1;gi<32;gi=gi+1)begin

277       V(S1[gi]) <+ transition(temp_out_S1[gi], tdel, trise, tfall);

278       V(S2[gi]) <+ transition(temp_out_S2[gi], tdel, trise, tfall);

279     end

280

281   end

282

283 endmodule
```

Appendix C

Publication List

Papers Published in Academic Journals

(1). **C. Pan**, H. San, "A 6th-Order Quadrature Bandpass Delta Sigma AD Modulator Using Dynamic Amplifier and Noise Coupling SAR Quantizer," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E102-A, No.3, pp.507-517, Mar. 2019.

(2). **C. Pan**, H. San, "Experimental Implementation of $\Delta\Sigma$AD Modulator with Dynamic Analog Components," Analog Integrated Circuits and Signal Processing, Springer, Vol.97, Issue 2, pp.215-223, Nov. 2018.

(3). **C. Pan**, H. San, "A Noise Coupled $\Delta\Sigma$AD Modulator Using Passive Adder Embedded Noise Shaping SAR Quantizer," IEICE Trans. on Electronics, Vol.E101-C, No.7, pp.480-487, Jul. 2018.

(4). **C. Pan**, H. San, "A 2nd-order $\Delta\Sigma$AD Modulator using Dynamic Analog Components with Simplified Operation Phase," IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E101-A, No.2, pp.425-433, Feb. 2018.

(5). **C. Pan**, H. San,"A $\Delta\Sigma$AD Modulator with SAR Quantizer and Ring Amplifier," IEICE Trans. on Fundamentals (Japanese Edition), Vol. J99-A, No.8, pp.262–269, Aug. 2016.

Papers Published in International Conference

(1). **C. Pan**, H. San, "A 6th-Order Complex Bandpass $\Delta\Sigma$AD Modulator Using Dynamic Amplifier and Noise Coupling SAR Quantizer," IEEE 2018 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2018), pp.447-452, Nov.30, 2018, Ishigaki, Japan.

(2). **C. Pan**, H. San, T. Shibata, "A 720μW 77.93dB SNDR $\Delta\Sigma$AD Modulator Using Dynamic Analog Components with Simplified Operation Phase," IEEE 2018 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2018), pp.442-446, Nov.30, 2018, Ishigaki, Japan. (Outstanding Student Paper Award)

(3). **C. Pan**, H. San, "CMOS $\Delta\Sigma$AD modulator using Dynamic Analog Components," International Conference on Mechanical, Electrical and Medical (ICMEMIS 2018), Nov.5, 2018, Kiryu, Japan. (Best Paper Award)

(4). S. Yamada, T. Teranishi, **C. Pan** and H. San, "Complex Bandpass $\Delta\Sigma$AD Modulator using Passive-adder Embedded SAR Quantizer," 2018 International Conference on Analog VLSI Circuits (AVIC), pp.-, Nov.3, 2018, Chiang Mai, Thailand.

(5). **C. Pan**, H. San, T. Shibata, "A 2nd-order $\Delta\Sigma$AD modulator using ring amplifier and SAR quantizer with simplified operation mode," IEEE Mixed Design of Integrated Circuits and Systems (MIXDES 2017), pp.45-49, Jun.22, 2017, Bydgoszcz, Poland.

(6). **C. Pan**, H. San, T. Shibata, "A 2nd-order Delta Sigma AD Modulator using Dynamic Amplifier and Dynamic SAR Quantizer," IEEE 2016 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2016), pp.528-532, Oct.26, 2016, Phuket, Thailand.

(7). **C. Pan**, H. San, "A Low-Distortion Delta-Sigma Modulator with Ring Amplifier and Passive Adder Embedded SAR Quantizer," IEEE 2015 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2015), pp.299-302, Nov.9, 2015, Bali, Indonesia.

Papers Published in Domestic Conference

(1). 寺西　司，潘　春暉，傘　昊，"複素バンドパスΔΣADC低電力技術に関する提案，"電気学会電子回路研究会，平成30年12月20日，東京．

(2). 佐々木美波，大津俊貴，潘　春暉，傘　昊，松浦達治，堀田正生，"SOTB CMOSを用いる低電源電圧逐次比較ADCの検討，"電気学会電子回路研究会，平成30年12月20日，東京．

(3). 大津俊貴，佐々木美波，山田秀一郎，潘　春暉，傘　昊，松浦達治，堀田正生，"SOTBを用いた非2進サイクリックADCの検討，"電気学会電子回路研究会，平成30年12月20日，東京．

(4). 潘　春暉，傘　昊，柴田随道，"ダイナミックアナログ回路を用いたCMOS ΔΣAD変調器，"電気学会，電子・情報・システム部門大会，平成30年9月5日，札幌，pp.266-270．

(5). 寺西　司，潘　春暉，傘　昊，"逐次比較量子化器を用いる複素バンドパスΔΣADC低電力手法の提案，"電気学会電子回路研究会，ECT-18-24，平成30年3月8日，横浜．

(6). 潘　春暉，傘　昊，"量子化雑音帰還機能を持つ逐次比較量子化器を用いるΔΣAD変調器，"電子情報通信学会，ICD/CPSY/CAS研究会，Vol，117，No.343，平成29年12月14日，石垣島，pp.165-169．

(7). 潘　春暉，日比野哲丈，傘　昊，"リングアンプと逐次比較量子化器を用いるΔΣAD変調器最適化設計の一手法，"電気学会電子回路研究会，ECT-016-092，平成28年12月14日，東京，pp.49-53．

(8). 大浦颯人，潘　春暉，傘　昊，"非2進荷重DACを用いる逐次比較ADC高精度化手法の検討，"電気学会電子回路研究会，ECT-016-094，平成28年12月14日，東京，pp.59-64．

(9). 潘　春暉，傘　昊，"逐次比較量子化器とリングアンプを用いるΔΣAD変調器の検討，"電子情報通信学会第２８回回路とシステムワークショップ，平成27年8月3日，淡路島，pp.105-109．