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A NOVEL DOUBLE GATE FINFET TRANSISTOR: OPTIMIZED POWER AND PERFORMANCE ANALYSIS FOR EMERGING NANOTECHNOLOGIES

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ABSTRACT
Abstract—FinFET technology has been proposed as a promising alternative for deep sub-micron CMOS technology, because of its superior device performance, scalability, lower leakage power consumption and cost-effective fabrication process. Fin-type field-effect transistors (FinFETs) are capable substitutes for bulk CMOS at the nano-scale. Previous works have studied the performance or power advantages of FinFET circuits over bulk CMOS circuits. This paper elucidates the dependability analysis of Average power, Leakage power, Leakage current and Delay of AND gate using double gate FinFET. Our experiments compare FinFET circuits at different voltages at 45 nm technology in virtuoso tool of cadence, showing that DG FinFET circuits have better dependability and scalability.

Keywords—double gate FinFET; fin width; low power circuit; device analysis

1. INTRODUCTION

FinFET devices have been proposed as the most likely candidate to substitute bulk MOSFETs for ultimate scaling [1]. The FinFET devices can be employed either with two gates tied together [a three-terminal (3T) structure] or with two independently biased gates [a four-terminal (4T) structure] [2]. The ITRS has proposed multi-gate FETs such as planar double gate FETs and FinFETs as a possible scaling path for low power and high performance CMOS technologies [3]. Although early double-gate FETs presented manufacturing challenges associated with vertical structures, more recently, double-gate devices called FinFETs or wraparound FETs that are compatible with standard CMOS over most of their processing steps have been demonstrated [4].

The channel of a FinFET is a slab (fin) of undoped silicon perpendicular to the substrate. At least two sides of the fin are wrapped around by oxide simultaneously. In this way, the active regions are broken up into several fins and a gate overlaps the channel regions of the fins on either side. Consequently, the increased electrostatic control of the gate over the channel makes very high *I*on/*I*off ratios achievable. FinFETs have also shown excellent scalability, suppression of short channel effects, and limited parametric variations. A FinFET with independent gates is a novel variant of double gate devices. Two isolated gates are designed by removing the gate regions at the top of the fin. Although the gates are electrically isolated, their electrostatics is highly coupled. The threshold voltage of either of the gates can be easily influenced by applying an appropriate voltage to the other gate. This technology is called multiple independent-gate FET (MIGFET) [5] and can be integrated with regular double-gate devices on the same chip. A successful implementation of a FinFET device with three independent gates has also been reported [6].

2. DEVICE ARCHITECTURE

Conventional DG-FinFET structure is shown in figure. It is a double gate structure. All the transistors are having tied gates. The channel of a FinFET is a tiny slab (fin) of undoped silicon perpendicular to the substrate. Figure 1 illustrates a simplified perspective 3D and cross-sectional view of a typical double gate FinFET device structure. The source, drain and channel regions are doped with the same type of dopant. Hence, there is no pn junction along the channel length and the leakage current is thus reduced. The undoped channel eliminates Coulomb scattering due to impurities, resulting in higher mobility in FinFETs [7]. The ratio of p-type to n-type mobility is higher than CMOS. Unlike CMOS, threshold voltage is not modified by source-body voltage variation. This, along with improvement in mobility, paves the way for longer series stacked transistors in the pull-up or pull-down networks of logic gates.

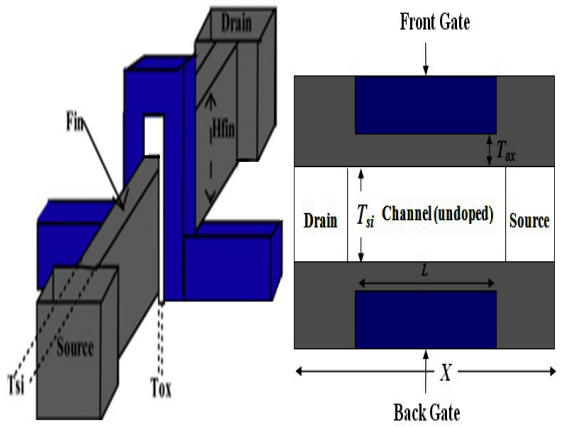

Figure 1: 3D and Cross section view of a typical FinFET

The gate oxide is formed on both sides of the fin simultaneously, which solves alignment issues of source and drain junctions and simplifies the process. For clarity, the followings are some critical geometrical parameters according to the figure.

1. Gate length (L): the physical gate length of FinFETs, defined by the spacer gap.
2. Fin height (H_{fin}): the height of silicon fin.
3. Fin width (T_{si}): the thickness of silicon fin, defined by the distance between the front and back gates.
4. Front or back gate thickness (T_{ox}): the thickness of the front or back gate oxide.

In FinFET-based circuits, a single-fin device cannot provide sufficient current to meet the performance constraints; hence, wider devices should be employed. In FinFET technology, the width of the device is proportional to the height of the fin. To maintain the mechanical stability, the height of the devices, however, is limited to several times the fin thickness. Therefore, to increase the size of the FinFET devices, multifin devices are used, which are built with several individual fins. Due to process variation, individual fins can have different threshold voltages. The gate work function, channel length, and fin thickness variation are the most important sources of variations in FinFET devices [8]. However, it is not the goal of this paper to discuss the effect of the different sources of threshold voltage variation. In our simulations, we include the effect of average power, leakage power, leakage current and delay on double gate FinFET. The height of the fin, *H*fin acts as the width of channel. Stronger devices can be built by using appropriate number of parallel fins in each transistor. So, the channel width of a FinFET device is given by

$$Width = nfin \times Hfin \qquad (1)$$

Where *n*fin is the number of fins. Taller fins result in more powerful devices, at the cost of granularity in gate width. Other important design parameters are fin thickness T_{si} and gate-source/drain underlap. Existence of gate-source/drain underlap and small T_{si} are necessary conditions for good suppression of short channel effects in FinFETs [9]. The ultimate double gate FinFET device uses a physical oxide with a large bandgap to isolate the gate from the conducting channel area.

By applying gate voltage to ac-cumulate or deplete majority carriers in the channel, we can modulate the channel conductance for controlling the channel current as a switch between the source and drain. Let the gate width of a FinFET with a single fin be *Wmin*. As we know that the gate width of a multi-fin FinFET is quantized in the number of fins. The higher values of widths are achieved by connecting a number of fins (n_{fin}) in parallel. Figure 2 shows an SG-mode FinFET in which four fins have been connected in parallel. The width of this device is 4Wmin. The area occupied by this device is proportional to $(n_{fin} - 1)/P_{fin}$, where P_{fin} is the fin pitch defined by the process technology.

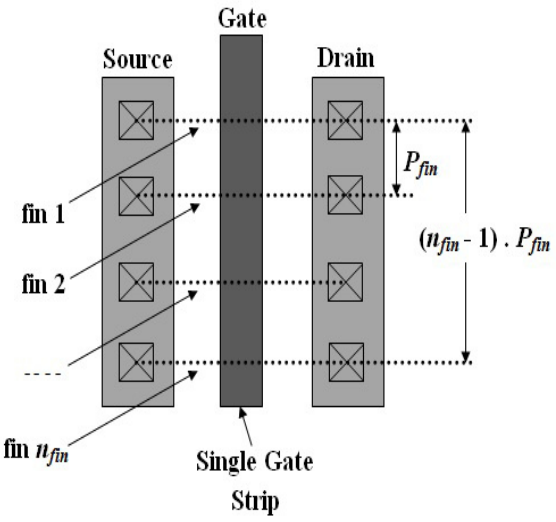

Figure 2: SG-mode FinFET

To accurate estimation of the leakage current, let us first examine the leakage current of the individual fins. Assuming that the threshold voltage of an individual fin has a normal (Gaussian) distribution $N(\mu V_{TX}, \sigma V_{TX})$, its leakage current has a lognormal distribution that is given by the following expression:

$$I_{Leakage} = WI_0 e^{-\frac{V_{TX}}{B}} \qquad (2)$$

$$B = m\frac{kT}{q} \qquad (3)$$

Where V_{TX} is the threshold voltage of an individual fin, *W* is the width of the single-fin FinFET, I_0 is a technology-dependent parameter and *m* is the body factor. *kT/q* is the thermal voltage (~ =26 mV at the room temperature), and *mkT/q* is referred to as constant *B* for simplicity. The leakage current of a multifin device with four fins is the sum of the leakage currents of the individual fins, as given by the following expression:

$$I_{Leakage} = WI_0[e^{-\frac{V_{T1}}{B}} + e^{-\frac{V_{T2}}{B}} + e^{-\frac{V_{T3}}{B}} + e^{-\frac{V_{T4}}{B}}] \qquad (4)$$

Where *VT*1, *VT*2, *VT*3, and *VT*4 are the threshold voltages of individual fins in the multifin device. In the general case, the leakage current of a multifin device is the sum of *n* lognormal variables, where *n* is the number of the fins in a multifin device. In FinFET technology, "device widths are dispensed in units of whole fins only." [10]

This is familiar as device width quantization, which bounds our ability to size transistors effectively in FinFET circuit. The fabrication process of double-gate MOSFET devices (e.g., FinFET) is more complicated than that of single gate devices, which will potentially convey more nonuniformity during fabrication. As for example, in FinFET devices that the gate oxide is on the etched sidewall of the fin, thus its uniformity is more difficult to control. The condition of the channel-oxide interface is determined by the sidewall roughness of the fin.

3. SHORTED-GATE AND INDEPENDENT-GATE FINFETS

FinFET devices come in many flavors. In shorted-gate (SG) FinFETs, the two gates are tied together, leading to a three-terminal device. This can be of use as a direct replacement for the conventional bulk-CMOS devices. In independent-gate (IG) FinFETs, the top portion of the gate is etched out, giving way to two independent gates. Because the two independent gates can be controlled separately thus IG-mode FinFETs offer more design options.

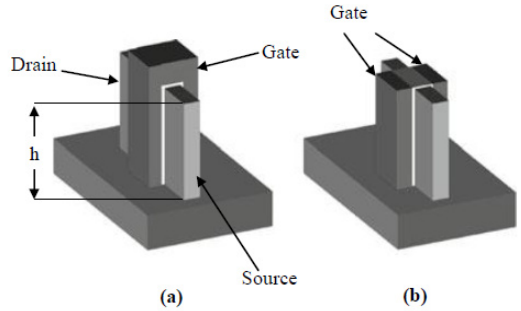

Figure 3. (a) SG-mode FinFET (b) IG-mode FinFET

4. LOGIC DESIGN IN FINFET TECHNOLOGY

In this section, we present the logic design of AND gate using double gate FinFET. Figure 4 shows the symbols for independent-gate (IG) and shorted-gate (SG) n-type and p-type DG FinFETs.

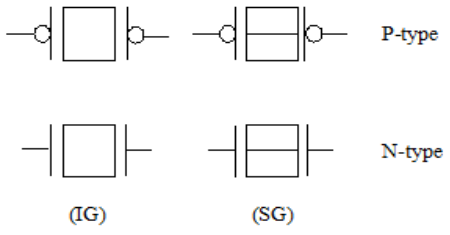

Figure 4. Symbols for independent-gate (IG) and shorted-gate (SG) n-type and p-type double-gate FinFETs.

The proposed AND gate is realized using the virtuoso tool of cadence. The spectre simulator of cadence is used to simulate the output. The circuit implementation of AND gate using double gate FinFET is shown in figure 5. Here the gate of two PMOS or NMOS transistors are shorted to formed a FinFET like structure. In this circuit, the supply voltages are given 0.5 V, 0.6 V, 0.7 V, 0.8 V and 0.9 V respectively at 45 nm technology.

The AND gate is a basic digital logic gate that implements logical conjunction. That behaves according to the truth table shown in Table I. An output HIGH (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH (1), a LOW (0) output results. In another words, the function of AND (A.B) effectively finds the minimum between two binary digits, just as the OR function finds the maximum. So that the output is always 0 except when all the inputs are 1s.

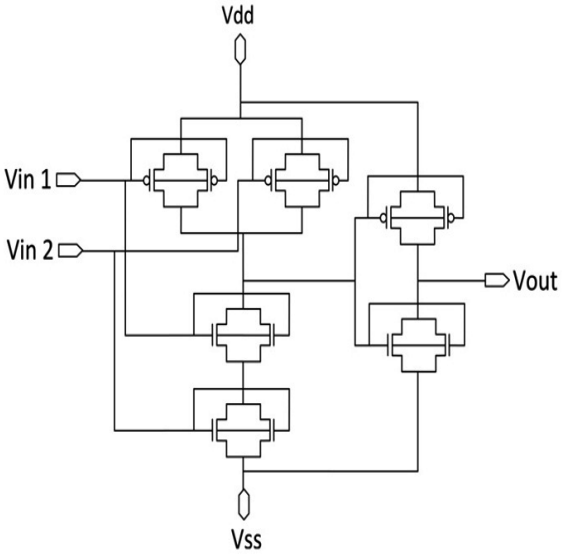

Figure 5. Schematic of AND gate using double gate FinFET.

TABLE I. TRUTH TABLE OF AND GATE

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

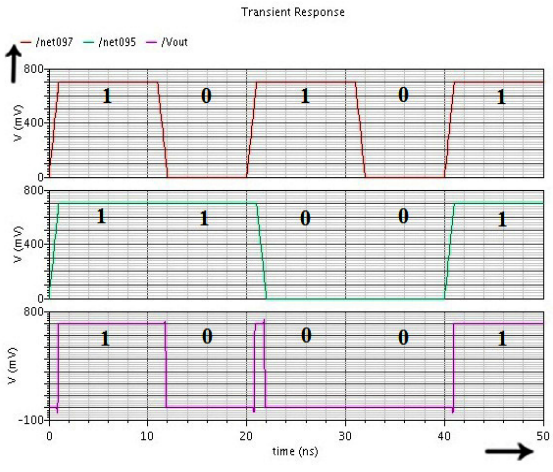

Figure 6. Simulated Transient Response of double Gate FinFET in Cadence Tool.

The input and output waveforms simulated for the AND gate using double gate FinFET is shown in figure 6 and proposed DC response of DG FinFET is shown in figure 7. Cadence simulation of transient analysis and DC analysis gave good results. In order to examine and compare device performance due to process variation, we vary fin width t_{Si} and gate oxide thickness t_{ox} as individual parameters and also as different combinations of both.

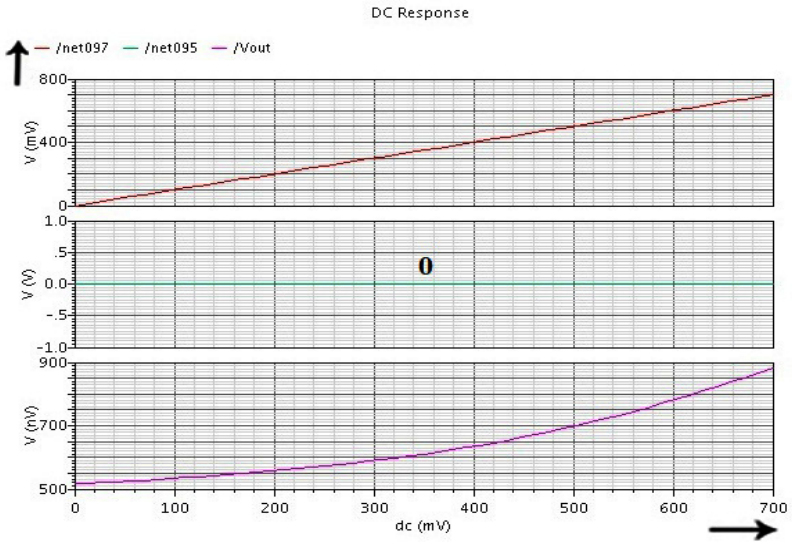

Figure 7. Simulated DC Response of double Gate FinFET in Cadence Tool.

5. RESULT AND DISCUSSION

In this section, we present the simulation results of AND gate at 45nm and 180nm technology from virtuoso tool of cadence. Figure 8 and 9 show the simulated leakage power curve of DG FinFET at 0.7 V power supply at 180 nm and 45 nm technology respectively. In 180 nm technology the average power consumption is 10.75 nW whereas in 45 nm technology the average power consumption is 7.467 nW. Our experimental result gives minimum leakage power as compared to 180 nm technology.

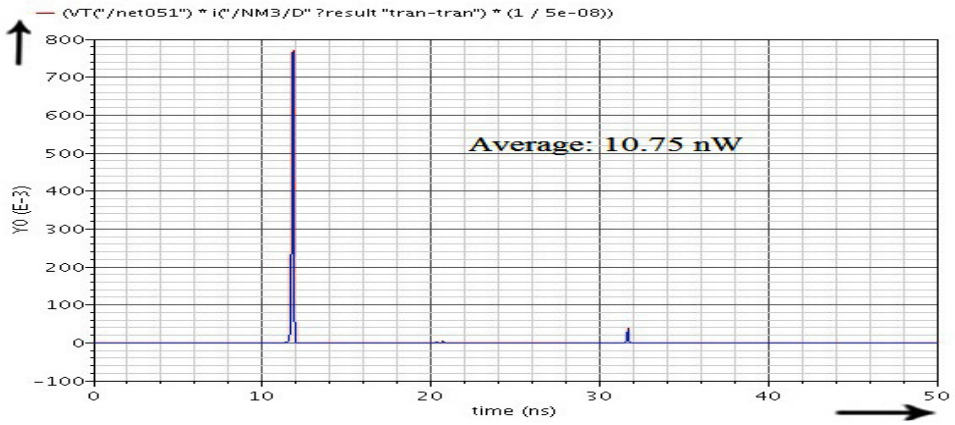

Figure 8. Simulated Leakage power of double Gate FinFET at 180 nm technology in Cadence Tool.

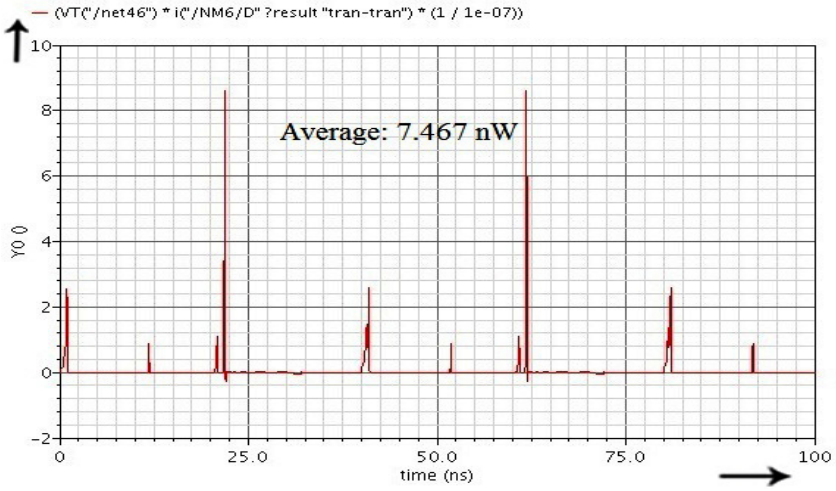

Figure 9. Simulated Leakage power of double Gate FinFET at 45 nm technology in Cadence Tool.

The proposed figure 10 and 11 is analyzed by varying the supply voltage to five different values at 0.5V, 0.6V, 0.7V, 0.8V and 0.9V respectively. The leakage current value is calculated in order to estimate the power consumption at five different voltage variations. The following figure's gives the analysis of Voltage, Current, Power and delay with respective technologies.

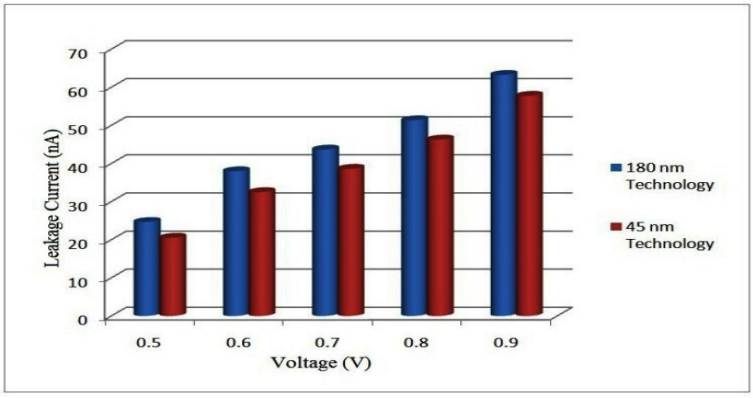

Figure 10. Comparison of Leakage current variation at different voltages at 45 nm and 180 nm technology in Cadence tool.

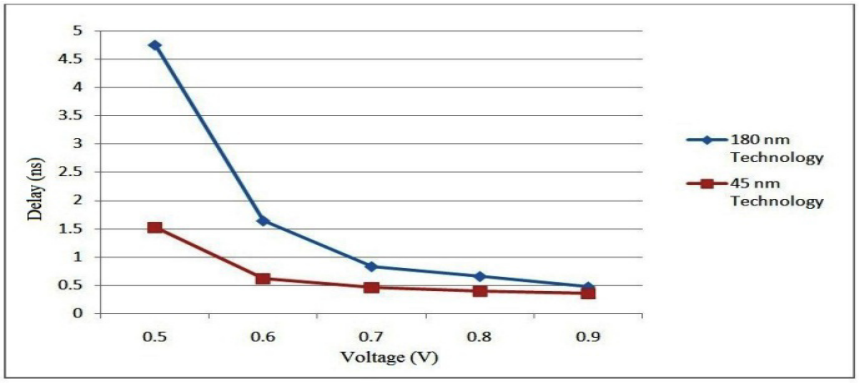

Figure 11. Comparison of Delay variation at different voltages at 45 nm and 180 nm technology in Cadence tool.

TABLE II. COMPARISION OF AVERAGE POWER, LEAKAGE POWER, LEAKAGE CURRENT, DELAY AND PDP AT DIFFERENT VOLTAGES AT 180 NM AND 45 NM TECHNOLOGY IN CADENCE TOOL

Voltage (V)	180 nm Technology					45 nm Technology				
	Average Power (nW)	*Leakage Power (nW)*	*Leakage Current (nA)*	*Delay (ns)*	*PDP (Joule)*	*Average Power (nW)*	*Leakage Power (nW)*	*Leakage Current (nA)*	*Delay (ns)*	*PDP (Joule)*
0.5	19.21	5.674	24.65	4.752	26.96×10^{-18}	11.11	2.763	20.52	1.522	4.205×10^{-18}
0.6	28.48	7.347	37.97	1.641	12.05×10^{-18}	20.33	4.391	32.48	0.608	2.669×10^{-18}
0.7	35.68	10.75	43.65	0.832	8.944×10^{-18}	27.38	7.467	38.60	0.452	3.375×10^{-18}
0.8	44.67	21.79	51.35	0.658	14.33×10^{-18}	36.58	17.84	46.28	0.388	6.921×10^{-18}
0.9	58.76	25.38	63.25	0.472	11.97×10^{-18}	50.60	21.98	57.75	0.349	7.671×10^{-18}

Table II shows the Comparison of average power, leakage power, leakage current, delay and PDP at different voltages at 45 nm and 180 nm technologies.

6. CONCLUSION

FinFETs are a promising substitute for bulk CMOS for meeting the challenges being posed by the scaling of conventional MOSFETs. Due to its double-gate structure, it offers innovative circuit design styles. An analytical model for the Average power, Leakage power, Leakage current and Delay of DG FinFET has been developed and validated with the help of device simulations and experimental results. Here a novel self-aligned double-gate SOI structure (FinFET) is proposed as bulk CMOS at the nanoscale. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count.

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