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Fast battery-charging architecture

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ABSTRACT

The disclosure describes a power-efficient, low-footprint, and fast battery charger based on a hybrid of the charge pump and the three-level chargers. The charger is low cost, reduces thermal dissipation, increases battery-charging speed, and is compatible with wired and wireless charging.

KEYWORDS

- Buck converter
- Charge pump
- Three-level power converter
- Battery charging efficiency
- Power delivery
- Programmable power supply
- Fast charge

BACKGROUND

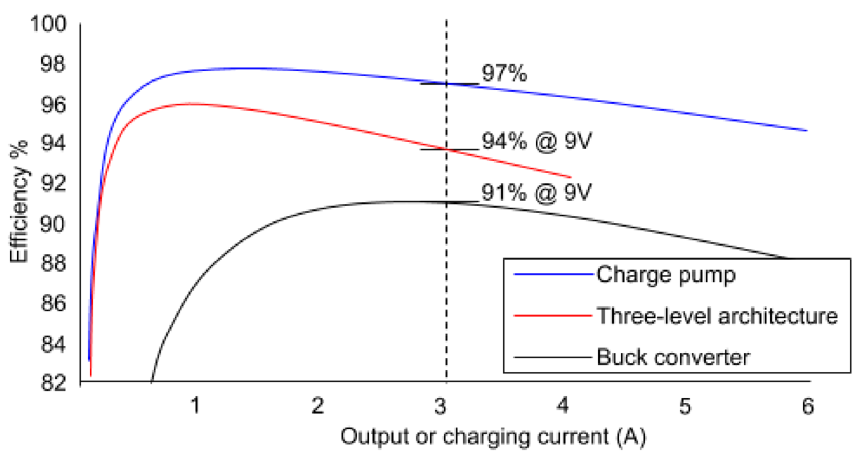

Fig. 1: Efficiencies of the charge pump, three-level, and buck converter architectures

Fig. 1 illustrates the efficiencies of various types of DC-DC converters, e.g., charge pump, three-level, and buck converters, as a function of output or charging current. At typical operating conditions, e.g., around 3 amperes and 9 volts, the buck converter has a 91% efficiency, which is exceeded by the efficiency of both the three-level architecture (94%) and the charge pump (97%). It would thus appear that for most applications the choice of DC-DC converter is the charge pump.

However, for reasons of micro-adjustability of output voltage, and for reasons of backward compatibility, e.g., with the power delivery 2.0 (PD 2.0) standard, in the type-C or legacy AC chargers, the charge pump is not used in a standalone manner to charge the battery. Also, if the charge pump were to be used in a standalone manner, the charge pump input current would need to be maintained at half the 1C rating to ensure the battery charging current maintains its C-rate at 1C. This means that battery current is shared with the system load and that the maximum output power of the adaptor is not reached.

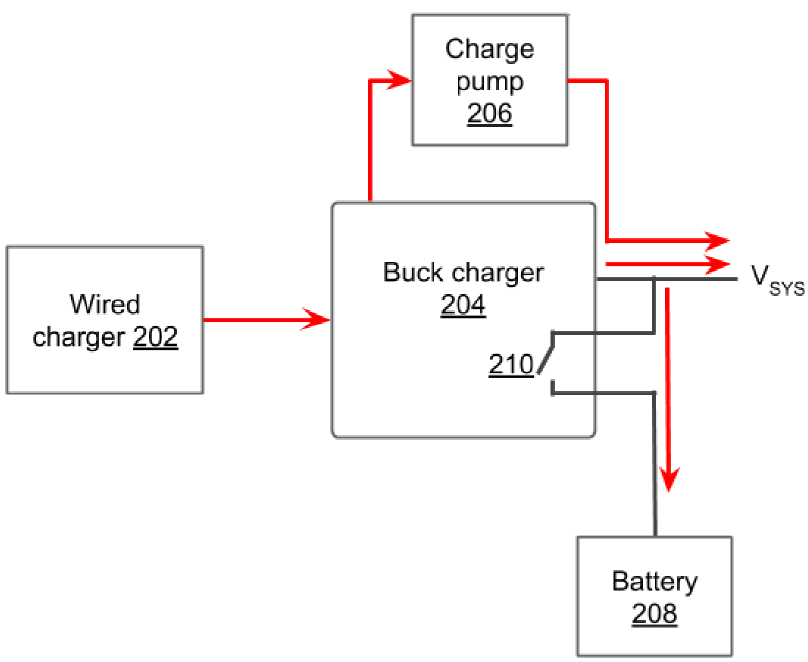

Fig. 2: Traditional combination of buck charger and charge pump

For the reasons stated above, the traditional fast-charging architecture - the PPS (programmable power supply) adaptor - combines the buck converter and the charge pump as shown in Fig. 2. Under this architecture, a wired charger (202) feeds a buck charger (204), whose output is partially fed to a charge pump (206) and partially to the load (V_{SYS}) and the battery (208). Based on the position of the battery switch (210), both the charge pump and the buck charger feed either the load or the battery. At high loads, the excess power needed to ensure a C-rate of 1C is provided by the buck charger; at light loads, the charge pump provides a larger fraction of power. The red arrows indicate directions of current flow. The traditional architecture of Fig. 2 occupies substantial board space, is expensive, and does not reach higher power efficiencies that are physically possible.

DESCRIPTION

From Fig. 1, it is seen that the buck converter is exceeded in efficiency not only by the charge pump but also by the three-level converter. The techniques of this disclosure combine the three-level and the charge-pump architectures to achieve fast charging at higher efficiencies than is possible with the traditional architecture of Fig. 2. The disclosed fast-charging architecture also occupies less space than traditional architectures.

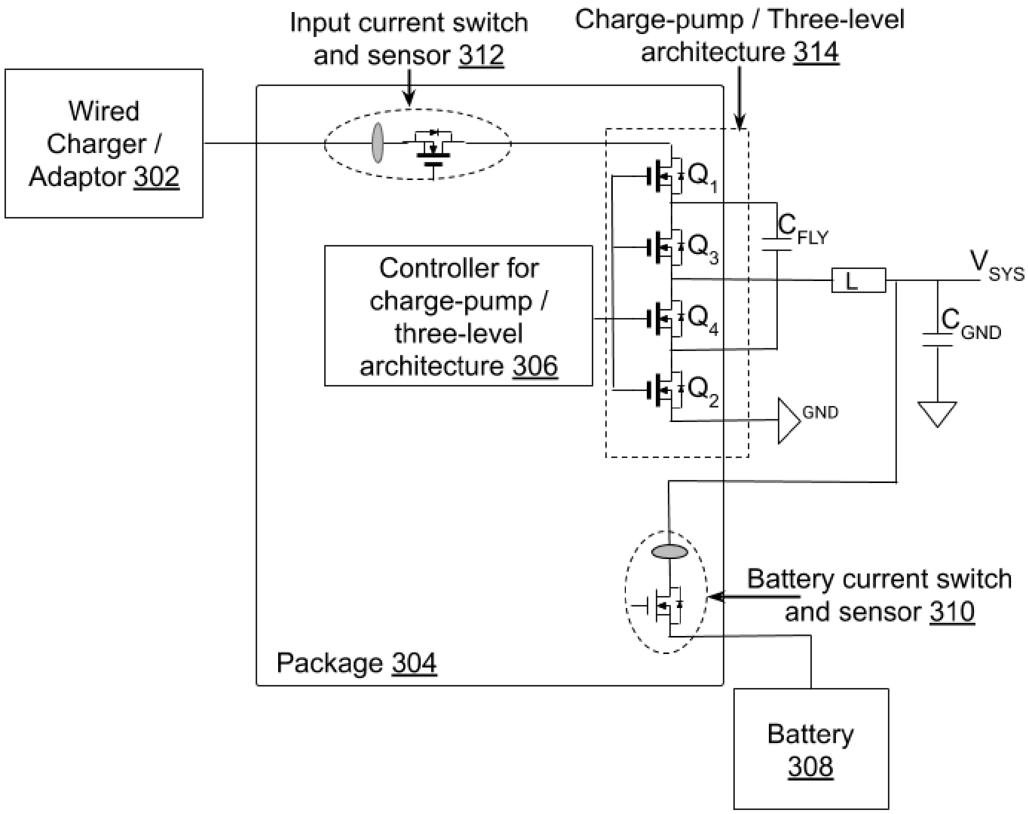

Fig. 3: Fast, high-efficiency charging using three-level and charge-pump architectures

Fig. 3 illustrates fast, high-efficiency charging using a combination of three-level and charge-pump architectures, per techniques of this disclosure. The charge-pump/three-level architecture (314) includes FETs Q_1 through Q_4 connected to each other and to a controller (306) in the topology shown in Fig. 3. Based on adaptor type (PPS charger or not), and the battery and input voltages and currents, the controller generates signals to switch mode between charge pump and three-level architecture. A battery current sensor (310) senses current from the battery (308) that is being charged, and an input current sensor (312) senses input current from the connected wired charger or adaptor (302). The input current sensor, battery current sensor, controller, and charge-pump/three-level architecture can advantageously be integrated into a single package (304), e.g., ASIC. At the output, the package is connected to the load V_{SYS} via a flying capacitor C_{FLY}, an inductor L, a capacitor-to-ground C_{GND}, etc. connected in the topology shown.

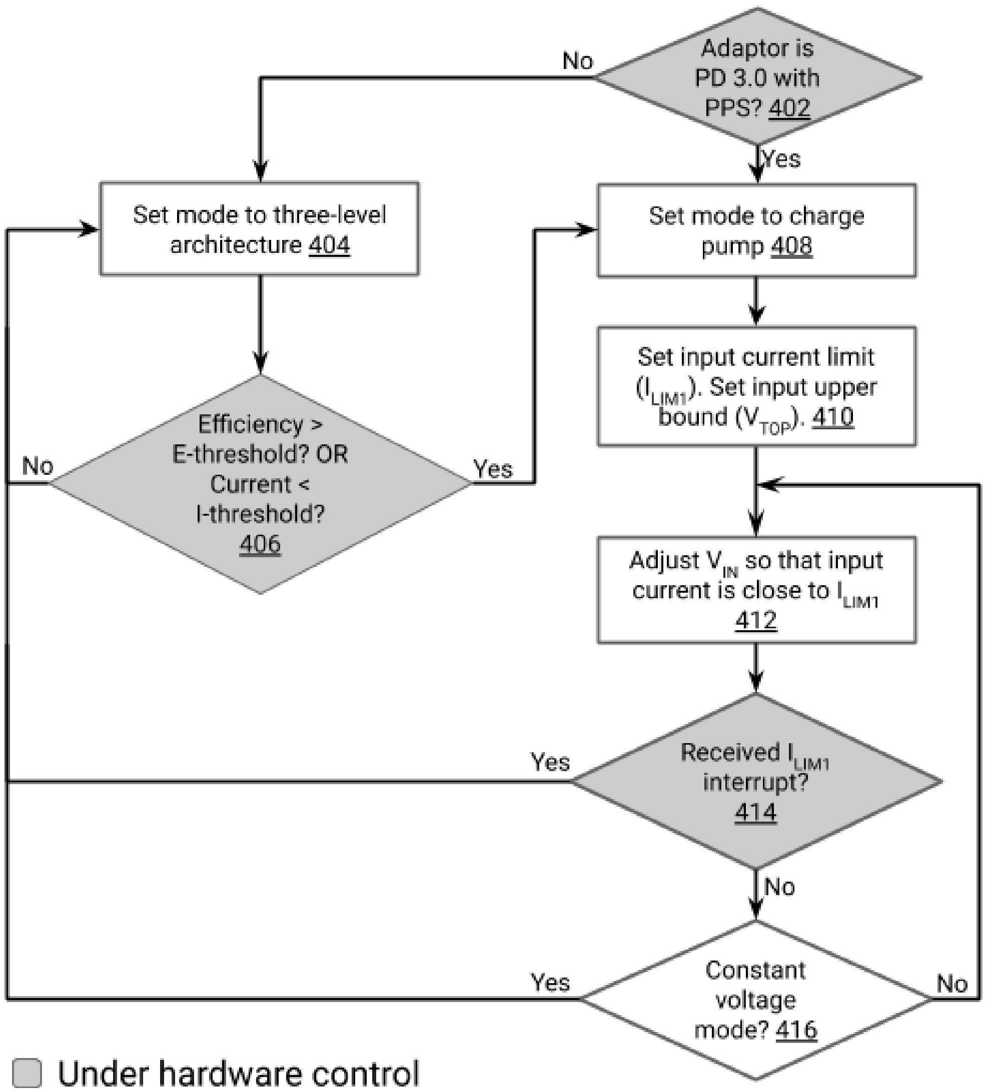

Fig. 4: Actions of the controller to switch mode between charge pump and three-level architecture

Fig. 4 illustrates actions performed by the controller to switch mode between charge pump and three-level architecture. If the adaptor is compliant with the PD 3.0 standard with programmable power supply (PPS), then the mode is set to charge pump (408); else, the mode is set to three-level architecture (404). The controller retains the three-level mode as long as the measured efficiency is less than an efficiency threshold, or as long as measured input current is greater than a current threshold (406). Efficiency is measured as

$$\text{Efficiency} = \frac{V_{BAT} I_{BAT}}{V_{IN} I_{IN}},$$

where V_{BAT} and I_{BAT} are respectively the battery voltage and battery current, and V_{IN} and I_{IN} are respectively the input voltage and the input current. An example efficiency threshold is 92%. Input current can be measured by turning off the battery switch for a short time and measuring the current at the input current sensor. An example current threshold is 100 mA. An efficiency above, e.g., 92%, or a current below, e.g., 100 mA, is indicative of light load, a condition better served by charge pump mode.

In charge pump mode, a limit is set (410) to the input current (I_{LIM1}) and to the input voltage (V_{TOP}). An example limit on the input current is one-half the 1C rating of the battery, e.g., I_{LIM1}=(½)1C. An example I_{LIM1} for a 4000 mAh battery and a 20 W PPS adaptor, is I_{LIM1}=2000 mA. The input voltage (V_{IN}) is adjusted such that the input current is close to I_{LIM1} (412). The receipt of an I_{LIM1} interrupt is indicative of increasing system load. Therefore, if an I_{LIM1} interrupt is received (414), the mode is switched to three-level architecture. Additionally, for three-level architecture, a second current limit I_{LIM2} can be imposed on the input current based on adaptor wattage and voltage. For a 20 W, 8 V PPS adaptor, I_{LIM2} can be set to the maximum current sourced from the adaptor, e.g., I_{LIM2} = 20 W / 8 V = 2,500 mA. So long as the I_{LIM1} interrupt is not received, and so long the battery has not reached constant voltage mode (416), e.g., it is in taper mode, the controller retains the charge pump mode. If the I_{LIM1} interrupt is not received and the battery has reached constant voltage mode then the controller switches to three-level architecture.

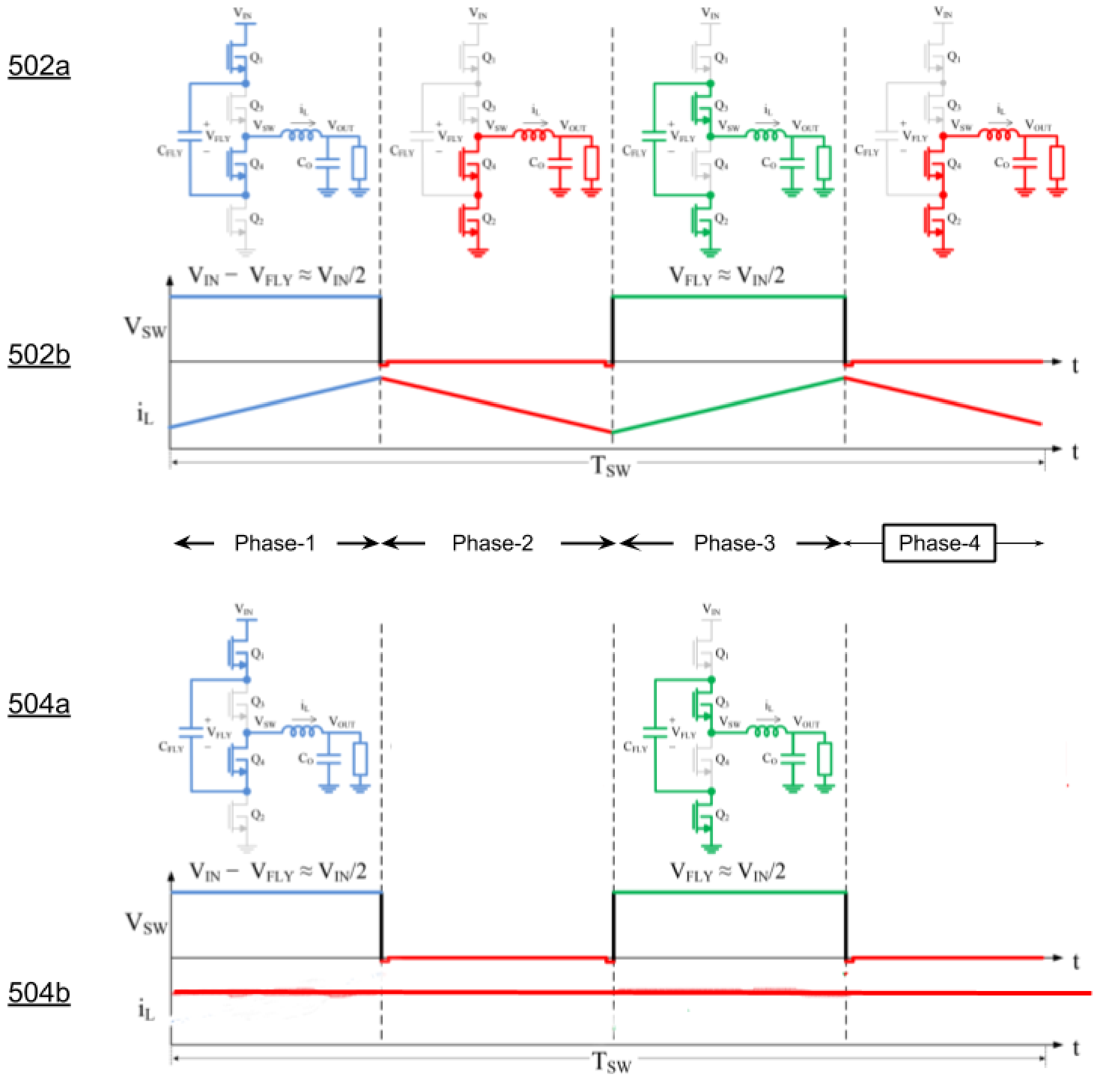

Fig. 5: Mechanism to switch modes between charge pump and three-level architecture

Fig. 5 illustrates a mechanism to switch modes between charge pump and three-level architecture. To achieve three-level converter operation, the switching waveform 502b (V_{SW}) is applied to FETs Q_1 through Q_4. The colored portions in 502a indicate the active parts of the charge-pump/three-level architecture at various phases of the switching waveform. During phase-1, Q_1 and Q_4 are on, and these two FETs enable passage of input energy to the inductor and the flying capacitor C_{FLY}. During phase-2, Q_2 and Q_4 are on, and enable the discharge of the inductor. During phase-3, Q_2 and Q_3 are on, and these two FETs enable passage of energy from the flying capacitor to the inductor. During phase-4, Q_2 and Q_4 are on, and enable the discharge of the inductor.

To achieve charge-pump operation, the switching waveform 504b (V_{SW}) is applied to FETs Q_1 through Q_4. The colored portions in 504b indicate the active parts of the charge-pump/three-level architecture at various phases of the switching waveform. It is observed that the charge pump mode is achieved by retaining as active phases 1 and 3 of the three-level mode.

In both charge-pump and three-level modes, i_L denotes the current through the output inductor. The waveforms and active circuit-parts of Fig. 5 apply when the duty cycle of the switching waveform is less than 50%. A similar mechanism to switch modes applies when the duty cycle of the switching waveform is greater than 50%. In that case, the sequence of active circuit-parts are slightly different from those shown in Fig. 5. However, in charge pump mode, the duty cycle is set to 50%.

Per techniques of this disclosure, switching between two charging architectures to optimize efficiency based on load is achieved by switching waveforms. Since the two constituent architectures use the same hardware, the disclosed fast charger is space efficient as well as power efficient.

CONCLUSION

The disclosure describes a power-efficient, low-footprint, and fast battery charger based on a hybrid of the charge pump and the three-level chargers. The charger is low cost, reduces thermal dissipation, increases battery-charging speed, and is compatible with wired and wireless charging.

REFERENCES

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