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# Modeling of Ultra Low Capacitance Transient Voltage Suppression Diode for High ESD Protection

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**Abstract**
To improve key properties such as ultra-low capacitance (ULC) and high-voltage (HV) breakdown, we have performed a simulation work about transient voltage suppression (TVS) diodes. ULC-TVS diode was designed to employ a double deep trench to cut off the various parasitic effects that may degrade the device performance. The electrostatic discharge (ESD) protection is the targeting for the best applications in high-frequency and high-speed ICs. In this work, the device could present excellent performance in terms of very responsive ESD properties, high breakdown voltage, low leakage current, and very low capacitance level. The double trenches are aligned to the top electrode contact to restrict field crowding effects by the strong electric field intensity. The performance would be sufficient for the robust ESD nature up to IEC61000-4-2 (30 kV) and compatible with strong surge protection IEC61000-4-5 (10A). Their electrical properties have been evaluated for structure from simulation and the results are obtained at the device parameters. Several process of device design related effects on the electrical capability and can be optimized.
**Keywords:** ULC-TVS diode, simulation (TCAD), characteristics, capacitance, ESD protection.

## 1. Introduction

The electrostatic discharge (ESD) is the immediate flow of electricity between two objects caused by contacts, an electrical short, or dielectric breakdown. One of the few things failure problems with the circuit technologies. The bidirectional input/output (I/O) uses of protection elements, it is known as making devices, self-protecting and provides specified ESD robustness through proper device design. Transient voltage suppression (TVS) diodes are used to protection trace from high voltage spikes as the part of an effective ESD protection concept, it has to fulfill certain electrical requirements. Moreover, the electrical characteristics of Zener and avalanche diode are similar [1].

Ultra-low-capacitance TVS (ULC-TVS) diode is the one of family TVS diodes [1-2]. The capacitance of ULC-TVS is smaller than standard TVS diodes for the typical of capacitances are between 0.4-0.9pF, and it was designed for protection high-speed data and also for radio frequency (RF) antennas such as global positioning system (GPS), frequency modulation (FM) radio, and near field communication (NFC) antenna lines [3].

In this work, we demonstrated the new ULC-TVS diode structure fabrication and current-voltage (I-V) characterization were used Silvaco 2-D simulation software for low capacitance and higher stability. A reference ESD device modeled as T. Keena et al. (US 7538395 B2) [2] as a standard device and then compared to the new modified ESD device. We carried out our simulation using Athena and Atlas TCAD software version 5.20.0.R and 5.18.3.R, respectively. The TCAD simulations as a detailed explanation of the effects of trench depth along with n-Si epitaxy layer thickness and a trench wide [4-6]. The significant of temperature protection device is used to protect internal circuits or devices overheating, which act as temperature detectors [7]. However, if the high voltage of the device is proposed, and it can be accepted for very high-temperature dependence [8-10]. In the structure of this device is influenced to reduce the electric field on breakdown voltage with using isolation trenches [11-13].

## 2. Device Structure

Fig. 1 (a) shows the schematic cross section ULC-TVS diode. The ULC-TVS diode with large trenches enough for the standard structure [2]. The simulated is believed very well with the result values. When positive bias event occurs on the device, the series combination TVS diode and Zener diode (in the section-1) will protect otherwise when negative bias event occurs on second TVS diode in the section-2. The designed structures are offering to the prospect of improving the capacitance performance for the ESD robustness. For Fig. 1 (b) is presented the circuit of an ESD protection device in accordance with this devices.

 

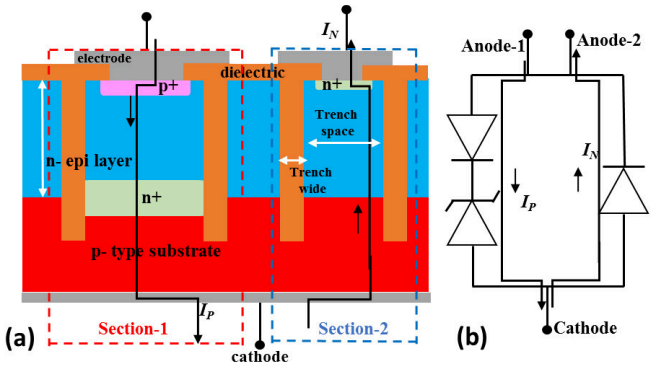


Fig.1 (a) the schematic cross section diagram of new ULC-TVS diode ($I_N$ and $I_P$ are negative and positive current through in each section by applying negative and the positive voltage, respectively), (b) an equivalent circuit diagram of the component.

In order to develop, the device was demonstrated from standard device structure [2] to the new structure of the device. The schematic cross section of the structure under study is shown in the Fig.2, where the color is representing the doping concentration levels. The trenches depth were separated two sections (section-1 are included TVS diode and Zener diode, and other section included TVS diode). That contain the active BV devices which are on the top of high dose purity dopant p+ and n+ contact regions. The trench is filled with silicon dioxide ($SiO_2$) and increase the size of trench become too large enough, called trench width. The result in this structure formed by I-V characterization of adjusted by n-Si epitaxy layers (from 6 to 10μm) called trench depth, epitaxial doping concentration, implantation area of p+, n+ contact regions. The completed structure and contacts are placed at the top device, whereas the bottom contact at the wafer substrate backside.

This device simulation structure is difficult to analyze the capacitance until the charges are balanced between p-type and n-type layers due to the charge compensation principle [14]. I-V characteristic is increased with increasing thickness of the n- epitaxial layer, epi layer doping concentration. For a given 10μm n-Si epitaxy layer and depth of the trench 11~12μm. In the result, it increases the maximum of the BV, which is due to the increase in the depletion layer of the device [18]. This leads to the increase in the probability of being damaged by ESD [15].

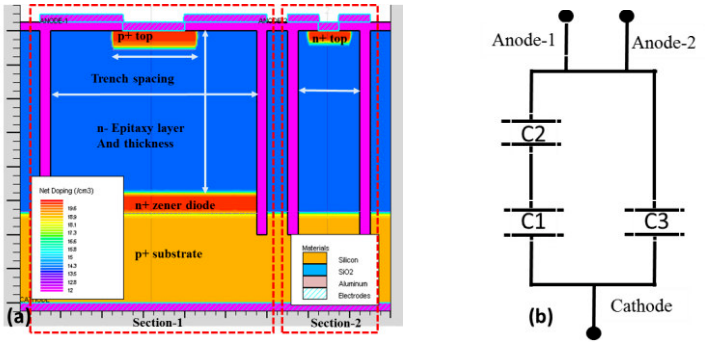


Fig.2 (a) the ULC-TVS diode structure simulated in 2-D ATHENA, (b) illustrates an embodiment of a portion capacitor of a circuit representation of the device.

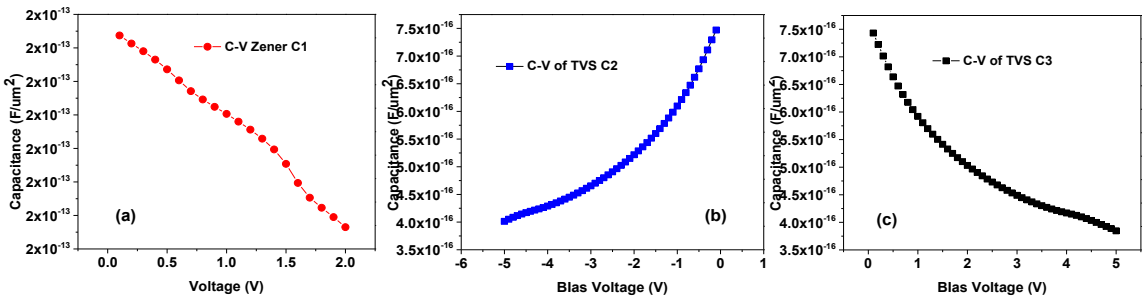


Fig.3 the simulation of capacitance from the structure of ULC-TVS diode as a function of voltage one by one junction (a) capacitance of the Zener diode section-1, (b) capacitance of TVS diode section-1, and (c) the capacitance of TVS diode section-2.

Recently, the electronic component dimension has been moved forward to the nanometer scale to realize the higher integration density, and increase the probability of the component damaged by ESD. In this

 

case, the simulation in the simple way to achieve a small capacitance in internal series connection of capacitor in the device with the high voltage of TVS diode. Low capacitance is shown as $2.7X10^{-13}F/\mu m^2$, $7.52X10^{-16}F/\mu m^2$, $7.46X10^{-16}F/\mu m^2$ of C1, C2, and C3, respectively. It is required to eliminate high ESD robustness. In fact, smaller capacitance value can't obtain in lower voltage diode that relates to use the narrow and heavy doped of the base layer. From the simulation process, the capacitance value was shown one by one junction, as shown in fig. 3. Whereas, it could be reduced by minimizing the p-n junction area [17].

## 3. Simulation Result and Discussion

The ESD protection devices used in this investigation and comparison from the simulation result of device standard. To explain the behavior were performed through TCAD Athena and Atlas Silvaco software simulation. The results of these simulations are presented in the following.

In Fig.4 (a), shown the I-V characteristic of the simulation standard diode [2], the I-V characteristic of the conventional TVS diode were presented the breakdown voltage (BV) of 60V and 55V, from the section-1 and section-2, respectively. The Fig.4 (b) shown the BV of the simulated modification TVS diode called as ULC-TVS. The BV of modification ULC-TVS diode is presenting higher BV than conventional of 200V and 220V from the diode section-1 and 2, respectively. At low leakage current density of $5pA/\mu m^2$.

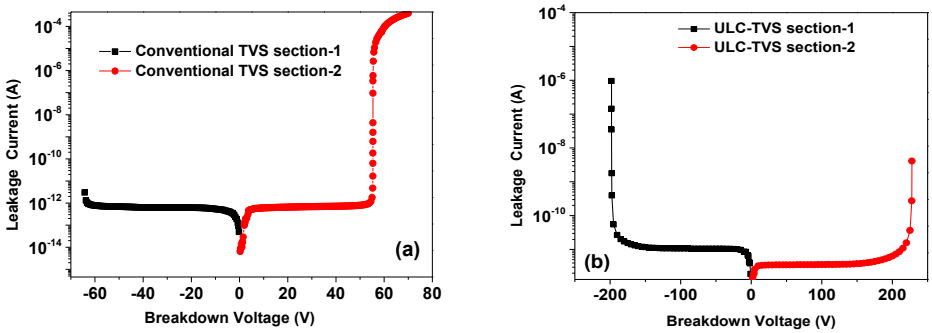


Fig. 4 I-V characteristic of the diode from section-1 and section-2 of (a) standard TVS and (b) ULC-TVS diode (new modification).

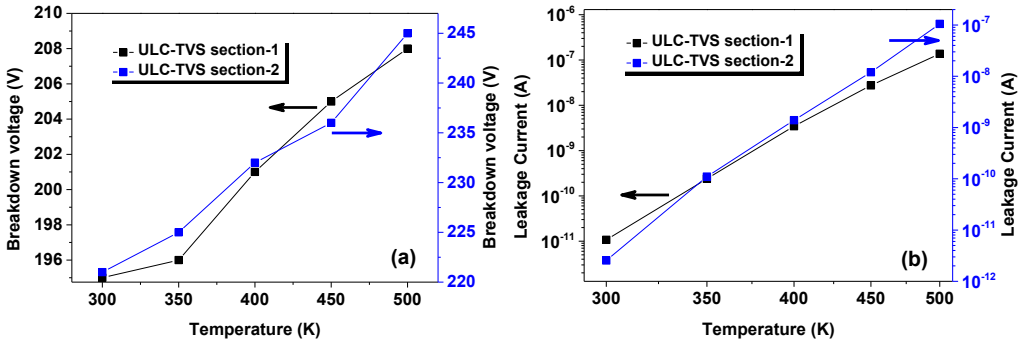


Fig. 5, I-V-T characteristic simulated at the various temperature range of 300, 350, 400, 450, and 500K (a) temperature vs. breakdown voltage, and (b) temperature vs. leakage current.

Fig. 5, shows I-V-T curves of the modification ULC-TVS device simulated at various temperatures, which range from 300K to 450K in a step of 50K. The reverse leakage current ($I_R$) increases as the increasing operation temperature when the carriers in semiconductor materials are followed by the Boltzmann statistics. The temperature dependence of reverse current was kept increase at less from $2.55X10^{-12}$ Amp at 300K to $1.05X10^{-7}$ Amp at 500K. The affection of the diffusion on $I_R$ condition mechanism, for the one side of reverse current given by the Schottky equation, can be expressed as [3, 16]

$$I_R = Aq\sqrt{\frac{D_P}{\tau_P}}\frac{n_i^2}{N_D} + \frac{eAWn_i}{\tau_g} \qquad (1)$$

Where $A$ is the p-n junction area, $ND$ is the base doping concentration, $W$ is the depletion region width, $Dp$ is the diffusion coefficient of the hole in p-type, $\tau_p$ is the mean lifetime of hole recombination and $\tau_g$ is the mean time to generate electron-hole pairs. Since $n_i \sim \exp(-Eg/2k_BT)$, the temperature dependence in the exponential terms are stronger than other terms $I_R$ from Eq. 1, can be rewritten as the Eq. 2 bellowing. As the same time, the reverse leakage current conduction mechanism of the p-n junction are characterized by thermal activation energy of the junction. In case of energy activation must close to Si band gap $E_g$ or $E_g/2$.

 

$$I_R \sim \exp\left(\frac{E_g}{K_B T}\right) + \exp\left(\frac{E_g}{2K_B T}\right) \qquad (2)$$

The structure geometrical dimensions, doping concentration, implantation and trench spaces were changed and collected the results. The BV of the device can be adjusted by doping concentration and thickness of the n- epi-layer. The BV were increased with epi-layer thickness increasing as shown in the Fig.6 (a), and (b). However, the depletion region is entered by the doping concentration process and their spacing charge generation from the neighboring regions. Otherwise, the voltage is increased, the electric field in the depletion region increase to the higher value. The BV is determined by the breakdown field of the material in the junction. As the result to increase the BV while adjusted the dopant impurity on the top contact region of both sides (p+ and n+ regions from the section-1 and section-2, respectively), the breakdown is inversely proportional to the doping density if the one region is weak doping dependence of the electric field at the breakdown [19], as shown in fig.6 (c). The most importance parameter is wide trench isolation because trench isolation is charge induced by the trench inner device between trenches (spacing of trench) and width trench in fig. 6 (d) and (e), respectively. The region resistance decrease with increasing trench width as the trench width increase, the trench becomes wider and the peak electric field is reduced [20].

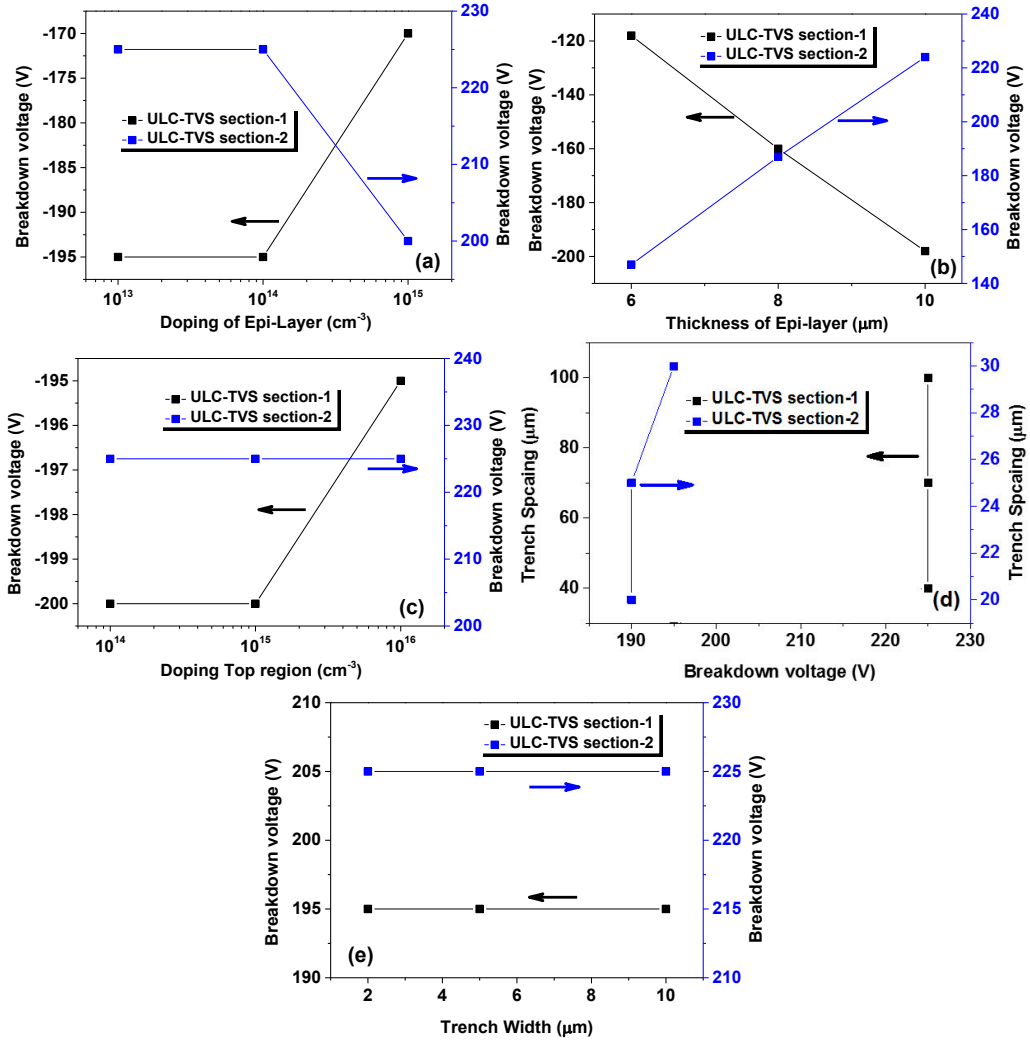


Fig.6 I-V characteristics of device adjusted by changing some parameters, (a) Epi-layer doping concentration, (b) the thickness of Epi-layer, (c) doping top contacts region of both sections, and (d) spacing between trench, and (e) wide of the isolation trench.

## 4. Conclusions

From the result of ULC-TVS diode simulation, we examined every parameters for fabrication processes including epi layer thickness, epi layer doping concentration, implantation condition, trench width, space between trench, annealing temperature/time, and concentration profile of p/n impurities as well and the properties of those parameters as shown in the I-V characteristic by using TCAD Silvaco program. Low

 

capacitance of these devices is measured by simulation program one by one section. The capacitance is known as an important parameter of the ESD protection device that it presents a speed response time. For the capacitance should be smaller as much as possible to minimize the RC time constant that knows as the limiting speed parameter of the device. To compare with the original structure we found that the width and depth trench isolation can be the improvement the breakdown voltage and capacitance. In this research, the high voltage is achieved 200 V to 220 V, and compound capacitances in series and parallel is ~$1.37X10^{-15}$F. Therefore in the future, we should try to extract the other important characteristics to optimize the device properties such as time-response and ESD simulation.

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